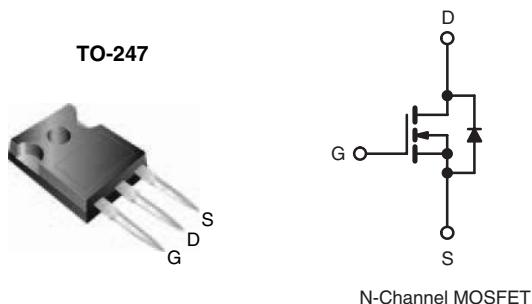


Power MOSFET

PRODUCT SUMMARY	
V _{DS} (V)	200
R _{DS(on)} (Ω)	V _{GS} = 10 V 0.055
Q _g (Max.) (nC)	230
Q _{gs} (nC)	42
Q _{gd} (nC)	110
Configuration	Single



FEATURES

- Dynamic dV/dt Rating
- Repetitive Avalanche Rated
- Isolated Central Mounting Hole
- Fast Switching
- Ease of Parallelizing
- Simple Drive Requirements
- Lead (Pb)-free Available



DESCRIPTION

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-247 package is preferred for commercial-industrial applications where higher power levels preclude the use of TO-220 devices. The TO-247 is similar but superior to the earlier TO-218 package because of its isolated mounting hole. It also provides greater creepage distance between pins to meet the requirements of most safety specifications.

ORDERING INFORMATION

Package	TO-247
Lead (Pb)-free	IRFP260PbF SiHFP260-E3
SnPb	IRFP260 SiHFP260

ABSOLUTE MAXIMUM RATINGS T_C = 25 °C, unless otherwise noted

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V _{DS}	200	V
Gate-Source Voltage	V _{GS}	± 20	
Continuous Drain Current	V _{GS} at 10 V	T _C = 25 °C	I _D
		T _C = 100 °C	46
Pulsed Drain Current ^a	I _{DM}	180	A
		2.2	W/°C
Single Pulse Avalanche Energy ^b	E _{AS}	1000	mJ
Repetitive Avalanche Current ^a	I _{AR}	46	A
Repetitive Avalanche Energy ^a	E _{AR}	28	mJ
Maximum Power Dissipation	P _D	280	W
Peak Diode Recovery dV/dt ^c	dV/dt	5.0	V/ns
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to + 150	°C
Soldering Recommendations (Peak Temperature)	for 10 s	300 ^d	
Mounting Torque	6-32 or M3 screw	10	lbf · in
		1.1	N · m

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).

b. V_{DD} = 50 V, starting T_J = 25 °C, L = 708 μH, R_G = 25 Ω, I_{AS} = 46 A (see fig. 12).

c. I_{SD} ≤ 46 A, dI/dt ≤ 230 A/μs, V_{DD} ≤ V_{DS}, T_J ≤ 150 °C.

d. 1.6 mm from case.

* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	40	$^{\circ}\text{C}/\text{W}$
Case-to-Sink, Flat, Greased Surface	R_{thCS}	0.24	-	
Maximum Junction-to-Case (Drain)	R_{thJC}	-	0.45	

SPECIFICATIONS $T_J = 25 \text{ }^{\circ}\text{C}$, unless otherwise noted

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT	
Static								
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0 \text{ V}$	$I_D = 250 \mu\text{A}$	200	-	-	V	
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25 \text{ }^{\circ}\text{C}$, $I_D = 1 \text{ mA}$		-	0.24	-	$\text{V}/^{\circ}\text{C}$	
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250 \mu\text{A}$		2.0	-	4.0	V	
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 20 \text{ V}$		-	-	± 100	nA	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 200 \text{ V}$, $V_{GS} = 0 \text{ V}$		-	-	25	μA	
		$V_{DS} = 160 \text{ V}$, $V_{GS} = 0 \text{ V}$, $T_J = 125 \text{ }^{\circ}\text{C}$		-	-	250		
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10 \text{ V}$	$I_D = 28 \text{ A}^b$	-	-	0.055	Ω	
Forward Transconductance	g_{fs}	$V_{DS} = 50 \text{ V}$, $I_D = 28 \text{ A}^b$		24	-	-	S	
Dynamic								
Input Capacitance	C_{iss}	$V_{GS} = 0 \text{ V}$, $V_{DS} = 25 \text{ V}$, $f = 1.0 \text{ MHz}$, see fig. 5		-	5200	-	pF	
Output Capacitance	C_{oss}			-	1200	-		
Reverse Transfer Capacitance	C_{rss}			-	310	-		
Total Gate Charge	Q_g	$V_{GS} = 10 \text{ V}$	$I_D = 46 \text{ A}$, $V_{DS} = 160 \text{ V}$, see fig. 6 and 13 ^b	-	-	230	nC	
Gate-Source Charge	Q_{gs}			-	-	42		
Gate-Drain Charge	Q_{gd}			-	-	110		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 100 \text{ V}$, $I_D = 46 \text{ A}$, $R_G = 4.3 \Omega$, $R_D = 2.1 \Omega$, see fig. 10 ^b		-	23	-	ns	
Rise Time	t_r			-	120	-		
Turn-Off Delay Time	$t_{d(off)}$			-	100	-		
Fall Time	t_f			-	94	-		
Internal Drain Inductance	L_D	Between lead, 6 mm (0.25") from package and center of die contact		-	5.0	-	nH	
Internal Source Inductance	L_S			-	13	-		
Drain-Source Body Diode Characteristics								
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	46	A	
Pulsed Diode Forward Current ^a	I_{SM}			-	-	180		
Body Diode Voltage	V_{SD}	$T_J = 25 \text{ }^{\circ}\text{C}$, $I_S = 46 \text{ A}$, $V_{GS} = 0 \text{ V}^b$		-	-	1.8	V	
Body Diode Reverse Recovery Time	t_{rr}	$T_J = 25 \text{ }^{\circ}\text{C}$, $I_F = 46 \text{ A}$, $dI/dt = 100 \text{ A}/\mu\text{s}^b$		-	390	590	ns	
Body Diode Reverse Recovery Charge	Q_{rr}			-	4.8	7.2	μC	
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)						

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. Pulse width $\leq 300 \mu\text{s}$; duty cycle $\leq 2 \%$.

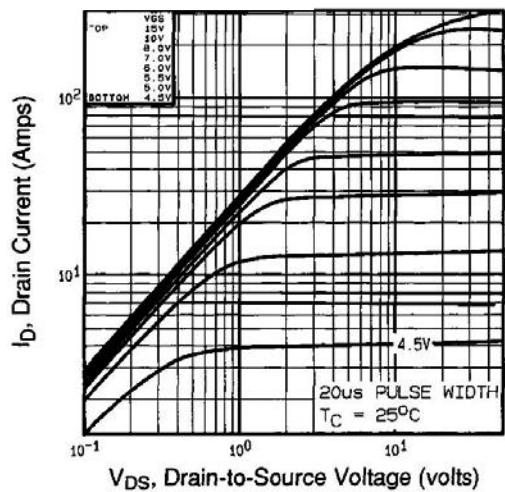
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted


Fig. 1 - Typical Output Characteristics, $T_C = 25\text{ }^\circ\text{C}$

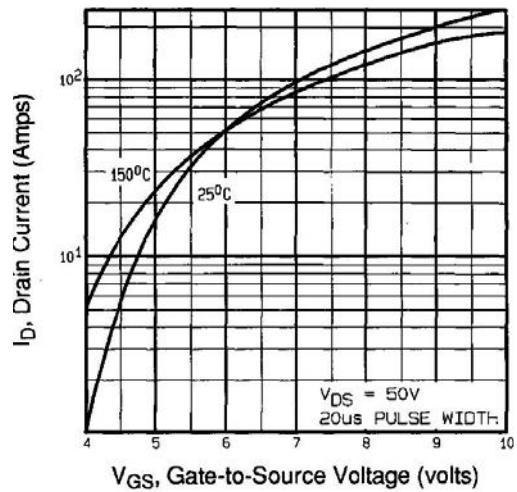


Fig. 3 - Typical Transfer Characteristics

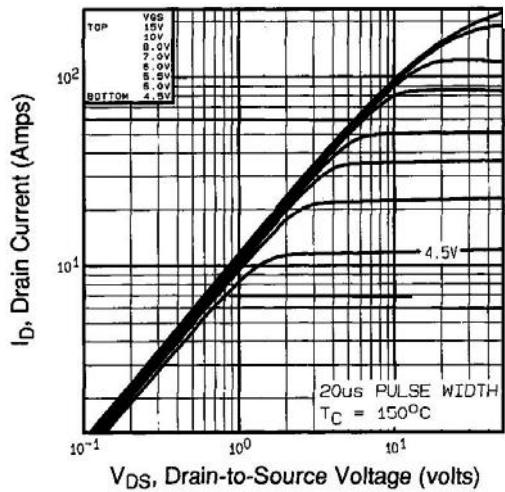


Fig. 2 - Typical Output Characteristics, $T_C = 150\text{ }^\circ\text{C}$

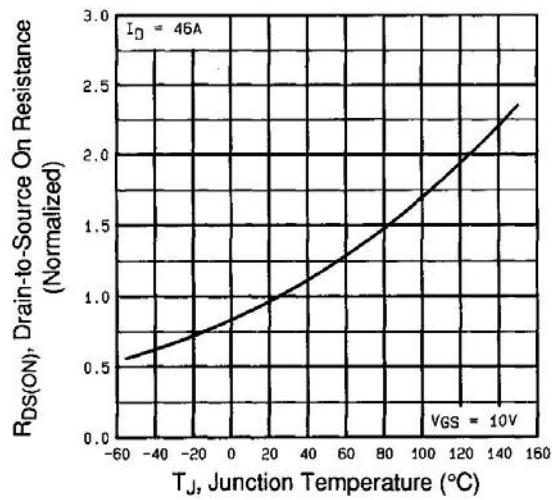


Fig. 4 - Normalized On-Resistance vs. Temperature

IRFP260, SiHFP260

Vishay Siliconix

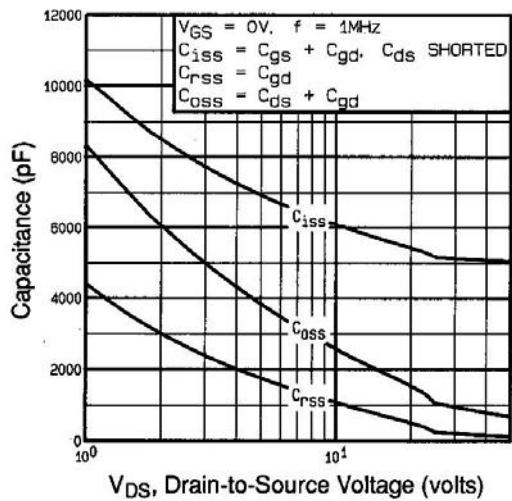


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

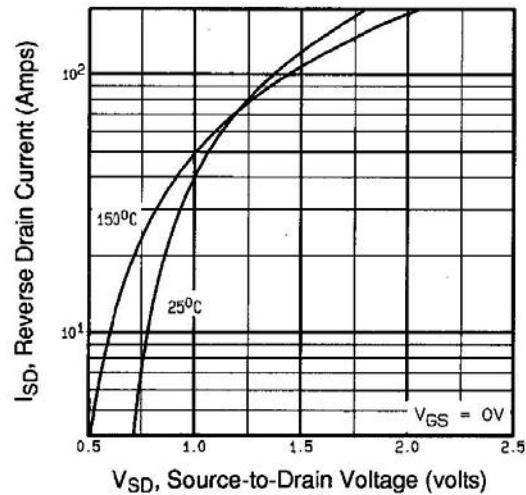


Fig. 7 - Typical Source-Drain Diode Forward Voltage

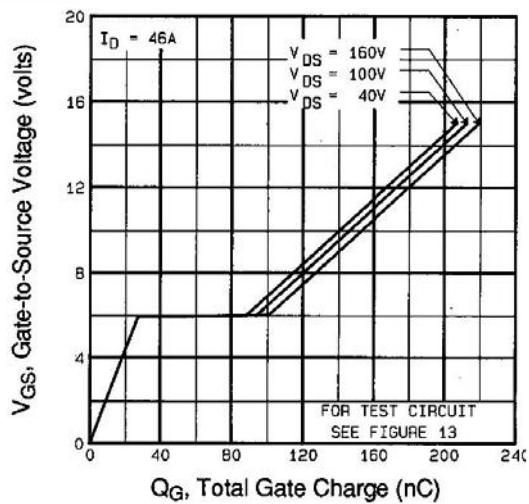


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

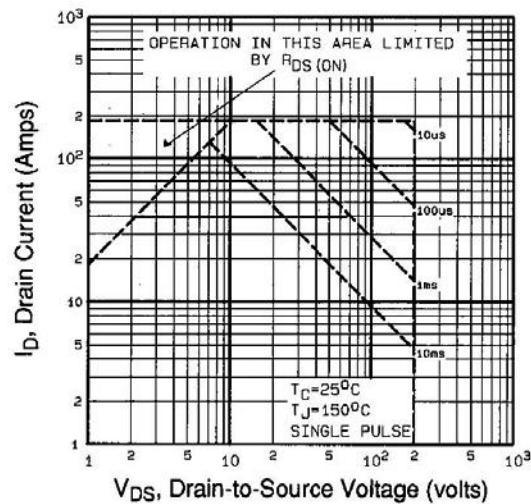


Fig. 8 - Maximum Safe Operating Area

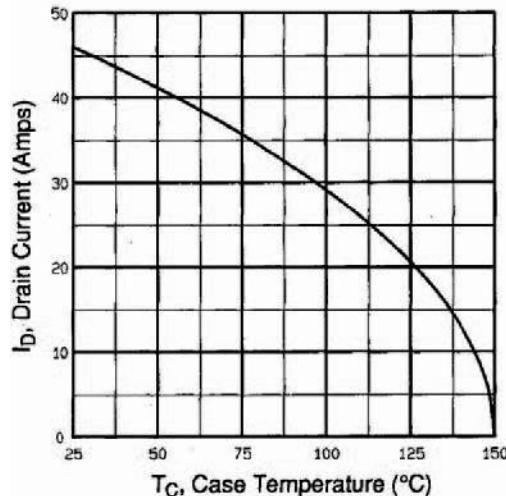


Fig. 9 - Maximum Drain Current vs. Case Temperature

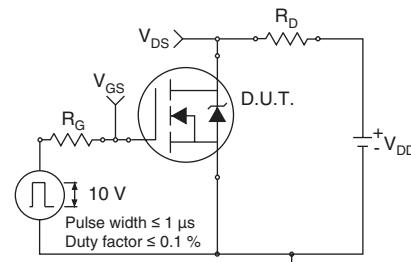


Fig. 10a - Switching Time Test Circuit

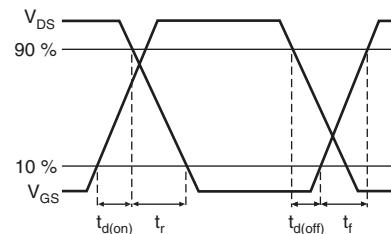


Fig. 10b - Switching Time Waveforms

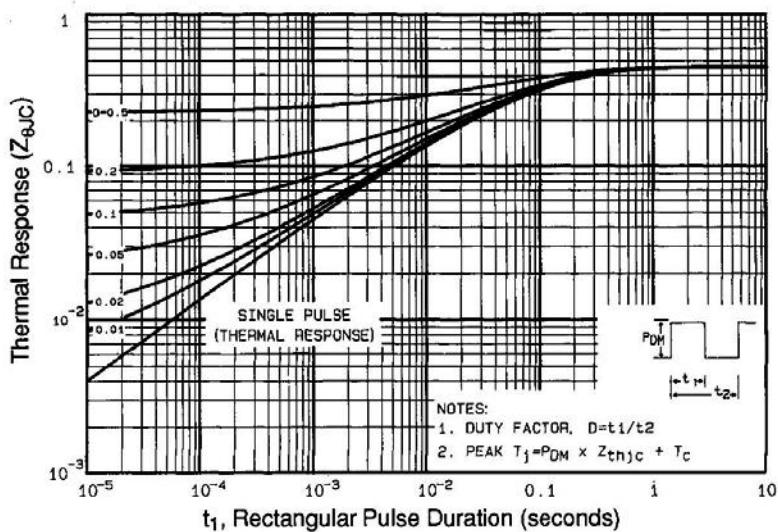


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

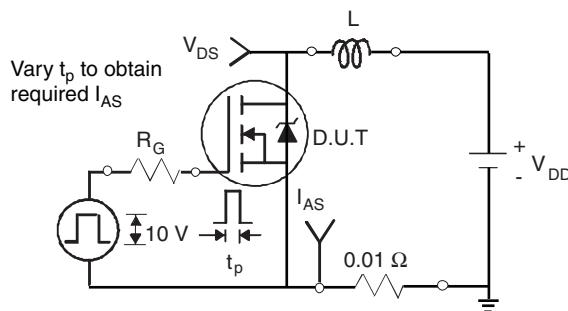


Fig. 12a - Unclamped Inductive Test Circuit

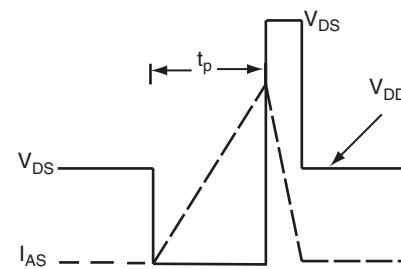


Fig. 12b - Unclamped Inductive Waveforms

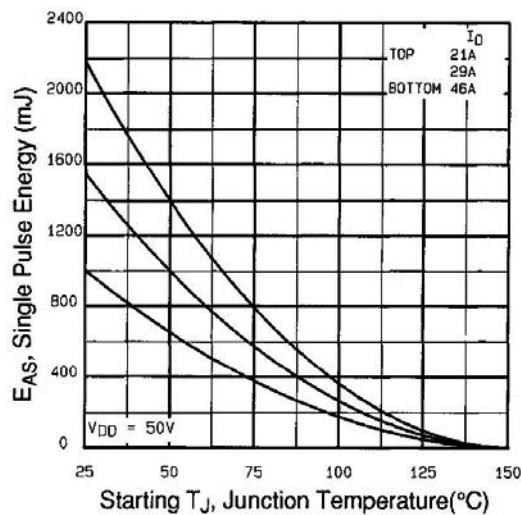


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

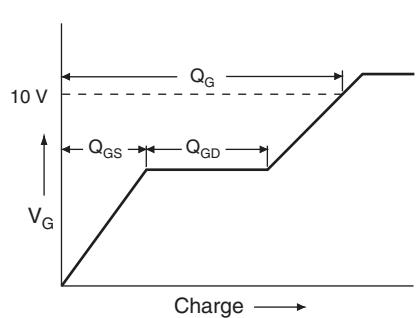


Fig. 13a - Basic Gate Charge Waveform

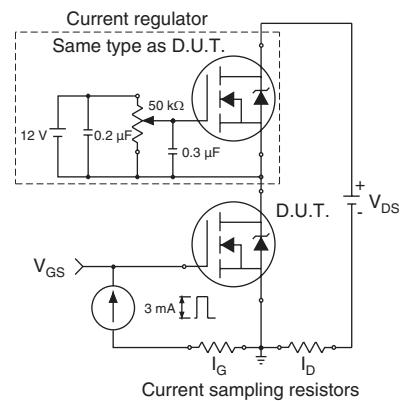
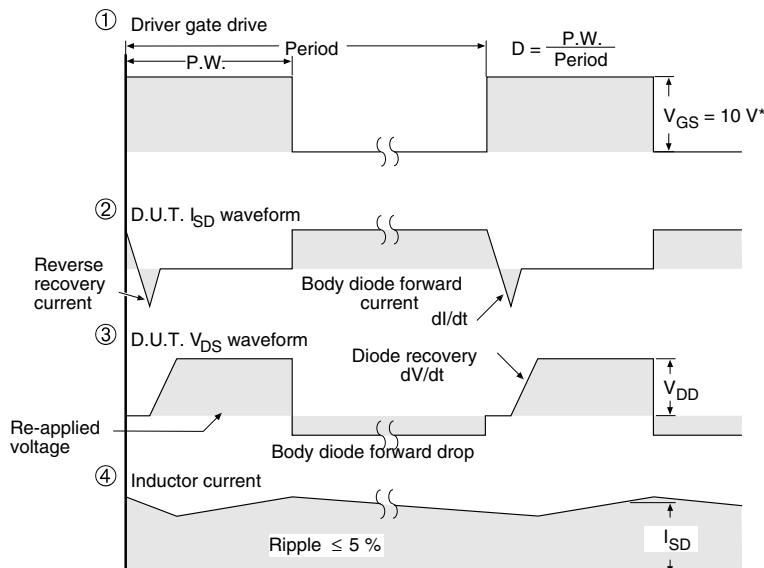
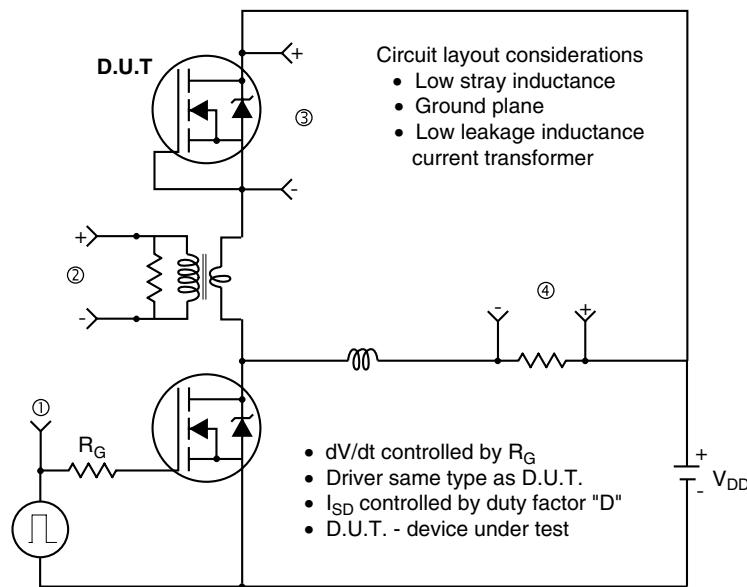


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



* $V_{GS} = 5$ V for logic level devices

Fig. 14 - For N-Channel

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