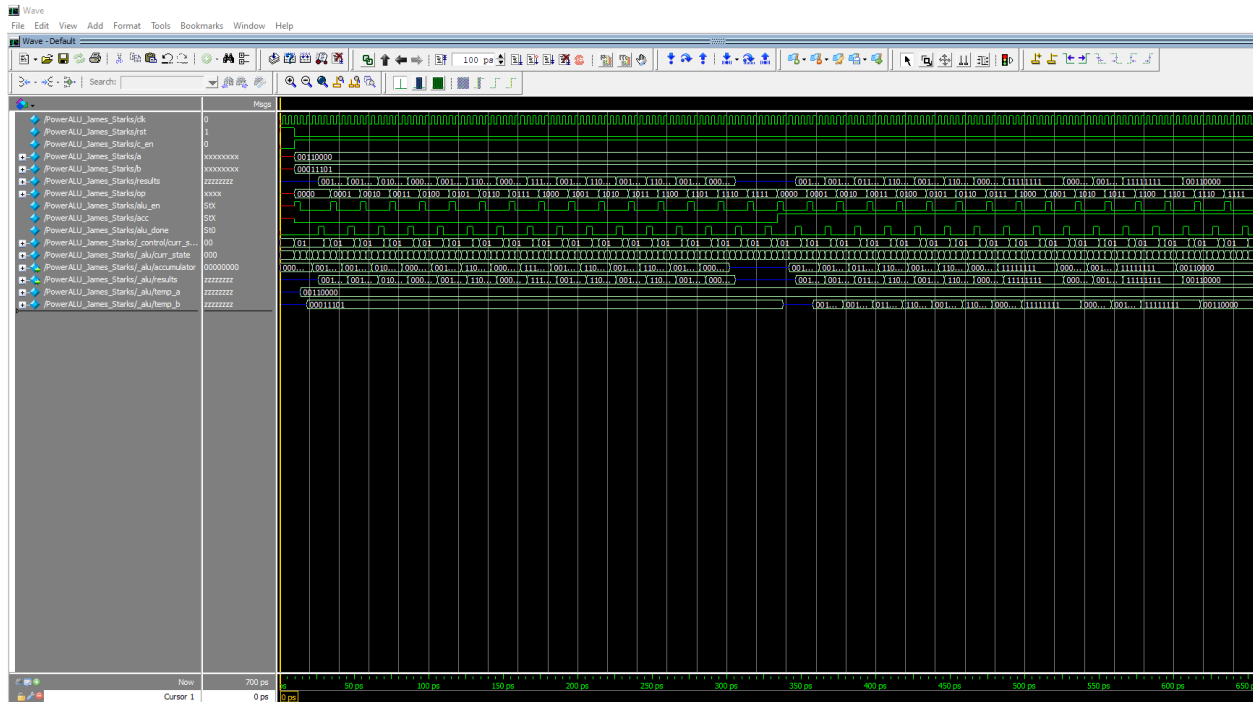


The figure consists of two state transition diagrams. The left diagram, titled "Control", shows a sequence of states: "Decode" (a rounded rectangle) is the initial state, reached from a "Reset" input. A "Clock" signal transitions the state to "Wait for ALU to finish" (a rounded rectangle). A decision diamond labeled "Done = 0" follows; if true, it loops back to "Decode". If false, it proceeds to a "Done = 1" state, which then loops back to "Decode". The right diagram, titled "ALU", shows a sequence of states: "Wait for Enable" (a rounded rectangle) is the initial state, reached from a "Reset" input. A "Clock" signal transitions the state to a decision diamond labeled "Enable = 0". If true, it loops back to "Wait for Enable". If false, it proceeds to "Load A" (a rounded rectangle). A "Clock" signal transitions the state to "Go" (a rounded rectangle). A "Clock" signal transitions the state to "Done" (a rounded rectangle). A "Clock" signal transitions the state back to "Wait for Enable". A "Reset" input transitions the state back to "Wait for Enable". A "Done = 1" signal from the "Control" component transitions the state back to "Wait for Enable".

[illegible]

Waveforms



I used ModelSim for this project.

Check Table

Opcode	A	B	ACC	Accumulator	Results	Expected
Transfer	00110000	00011101	0	zzzzzzzz	00110000	00110000
Increment	00110000	00011101	0	00110000	00110001	00110001
Add	00110000	00011101	0	00110001	01001101	01001101
Sub	00110000	00011101	0	01001101	00010011	00010011
Decrement	00110000	00011101	0	00010011	00101111	00101111
1's Complement	00110000	00011101	0	00101111	11001111	11001111
A AND B	00110000	00011101	0	11001111	00010000	00010000
A NAND B	00110000	00011101	0	00010000	11101111	11101111
A OR B	00110000	00011101	0	11101111	111101	00111101
A NOR B	00110000	00011101	0	00111101	11000010	11000010
A XOR B	00110000	00011101	0	11000010	101101	00101101
A XNOR B	00110000	00011101	0	00101101	11010010	11010010
GT	00110000	00011101	0	11010010	00110000	00110000
LT	00110000	00011101	0	00110000	00011101	00011101
EQ	00110000	00011101	0	00011101	zzzzzzzz	zzzzzzzz
NOP	00110000	00011101	0	zzzzzzzz	zzzzzzzz	zzzzzzzz
Transfer	00110000	00011101	1	zzzzzzzz	00110000	00110000

Increment	00110000	00011101	1	00110000	00110001	00110001
Add	00110000	00011101	1	00110001	00110001	00110001
Sub	00110000	00011101	1	01100001	01100001	01100001
Decrement	00110000	00011101	1	11001111	11001111	11001111
1's Complement	00110000	00011101	1	00101111	00101111	00101111
A AND B	00110000	00011101	1	11001111	11001111	11001111
A NAND B	00110000	00011101	1	00000000	00000000	00000000
A OR B	00110000	00011101	1	11111111	11111111	11111111
A NOR B	00110000	00011101	1	11111111	11111111	11111111
A XOR B	00110000	00011101	1	00000000	00000000	00000000
A XNOR B	00110000	00011101	1	00110000	00110000	00110000
GT	00110000	00011101	1	11111111	11111111	11111111
LT	00110000	00011101	1	11111111	11111111	11111111
EQ	00110000	00011101	1	00110000	00110000	00110000
NOP	00110000	00011101	1	00110000	00110000	00110000

Transcript.txt is included, which is all printout of all the monitor statements.