I/O PORT CONTROL REGISTER

PORT A CONTROL REGISTERS (PCONA, PDATA, PUPA)

Port A control registers are shown in Table 8-2:

Register	Address	R/W	Description	Reset Value
PCONA	0x01D20000	R/W	Configures the pins of port A	0x3ff
PDATA	0x01D20004	R/W	The data register for port A	Undef.

Table 8-2. Port of Group A Control Registers (PCONA,PDATA)

PCONA	Bit	Description	
PA9	[9]	0 = Output	1 = ADDR24
PA8	[8]	0 = Output	1 = ADDR23
PA7	[7]	0 = Output	1 = ADDR22
PA6	[6]	0 = Output	1 = ADDR21
PA5	[5]	0 = Output	1 = ADDR20
PA4	[4]	0 = Output	1 = ADDR19
PA3	[3]	0 = Output	1 = ADDR18
PA2	[2]	0 = Output	1 = ADDR17
PA1	[1]	0 = Output	1 = ADDR16
PA0	[0]	0 = Output	1 = ADDR0

PDATA	Bit	Description
PA[9:0]	[9:0]	When the port is configured as an output port, the pin state is the same as the corresponding bit. When the port is configured as a functional pin, an undefined value will be read.

PORT B CONTROL REGISTERS (PCONB, PDATB)

Port B control registers are shown in Table 8-3:

Register	Address	R/W	Description	Reset Value
PCONB	0x01D20008	R/W	Configures the pins of port B	0x7ff
PDATB	0x01D2000C	R/W	The data register for port B	Undef.

Table 8-3. Port of Group B Control Registers (PCONB,PDATB)

PCONB	Bit	Description	
PB10	[10]	0 = Output	1 = nGCS5
PB9	[9]	0 = Output	1 = nGCS4
PB8	[8]	0 = Output	1 = nGCS3
PB7	[7]	0 = Output	1 = nGCS2
PB6	[6]	0 = Output	1 = nGCS1
PB5	[5]	0 = Output	1 = nWBE3/nBE3/DQM3
PB4	[4]	0 = Output	1 = nWBE2/nBE2/DQM2
PB3	[3]	0 = Output	1 = nSRAS/nCAS3
PB2	[2]	0 = Output	1 = nSCAS/nCAS2
PB1	[1]	0 = Output	1 = SCLK
PB0	[0]	0 = Output	1 = SCKE

PDATB	Bit	Description
PB[10:0]	[10:0]	When the port is configured as an output port, the pin state is the same as the corresponding bit. When the port is configured as a functional pin, an undefined value will be read.

PORT C CONTROL REGISTERS (PCONC, PDATC, PUPC)

Port C control registers are shown in Table 8-4:

Register	Address	R/W	Description	Reset Value
PCONC	0x01D20010	R/W	Configures the pins of port C	0xaaaaaaaa
PDATC	0x01D20014	R/W	The data register for port C	Undef.
PUPC	0x01D20018	R/W	pull-up disable register for port C	0x0

Table 8-4. Port of Group C Control Registers (PCONC,PDATC,PUPC)

PCONC	Bit	Description	
PC15	[31:30]	00 = Input 10 = DATA31	01 = Output 11 = nCTS0
PC14	[29:28]	00 = Input 10 = DATA30	01 = Output 11 = nRTS0
PC13	[27:26]	00 = Input 10 = DATA29	01 = Output 11 = RxD1
PC12	[25:24]	00 = Input 10 = DATA28	01 = Output 11 = TxD1
PC11	[23:22]	00 = Input 10 = DATA27	01 = Output 11 = nCTS1
PC10	[21:20]	00 = Input 10 = DATA26	01 = Output 11 = nRTS1
PC9	[19:18]	00 = Input 10 = DATA25	01 = Output 11 = nXDREQ1
PC8	[17:16]	00 = Input 10 = DATA24	01 = Output 11 = nXDACK1
PC7	[15:14]	00 = Input 10 = DATA23	01 = Output 11 = VD4
PC6	[13:12]	00 = Input 10 = DATA22	01 = Output 11 = VD5
PC5	[11:10]	00 = Input 10 = DATA21	01 = Output 11 = VD6
PC4	[9:8]	00 = Input 10 = DATA20	01 = Output 11 = VD7
PC3	[7:6]	00 = Input 10 = DATA19	01 = Output 11 = IISCLK
PC2	[5:4]	00 = Input 10 = DATA18	01 = Output 11 = IISDI
PC1	[3:2]	00 = Input 10 = DATA17	01 = Output 11 = IISDO
PC0	[1:0]	00 = Input 10 = DATA16	01 = Output 11 = IISLRCK

PDATC	Bit	Description
PC[15:0]	[15:0]	When the port is configured as an input port, the corresponding bit is the pin state. When the port is configured as an output port, the pin state is the same as the corresponding bit. When the port is configured as a functional pin, an undefined value will be read.

PUPC	Bit	Description
PC[15:0]	[15:0]	0: the pull up resistor attached to the corresponding port pin is enabled. 1: the pull up resistor is disabled.

PORT D CONTROL REGISTERS (PCOND, PDATD, PUPD)

Port D control registers are shown in Table 8-5.

Register	Address	R/W	Description	Reset Value
PCOND	0x01D2001C	R/W	Configures the pins of port D	0x0000
PDATD	0x01D20020	R/W	The data register for port D	Undef.
PUPD	0x01D20024	R/W	Pull-up disable register for port D	0x0

Table 8-5. Port of Group D Control Registers (PCOND, PDATD, PUPD)

PCOND	Bit	Description
PD7	[15:14]	00 = Input 01 = Output 10 = VFRAME 11 = Reserved
PD6	[13:12]	00 = Input 01 = Output 10 = VM 11 = Reserved
PD5	[11:10]	00 = Input 01 = Output 10 = VLINE 11 = Reserved
PD4	[9:8]	00 = Input 01 = Output 10 = VCLK 11 = Reserved
PD3	[7:6]	00 = Input 01 = Output 10 = VD3 11 = Reserved
PD2	[5:4]	00 = Input 01 = Output 10 = VD2 11 = Reserved
PD1	[3:2]	00 = Input 01 = Output 10 = VD1 11 = Reserved
PD0	[1:0]	00 = Input 01 = Output 10 = VD0 11 = Reserved

PDATD	Bit	Description
PD[7:0]	[7:0]	When the port is configured as an input port, the corresponding bit is the pin state. When the port is configured as an output port, the pin state is the same as the corresponding bit. When the port is configured as a functional pin, an undefined value will be read.

PUPD	Bit	Description
PD[7:0]	[7:0]	0: the pull up resistor attached to the corresponding port pin is enabled. 1: the pull up resistor is disabled.

PORT E CONTROL REGISTERS (PCONE, PDATE)

Port E control registers are shown in Table 8-6:

Register	Address	R/W	Description	Reset Value
PCONE	0x01D20028	R/W	Configures the pins of port E	0x00
PDATE	0x01D2002C	R/W	The data register for port E	Undef.
PUPE	0x01D20030	R/W	pull-up disable register for port E	0x00

Table 8-6. Port of Group E Control Registers (PCONE, PDATE)

PCONE	Bit	Description
PE8	[17:16]	00 = Reserved(ENDIAN) 01 = Output 10 = CODECLK 11 = Reserved PE8 can be used as ENDIAN only during the reset cycle.
PE7	[15:14]	00 = Input 01 = Output 10 = TOUT4 11 = VD7
PE6	[13:12]	00 = Input 01 = Output 10 = TOUT3 11 = VD6
PE5	[11:10]	00 = Input 01 = Output 10 = TOUT2 11 = TCLK in
PE4	[9:8]	00 = Input 01 = Output 10 = TOUT1 11 = TCLK in
PE3	[7:6]	00 = Input 01 = Output 10 = TOUT0 11 = Reserved
PE2	[5:4]	00 = Input 01 = Output 10 = RxD0 11 = Reserved
PE1	[3:2]	00 = Input 01 = Output 10 = TxD0 11 = Reserved
PE0	[1:0]	00 = Input 01 = Output 10 = Fpllo out 11 = Fout out

NOTE: Please refer to Fig. 5-1 when selecting Fpllo or Fout.

PDATE	Bit	Description
PE[8:0]	[8:0]	When the port is configured as an output port, the pin state is the same as the corresponding bit. When the port is configured as a functional pin, the undefined value will be read.

PUPE	Bit	Description
PE[7:0]	[7:0]	0: the pull up resistor attached to the corresponding port pin is enabled. 1: the pull up resistor is disabled. PE8 do not have programmable pull-up resistor.

PORT F CONTROL REGISTERS (PCONF, PDATF, PUPF)

Port F control registers are shown in Table 8-7 below:

Register	Address	R/W	Description	Reset Value
PCONF	0x01D20034	R/W	Configures the pins of port F	0x0000
PDATF	0x01D20038	R/W	The data register for port F	Undef.
PUPF	0x01D2003C	R/W	pull-up disable register for port F	0x000

Table 8-7. Port of Group F Control Registers (PCONF, PDATF, PUPF)

PCONF	Bit	Description
PF8	[21:19]	000 = Input 001 = Output 010 = nCTS1 011 = SIOCLK 100 = IISCLK Others = Reserved
PF7	[18:16]	000 = Input 001 = Output 010 = RxD1 011 = SIORxD 100 = IISDI Others = Reserved
PF6	[15:13]	000 = Input 001 = Output 010 = TxD1 011 = SIORDY 100 = IISDO Others = Reserved
PF5	[12:10]	000 = Input 001 = Output 010 = nRTS1 011 = SIOTxD 100 = IISLRCK Others = Reserved
PF4	[9:8]	00 = Input 01 = Output 10 = nXBREQ 11 = nXDREQ0
PF3	[7:6]	00 = Input 01 = Output 10 = nXBACK 11 = nXDACK0
PF2	[5:4]	00 = Input 01 = Output 10 = nWAIT 11 = Reserved
PF1	[3:2]	00 = Input 01 = Output 10 = IICSDA 11 = Reserved
PF0	[1:0]	00 = Input 01 = Output 10 = IICSCL 11 = Reserved

PDATF	Bit	Description
PF[8:0]	[8:0]	When the port is configured as an input port, the corresponding bit is the pin state. When the port is configured as an output port, the pin state is the same as the corresponding bit. When the port is configured as a functional pin, the undefined value will be read.

PUPF	Bit	Description
PF[8:0]	[8:0]	0: the pull up resistor attached to the corresponding port pin is enabled. 1: the pull up resistor is disabled.

PORT G CONTROL REGISTERS (PCONG, PDATG, PUPG)

Port G control registers are shown in Table 8-8:

If PG0 - PG7 are to be used for wake-up signals in power down mode, the ports will be set in the interrupt mode.

Register	Address	R/W	Description	Reset Value
PCONG	0x01D20040	R/W	Configures the pins of port G	0x0
PDATG	0x01D20044	R/W	The data register for port G	Undef.
PUPG	0x01D20048	R/W	Pull-up disable register for port G	0x0

Table 8-8. Port of Group G Control Registers (PCONG, PDATG, PUPG)

PCONG	Bit	Description
PG7	[15:14]	00 = Input 01 = Output 10 = IISLRCK 11 = EINT7
PG6	[13:12]	00 = Input 01 = Output 10 = IISDO 11 = EINT6
PG5	[11:10]	00 = Input 01 = Output 10 = IISDI 11 = EINT5
PG4	[9:8]	00 = Input 01 = Output 10 = IISCLK 11 = EINT4
PG3	[7:6]	00 = Input 01 = Output 10 = nRTS0 11 = EINT3
PG2	[5:4]	00 = Input 01 = Output 10 = nCTS0 11 = EINT2
PG1	[3:2]	00 = Input 01 = Output 10 = VD5 11 = EINT1
PG0	[1:0]	00 = Input 01 = Output 10 = VD4 11 = EINT0

PDATG	Bit	Description
PG[7:0]	[7:0]	When the port is configured as an input port, the corresponding bit is the pin state. When the port is configured as an output port, the pin state is the same as the corresponding bit. When the port is configured as a functional pin, the undefined value will be read.

PUPG	Bit	Description
PG[7:0]	[7:0]	0: the pull up resistor attached to the corresponding port pin is enabled. 1: the pull up resistor is disabled.

EXTINT (EXTERNAL INTERRUPT CONTROL REGISTER)

The 8 external interrupts can be requested by various signaling methods. The EXTINT register configures the signaling method between the level trigger and edge trigger for the external interrupt request, and also configures the signal polarity.

Register	Address	R/W	Description	Reset Value
EXTINT	0x01D20050	R/W	External Interrupt control Register	0x000000

Table 8-10. External Interrupt Control Register (EXTINT)

EXTINT	Bit	Description
EINT7	[30:28]	Setting the signaling method of the EINT7. 000 = Low level interrupt 001 = High level interrupt 01x = Falling edge triggered 10x = Rising edge triggered 11x = Both edge triggered
EINT6	[26:24]	Setting the signaling method of the EINT6. 000 = Low level interrupt 001 = High level interrupt 01x = Falling edge triggered 10x = Rising edge triggered 11x = Both edge triggered
EINT5	[22:20]	Setting the signaling method of the EINT5. 000 = Low level interrupt 001 = High level interrupt 01x = Falling edge triggered 10x = Rising edge triggered 11x = Both edge triggered
EINT4	[18:16]	Setting the signaling method of the EINT4. 000 = Low level interrupt 001 = High level interrupt 01x = Falling edge triggered 10x = Rising edge triggered 11x = Both edge triggered
EINT3	[14:12]	Setting the signaling method of the EINT3. 000 = Low level interrupt 001 = High level interrupt 01x = Falling edge triggered 10x = Rising edge triggered 11x = Both edge triggered
EINT2	[10:8]	Setting the signaling method of the EINT2. 000 = Low level interrupt 001 = High level interrupt 01x = Falling edge triggered 10x = Rising edge triggered 11x = Both edge triggered
EINT1	[6:4]	Setting the signaling method of the EINT1. 000 = Low level interrupt 001 = High level interrupt 01x = Falling edge triggered 10x = Rising edge triggered 11x = Both edge triggered
EINT0	[2:0]	Setting the signaling method of the EINT0. 000 = Low level interrupt 001 = High level interrupt 01x = Falling edge triggered 10x = Rising edge triggered 11x = Both edge triggered

NOTE: Because each external interrupt pin has a digital filter, the interrupt controller can recognize a request signal that is longer than 3 clocks.

EXTINTPND (EXTERNAL INTERRUPT PENDING REGISTER)

The external interrupt requests(4, 5, 6, and 7) are 'OR'ed to provide a single interrupt source to interrupt controller. EINT4, EINT5, EINT6, and EINT7 share the same interrupt request line(EINT4/5/6/7) in interrupt controller. If each of the 4 bits in the external interrupt request is generated, EXTINTPNDn will be set as 1. The interrupt service routine must clear the interrupt pending condition(INTPND) after clearing the external pending condition(EXTINTPND). EXTINTPND is cleared by writing 1.

Register	Address	R/W	Description	Reset Value
EXTINTPND	0x01D20054	R/W	External interrupt pending Register	0x00

Table 8-11. D[15:0] Pull-Up Control Register (PUPS)

PUPS	Bit	Description
EXTINTPND3	[3]	If EINT7 is activated, EXINTPND3 bit is set to 1, and also INTPND[21] is set to 1.
EXTINTPND2	[2]	If EINT6 is activated, EXINTPND2 bit is set to 1, and also INTPND[21] is set to 1.
EXTINTPND1	[1]	If EINT5 is activated, EXINTPND1 bit is set to 1, and also INTPND[21] is set to 1.
EXTINTPND0	[0]	If EINT4 is activated, EXINTPND0 bit is set to 1, and also INTPND[21] is set to 1.