

WM-G-MR-09
Application Circuit
WLAN 802.11b/g 8.2mmx8.4mm SiP Module

Block Diagram

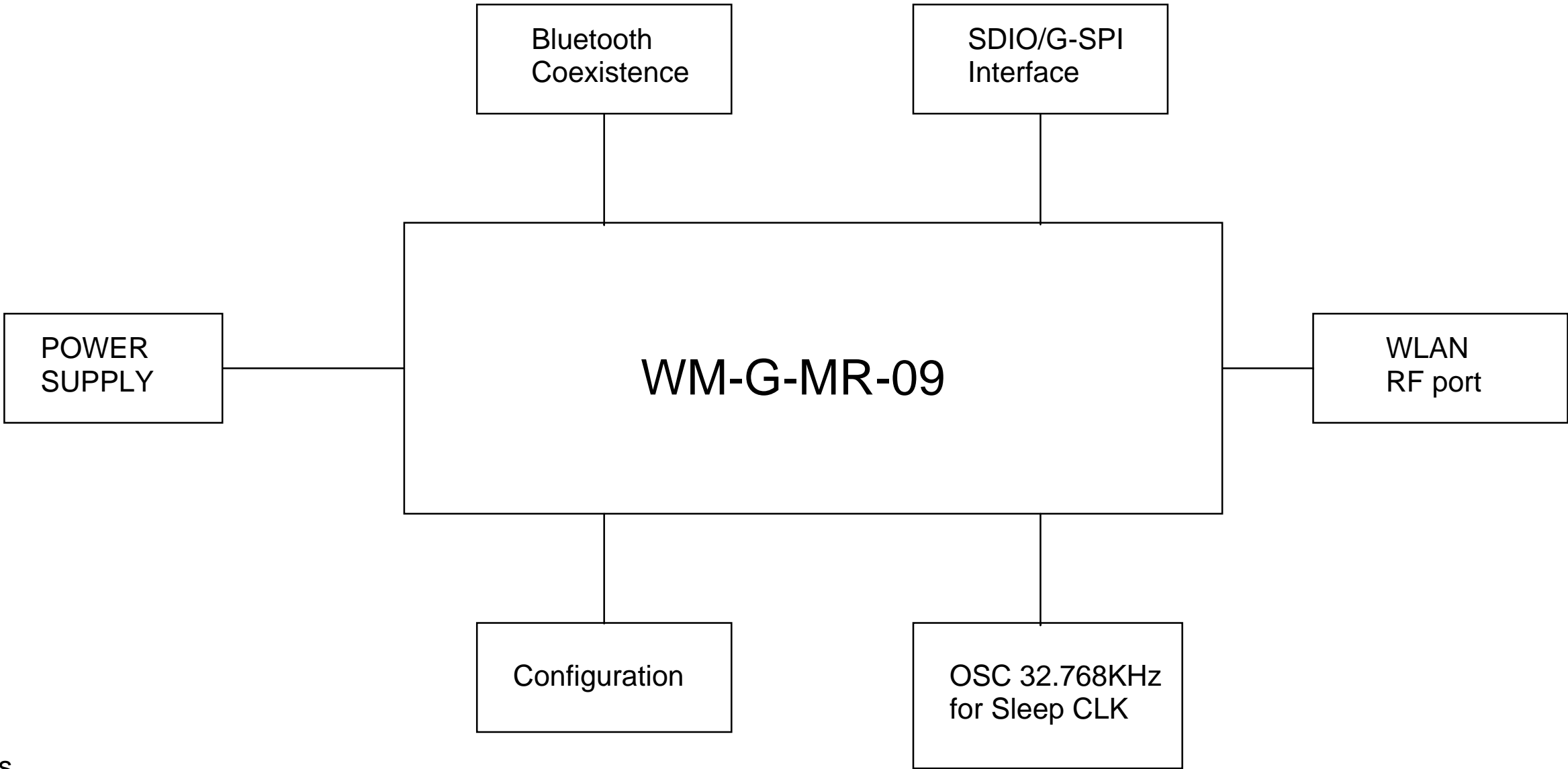
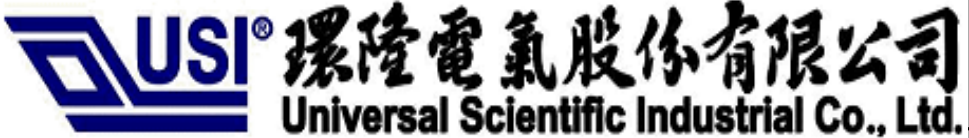


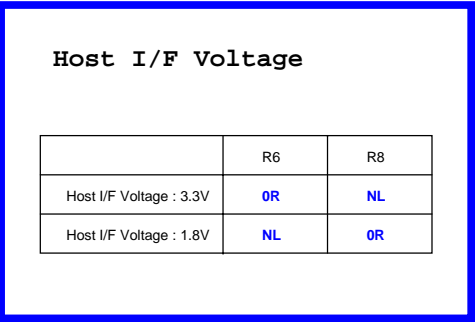
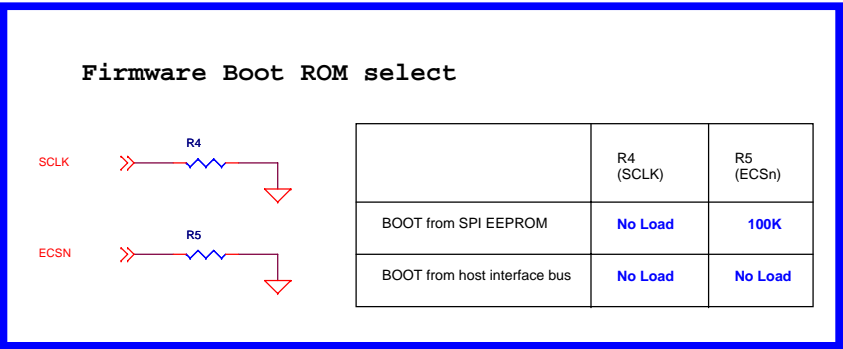
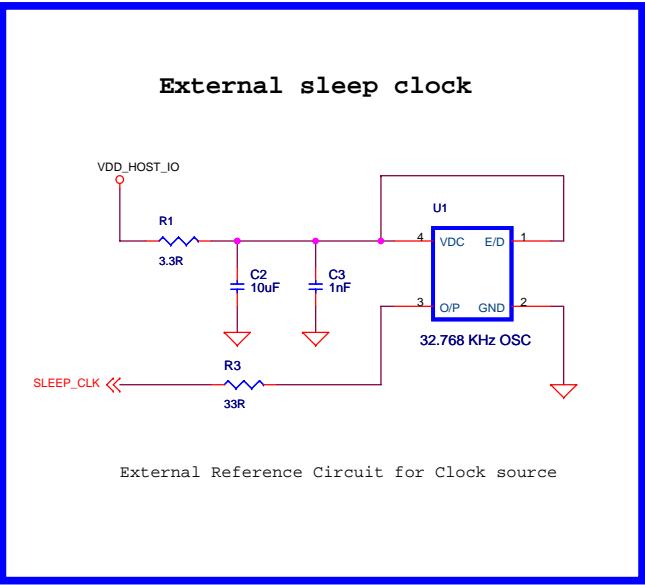
Table of Contents

- 1 Blockdiagram
- 2 Schematic
- 3 Bluetooth Coexistence
- 4 Change History



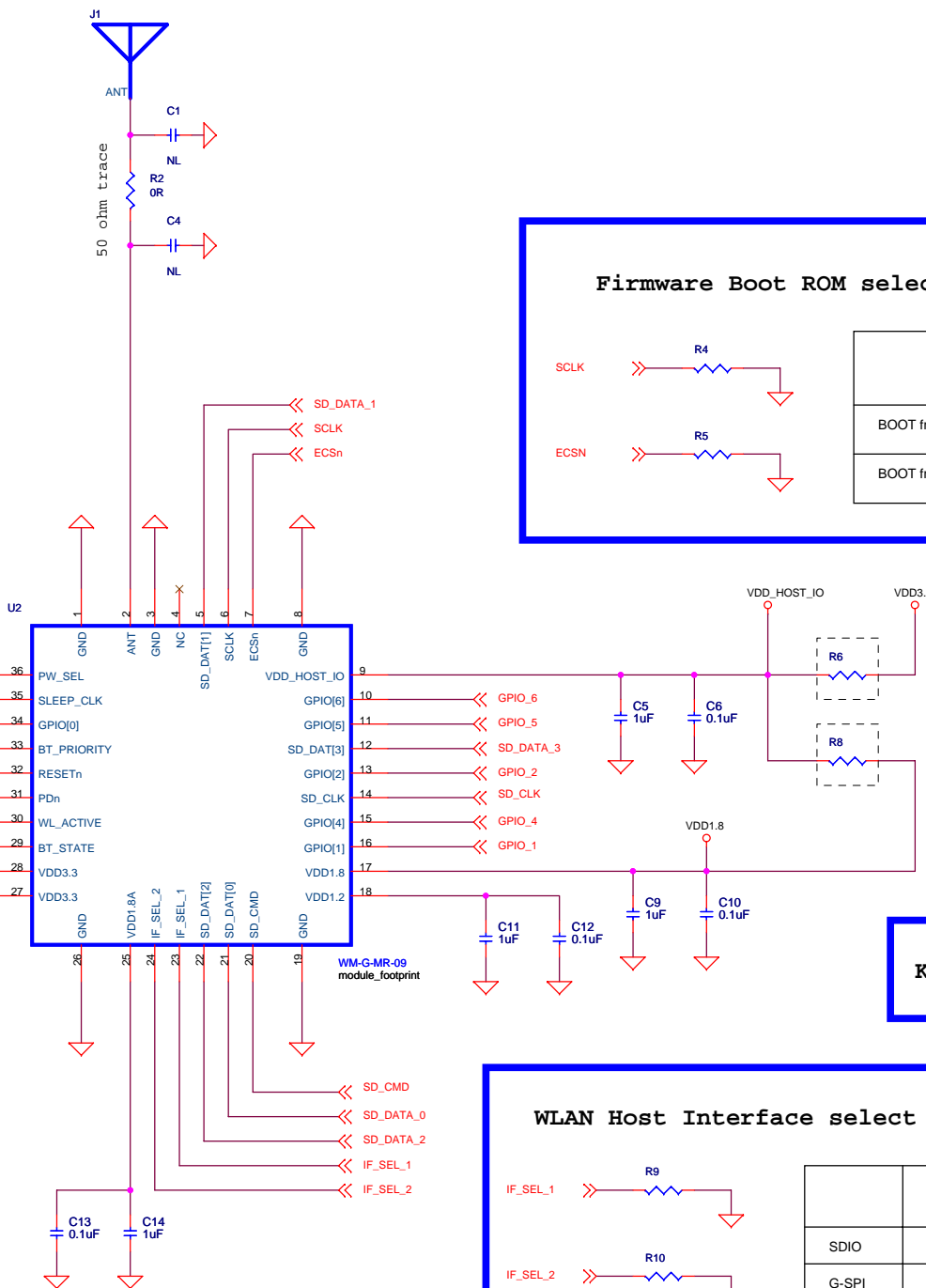
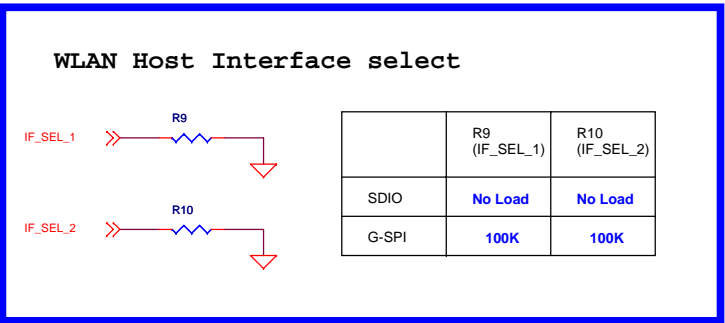
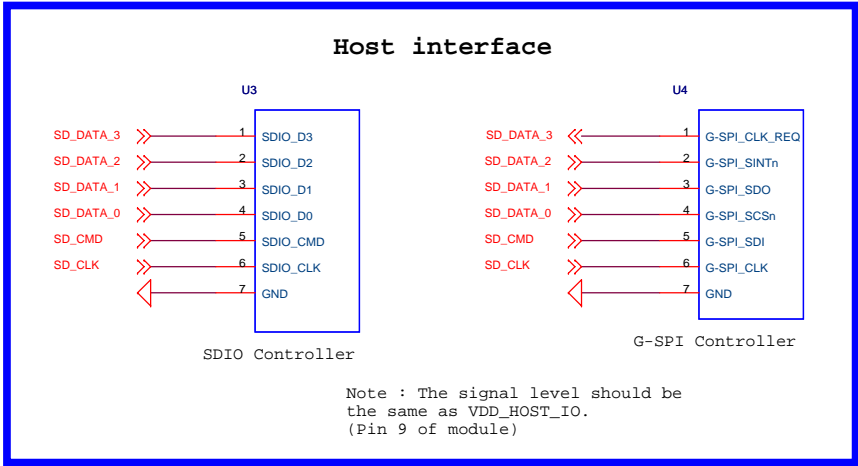
Design Engineer : Camus Chen

Title			WM-G-MR-09 Application Circuit		
Size	Document Number				Rev
	<Doc>				0.2
Date:			Friday, October 12, 2007		
Sheet			1 of 4		

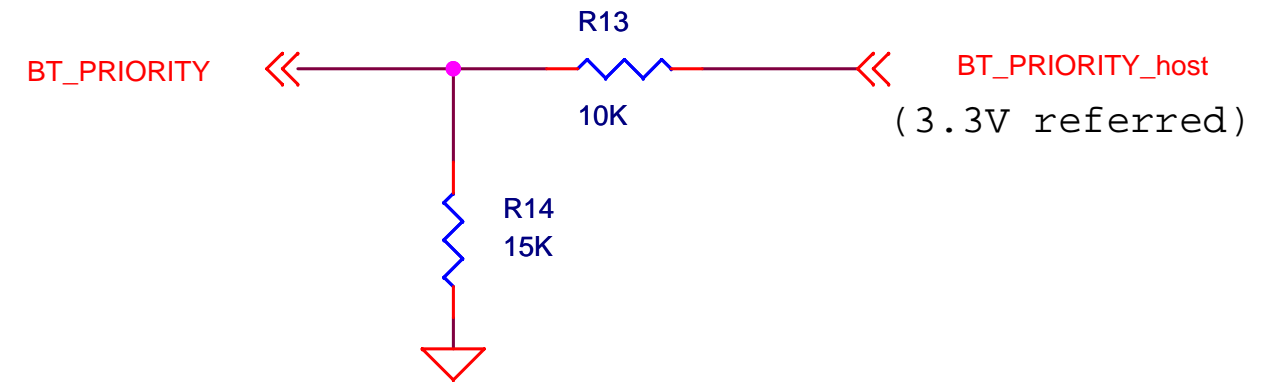
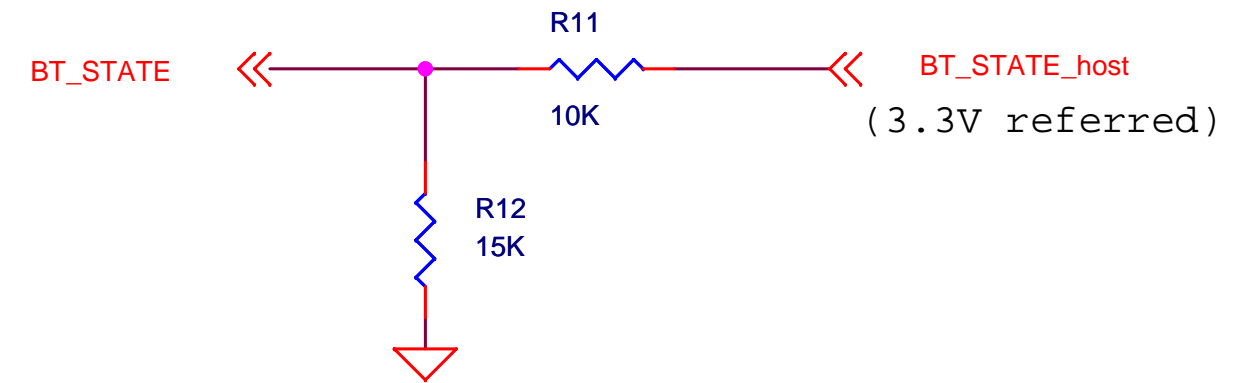
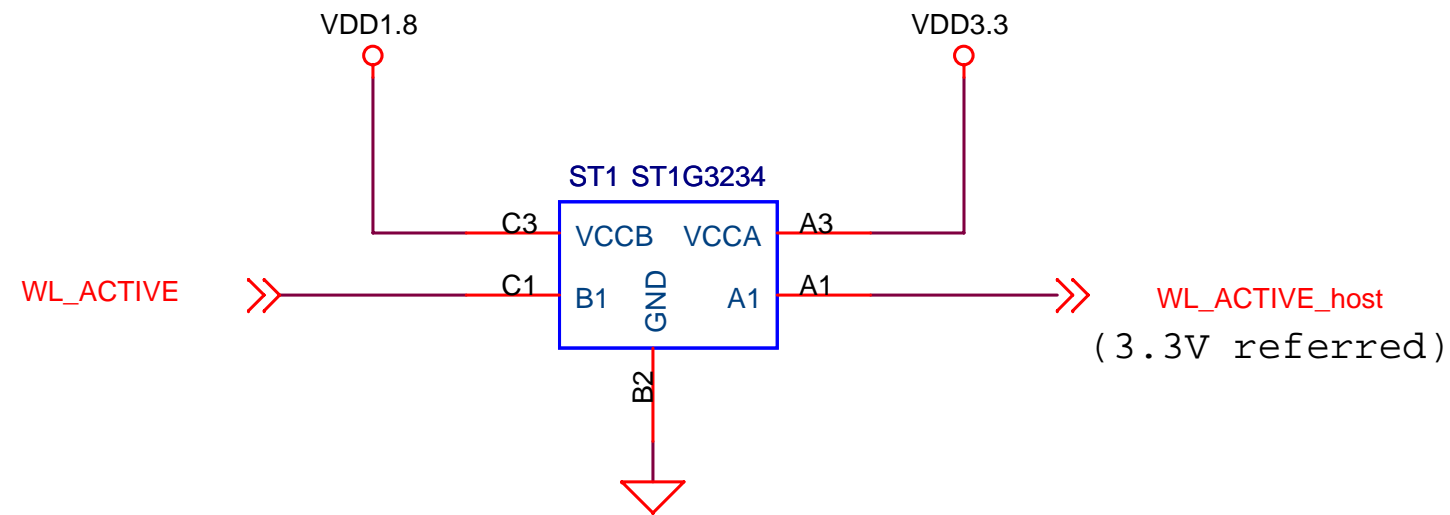


Power

VDD_3.3 : Max Current rating = 300 mA

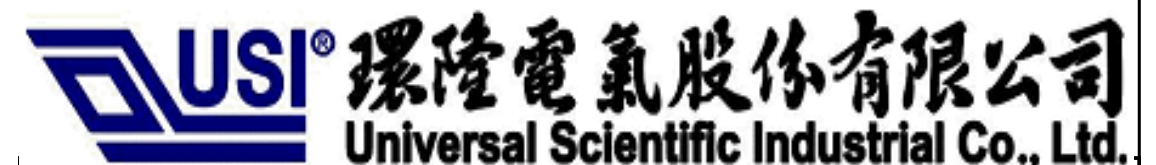


Level of WL_ACTIVE, BT_STATE
and BT_PRIORITY are 1.8V



WL_ACTIVE	O	Bluetooth WLAN Active 2-Wire BCA Mode: When high, WLAN is transmitting or receiving packets. 3-Wire BCA Mode: 0 = Bluetooth device allowed to transmit 1 = Bluetooth device not allowed to transmit In 3/4WBCA mode, the signal output is programmable and can be low during both Bluetooth Rx and Tx timeslots. This pin drives low when PDn is asserted. In WLAN sleep mode, all I/O pads are powered down. This pad will stay at a low state when in power down mode.
BT_PRIORITY	I	Bluetooth Priority 2-Wire BCA Mode: When high, Bluetooth is transmitting or receiving high priority packets. 3-Wire BCA Mode: When high, Bluetooth is requesting to transmit or receive packets.
BT_STATE	I	Bluetooth State 0 = normal priority, Rx 1 = high priority, Tx BT_STATE is used to input the Bluetooth priority and direction of traffic following the assertion of the BT_PRIORITY input.

3



Design Engineer : Camus Chen


Title
WM-G-MR-09 Application Circuit

Size	Document Number <Doc>	Rev 0.2
------	--------------------------	------------

Date:	Friday, October 12, 2007	Sheet	3	of	4
-------	--------------------------	-------	---	----	---

Change History

- 20070629: First Release
- 20070914: U2 pin4 change to NC
U2 pin9 change to VDD3.3
Remove VDD_HOST_IO, R6, R8
Leave U2 pin4 & pin 36 as NC
- 20070917: Restore R6 & R8
- 20071012: U2 pin9 restore to VDD_HOST_IO
Swap ST1G3234 pin A1, A3 and C1, C3
Sleep clock powered by VDD_HOST_IO
Add level description for WL_ACTIVE, BT_STATE and BT_PRIORITY



環隆電氣股份有限公司
Universal Scientific Industrial Co., Ltd.

Design Engineer : Camus Chen

Title WM-G-MR-09 Application Circuit		
Size	Document Number <Doc>	Rev 0.1
Date:	Friday, October 12, 2007	Sheet 4 of 4