# Data Sheet
# of 802.11g
# WM-G(B)-MR-08 Wireless Lan Module

# Introduction

The 802.11 Wireless SiP module WM-G-MR-08 which refers as “SiP-g module” is a full function 54 Mbps wireless networking module that provides PC Card 16 bit /CF+, host interface via 70 pins surface mount type solder balls for direct soldering assembly. The host interface can be set at factory to enables different system interface, which is flexible for system/processor’s resource management.

The small size & low profile physical design make it easier for system design to enable high performance wireless connectivity without space constrain . The low power consumption and excellent radio performance make it the best solution for OEM customers who require embedded 802.11g Wi-Fi features, such as, Wireless PDA, Scanner Smart phone, Media player Notebook, barcode ,mini-Printer, VoIP phone etc.

For hardware feature, Marvell “Libertas” chipset solution is used. The ZERO IF radio architecture & high integration MAC/BB chip provide excellent sensitivity with rich system performance.
WM-G-MR-08 provides outstanding BT WiFi co-existence solution through 2 wires , 3 wires hardware interface to optimized connection with 3’rd party BT module even without good antenna isolation between BT & WiFi module.

In addition to WEP 64/128, WPA and TKIP, AES is supported to provide the latest security requirement on your network.

For the software and driver development, USI provides extensive technical document and reference software code for the system integration under the agreement of Marvell International Ltd.

Hardware evaluation kit and development utilities will be released base on listed OS and processors to OEM customers.

## Features

- Lead Free design which supporting Green design requirement. RoHS Compliance.
- 2 wires , 3 wires QoS aware hardware signaling BT WiFi co-existence supported.
- Small size suitable for low volume system integration.
- Low power consumption & excellent power management performance, extend battery life.
- 2.412-2.484 GHz two SKUS for worldwide market.
- Easy for integration into mobile and handheld device with flexible system configuration and antenna design.

| Change Sheet | | | | | |
|---|---|---|---|---|---|
| Rev. | Date | Description of change | | | Approval & Date |
| | | Page | Par | Change(s) | |
| 1.0 | 04/20/07 | All | All | Draft version for Review | |
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## 1. EXECUTIVE SUMMARY

WM-G-MR-08 802.11g/(b) Wireless module is the solution which targeting for system customer who require small size & cost effective 802.11g solution. This module is part of the embedded wireless module product line offered by USI communication BU.

The WM-G-MR-08 module providing Surface mount type IO interface for assembly. This product is designated for use in embedded applications mainly in the mobile device, which required, small size and high data rate wireless connectivity. The application such as, Wireless PDA, DSC, Media Adapter, Barcode scanner, mini-Printer, VoIP phone, Data storage device could be the potential application for wireless WM-G-MR-08.

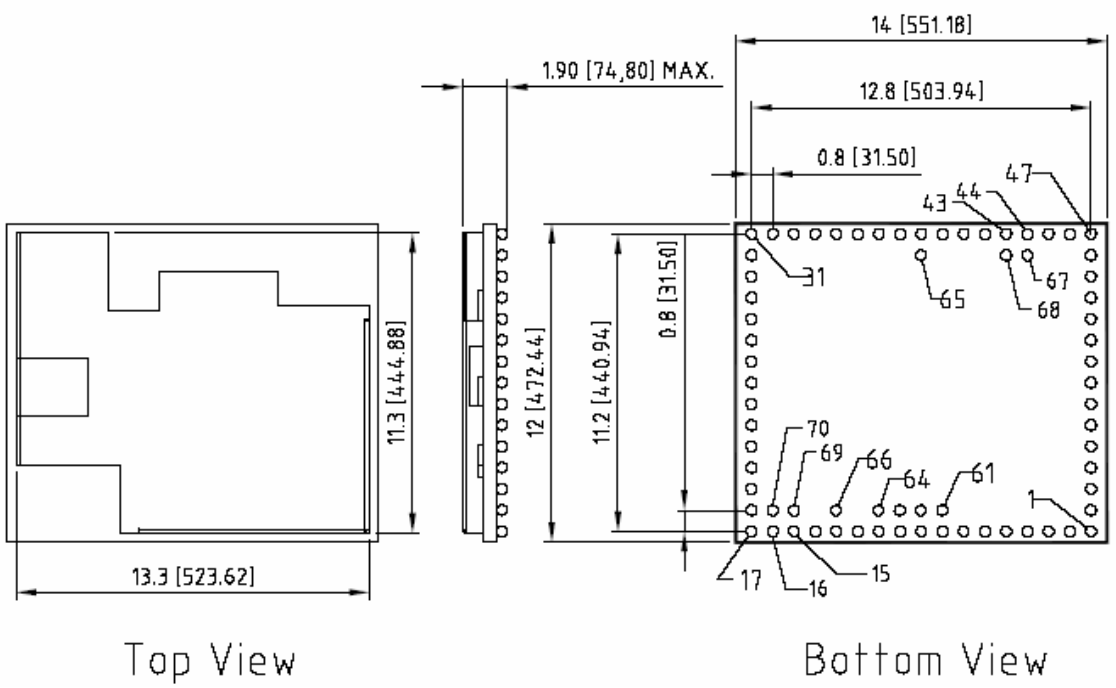
# 2. MAJOR SPECIFICATION

### WM-G-MR-08 MAJOR SPECIFICATION IN RF PERFORMANCE AND CURRENT CONSUMPTION

| Model Number | **WM-G-MR-08** |
|---|---|
| Product Name | 802.11g SIP Module |
| Interface | CF+/CF 1.4<br>SDIO 1.0 |
| Main Chips | 88W8385<br>88W8015 |
| Package | 70 pins BGA |
| Wireless Standard | IEEE 802.11b+g |
| Tx Power (minimum) | 12 dBm@54Mbps |
| Sensitivity (minimum) | -68dBm @54Mbps |
| OSs Support | WinCE 4.2/5.0<br>Pocket PC 2003<br>Linux 2.4.20 above |
| Current consumption @ 12 dBm Measured on demo-board | Transmit continuous mode : 536mA @ Maximum<br>packet mode : 238mA @ Average<br>Receive: 320mA @ Maximum<br>258mA @ Average<br>PS : 21mA (internal sleep clock)<br>PS : 1mA (external sleep clock)<br>Full power down: 0.6mA |
| Dimensions | 12 x 14 x 1.9 mm |

## 2.2 MECHANICAL CHARACTERISTICS

Overall Dimensions (Unit: mm)




Note: Ball pitch is 0.8 mm and with 0.5 mm ball diameter

# 3 PINOUTS AND SIGNAL DESCRIPTIONS

This section describes module signals and the associated pins.

## 3.1 PIN DEFINITIONS

### 3.1.1 Package- and interface-independent pins

| Module Pin(s) | Signal Name | Direction | Description | Remarks |
|---|---|---|---|---|
| 1 | ANT1 | -- | Antenna RF port 1, for transmission and reception, 50 ohms | |
| 3 | ANT2 | -- | Antenna RF port 2, for reception only, 50 ohms | |
| 40, 42 | AGC1, AGC2 | | Automatic gain control configuration pins | |
| 50 | VIO | I | 3.3 volt clamping | |
| 41 | LED | O | Module status LED controller output<br>LED Off: Open drain internal 200k ohms<br>LED On: Low-Z current sink, 8.76 mA typical | |
| 65 | PDn | | For Full Power Down feature | |
| 66 | VDDSHI | Power | Digital I/O power supply. Covers the serial host interface of SPI and SDIO. When using SDIO or SPI, can be between 1.8 and 3.3V. | |

### 3.1.2 CF interface

| Module Pin | Signal Name | Dir. | Description | Remarks |
|---|---|---|---|---|
| 57 | A0 | I | Address 0 | CF address A0-A10 |
| 58 | A1 | I | Address 1 | |
| 59 | A2 | I | Address 2 | |
| 6 | A3 | I | Address 3 | |
| 7 | A4 | I | Address 4 | |
| 8 | A5 | I | Address 5 | |
| 9 | A6 | I | Address 6 | |
| 10 | A7 | I | Address 7 | |
| 15 | A8 | I | Address 8 | |
| 17 | A9 | I | Address 9 | |
| 22 | A10 | I | Address 10 | |
| 51 | -STSCHG | I/O | Card status changed. Active low. Its use is controlled by the Card Configuration and Status Register. | |
| 24 | -CE1 | I | Card enable 1 | |
| 21 | -CE2 | I | Card enable 2 | |
| 56 | D0 | I/O | Data 0 | CF data D0-D15 |

| | | | | |
|---|---|---|---|---|
| 54 | D1 | I/O | Data 1 | |
| 12 | D2 | I/O | Data 2 | |
| 32 | D3 | I/O | Data 3 | |
| 31 | D4 | I/O | Data 4 | |
| 29 | D5 | I/O | Data 5 | |
| 27 | D6 | I/O | Data 6 | |
| 25 | D7 | I/O | Data 7 | |
| 55 | D8 | I/O | Data 8 | |
| 53 | D9 | I/O | Data 9 | |
| 52 | D10 | I/O | Data 10 | |
| 30 | D11 | I/O | Data 11 | |
| 28 | D12 | I/O | Data 12 | |
| 26 | D13 | I/O | Data 13 | |
| 11 | D14 | I/O | Data 14 | |
| 23 | D15 | I/O | Data 15 | |
| 48 | -INPACK | O | Input port acknowledge | |
| 18 | -IORD | I | IO/read | |
| 16 | -IOWR | I | I/O write | |
| 20 | -OE | I | Output enable | |
| 38 | IREQ | O | Interrupt request | |
| 5 | -REG | I | Register select and I/O enable | |
| 39 | RESET | I | Positive reset | |
| 33 | VCC | -- | +3.3V power | |
| 34 | VCC | -- | +3.3V power | |
| 35 | VCC | -- | +3.3V power | |
| 46 | VCC | -- | +3.3V power | |
| 47 | VCC | -- | +3.3V power | |
| 13 | -WAIT | O | Extend bus cycle | |
| 49 | -WE | I | Write enable | |
| 14 | -IOIS16 | I/O | I/O port is 16 bits | |
| 2, 4, 36, 37, 43, 44, 45, 60 | GND | | Ground | |

### 3.1.3 SDIO interface (4-bit and 1-bit modes)

| SD Pin | Module Pin(s) | SD 4-bit Mode | | SD 1-bit Mode | |
|---|---|---|---|---|---|
| 1 | 16 | CD/DAT[3] | Data line 3 | N/C | Not used |
| 2 | 20 | CMD | Command line | CMD | Command line |
| 3 | 2, 4, 36, 37, 43, 44, 45, 60 | VSS1 | Ground | VSS1 | Ground |
| 4 | 33, 34, 35, 46, 47 | VDD | Supply voltage | VDD | Supply voltage |
| 5 | 21 | CLK | Clock, up to 25MHz | CLK | Clock |
| 6 | 2, 4, 36, 37, 43, 44, 45, 60 | VSS2 | Ground | VSS2 | Ground |
| 7 | 19 | DAT[0] | Data line 0 | DATA | Data line |

| | | | | | |
|---|---|---|---|---|---|
| 8 | 18 | DAT[1] | Data line 1 or interrupt (optional) | IRQ | Interrupt |
| 9 | 17 | DAT[2] | Data line 2 or Read Wait (optional) | RW | Read Wait (optional) |

### 3.1.4 GSPI interface

| GSPI Pin(s) | GSPI Pin name | Module Pin(s) | Description |
|---|---|---|---|
| 1 | SPI_RSTn | 69 | SPI Unit Reset Input |
| 2 | Sleep_CLK | 70 | External Sleep Clock Input |
| 3 | SPI_CLK_EN | 14 | SPI Unit Clock Enable Output |
| 4 | SPI_SCSn | 19 | SPI Unit Active Low Chip Select Input |
| 5 | SPI_INIn | 17 | SPI Unit Active Low Interrupt Output |
| 6 | SPI_SDO | 18 | SPI Unit Data Output |
| 7 | SPI_SDI | 20 | SPI Unit Data Input |
| 8 | SPI_CLK | 21 | SPI Unit Clock Input |

**External Sleep Clock Circuit diagram refer to Section 8**

### 3.1.5 Bluetooth (BT) coexistence interface (BCI) pins (three-wire QoS-aware BCI and two-wire Cambridge Silicon Radio [CSR] BCI)

| Module Pin(s) | Pin name | Direction | 3-wire QoS-aware BCI | 2-wire CSR BCI |
|---|---|---|---|---|
| 61 | WL-Active | Output | BT_Tx_CONFIRM | WL_ACTIVE |
| 62 | BT-Priority | Input | BT_REQ | BT-Priority: BT active with high priority packet |
| 63 | NC | | | |
| 64 | BT-State | Input | BT Priority and RX/TX info | N/A |

### 3.1.6 Additional pins

| Module Pin(s) | Pin name | Direction | Remarks |
|---|---|---|---|
| 67 | ANT_SEL-P | O | For second antenna design, differential antenna selects positive output. |
| 68 | ANT_SEL-N | O | For second antenna design, differential antenna selects negative output. |

## 4 DC ELECTRICAL AND CURRENT CONSUMPTION

### 4.1 Absolute Maximum Ratings

| Item | Symbol | Value | Unit |
|---|---|---|---|
| Supply Voltage | VCC | +3.6 | V |
| Input Voltage | Vin | -0.5~VCC+0.5 | V |
| Storage Temperature | T_st | -20~+85 | ° C |

### 4.2 Recommended Operating Conditions

| Item | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Supply Voltage | VCC | 2.8 | 3.3 | 3.6 | V |
| Operating Temperature | T_op | -10 | | +70 | ° C |

### 4. 3 DC Electricals

VDD=3.3V

| Item | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Input Low Voltage | $V_{IL}$ | -0.5 | 0.35VDD | V |
| Input High Voltage | $V_{IH}$ | 0.5VDD | VDD+0.5 | V |
| Output Low Voltage | $V_{OL}$ | | 0.4 | V |
| Output High Voltage | $V_{OH}$ | 2.4 | | V |
| Hysteresis | $V_{HYS}$ | 200 | | mV |

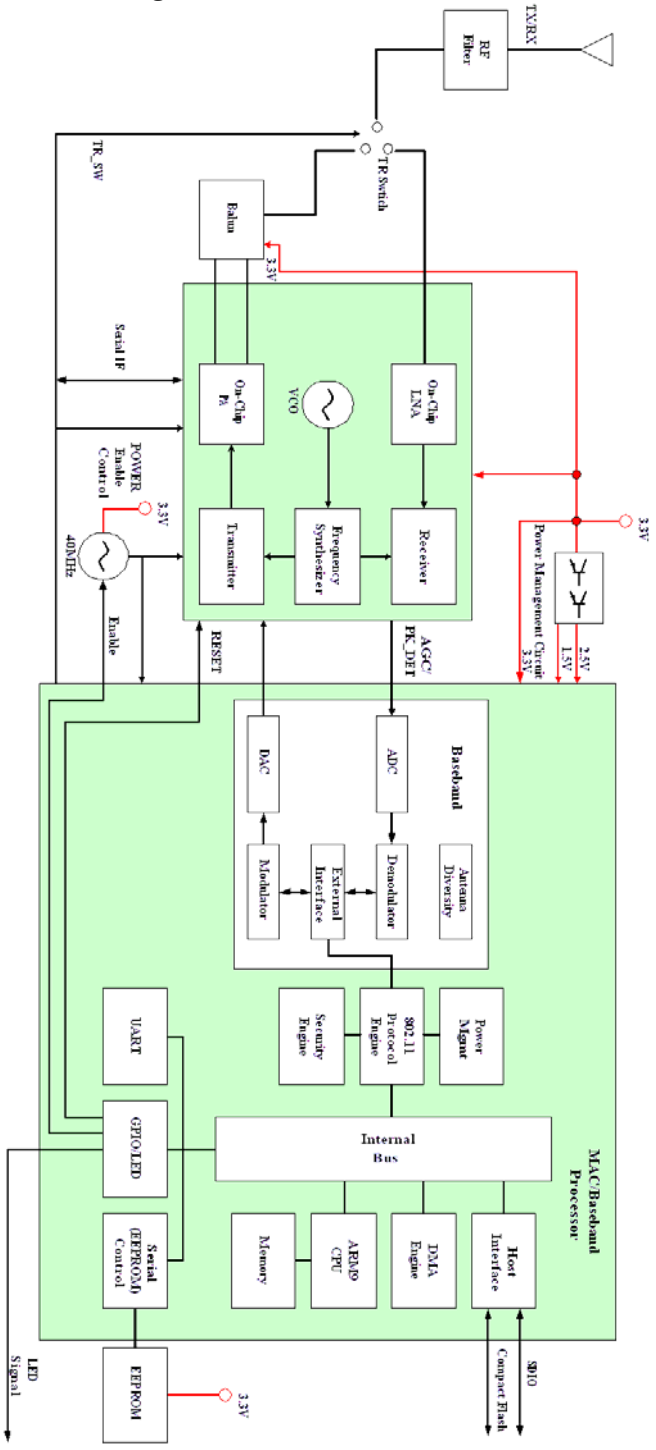
### 4.4 AC Electricals

VDD=3.3V

| Item | Symbol | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|
| Switching Current High | $I_{OH}$ | 11.3 | 32 | mA | 0.7VDD=2.31V |
| Switching Current Low | $I_{OL}$ | 10.5 | 38 | mA | 0.18VDD=0.6V |
| Output Rise Slew Rate | $T_{SLEW\_RISE}$ | 0.518 | 4.0 | V/ns | 0.2VDD-0.6VDD |
| Output Fall Slew Rate | $T_{SLEW\_FALL}$ | 0.592 | 4.0 | V/ns | 0.6VDD-0.2VDD |

# 5. MODULE BLOCK DIAGRAMS

WM-G-MR-08 Block Diagram

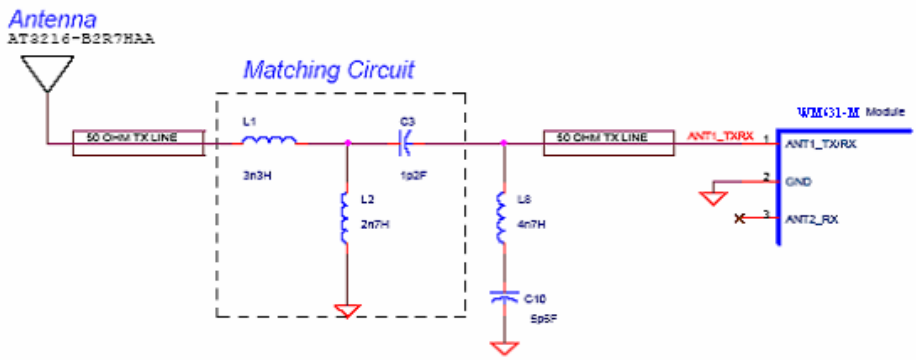


# 6. REFERENCE DESIGNS

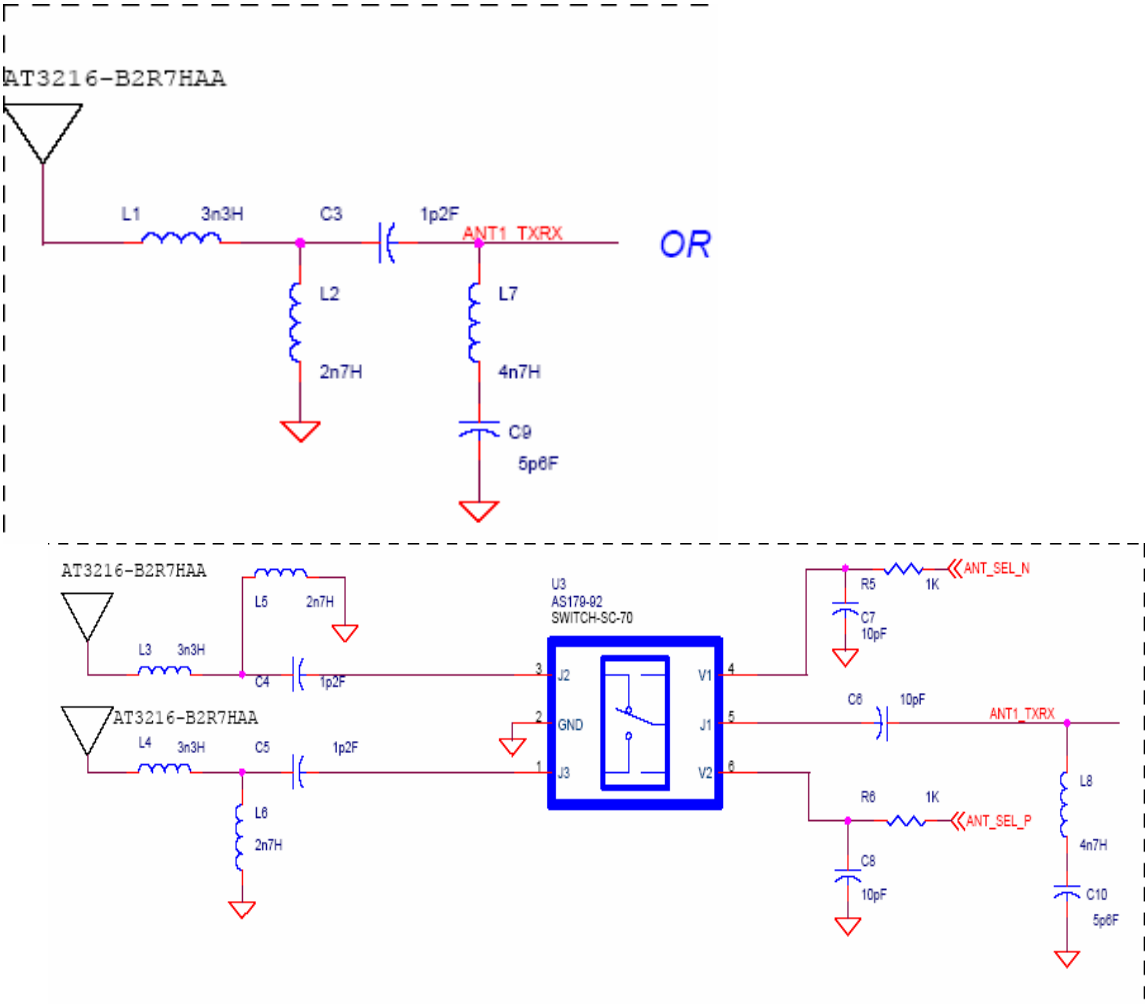
This section contains reference designs for single-antenna, dual-antenna, and full-power-down implementations.

Values given for components in matching circuits are antenna dependent.

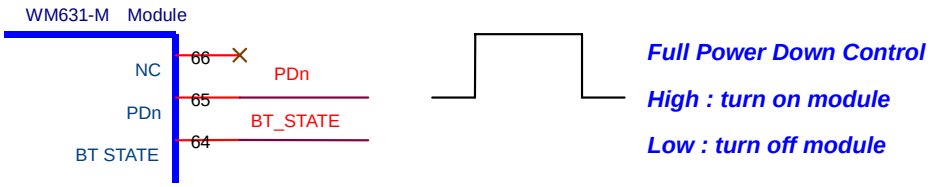
Single-antenna cable path for all modules. Note that pin 3, ANT2_RX, must be connected as shown here.



## 6.1 DUAL ANTENNA CABLE PATH DESIGNS




## 6.2 REFERENCE DESIGN FOR FULL POWER DOWN FEATURE. PULL PDN HIGH TO TURN THE MODULE ON, AND PULL IT LOW TO TURN THE MODULE OFF.



### 6.3 PIN 40 AND 42 LAYOUT FOR DIFFERENT INTERFACES

| Module Pin | Signal Name | CF | SDIO | G-SPI | Remarks |
|---|---|---|---|---|---|
| 40 | AGC1 | R: 100 K ohm | NL (Not assemble) | NL (Not assemble) | |
| 42 | AGC2 | NL (Not assemble) | R: 100 K ohm | NL (Not assemble) | |

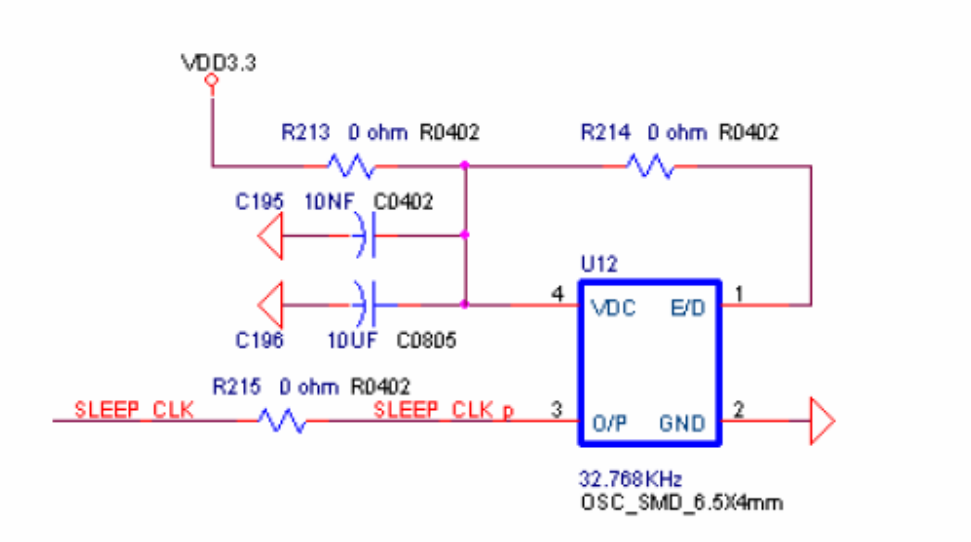
### 6.4 CUSTOMER'S PAD DESIGN RECOMMENDATION:

| Solder Mask Define Rule | Optimal SMD | Minimal SMD |
|---|---|---|
| Solder pad diameter | 0.55mm | 0.44mm |
| Solder mask opening | 0.45mm | 0.36mm |

| Non-Solder Mask Define Rule | Optimal SMD | Minimal SMD |
|---|---|---|
| Solder pad diameter | 0.55mm | 0.44mm |
| Solder mask opening | 0.45mm | 0.36mm |

## 6.5 EXTERNAL SLEEP CLOCK CIRCUIT DIAGRAM

The implementation of external sleep clock can reach low power consumption as full power down mode.



## 7 RELIABILITY

The WM-G-MR-08 module guarantee an MTBF of 150,000 hrs based on an ambient temperature and workload of 2,920 hours. The workload is based on a unit working for 8 hours per day, 365 days per year.
The MTBF estimation base on is Bell code standard, Class II.

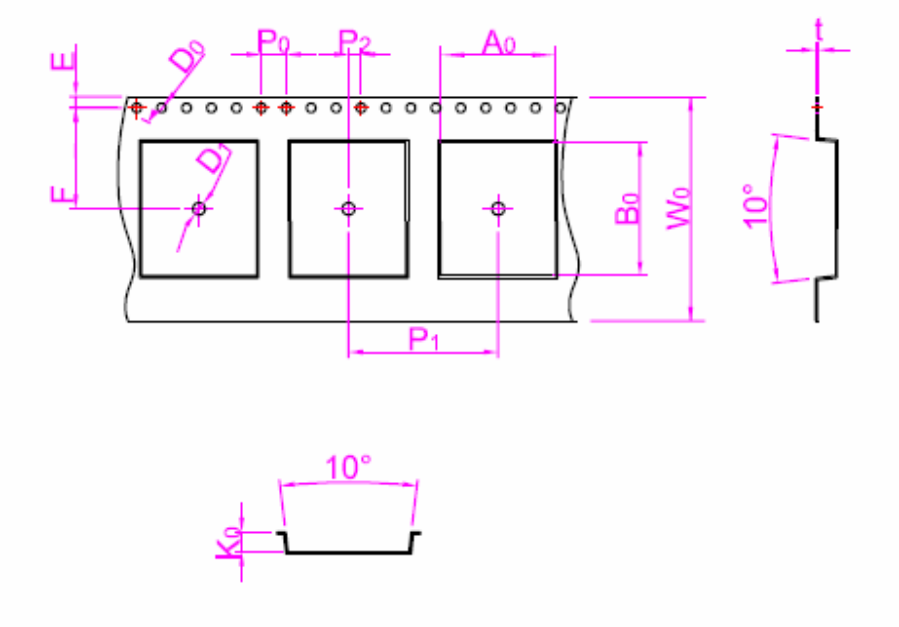
## 8 PACKAGE & STORAGE CONDITION

8.1 Package Dimension


8 .2 ESD Level

Note:

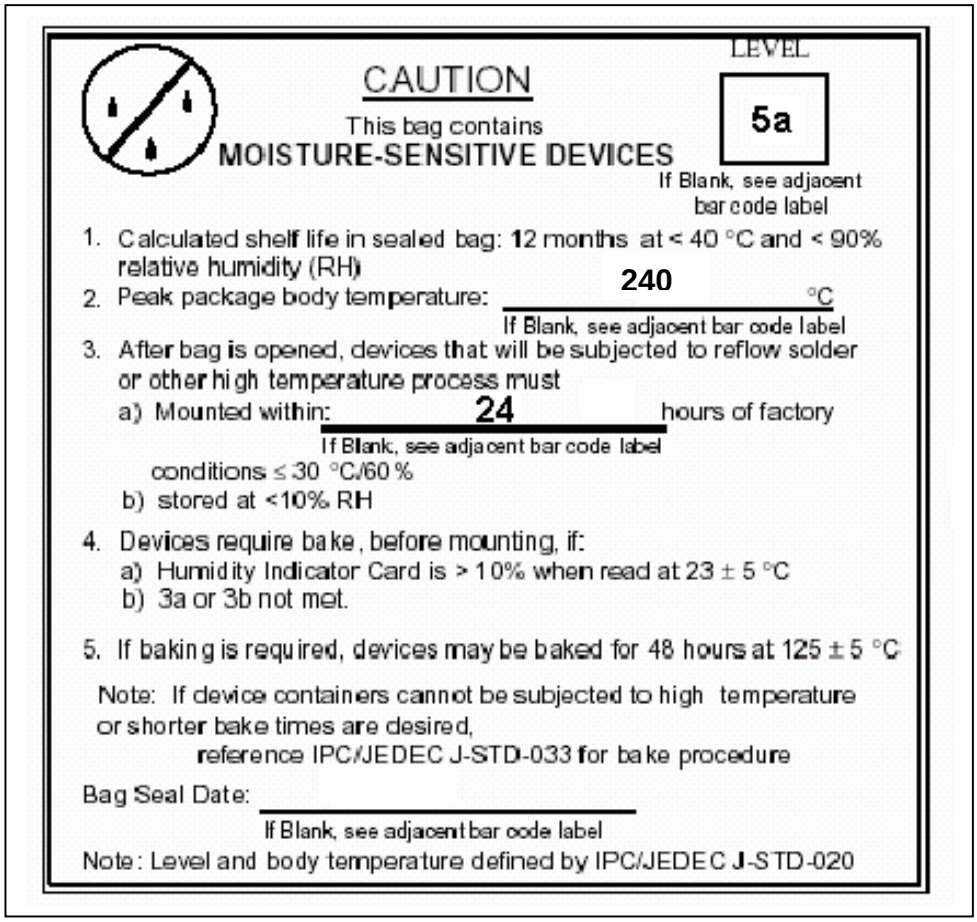
1. Surface Resistivity:
   Interior:$10^{9}$~$10^{11}\,\Omega$/SQUARE
   EXTERIOR:$10^{8}$~$10^{12}\,\Omega$/SQUARE
2. Dimension:475*420mm
3. Tolerance:+5,0mm
4. Color:
   Background : Gray
   Text : Red




| ITEM | $A_0$ | $B_0$ | $D_0$ | $D_1$ | E | F | $K_0$ |
|---|---|---|---|---|---|---|---|
| SPEC | 12.3±0.1 | 14.3±0.1 | 1.50+0.1/-0 | 1.5+0.1/-0 | 1.75±0.1 | 11.5±0.1 | 2.1±0.1 |
| ITEM | $K_1$ | $P_0$ | $P_1$ | $P_2$ | $P_0$ X10 | t | $W_0$ |
| SPEC | | 4.00±0.1 | 16.0±0.1 | 2.00±0.1 | Cumulative Tolerance ±0.2 | 0.40±0.05 | 24±0.3 |

NOTES:
1.Material: Conductive Polystyrene (Recycle)
2.Color: Black
3.Surface resistance: $10^6$ Ohms/square 以下
3.Cumulative tolerance per 10 pictches($P_0$) is ±0.2mm.
4.Carrier camber shall be not more than 1mm per 100mm,noncumulative over 250mm
5.$A_0$ & $B_0$ are measured on the plane by 0.3 mm above the bottom of the pocket.
6.$K_0$ is measured from the inside bottom of the pocket to the top surface of the carrier.
7.Pocket position relative to sprocket hold is measured as true position of pocket, not sprocket hold.

8.3. Storage and Baking



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For Additional information, please contact the following:
***Universal Scientific Industrial Co., Ltd.***
***Headquarters***
141, Lane 351, Taiping Road, Sec. 1, Tsao-Tuen, Taiwan,
Http://www.usi.com.tw
Tel: + 886-49-2350876, 2325876
Fax: +886-49-3439561, 2337360,2351093
E-mail:usi@ms.usi.com.tw