

1	2	3	4
A	23 PA0/WKUP/USART2_CTS/UART4_TX/ETH_MII_CRS/TIM2_CH1_ETR/TIM5_CH1/TIM8_ETR 24 PA1/USART2_RTS/UART4_RX/ETH_RMII_REF_CLK/ETH_MII_RX_CLK/TIM5_CH2/TIM2_CH2 25 PA2/USART2_TX/TIM5_CH3/TIM9_CH1/TIM2_CH3/ETH_MDIO 26 PA3/USART2_RX/TIM5_CH4/TIM9_CH2/TIM2_CH4/OTG_HS_ULPI_D0/ETH_MII_COL 29 PA4/SPI1_NSS/SPI3_NSS/USART2_CK/DCMI_HSYNC/OTG_HS_SOF/I2S3_WS 30 PA5/SPI1_SCK/OTG_HS_ULPI_CK/TIM2_CH1_ETR/TIM8_CH1N 31 PA6/SPI1_MISO/TIM8_BKIN/TIM13_CH1/DCMI_PIXCLK/TIM3_CH1/TIM1_BKIN 32 PA7/SPI1_MOSI/TIM8_CH1N/TIM14_CH1/TIM3_CH2/ETH_MII_RX_DV/TIM1_CH1N/ETH_RMII_CRS_DV 67 PA8/MCO1/USART1_CK/TIM1_CH1/I2C3_SCL/OTG_FS_SOF 68 PA9/USART1_TX/TIM1_CH2/I2C3_SMBA/DCMI_D0 69 PA10/USART1_RX/TIM1_CH3/OTG_FS_ID/DCMI_D1 70 PA11/USART1_CTS/CAN1_RX/TIM1_CH4/OTG_FS_DM 71 PA12/USART1_RTS/CAN1_TX/TIM1_ETR/OTG_FS_DP 72 PA13/JTMS-SWDIO 76 PA14/JTCK-SWCLK 77 PA15/JTDI/SPI3_NSS/I2S3_WS/TIM2_CH1_ETR/SPI1_NSS	PD0/FSMC_D2/CAN1_RX PD1/FSMC_D3/CAN1_TX PD2/TIM3_ETR/UART5_RX/SDIO_CMD/DCMI_D11 PD3/FSMC_CLK/USART2_CTS PD4/FSMC_NOE/USART2_RTS PD5/FSMC_NWE/USART2_TX PD6/FSMC_NWAIT/USART2_RX PD7/USART2_CK/FSMC_NE1/FSMC_NCE2 PD8/FSMC_D13/USART3_TX PD9/FSMC_D14/USART3_RX PD10/FSMC_D15/USART3_CK PD11/FSMC_CLE/FSMC_A16/USART3_CT PD12/FSMC_ALE/FSMC_A17/TIM4_CH1/USART3_RTS PD13/FSMC_A18/TIM4_CH2 PD14/FSMC_D0/TIM4_CH3 PD15/FSMC_D1/TIM4_CH4	81 82 83 84 85 86 87 88 89 90 91 92 93 94 95 96 97 98 99
B	35 PB0/TIM3_CH3/TIM8_CH2N/OTG_HS_ULPI_D1/ETH_MII_RXD2/TIM1_CH2N 36 PB1/TIM3_CH4/TIM8_CH3N/OTG_HS_ULPI_D2/ETH_MII_RXD3/TIM1_CH3N 37 PB2/BOOT1 89 PB3/JTDO/TRACESWO/SPI3_SCK/I2S3_CK/TIM2_CH2/SPI1_SCK 90 PB4/NJTRST/SPI3_MISO/TIM3_CH1/SPI1_MISO/I2S3ext_SD 91 PB5/I2C1_SMBA/CAN2_RX/OTG_HS_ULPI_D7/ETH_PPS_OUT/TIM3_CH2/SPI1_MOSI/SPI3_MOSI/DCMI_D10/I2S3_SD 92 PB6/I2C1_SCL/TIM4_CH1/CAN2_TX/DCMI_D5/USART1_TX 93 PB7/I2C1_SDA/FSMC_NL/DCMI_VSYNC/USART1_RX/TIM4_CH2 95 PB8/TIM4_CH3/SDIO_D4/TIM10_CH1/DCMI_D6/ETH_MII_TXD3/I2C1_SCL/CAN1_RX 96 PB9/SPI2_NSS/I2S2_WS/TIM4_CH4/TIM11_CH1/SDIO_D5/DCMI_D7/I2C1_SDA/CAN1_TX 47 PB10/SPI2_SCK/I2S2_CK/I2C2_SCL/USART3_TX/OTG_HS_ULPI_D3/ETH_MII_RX_ER/TIM2_CH3 48 PB11/I2C2_SDA/USART3_RX/OTG_HS_ULPI_D4/ETH_RMII_TX_EN/ETH_MII_TX_EN/TIM2_CH4 51 PB12/SPI2_NSS/I2S2_WS/I2C2_SMBA/USART3_CK/TIM1_BKIN/CAN2_RX/OTG_HS_ULPI_D5/ETH_RMII_TXD0/ETH_MII_TXD0/OTG_HS_ID 52 PB13/SPI2_SCK/I2S2_CK/USART3_CTS/TIM1_CH1N/CAN2_TX/OTG_HS_ULPI_D6/ETH_RMII_TXD1/ETH_MII_TXD1 53 PB14/SPI2_MISO/TIM1_CH2N/TIM12_CH1/OTG_HS_DM/USART3_RTS/TIM8_CH2N/I2S2ext_SD 54 PB15/SPI2_MOSI/I2S2_SD/TIM1_CH3N/TIM8_CH3N/TIM12_CH2/OTG_HS_DP	PE0/TIM4_ETR/FSMC_NBL0/DCMI_D2 PE1/FSMC_NBL1/DCMI_D3 PE2/TRACECLK/FSMC_A23/ETH_MII_TXD3 PE3/TRACED0/FSMC_A19 PE4/TRACED1/FSMC_A20/DCMI_D4 PE5/TRACED2/FSMC_A21/TIM9_CH1/DCMI_D6 PE6/TRACED3/FSMC_A22/TIM9_CH2/DCMI_D7 PE7/FSMC_D4/TIM1_ETR PE8/FSMC_D5/TIM1_CH1N PE9/FSMC_D6/TIM1_CH1 PE10/FSMC_D7/TIM1_CH2N PE11/FSMC_D8/TIM1_CH2 PE12/FSMC_D9/TIM1_CH3N PE13/FSMC_D10/TIM1_CH3 PE14/FSMC_D11/TIM1_CH4 PE15/FSMC_D12/TIM1_BKIN	1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46
C	15 PC0/OTG_HS_ULPI_STP 16 PC1/ETH_MDC 17 PC2/SPI2_MISO/OTG_HS_ULPI_DIR/ETH_MII_TXD2/I2S2ext_SD 18 PC3/SPI2_MOSI/I2S2_SD/OTG_HS_ULPI_NXT/ETH_MII_TX_CLK 33 PC4/ETH_RMII_RX_D0/ETH_MII_RX_D0 34 PC5/ETH_RMII_RX_D1/ETH_MII_RX_D1 63 PC6/I2S2_MCK/TIM8_CH1/SDIO_D6/USART6_TX/DCMI_D0/TIM3_CH1 64 PC7/I2S3_MCK/TIM8_CH2/SDIO_D7/USART6_RX/DCMI_D1/TIM3_CH2 65 PC8/TIM8_CH3/SDIO_D0/TIM3_CH3/USART6_CK/DCMI_D2 66 PC9/I2S_CKIN/MCO2/TIM8_CH4/SDIO_D1/I2C3_SDA/DCMI_D3/TIM3_CH4 78 PC10/SPI3_SCK/I2S3_CK/UART4_TX/SDIO_D2/DCMI_D8/USART3_TX 79 PC11/UART4_RX/SPI3_MISO/SDIO_D3/DCMI_D4/USART3_RX/I2S3ext_SD 80 PC12/UART5_TX/SDIO_CK/DCMI_D9/SPI3_MOSI/I2S3_SD/USART3_CK 7 PC13 8 PC14/OSC32_IN 9 PC15/OSC32_OUT 12 PH0/PH0/OSC_IN 13 PH1/PH1/OSC_OUT	VBAT BOOT0 NRST VDD VDD VDD VDD VDD VDD VDDA VREF+ VSSA VSS VSS VSS VSS VCAP_1 VCAP_2	6 94 14 11 19 28 50 75 100 22 21 20 10 27 74 99 49 73
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