Yaotian Liu

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Education

Arizona State University 2023/08 – 2028/06 (Expected)
PhD in Computer Engineering Tempe, Arizona, US
- GPA: 4.0/4.0

Shanghai Jiao Tong University 2019/09 – 2023/06
Bachelor of Engineering in Microelectronics Science and Engineering Shanghai, China
- GPA: 3.7/4.3. Rank 19/67
- Outstanding Graduates

Work Experience

Shanghai Taize Semiconductor 2022/06 – 2022/09, 2023/03 – 2023/06
Digital IC Design Intern Shanghai, China
- Designed the micro-architecture of the data link layer of company's proprietary inter-chip connect.
- Helped to design and implement an accelerator for elliptic curve accumulation.

Research Experience

Arizona State University, ECEE 2023/08 – Now
Research Assistant, advised by Prof. Jeff Zhang Tempe, AZ, US
- **Intel University Challenge**
  - Implemented a Docker-based workflow for efficient cross-compiling.
  - Performed several experiments on the CVA6 core interrupt.
- **LLM-VeriPPA**, in submission to DAC 2024.
  - Implemented a Python-based workflow for automatically PPA (Power, Performance and Area) checking of Verilog designs.

Shanghai Jiao Tong University, Department of Micro/Nano Electronics 2023/01 – 2023/05
Final Year Project, advised by Prof. Yongfu Li Shanghai, China
- Implemented a ML-based functional ECO system, accepted by AICAS 2023.
- Implemented an ABC-based algorithm for efficient circuit pruning by removing functionally equivalent sub-circuits, which increase the performance of functional ECO.

Shanghai Jiao Tong University, AI Institute 2022/05 – 2022/09
Undergraduate Research Assistant, advised by Prof. Yunbo Wang Shanghai, China
- Implemented a reinforcement learning algorithm for automatically stock trading.
- Reproduced an baseline algorithm ytliu/FactorVAE (42 stars) from AAAI 2022.

Publications

- Liu, Y., Zhang, Y., Zhang, Q., Chen, R. and Li, Y., 2023, June. FEEP: Functional ECO synthesis with efficient patch minimization. In 2023 *IEEE 5th International Conference on Artificial Intelligence Circuits and Systems (AICAS)*.
- Thorat, K., Zhao, J., Liu, Y., Peng, H., Xie, X., Lei, B., Zhang, J. and Ding, C., 2023. Advanced Language Model-Driven Verilog Development: Enhancing Power, Performance, and Area Optimization in Code Synthesis. *arXiv preprint arXiv: 2312.01022.*

Open-Sourse Project

obsidian-pseudocode ytliu74/obsidian-pseudocode (56 stars)
- A plugin for Obsidian that facilitates the rendering of LaTeX-style pseudocode within a code block.

Skills

Programming Languages: Verilog, Python, C/C++, Javascript/Typescript.
Tech Skills: Git, Digital Logic Design, Pytorch, Linux, Matlab, Logical Synthesis.

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