CSC258: Computer Organization

Lab 1

Preparing for Lab 1

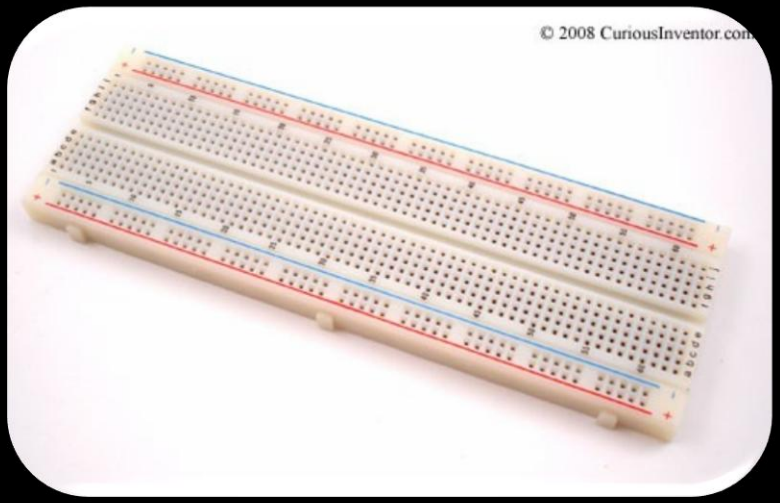
- Experience is the best teacher.
  - Preparing a design. → Pre-Lab
  - Implementing your design. → In-Lab
  - Debugging the circuit. → In-Lab

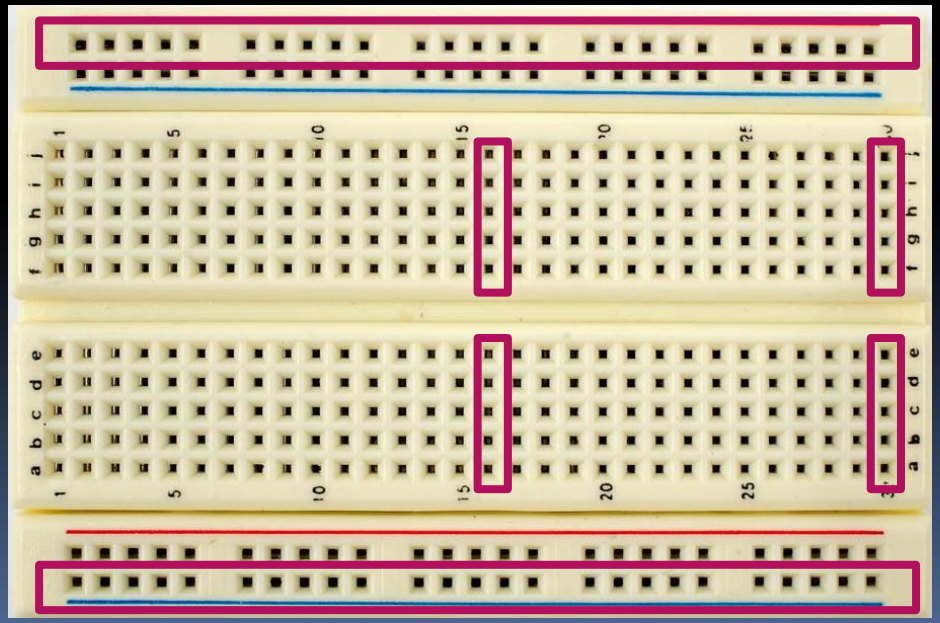
Equipment

- Breadboard
- Wires
- Gates

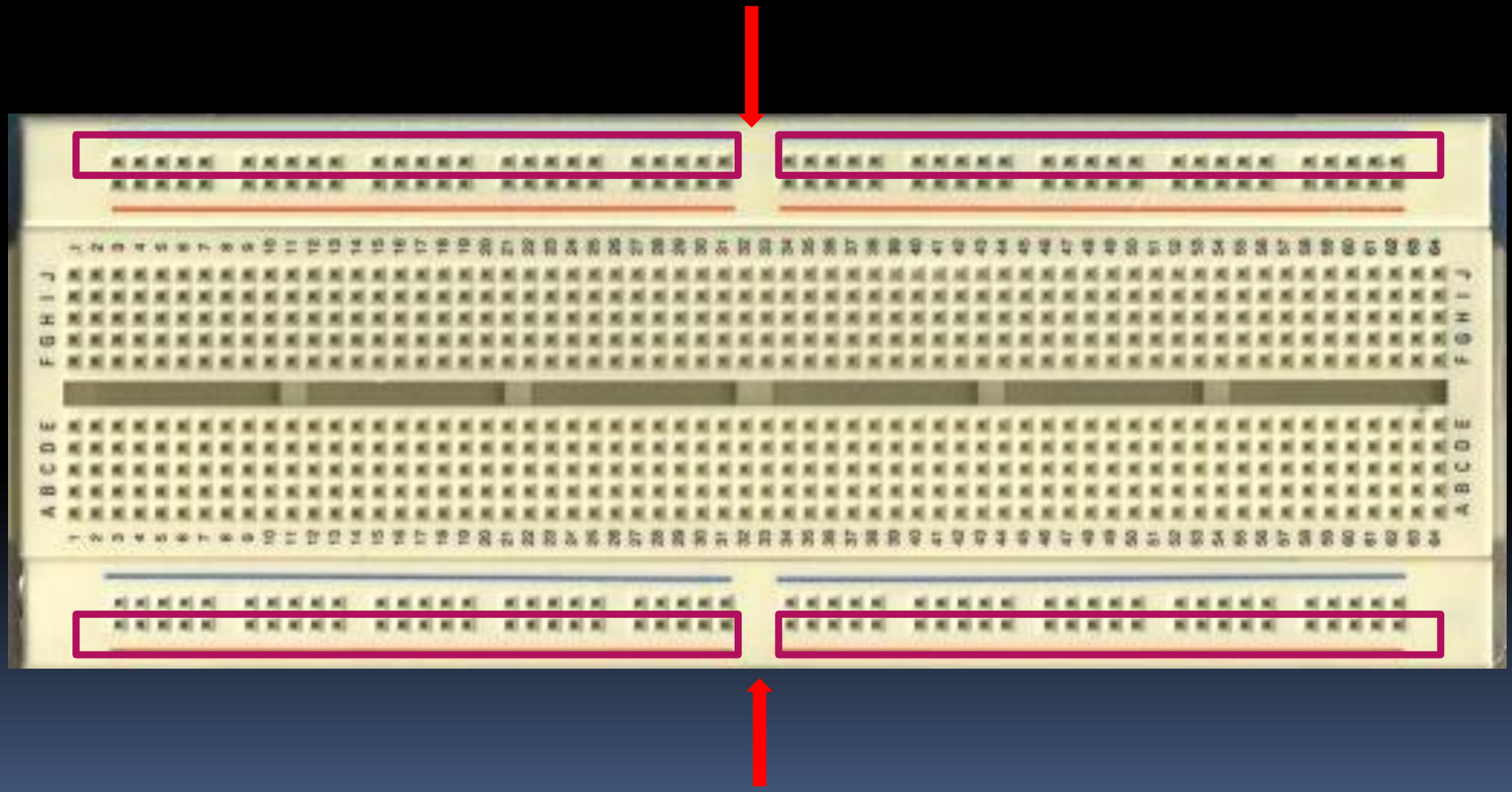
Breadboard

- The standard working area for connecting digital components together.
- Red and blue horizontal rows at top and bottom are connected.
- Columns in middle sections are connected.



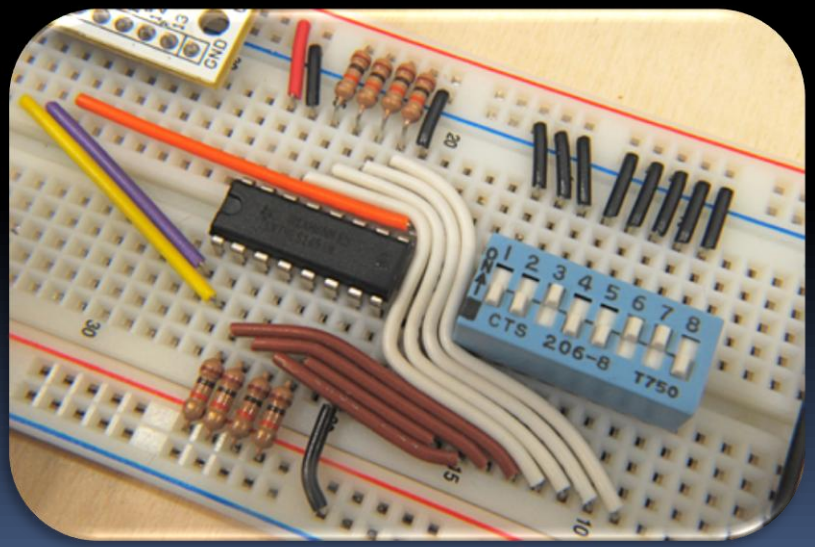


Breadboard - Caution



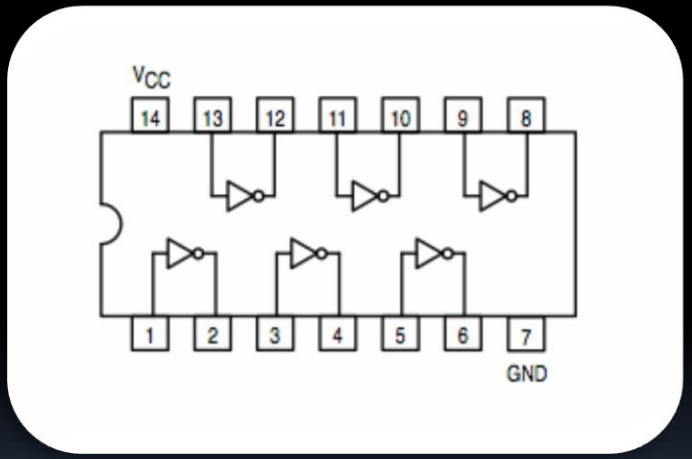
Wires

- Use this to connect different components together.
- Use the pre-cut wires whenever possible.
- Learn how to strip the coating off the end of a wire.



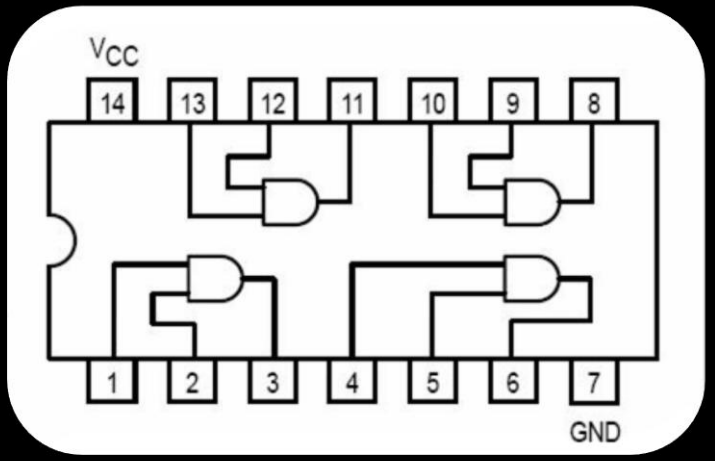
Gates

- IC chips will be supplied, which contain individual gates that you will use to create circuits.
- Example: 74LS04 (NOT)
  - Notch at one end helps determine alignment.
  - Sometimes a dot at pin #1.
  - V_{cc} and GND always have to be connected to the power source and the ground, respectively.

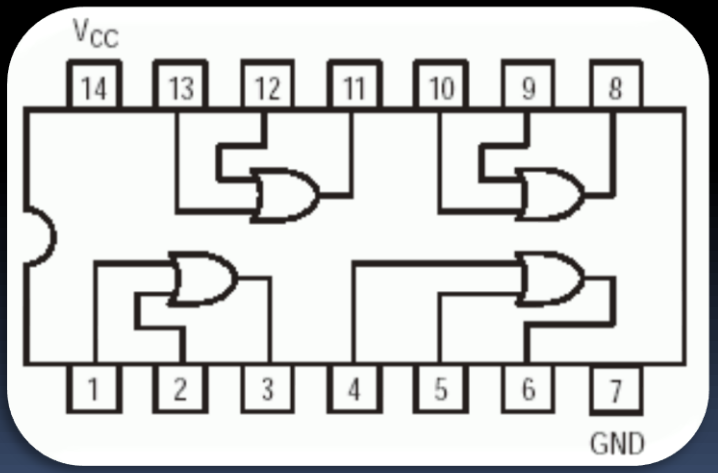


Other Gates

- 74LS08 (AND)



- 74LS32 (OR)



Pre-lab report

- Should include the following:
  - Lab number and title
  - Student info (last name, first name, student #)
  - Exercise parts
    - Each in its own clearly-labeled section.
    - Provide the calculations (if applicable).
    - Illustrate the solution (including pin labels).
  - Be neat.
- Both students in a team must fully understand and be able to explain everything in the pre-lab report.

Teaching Labs accounts

- Part III of the lab requires you to have active ECF account
- Activate your ECF account ASAP
  - https://ssl.ecf.utoronto.ca/ecf/weblogin/services/agree
  - Need to agree to the terms and conditions of use, then set an initial password
  - If you encounter issues, see http://www.undergrad.engineering.utoronto.ca/Student_Life/Engineering_Computing_Facility/ECFHelp.htm

Boolean expression notation

- AND operations are denoted in these expressions by the multiplication symbol.
  - e.g. $A \cdot B \cdot C = A*B*C = ABC = A \wedge B \wedge C = A\&B\&C$
- OR operations are denoted by the addition symbol.
  - e.g. $A+B+C = A \vee B \vee C = A|B|C$
- NOT is denoted by multiple symbols.
  - e.g. $\neg A = A' = \overline{A} = !A = \sim A$
- XOR
  - e.g. $A \oplus B$ = A ^ B (CAUTION! This is XOR in Verilog, different from the $\wedge$ symbol above)

Exercise #1

- Given inputs A, B and C:
  - Draw the diagram for AB:
  - Draw the diagram for $\bar{A}C$:
  - Draw the diagram for $AB + \bar{A}C$:

Exercise #2

- Design a circuit that has two inputs (`x` and `y`) and one output (`f`) that functions in the following way:
  - the function `f` is false (0) when `x` and `y` are the same.
  - the function `f` is true (1) when they are different.

Exercise #3

- Design a circuit with three inputs (`a`, `b`, and `c`) and three outputs (`f1`, `f2`, and `f3`).
  - The first output (`f1`) should be true (`1`) whenever all three of the inputs are low.
  - The second output (`f2`) should be true (`1`) whenever exactly two of the inputs are high.
  - The third output (`f3`) should be true (`1`) whenever the number of high inputs is odd.
  - In all other cases, the outputs should be false (`0`).

Things to note

- This will be the shortest lab you do in the course. ☺
- Whenever possible, use the tools and bring in a printed pre-lab report.
- Try to come up with the smallest circuits possible.
  - How do you reduce a complex circuit?
  - Think back to Boolean algebra axioms!
  - Simple reasoning helps as well ☺

In lab

- Respect the rules!
  - Positively no food or drinks!
    - If you need to drink, step out of the lab
      - There are water fountains by the south side washrooms
  - Clean up your workstation once you're done
- Time management is important
  - If you find yourself spending too much time on one part, you may be doing something wrong
    - Use TAs help
    - TAs are there to help you solve the problems, NOT to solve them for you