Dilated Involutional Pyramid Network(DInPNet): A Novel Model for Printed Circuit Board (PCB) Components Classification

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Speaker

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Overview

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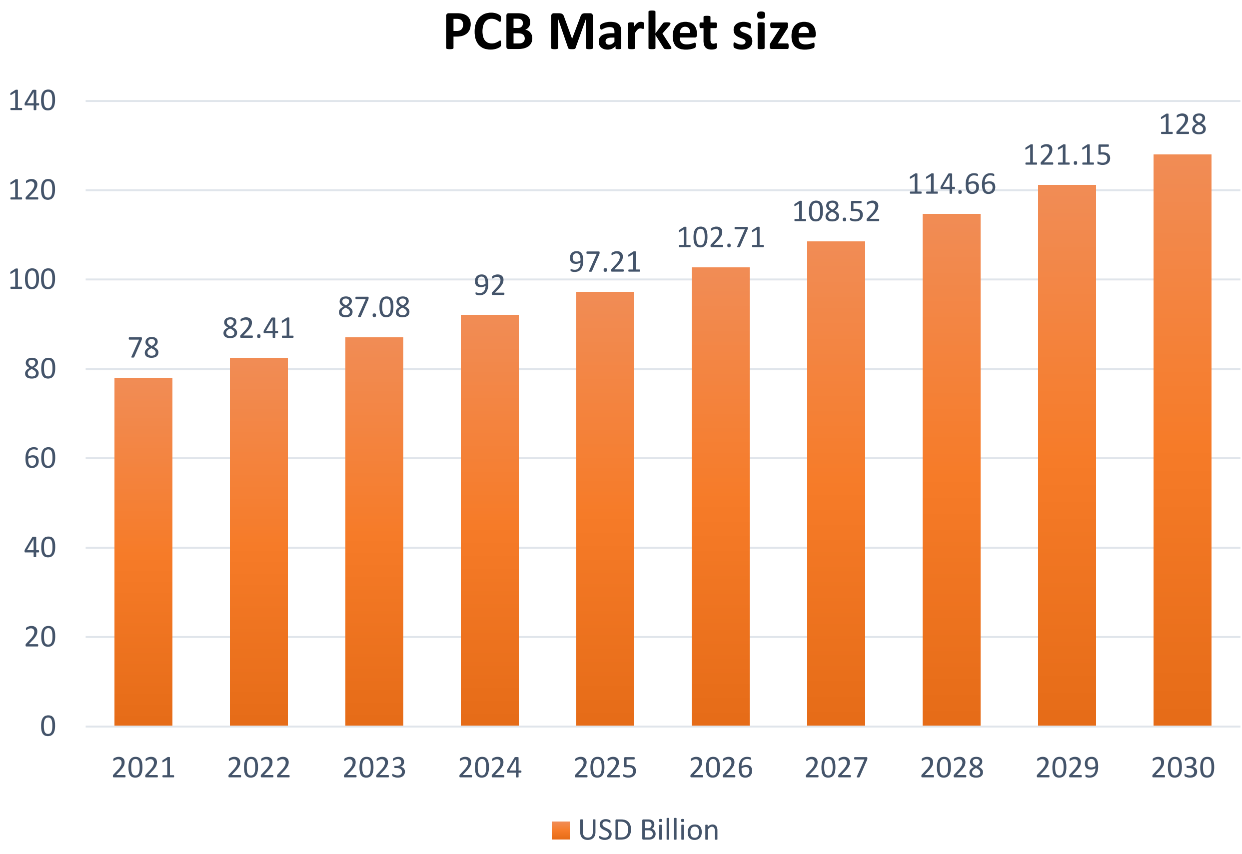
- ❑ Literature Review
- ❑ FICS-PCB Dataset
- ❑ DInPNet Architecture
- ❑ Experimental Results
- ❑ Summary

Background & Motivation

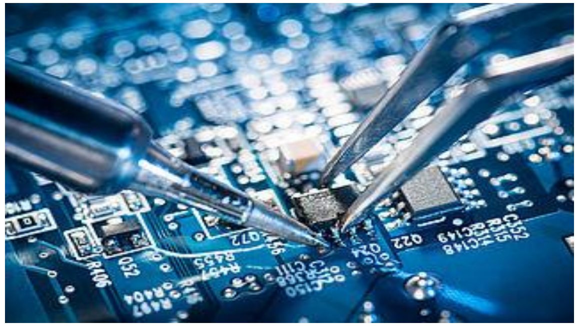
- PCBs global market is expected to reach $128 billion by 2030[1]
- Rise in variety of electronic components making PCB automatic visual inspection more challenging
- Inspection time ↓ Accuracy ↑ Quality control ↑ Cost ↓
- Deep learning for promising results



[1] *https://www.precedenceresearch.com/printed-circuit-board-market*

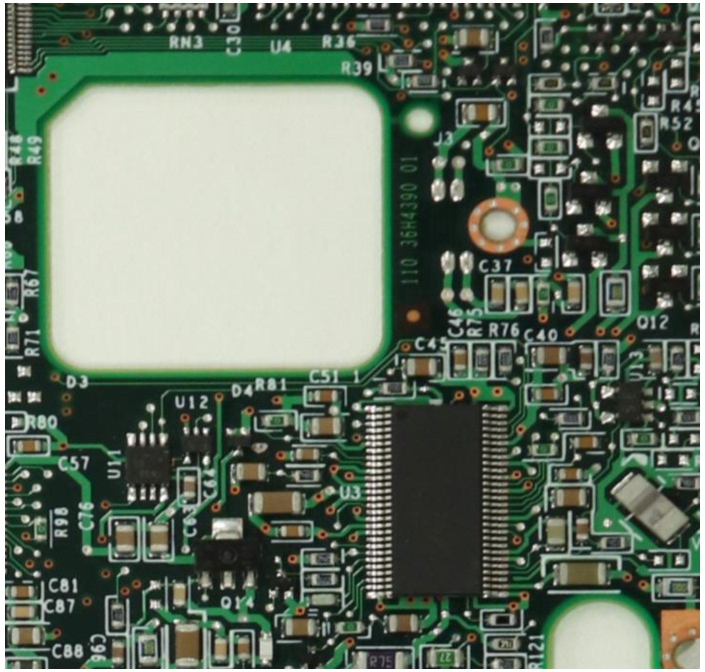
Applications

- Quality Control
- Inventory Management
- Bill of Materials
- E-waste Recycling
- Research and Development



Challenges

- Different shapes, sizes, and colours of PCB components
- High inter-class similarity & low intra-class distinction
- Challenging detection due to small sizes
- High variance (lighting, resolution, image artifacts)
- Severe class imbalance in some datasets like FICS-PCB



Literature Review

- PCB component segmentation, detection, and classification have been addressed in existing solutions, for solder joint inspection[1], defect detection[2], and efficient recycling of PCB[3]
- Traditional computer vision methods: Log-Gabor filters[1], clustering[4], and segmentation methodologies[5].
- Deep learning methods: CNNs for SMD classification[6], DL-based complete PCB image classification[7].

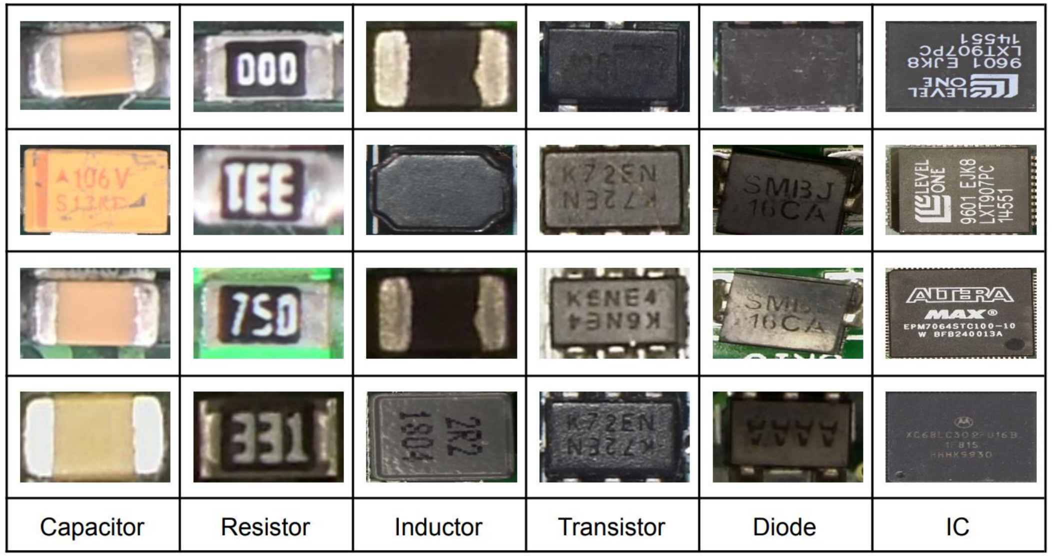
[1] N. S. S. Mar, "Design and development of automatic visual inspection system for pcb manufacturing," Robotics and computer-integrated manufacturing
[2] Nag, "WaferSegClassNet - A light-weight network for classification and segmentation of semiconductor wafer defects," Computers in Industry
[3] I. A. Soomro, "Printed circuit board identification using deep convolutional neural networks to facilitate recycling," Resources, Conservation and Recycling
[4] J.-O. Kim, "Automatic extraction of component inspection regions from printed circuit board," in 2012 IEEE/SICE International Symposium on System Integration
[5] W. Li, "Smd segmentation for automated pcb recycling," in 2013 11th IEEE International Conference on Industrial Informatics (INDIN).
[6] D.-u. Lim, "Smd classification for automated optical inspection machine using convolution neural network," in 2019 Third IEEE International Conference on Robotic Computing (IRC).
[7] I. A. Soomro, "Printed circuit board identification using deep convolutional neural networks to facilitate recycling," Resources, Conservation and Recycling

Limitations of Previous Methods

- Datasets used:
  - Small-scale
  - Unrepresentative of real-life scenarios
  - Publicly unavailable
  - No disclosure of class sizes, image-capturing techniques, sample distribution.
- Traditional approaches are unable to handle the challenge of increasing variance caused by evolving higher complexity and compact designs at the PCB level
- Our DL-based method is evaluated on the FICS-PCB dataset - Contains images with variation in imaging modality, scale, and illumination.

FICS-PCB Dataset

- 9,912 images of 31 distinct PCBs in the dataset taken from both the front and rear sides of the PCBs.
- Total of 77,347 annotated component images belonging to 12 the semi-conductor component classes.
- ‘transformers’, ‘2R7’, ‘3R3’, ‘fuses’, ‘transducers’, and ‘nan’ classes with less than 6 images excluded.



6 classes of PCB Components chosen

FICS-PCB Dataset

- The sample-wise distribution is highly imbalanced.
- The inductor class has the least number of 1292 samples. 80% (1034) of those images taken for training and rest for testing.
- For the remaining classes also, we take 1034 images for training and use the remaining images for testing.

	IC	Capacitor	Resistor	Inductor	Transistor	Diode
#Total Images	3243	36639	33182	1292	1398	1593
#Training Images	1034	1034	1034	1034	1034	1034
#Test Images	2209	35605	32148	258	364	559

Background of Proposed Method

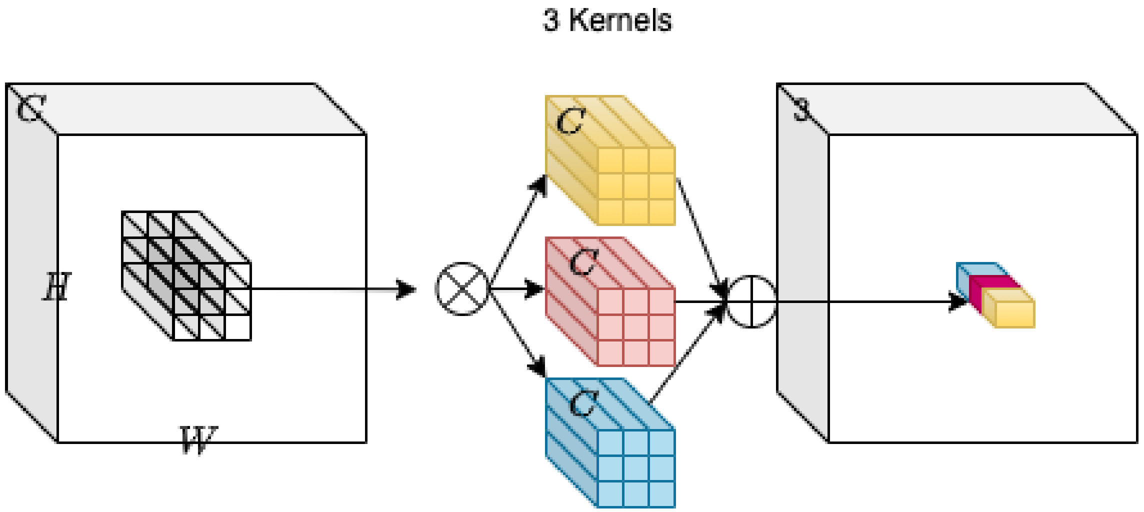
Convolution

- Spatial-agnostic:

  Reuse of the convolution kernels across locations

- Channel-specific:

  Each channel in the output tensor is based on a specific convolution filter



- Limitations:
  - Kernel unable to adapt to different visual patterns w.r.t. different spatial locations
  - Receptive field creates challenges w.r.t. capturing long-range spatial interactions.
  - Feature redundancy among channels – inter-channel information is unimportant

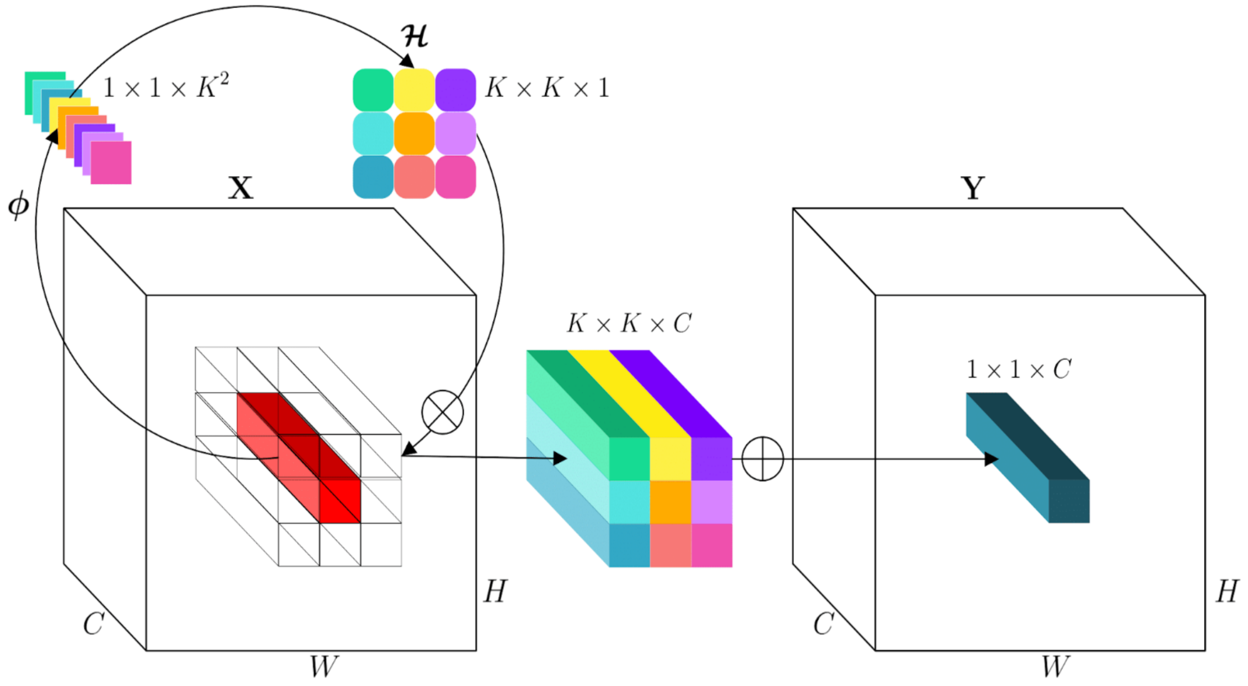
Involution

- Spatial-specific:

  Generating each kernel conditioned on specific spatial positions

- Channel-agnostic:

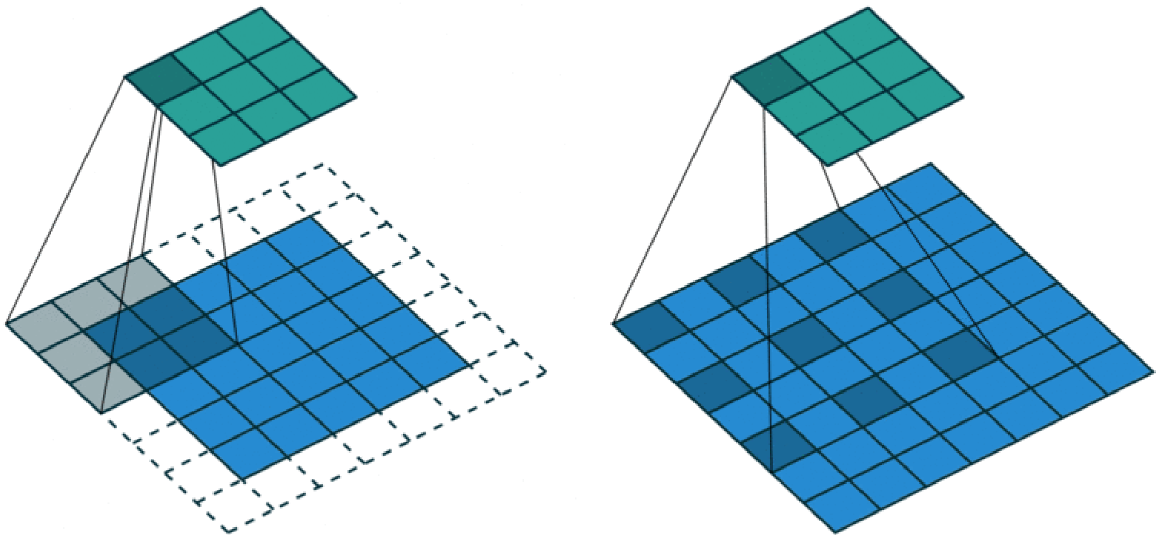
  Collecting information encoded from different channels



Kernel Generation:

- 1x1xC Conv $1x1xK^2$
- $1x1xK^2$ Conv KxKx1

Dilation



- ➢ Spacing between the values in the kernel.
- ➢ Controls the amount of "zero-padding" added around the values in the kernel.

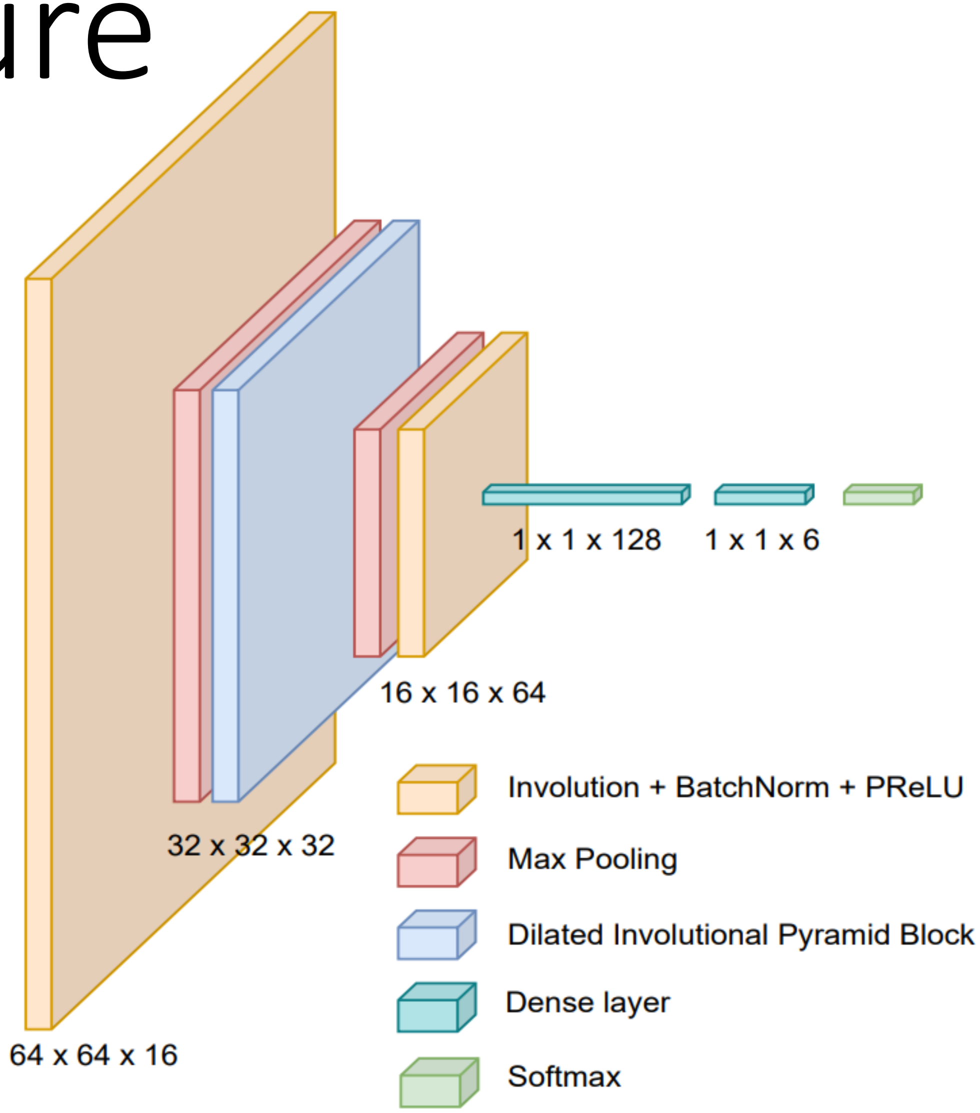
Proposed Method

Motivation

- Convolution is spatial-agnostic and channel-specific, whereas involution is space-dependent and channel-independent.
- Involutions overcome inter-channel redundancies and location-specific details learning challenges faced in convolutions.
- Dilations enlarge receptive field allowing the network to capture more context.
- Combining involution with dilation helps to capture both local and global contextual information in an efficient manner.

DInPNet Architecture

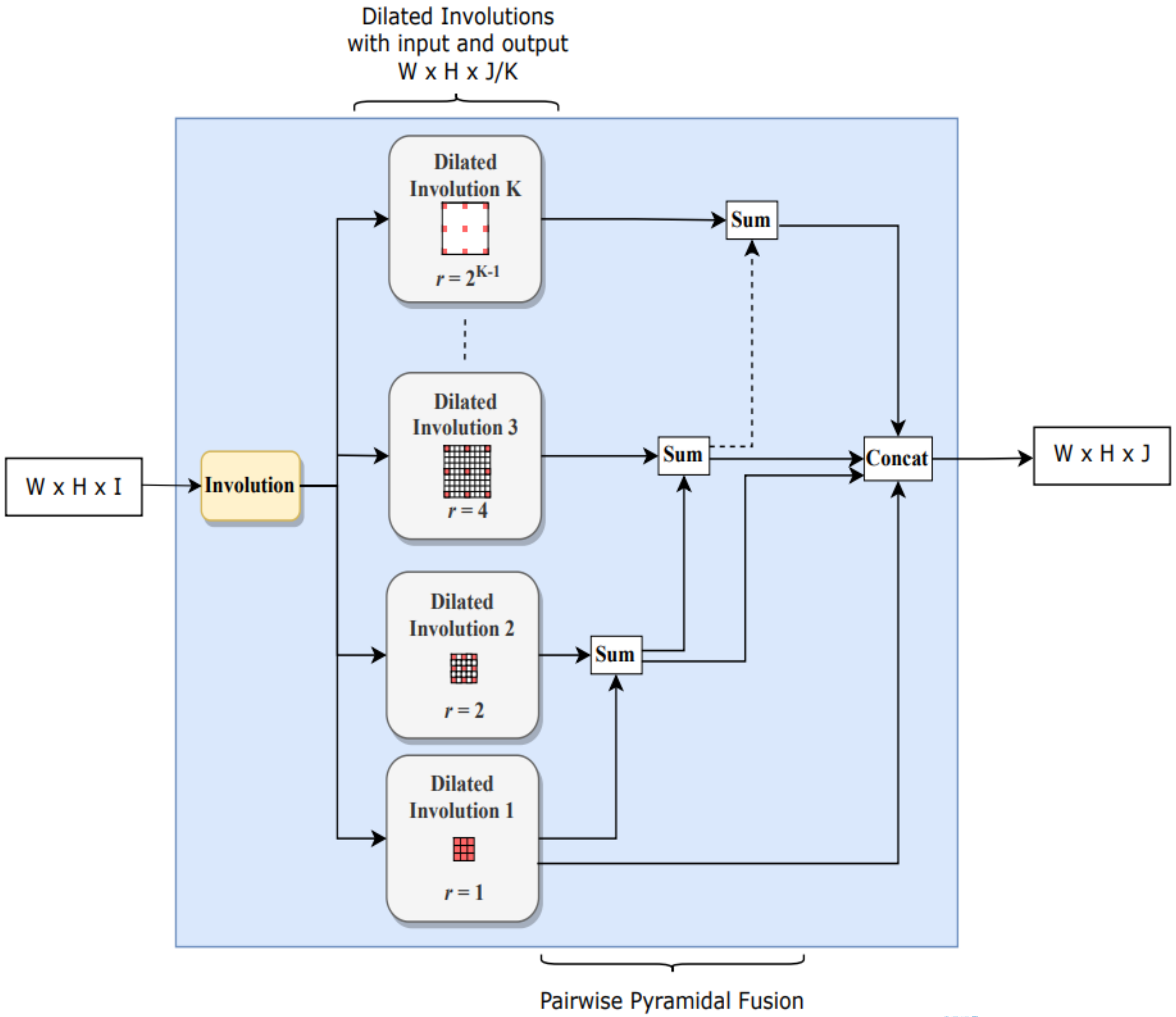
We built a custom architecture named DInPNet based on Involution and DInP block for PCB components classification.



- Image size: 64 x 64 x 3.
- Kernel size: 3 x 3
- Stride: 1
- Pool size: 2 x 2
- Parameters: 531,485

DInP Block

- Reduced parameters and computational complexity as compared to only convolution/involution layer
- Enable learning from enlarged field-of-view in low-dimensional space
- Enable learning of both location-specific details and spatial information.



Experiments

Experimental Setup and Metrics

Metrics used for evaluations:

- Accuracy
- Matthew's correlation coefficient (MCC)
- Precision
- Recall
- F1-Score

Hyper parameters settings used for training

Description	Value
Learning Rate	0.001
Image size	64x64
Batch size	16
Optimizer	Adam
Number of epochs	100
Loss	Cross Entropy

Network Comparison and Evaluation

- Higher the evaluation metrics the better the classification; Lower the number of parameters, better the computational efficiency.
- DInPNet outperforms all the methods that have been compared

Metric	Accuracy	MCC	Precision	Recall	F1	Parameters
LeNet5	71.67	63.91	94.15	71.67	78.34	**0.06M**
AlexNet	75.72	68.34	94.92	75.72	81.61	11.77M
MobileNetV2	91.07	86.44	92.20	92.21	91.40	2.23M
ResNet18	93.98	88.30	93.20	93.00	92.05	12.56M
DInPNet	**95.65**	**92.59**	**95.48**	**95.65**	**95.41**	0.53M

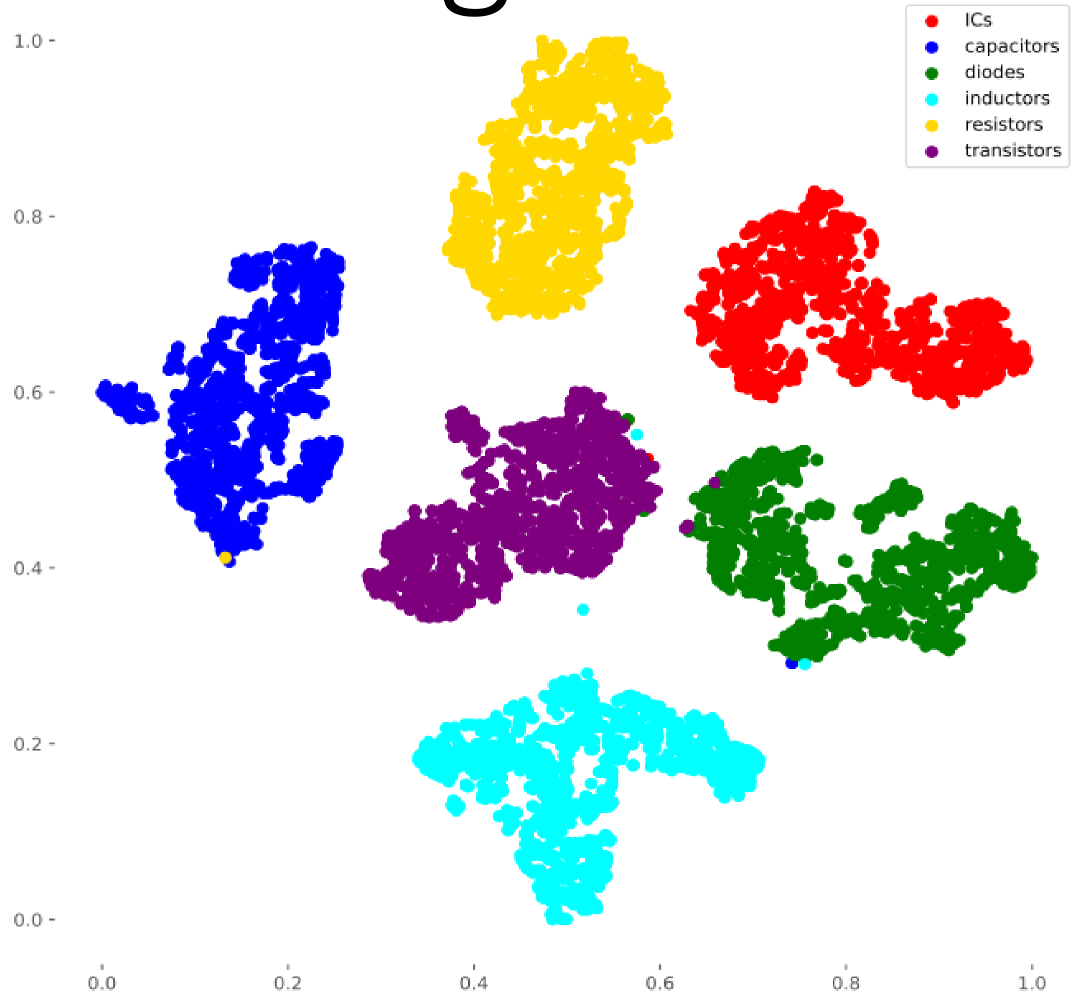
Class-wise Results of DInPNet

- Capacitor, inductor and resistor classes scores between 99% and 100%.
- ICs, Diodes, Transistors have F1 scores between 94%-95% (higher intra-class variability)

	Precision	Recall	F1 -Score
ICs	98	93	95
Capacitors	99	100	100
Diodes	95	96	95
Inductors	99	100	99
Resistors	100	100	100
Transistors	93	95	94

Visualization of Embeddings

- DInPNet extracts features efficiently which we visualize through t-SNE
- t-SNE: A dimensionality reduction technique used to visualize high-dimensional data projected into lower dimensionalities
- Network embeddings taken from the last layer before the dense layer of architecture.



Analysis of mispredicted PCB components

- “GT” refers to ground truth and “Pred” refers to the predicted class

(a)
GT: Diode
Pred: Transistor

(b)
GT: IC
Pred: Diode

(c)
GT: IC
Pred: Transistor

(d)
GT: Inductor
Pred: Resistor

Summary

- Proposed DInPNet - a lightweight network for PCB component classification suitable for low-resource and low-computing edge device platforms.
- Experiments on the FICS-PCB dataset show State-Of-The-Art results.
- First to present multi-class classification results on the FICS-PCB dataset.

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Thank You

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Vinaka
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