Synchronous Non-binary Counters

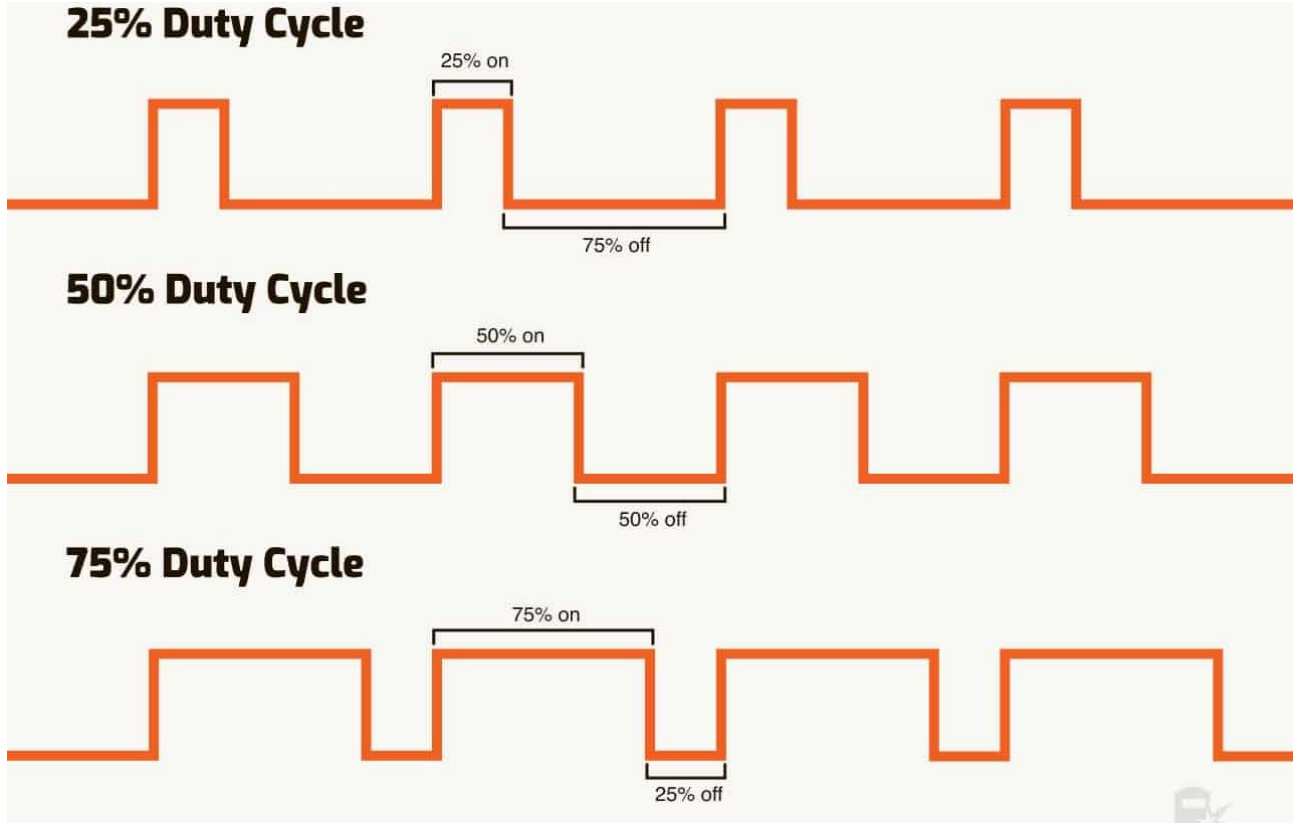
Sparsh Mittal

These are counters with unused states or different sequence of state transition.

Definition of duty cycle

A duty cycle is the fraction of a period in which a signal or system is active.

It's usually expressed as a percentage or ratio.



Non-binary counters

- A circuit with n flip-flops has 2^n binary states.
- Some counters may have fewer than 2^n states.
- Unused states are not listed in the state table.
- They may be
- Case 1: treated as don't-care conditions or
- Case 2: assigned specific next states.
- During its operation, a circuit may enter unused state due to an outside interference. In that case, it is necessary to ensure that the circuit eventually goes into one of the valid states.

Non-binary counters

Otherwise, if the sequential circuit circulates among unused states, there will be no way to bring it back to its intended sequence of state transitions.

If the unused states are treated as don't-care conditions (Case 1), then once the circuit is designed, it must be investigated to determine the effect of the unused states.

The next state from an unused state can be determined from circuit analysis.

Example 1: Design a counter to achieve the following sequence.

There is repeated sequence of six states, with flip-flops *B* and *C* repeating the binary count 00, 01, 10, and flip-flop *A* alternating between 0 and 1 every thre counts.

011 and 111, are not included in the count.

Present State			Next State		
A	*B*	*C*	*A*	*B*	*C*
0	0	0	0	0	1
0	0	1	0	1	0
0	1	0	1	0	0
1	0	0	1	0	1
1	0	1	1	1	0
1	1	0	0	0	0

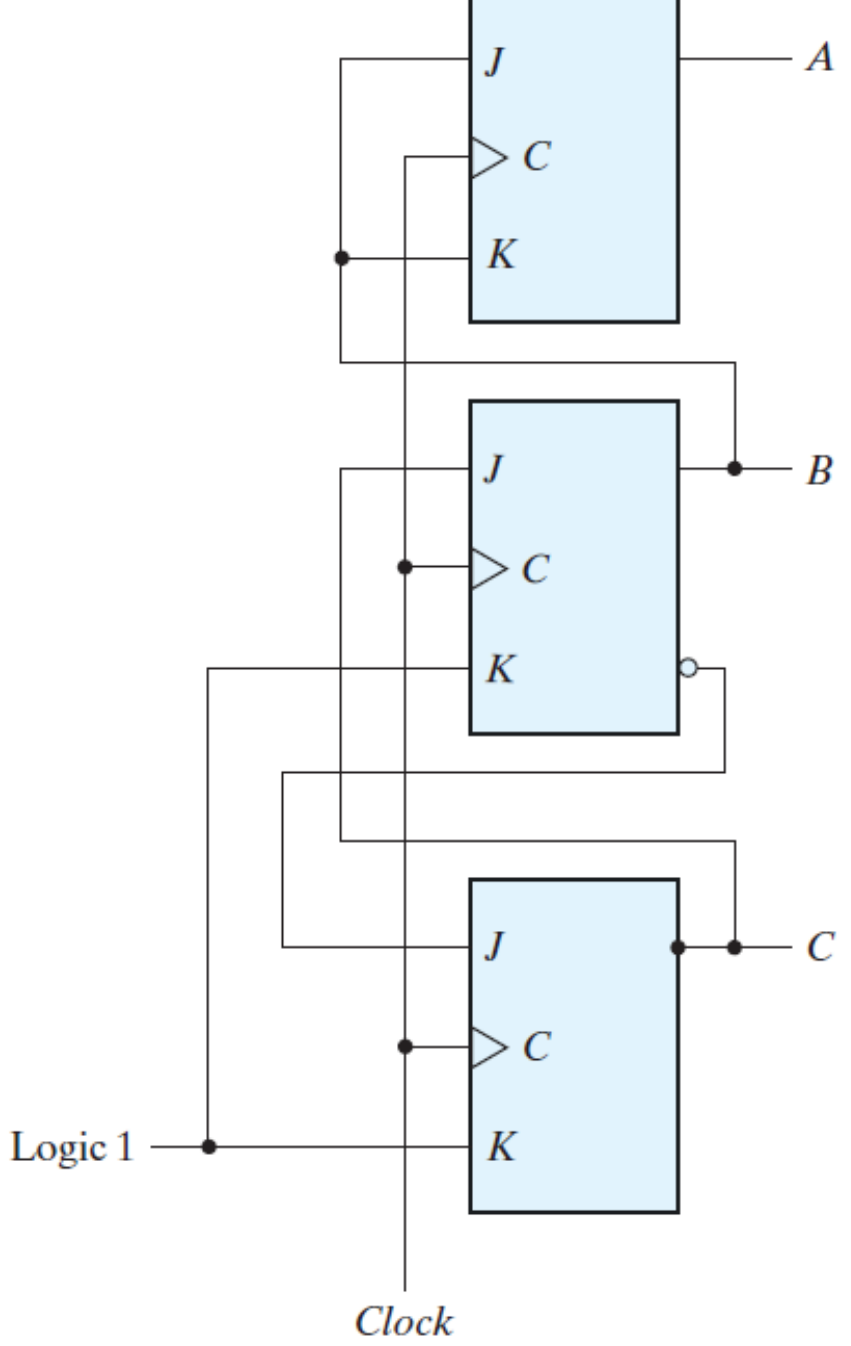
Example 1:

On using JK flip-flop:

$$J_A = B \qquad K_A = B$$
$$J_B = C \qquad K_B = 1$$
$$J_C = B' \qquad K_C = 1$$

State Table for Counter

Present State			Next State			Flip-Flop Inputs					
A	B	C	A	B	C	J_A	K_A	J_B	K_B	J_C	K_C
0	0	0	0	0	1	0	X	0	X	1	X
0	0	1	0	1	0	0	X	1	X	X	1
0	1	0	1	0	0	1	X	X	1	0	X
1	0	0	1	0	1	X	0	0	X	1	X
1	0	1	1	1	0	X	0	1	X	X	1
1	1	0	0	0	0	X	1	X	1	0	X



(a) Logic circuit diagram

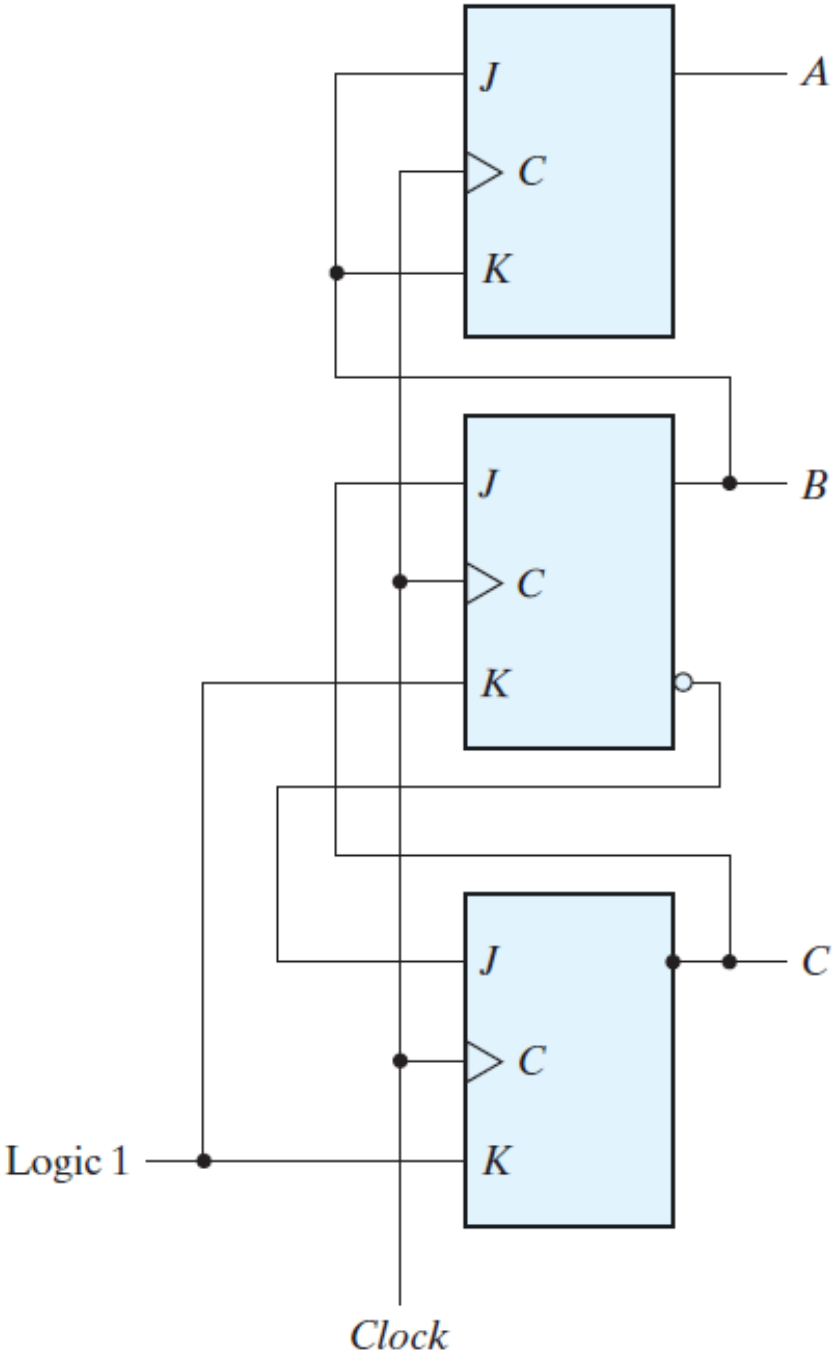
Example 1: analyzing unused states

If the circuit happens to be in state 011 because of an error signal, the circuit goes to state 100 after the application of a clock pulse.

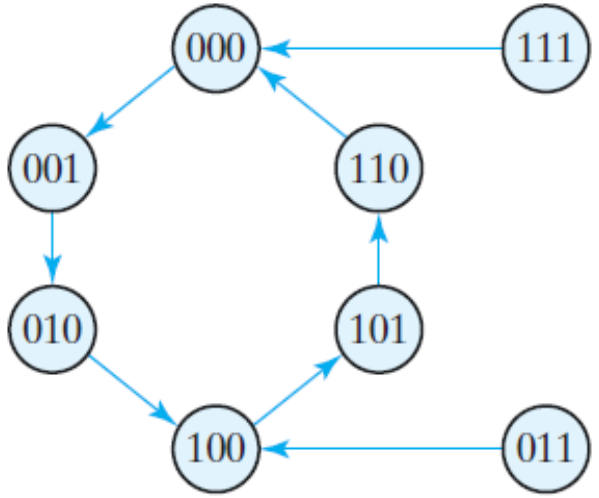
Explanation: When $B = 1$, the next clock edge complements A and clears C to 0, and when $C = 1$, the next clock edge complements B.

In a similar manner, we can evaluate the next state from present state 111 to be 000.

Example 1



(a) Logic circuit diagram



(b) State transition diagram

The counter is self-correcting, i.e., if the counter happens to be in one of the unused states, it eventually reaches the normal count sequence after one or more clock pulses.

Ring counter

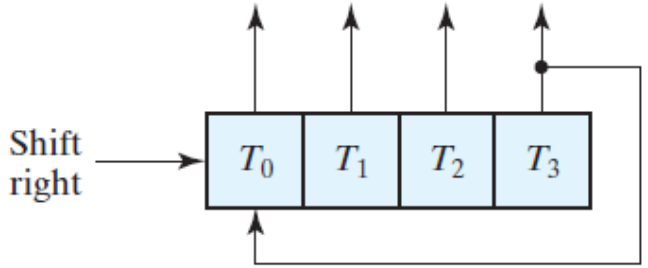
Definition

A ring counter is a circular shift register with only one flip-flop being set at any particular time.

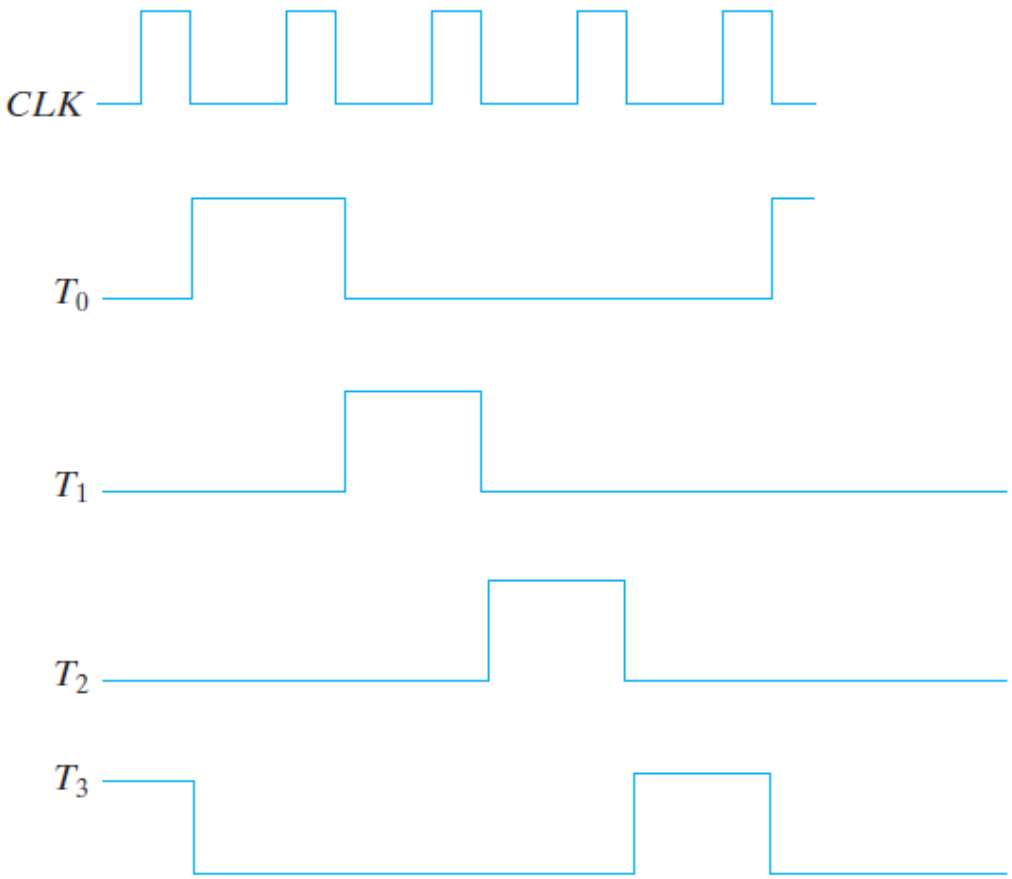
The single bit is shifted from one flip-flop to the next to produce the sequence of timing

signals.

Here is a four-bit shift register connected as a ring counter.



(a) Ring-counter (initial value = 1000)



(b) Sequence of four timing signals

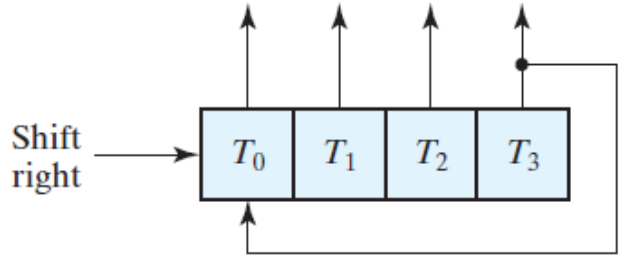
Working

The initial value of the register is set to 1000 using preset options.

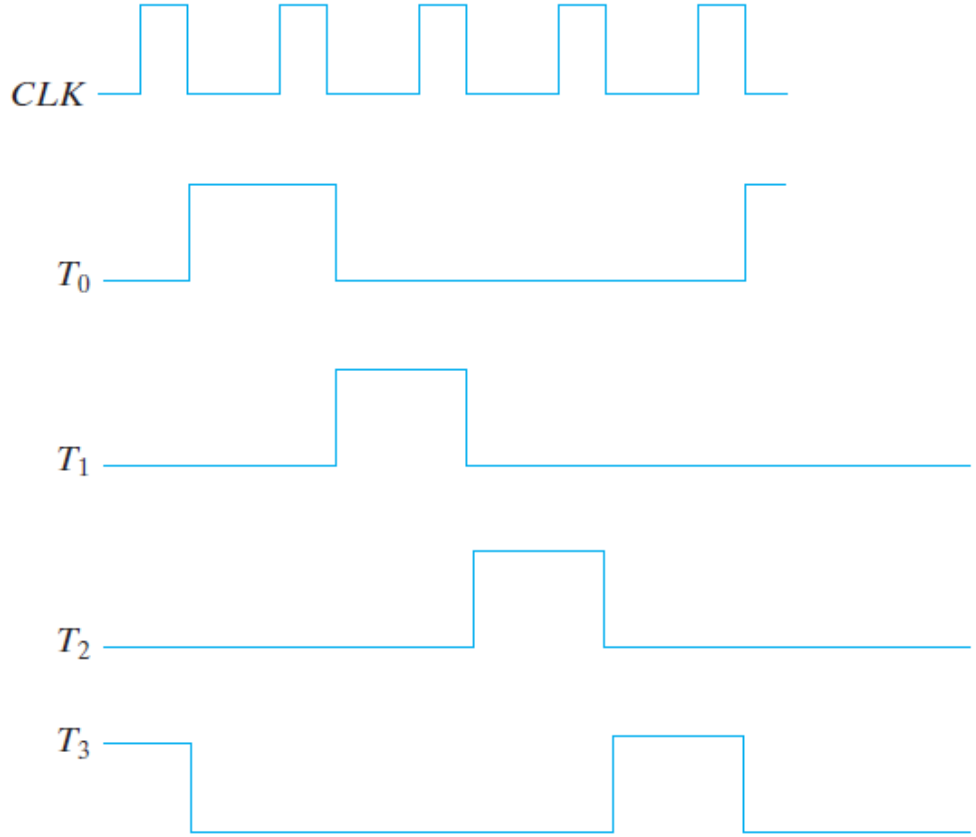
The single bit is shifted right with every clock pulse and circulates back from T3 to T0.

Each flip-flop is in the 1 state once every four clock cycles and produces one of the four timing signals shown here.

Each output becomes a 1 after the negative-edge transition of a clock pulse and remains 1 during the next clock cycle.



(a) Ring-counter (initial value = 1000)



(b) Sequence of four timing signals

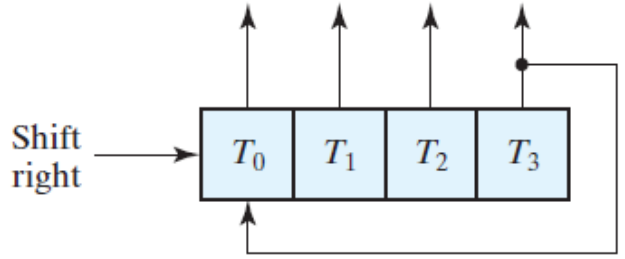
Duty cycle

The duty cycle of an an N-Bit ring counter is 100/N.

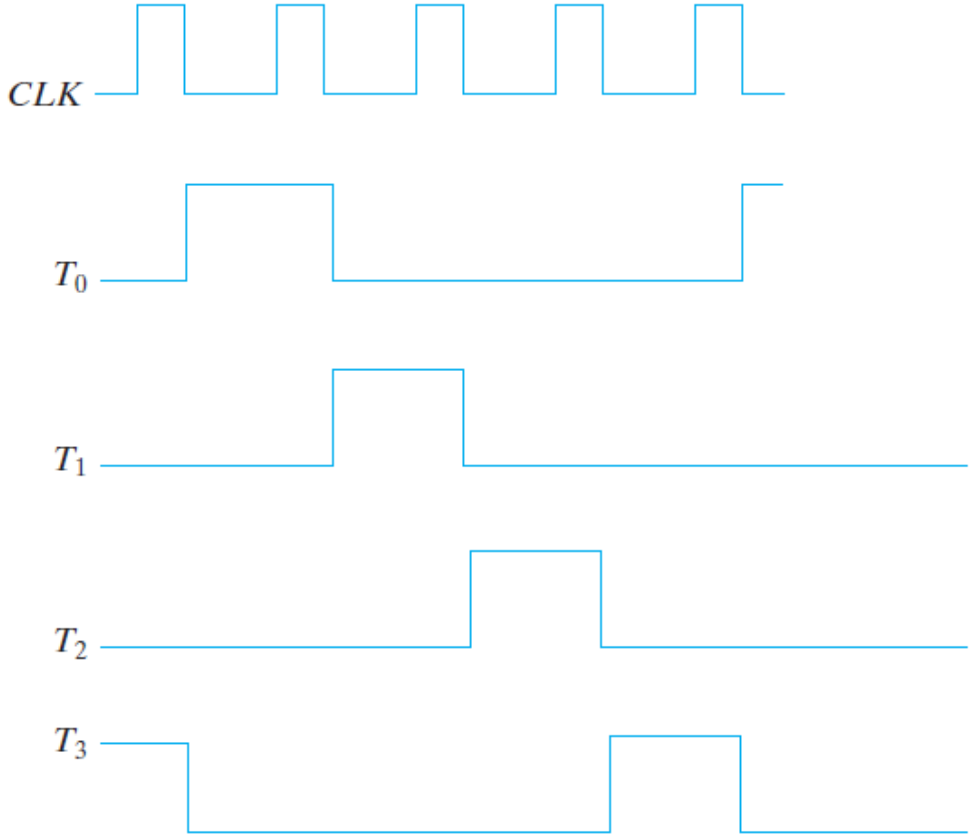
For example, for a 4-bit ring counter, it is 25%. This is because T0 is 1 for 25% of time.

Same is true for T1, T2 and T3.

An N-bit Ring counter is a modulo-N counter, because it shows N distinct states.



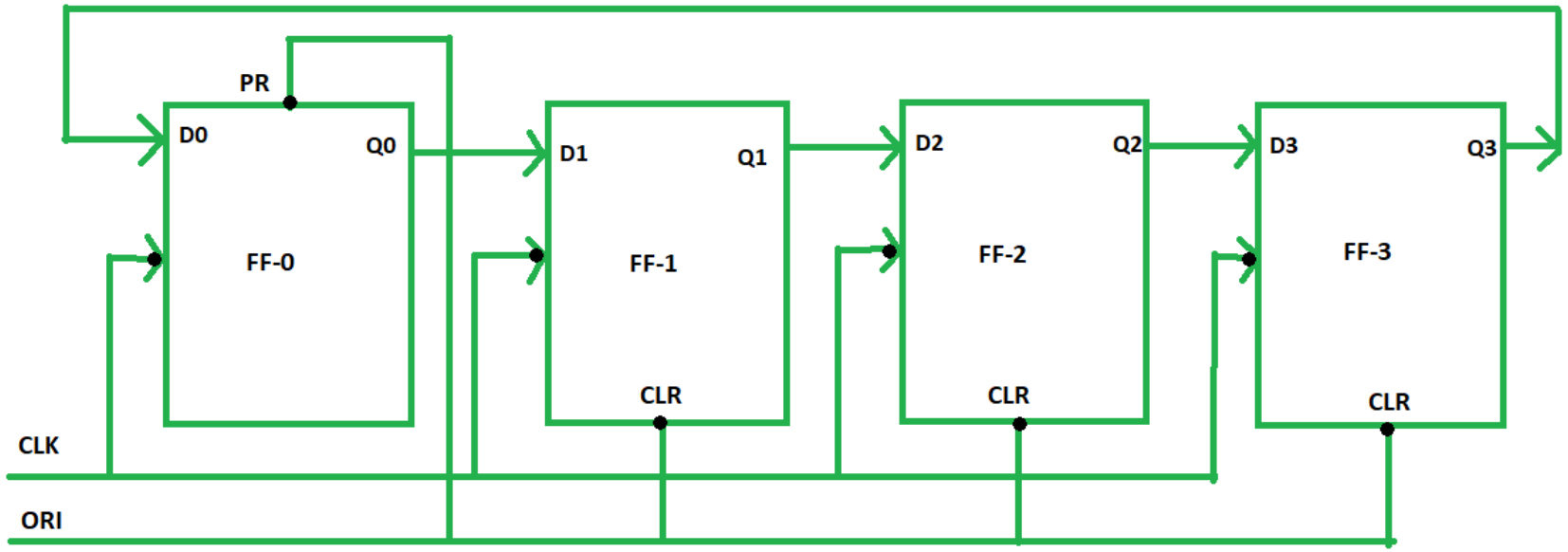
(a) Ring-counter (initial value = 1000)



(b) Sequence of four timing signals

Ring counter design

PR = preset. ORI = overriding input



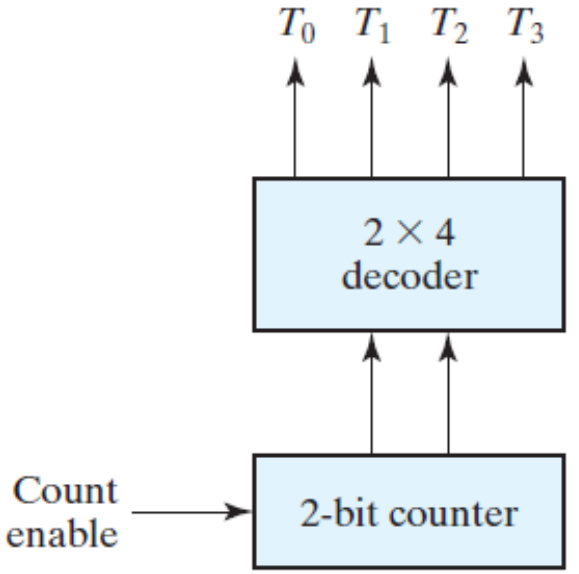
Ring Counter

The output of the last flip-flop is connected to the input of the first flip-flop in the case of the ring counter but in the case of the shift register it is taken as output.

Alternative design

The timing signals can be generated by a two-bit counter that goes through four distinct states.

The decoder shown here decodes the four states of the counter and generates the required sequence of timing signals.



(c) Counter and decoder

Application of Ring Counter

In hardware design to create finite-state machines that control sequential logic circuits.

To generate timing signals for synchronous systems such as clocks, timers, frequency dividers, etc.

To implement circular buffers or queues in memory devices such as RAMs or FIFOs.

To generate pseudo-random numbers or sequences for encryption or testing purposes.

To create rotating displays or LED chasers for decorative or signaling purposes.

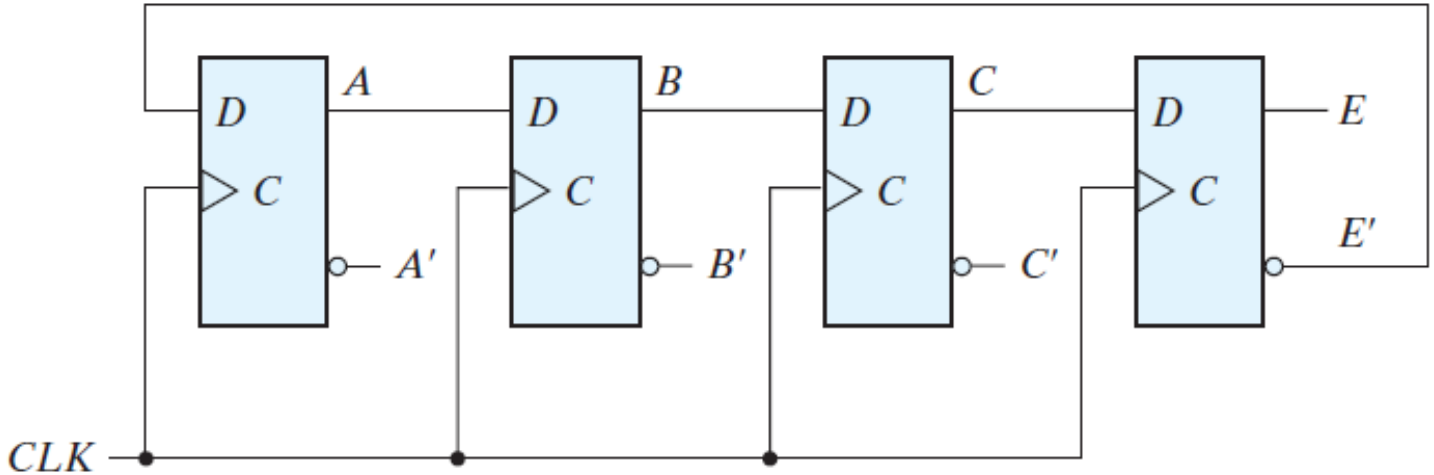
Johnson counter

Switch-tail ring counter

A k -bit ring counter circulates a single bit among the flip-flops to provide k distinguishable states.

The number of states can be doubled if the shift register is connected as a *switch-tail* ring counter.

A switch-tail ring counter is a circular shift register with the complemented output of the last flip-flop connected to the input of the first flip-flop.



(a) Four-stage switch-tail ring counter

Switch-tail ring counter

The register shifts its contents once to the right with every clock pulse, and at the same time, the complemented value of the E flip-flop is transferred into the A flip-flop.

Starting from a cleared state, the switch-tail ring counter goes through a sequence of eight states.

A k -bit switch-tail ring counter will go through a sequence of 2k states.

Starting from all 0's, each shift operation inserts 1's from the left until the register is filled with all 1's.

In the next sequences, 0's are inserted from the left until the register is again filled with all 0's.

Sequence number	Flip-flop outputs			
	A	*B*	*C*	*E*
1	0	0	0	0
2	1	0	0	0
3	1	1	0	0
4	1	1	1	0
5	1	1	1	1
6	0	1	1	1
7	0	0	1	1
8	0	0	0	1

Duty cycle

Lets see A. It is 1 for 50% of the time. Hence, its duty cycle is 50%.

In general, for an N-bit Johnson counter, duty cycle is 50%.

An N-bit Johnson counter is a modulo-2N counter, because it shows 2N distinct states.

Sequence number	Flip-flop outputs			
	A	*B*	*C*	*E*
1	0	0	0	0
2	1	0	0	0
3	1	1	0	0
4	1	1	1	0
5	1	1	1	1
6	0	1	1	1
7	0	0	1	1
8	0	0	0	1

In n-bit Johnson counter

- Number of used states=2n
- Number of unused states=$2^n - 2n$

In n-bit ring counter

- Number of used states=n
- Number of unused states=$2^n - n$