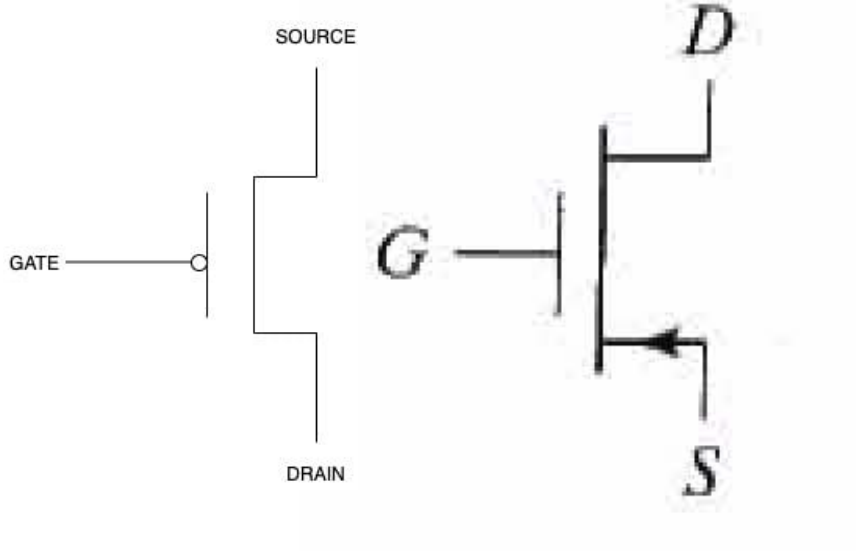
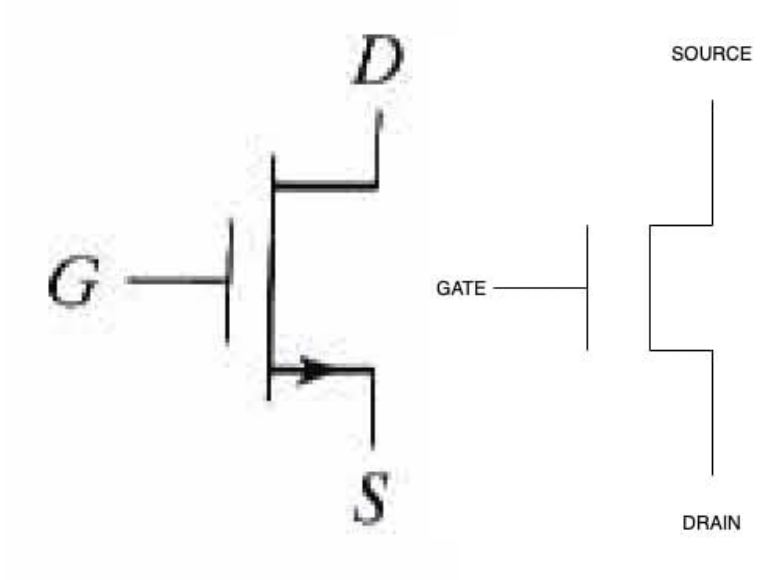
CMOS Circuits

Sparsh Mittal

Symbol for MOS transistor



P-channel

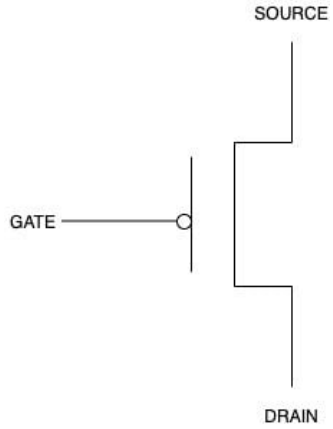


n-channel

Positive current flow: From source to drain From drain to source

Summary of working

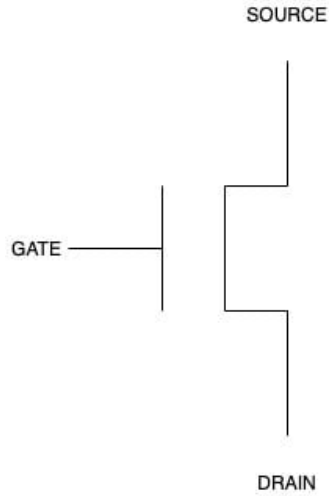
PMOS



GateVoltage =high
➔ Off

GateVoltage =Low
➔ On

NMOS



GateVoltage =high
➔ On

GateVoltage =Low
➔ Off

Points to remember

- 1. The n-channel MOS conducts when its gate-to-source voltage is positive.
- 2. The p-channel MOS conducts when its gate-to-source voltage is negative.
- 3. Either type of device is turned off if its gate-to-source voltage is zero.

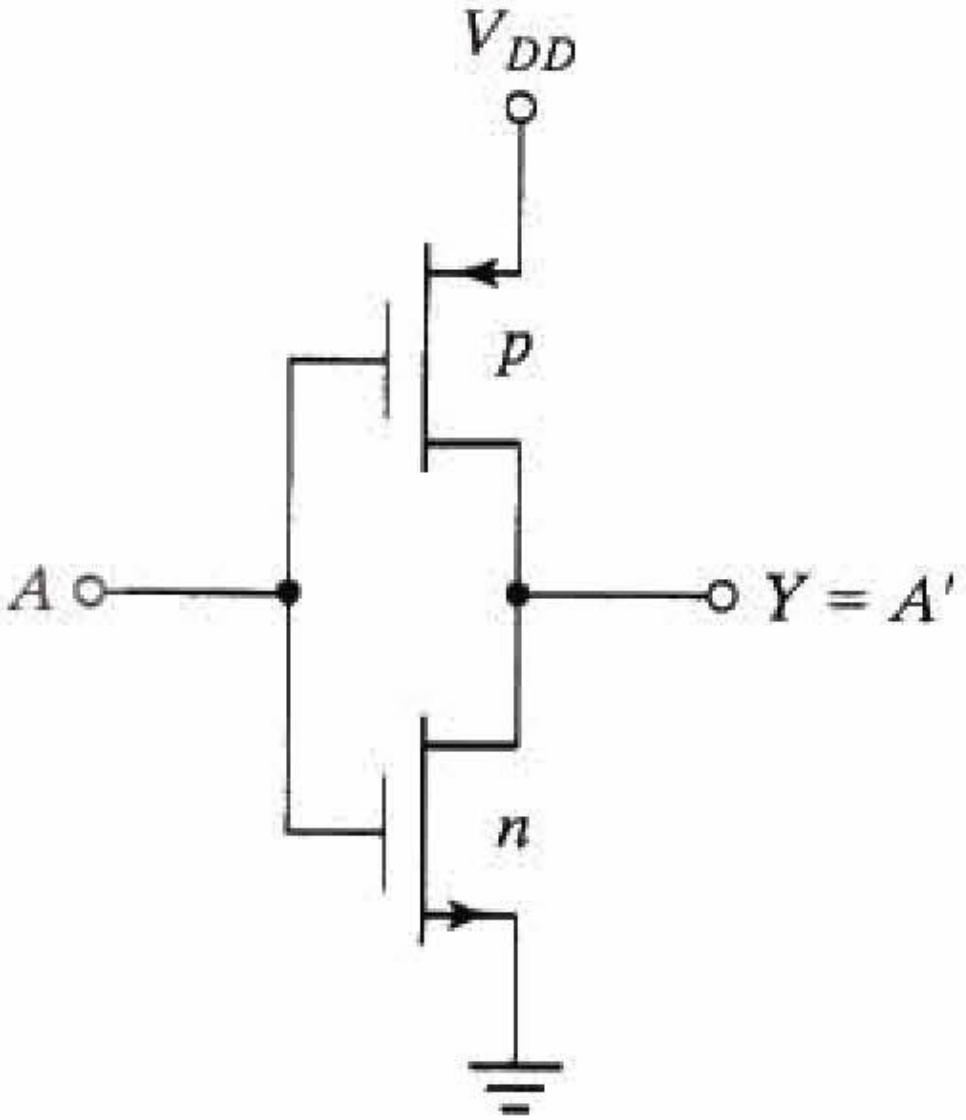
- PMOS: used in pull-up circuit
- NMOS: used in pull-down circuit

CMOS

- CMOS (Complementary MOS) circuits consist of both types of MOS devices, interconnected to form logic functions.
- The basic circuit is the inverter, which consists of one p-channel transistor and one n-channel transistor.
- The source terminal of the p-channel device is at VDD.
- Source terminal of n-channel device is at ground.
- Usually, high level is 5V and low level is 0V.

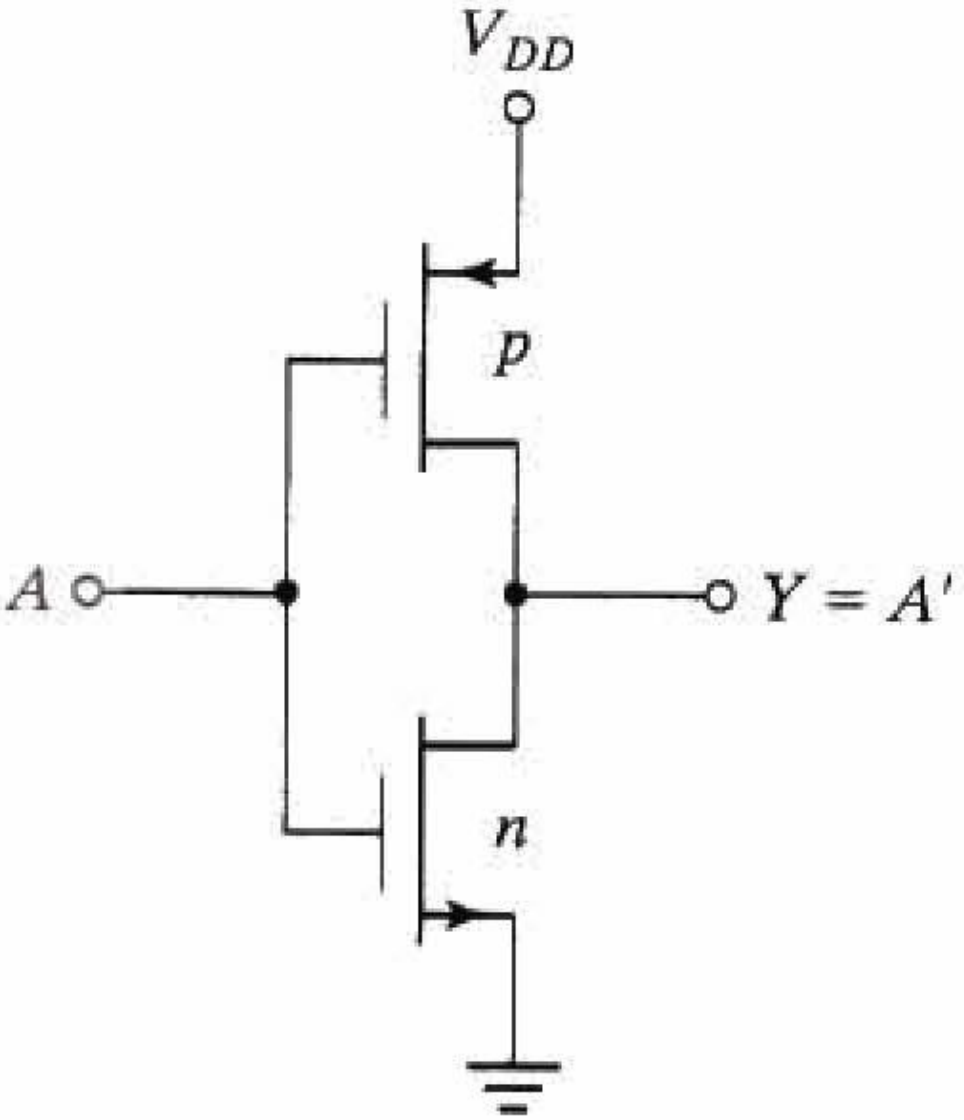
Inverter

- **When the input is low**, both gates are 0V.
- The input is at -VDD relative to the source of the p-channel, and at 0V relative to the source of the n-channel device.
- ➔ The p-channel device is turned on and the n-channel device is turned off.
- ➔ There is a low-impedance path from VDD to the output and a very high impedance path from output to ground.
- ➔ Output approaches VDD



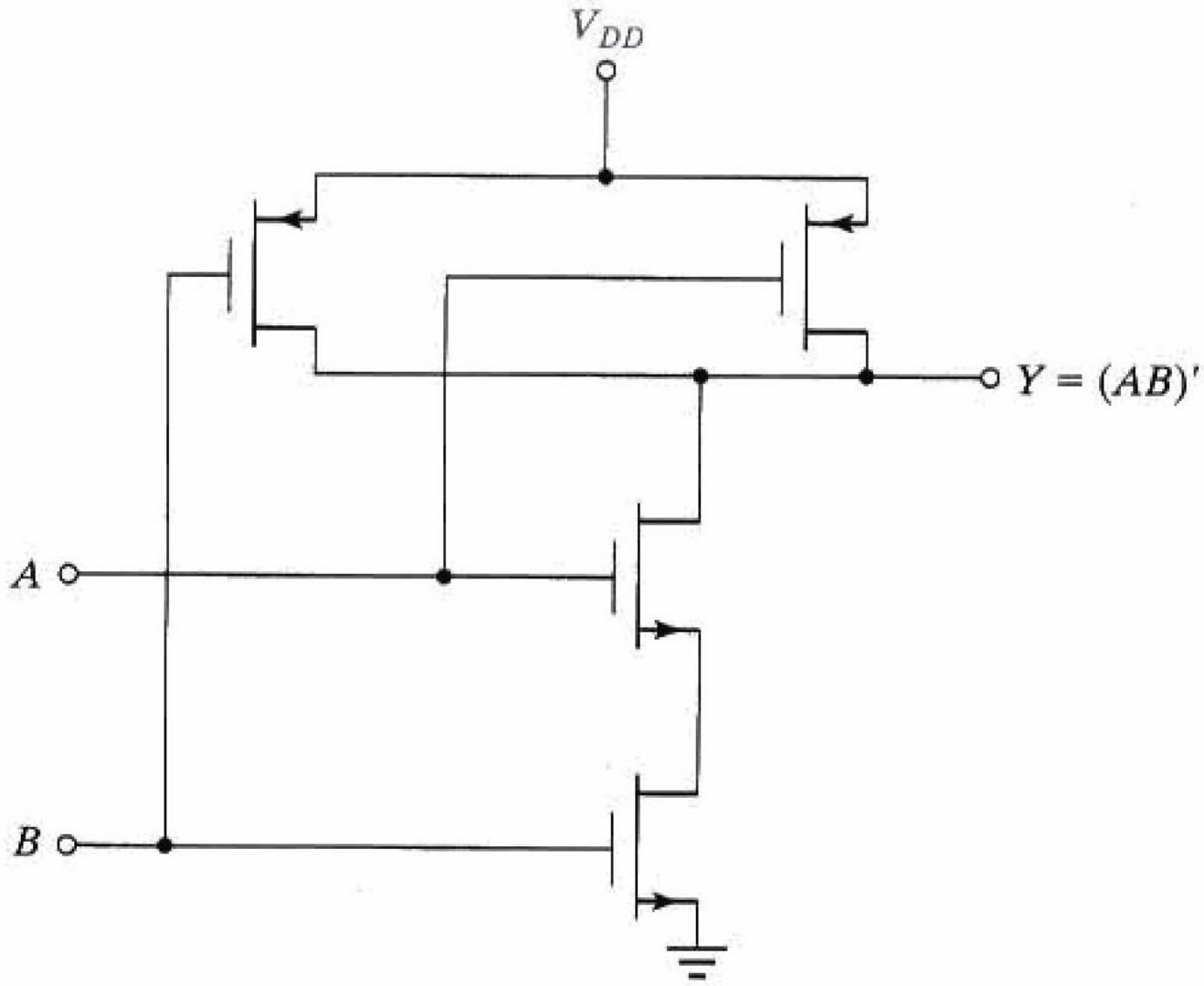
Inverter

- **When the input is high**, both gates are VDD
- Now, p-channel device is turned off and the n-channel device is turned on.
- ➔ There is a high-impedance path from VDD to the output and a low impedance path from output to ground.
- ➔ Output approaches low level of 0V.



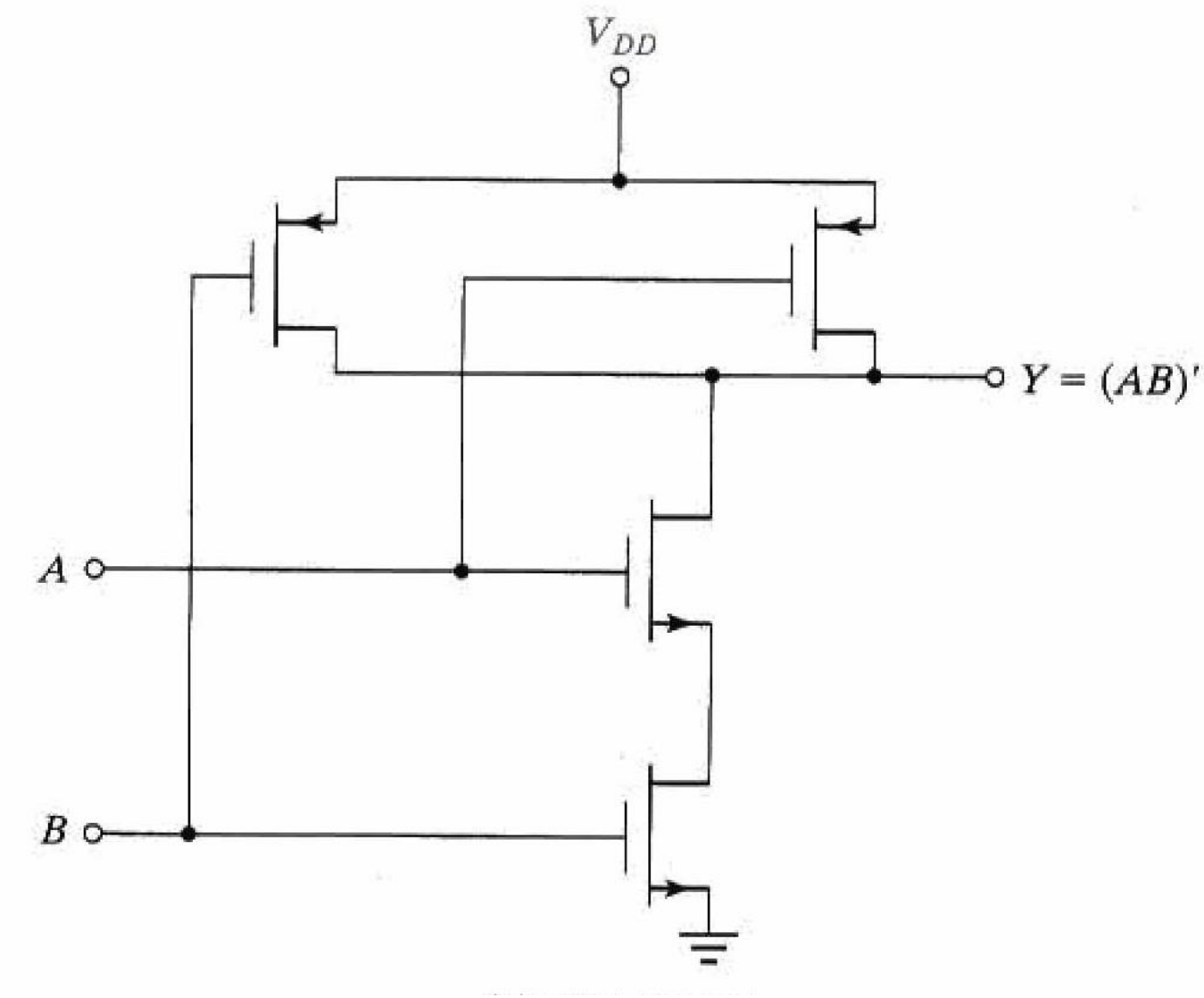
NAND gate

- A two-input NAND gate has two p-type units in parallel and two n-type units in series.
- **If all inputs are high**, both p-channel transistors turn off and both n-channel transistors turn on.
- The output has a low impedance to ground and produces a low state.



NAND gate

- **If any input is low**, the associated n-channel transistor is turned off and the associated p-channel transistor is turned on.
- The output is coupled to VDD (high).
- Multiple input NAND gates can be formed by placing equal number of p-type and n-type transistors.



NOR gate

- A two-input NOR gate has two n-type units in parallel and two p-type units in series.
- **When all inputs are low**, both p-channel units are on and both n-channel units are off.
- The output is coupled to VDD and goes to the high state.
- **If any input is high**, the associated p-channel transistor is turned off and the associated n-channel transistor turns on, connecting the output to ground, i.e., low-level output.