PAL

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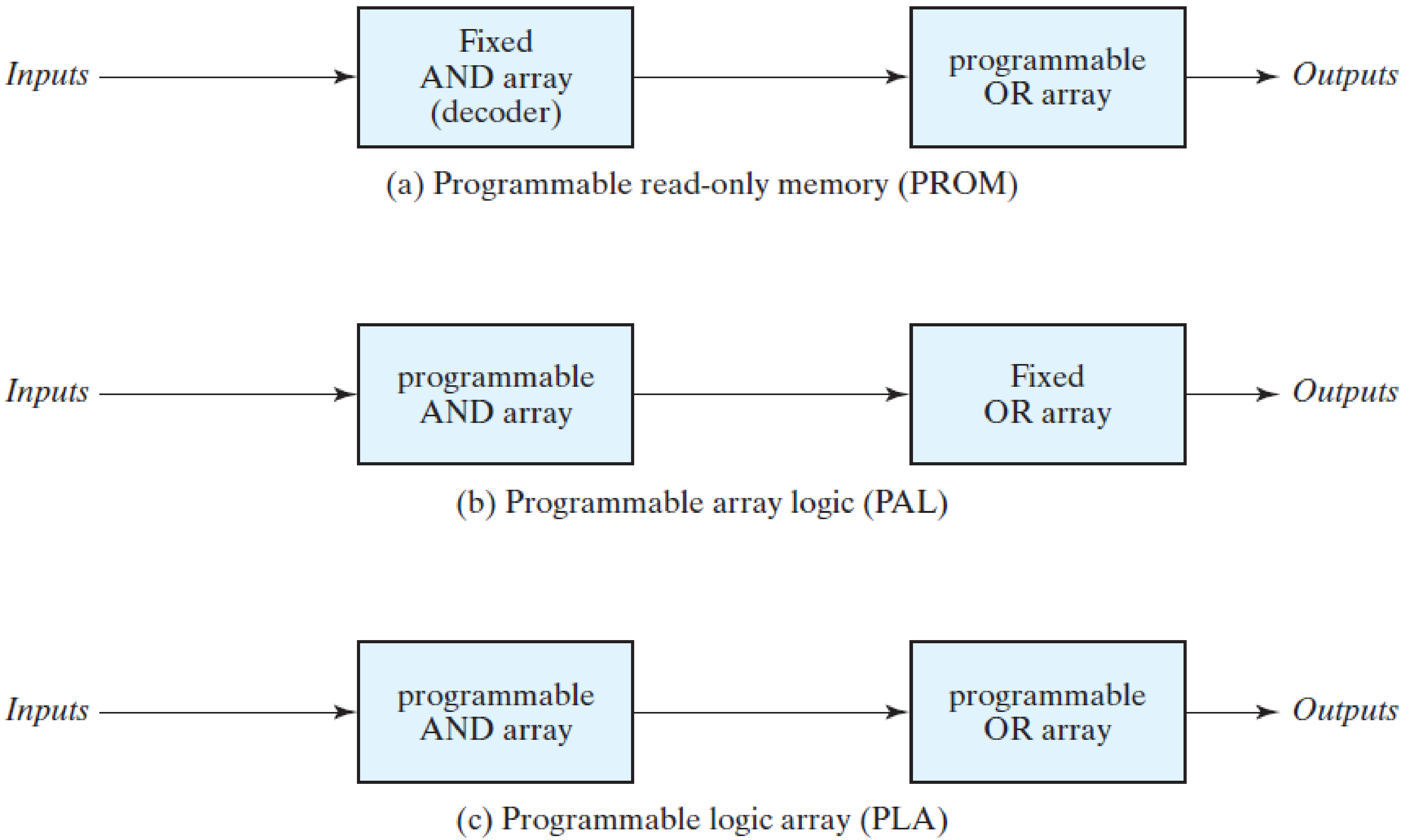


(a) Programmable read-only memory (PROM)

(b) Programmable array logic (PAL)

(c) Programmable logic array (PLA)

FIGURE 7.13
Basic configuration of three PLDs

The PAL is a programmable logic device with a fixed OR array and a programmable AND array.

Because only the AND gates are programmable, the PAL is easier to program than, but is not as flexible as, the PLA.

Sample PAL

A sample PAL with four inputs and four outputs.

Each input has a buffer–inverter gate, and each output is generated by a fixed OR gate.

There are four sections in the unit, each composed of an AND–OR array with three programmable AND gates in each section and one fixed OR gate.

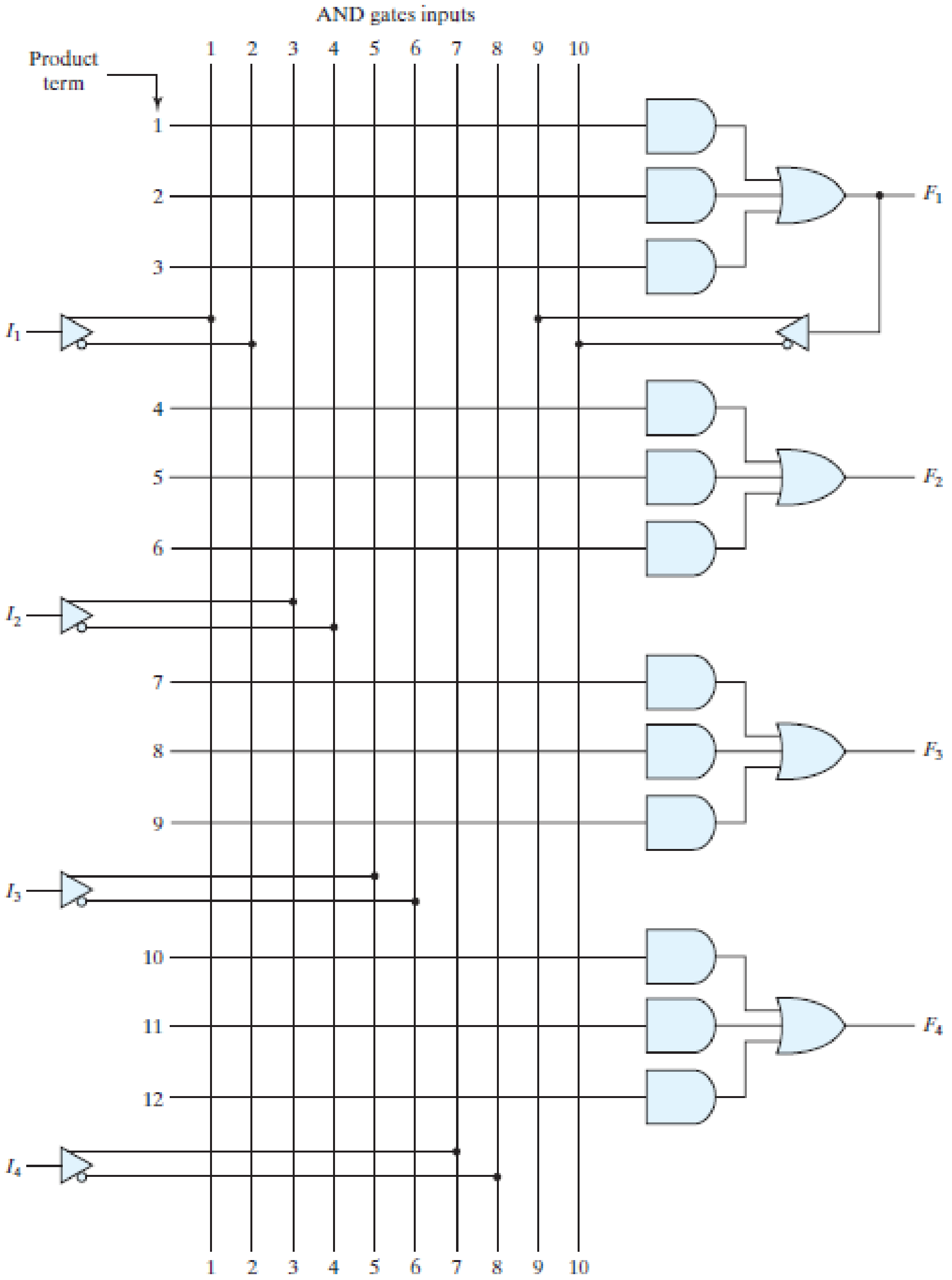


FIGURE 7.16
PAL with four inputs, four outputs, and a three-wide AND–OR structure

Sample PAL

Each AND gate has 10 programmable input connections

The horizontal line symbolizes the multiple-input configuration of the AND gate.

One of the outputs is connected to a buffer–inverter gate and then fed back into two inputs of the AND gates.

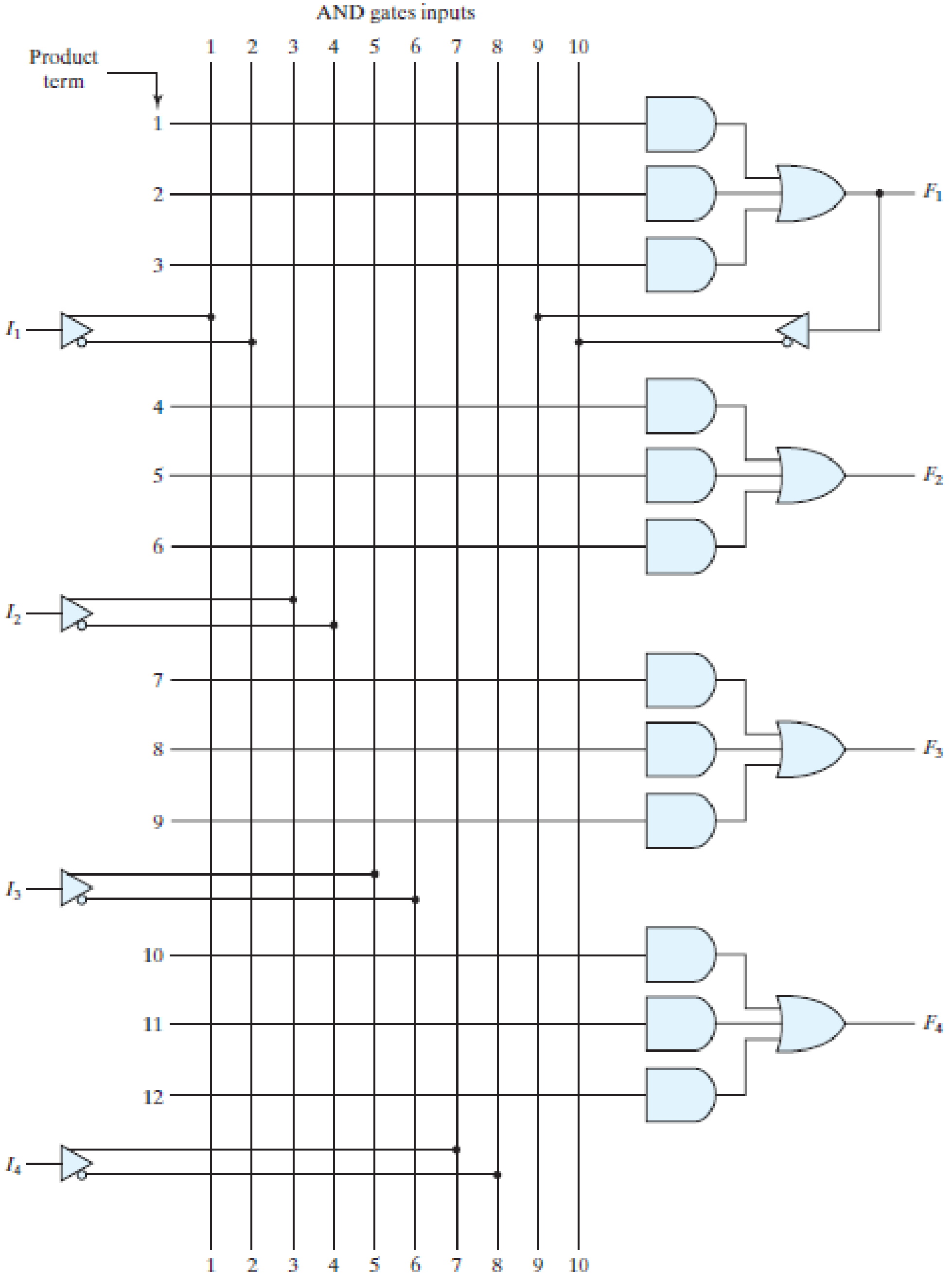


FIGURE 7.16
PAL with four inputs, four outputs, and a three-wide AND–OR structure

In designing with a PAL, the Boolean functions must be simplified to fit into each section.

Unlike the situation with a PLA, a product term cannot be shared among two or more OR gates.

Therefore, each function can be simplified by itself, without regard to common product terms.

The number of product terms in each section is fixed, and if the number of terms in the function is too large, it may be necessary to use two sections to implement one Boolean function.

Example of PAL

Implement this on PAL.

$w(A, B, C, D) = \sum(2, 12, 13)$

$x(A, B, C, D) = \sum(7, 8, 9, 10, 11, 12, 13, 14, 15)$

$y(A, B, C, D) = \sum(0, 2, 3, 4, 5, 6, 7, 8, 10, 11, 15)$

$z(A, B, C, D) = \sum(1, 2, 8, 12, 13)$

Example of PAL

Simplifying the four functions to a minimum number of terms results in the following Boolean functions:

$w = ABC' + A'B'CD'$

$x = A + BCD$

$y = A'B + CD + B'D'$

$z = ABC' + A'B'CD' + AC'D' + A'B'C'D$

$= w + AC'D' + A'B'C'D$

The PAL programming table is similar to the one used for the PLA, except that only the inputs of the AND gates need to be programmed.

Example of PAL

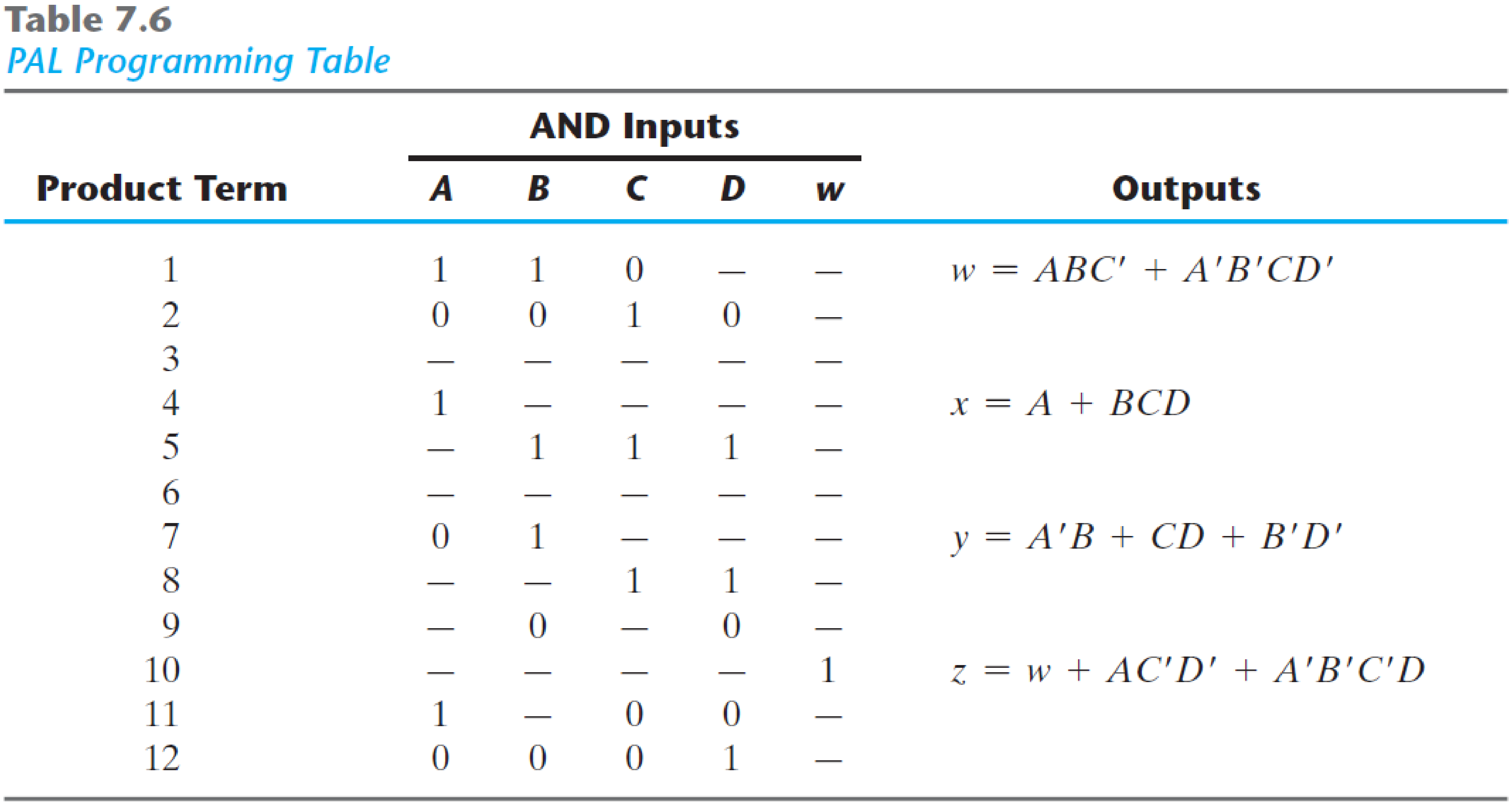


Table 7.6
PAL Programming Table

	AND Inputs					
Product Term	***A***	***B***	***C***	***D***	***w***	**Outputs**
1	1	1	0	—	—	$w = ABC' + A'B'CD'$
2	0	0	1	0	—	
3	—	—	—	—	—	
4	1	—	—	—	—	$x = A + BCD$
5	—	1	1	1	—	
6	—	—	—	—	—	
7	0	1	—	—	—	$y = A'B + CD + B'D'$
8	—	—	1	1	—	
9	—	0	—	0	—	
10	—	—	—	—	1	$z = w + AC'D' + A'B'C'D$
11	1	—	0	0	—	
12	0	0	0	1	—	

Fuse map

If the AND gate is not used, we leave all its input fuses intact.

Since the corresponding input receives both the true value and the complement of each input variable, we have *AA'* = 0 and the output of the AND gate is always 0.

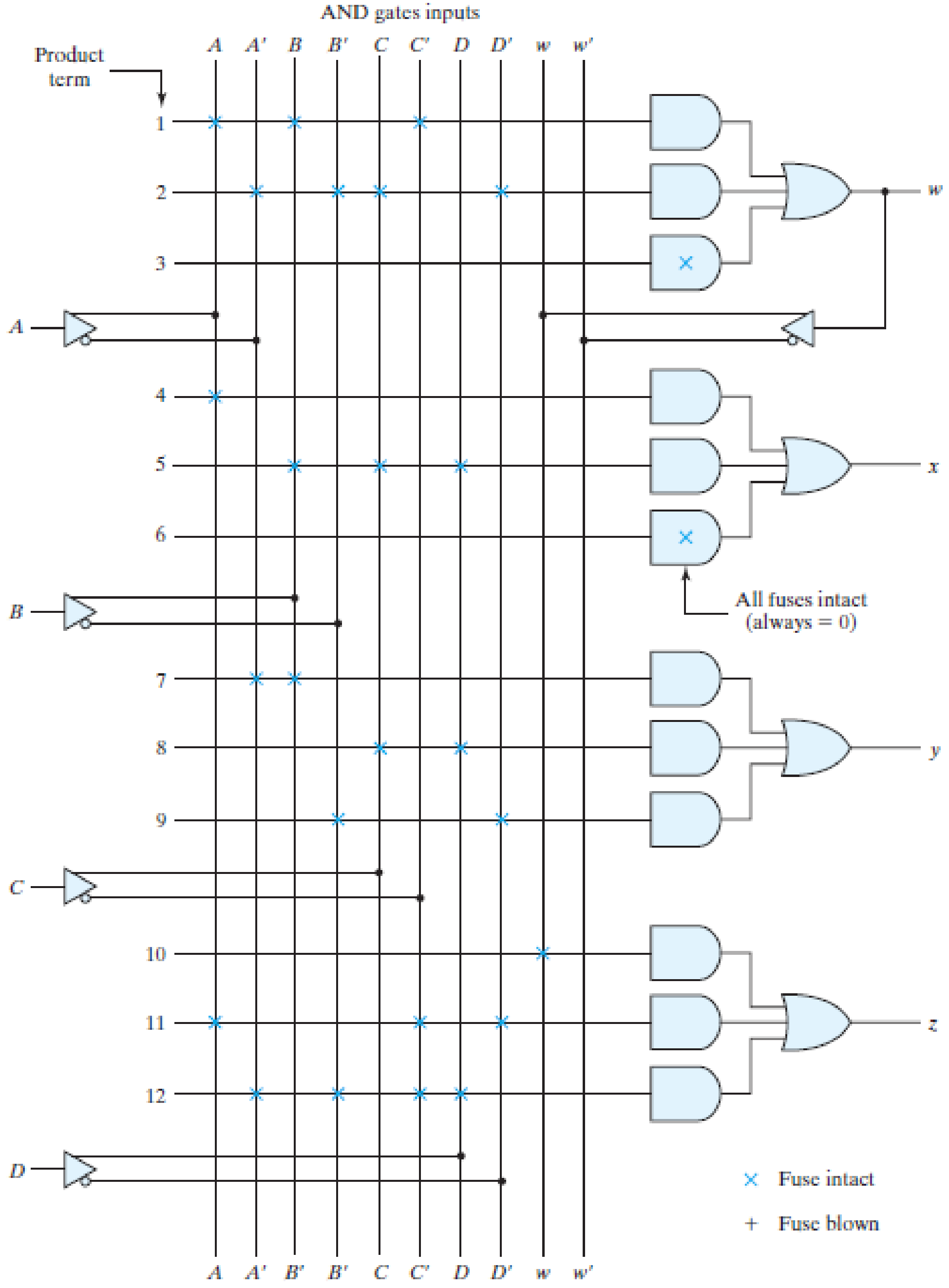
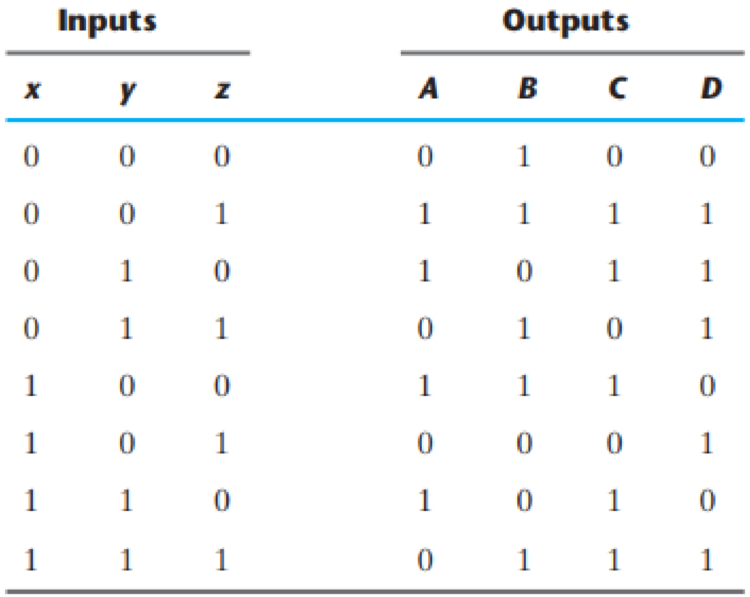


FIGURE 7.17
Fuse map for PAL as specified in Table 7.6

Problem – 7.25

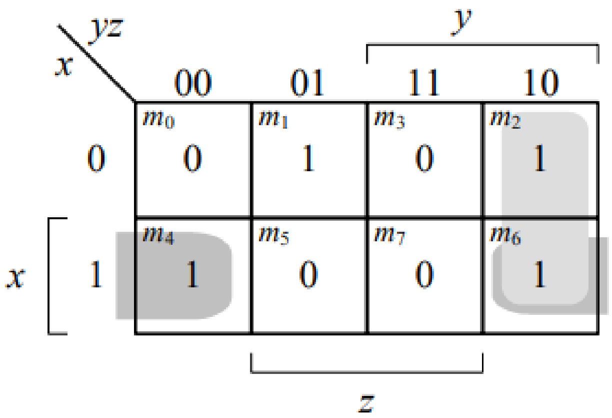
The following is a truth table of a three-input, four-output combinational circuit:



Inputs			Outputs			
x	*y*	*z*	*A*	*B*	*C*	*D*
0	0	0	0	1	0	0
0	0	1	1	1	1	1
0	1	0	1	0	1	1
0	1	1	0	1	0	1
1	0	0	1	1	1	0
1	0	1	0	0	0	1
1	1	0	1	0	1	0
1	1	1	0	1	1	1

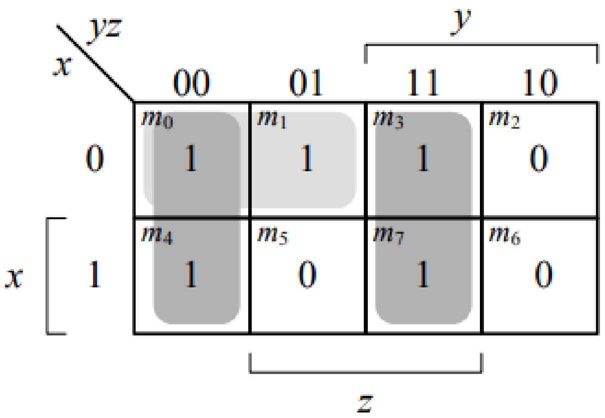
Tabulate the PAL programming table for the circuit, and mark the fuse map in a PAL diagram similar to the one shown in Fig. 7.17 .

Solution – 7.25



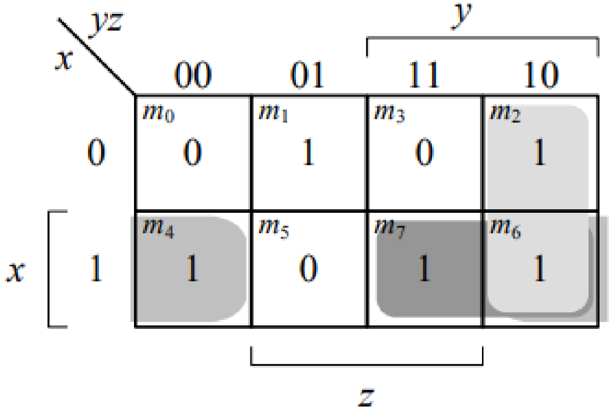
x \ yz	00	01	11	10
0	m_0 0	m_1 1	m_3 0	m_2 1
1	m_4 1	m_5 0	m_7 0	m_6 1

$A = yz' + xz' + x'y'z$



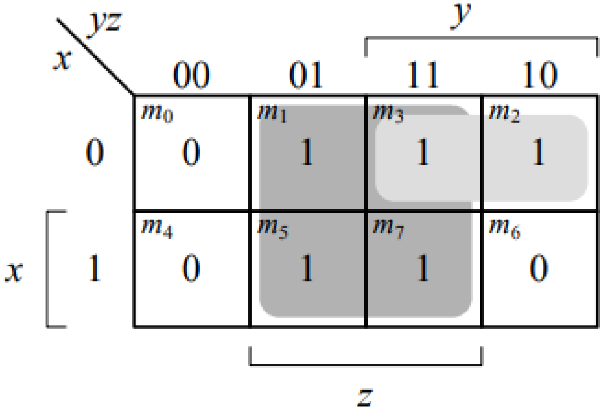
x \ yz	00	01	11	10
0	m_0 1	m_1 1	m_3 1	m_2 0
1	m_4 1	m_5 0	m_7 1	m_6 0

$B = y'z' + x'y' + yz$



x \ yz	00	01	11	10
0	m_0 0	m_1 1	m_3 0	m_2 1
1	m_4 1	m_5 0	m_7 1	m_6 1

$C = A + xyz$

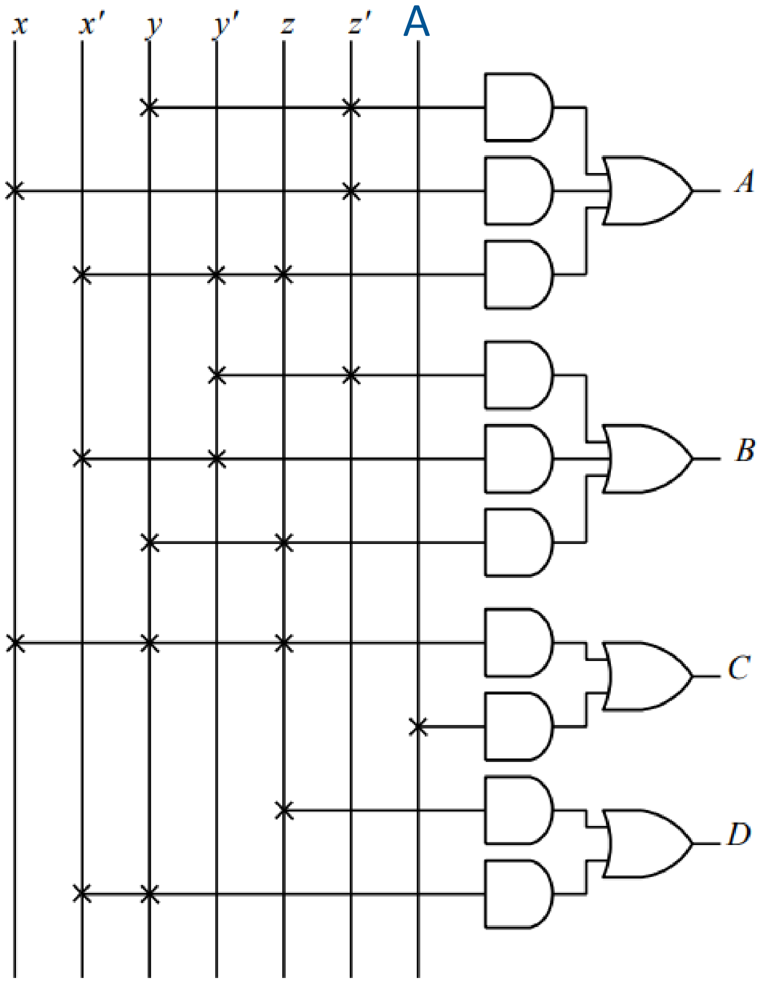


x \ yz	00	01	11	10
0	m_0 0	m_1 1	m_3 1	m_2 1
1	m_4 0	m_5 1	m_7 1	m_6 0

$D = z + x'y$

Product term	AND Inputs x	y	z	A	Outputs
1	-	1	0	-	A = yz' + xz' + x'y'z
2	1	-	0	-	
3	0	0	1	-	
4	-	0	0	-	B = y'z' + x'y' + yz
5	0	0	-	-	
6	-	1	1	-	
7	-	-	-	1	C = A + xyz
8	1	1	1	-	
9	-	-	-	-	
10	-	-	1	-	D = z + x'y
11	0	1	-	-	
12	-	-	-	-	

Solution – 7.25 (continued)



Product term	AND Inputs x	 y	 z	 A	Outputs
1	-	1	0	-	
2	1	-	0	-	A = yz' + xz' + x'y'z
3	0	0	1	-	
4	-	0	0	-	
5	0	0	-	-	B = y'z' + x'y' + yz
6	-	1	1	-	
7	-	-	-	1	
8	1	1	1	-	C = A + xyz
9	-	-	-	-	
10	-	-	1	-	
11	0	1	-	-	D = z + x'y
12	-	-	-	-	