JK and T Flipflop

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Versatility of JK flipflop

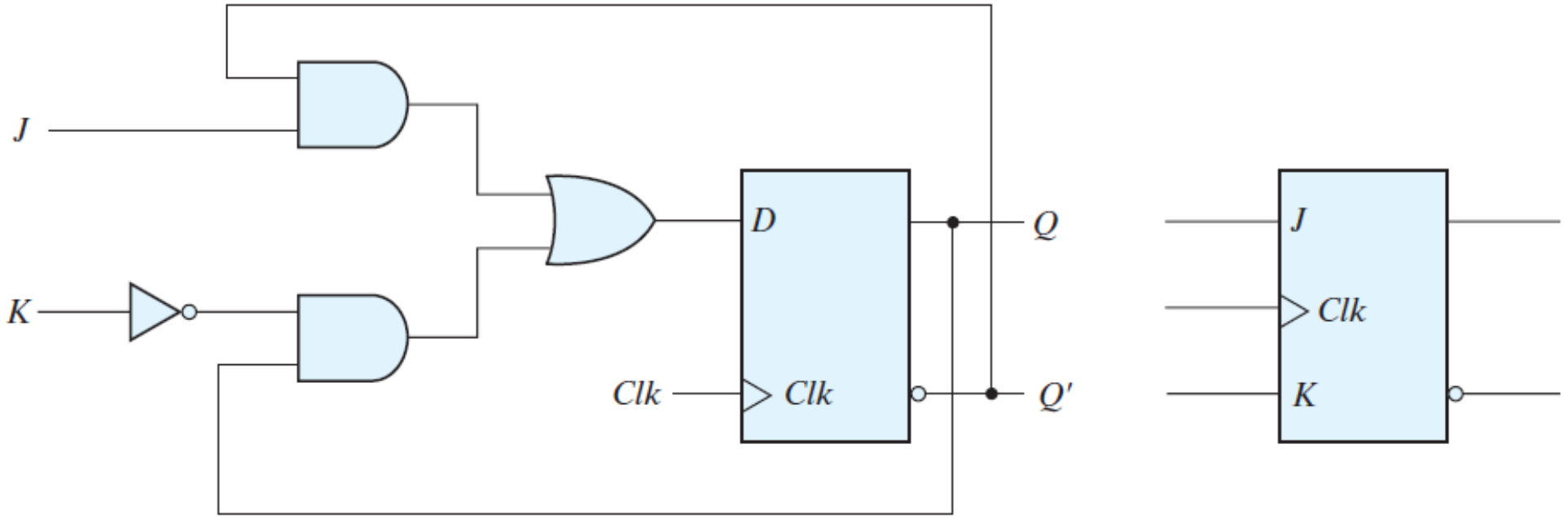
A flipflop can do three operations: Set it to 1, reset it to 0, or complement its output.

But, D flipflop can do only two operations since it has only 1 input.

Synchronized by a clock signal, the JK flip-flop has two inputs and performs all three operations.

JK Flip-flop

$$D = JQ' + K'Q$$



(a) Circuit diagram (b) Graphic symbol

FIGURE 5.12
JK flip-flop

JK flipflop

$$D = JQ' + K'Q$$

The J input sets the flip-flop to 1, the K input resets it to 0, and when both inputs are enabled, the output is complemented.

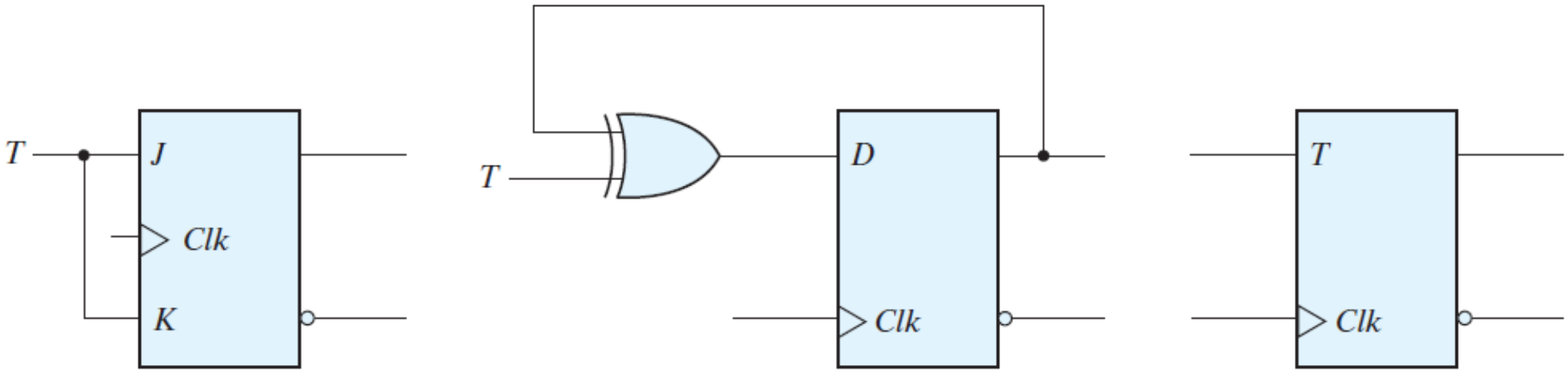
When $J = 1$ and $K = 0$, $D = Q + Q' = 1$, so the next clock edge sets the output to 1.

When $J = 0$ and $K = 1$, $D = 0$, so the next clock edge resets the output to 0.

When both $J = K = 1$ and $D = Q'$, the next clock edge complements the output.

When both $J = K = 0$ and $D = Q$, the clock edge leaves the output unchanged.

Toggle (T) flipflop



(a) From *JK* flip-flop (b) From *D* flip-flop (c) Graphic symbol

FIGURE 5.13
T flip-flop

$$D = T \oplus Q = TQ' + T'Q$$

The complementing flip-flop is useful for designing binary counters.

Characteristic table

Table 5.1
Flip-Flop Characteristic Tables

JK Flip-Flop

J	K	Q(t + 1)	
0	0	$Q(t)$	No change
0	1	0	Reset
1	0	1	Set
1	1	$Q'(t)$	Complement

D Flip-Flop

D	Q(t + 1)	
0	0	Reset
1	1	Set

T Flip-Flop

T	Q(t + 1)	
0	$Q(t)$	No change
1	$Q'(t)$	Complement

Characteristic Equation

$$Q(t+1) = D$$

Q(t) is simply written as Q.

$$Q(t+1) = JQ' + K'Q$$

$$Q(t+1) = T \oplus Q = TQ' + T'Q$$

Asynchronous (direct) set/reset

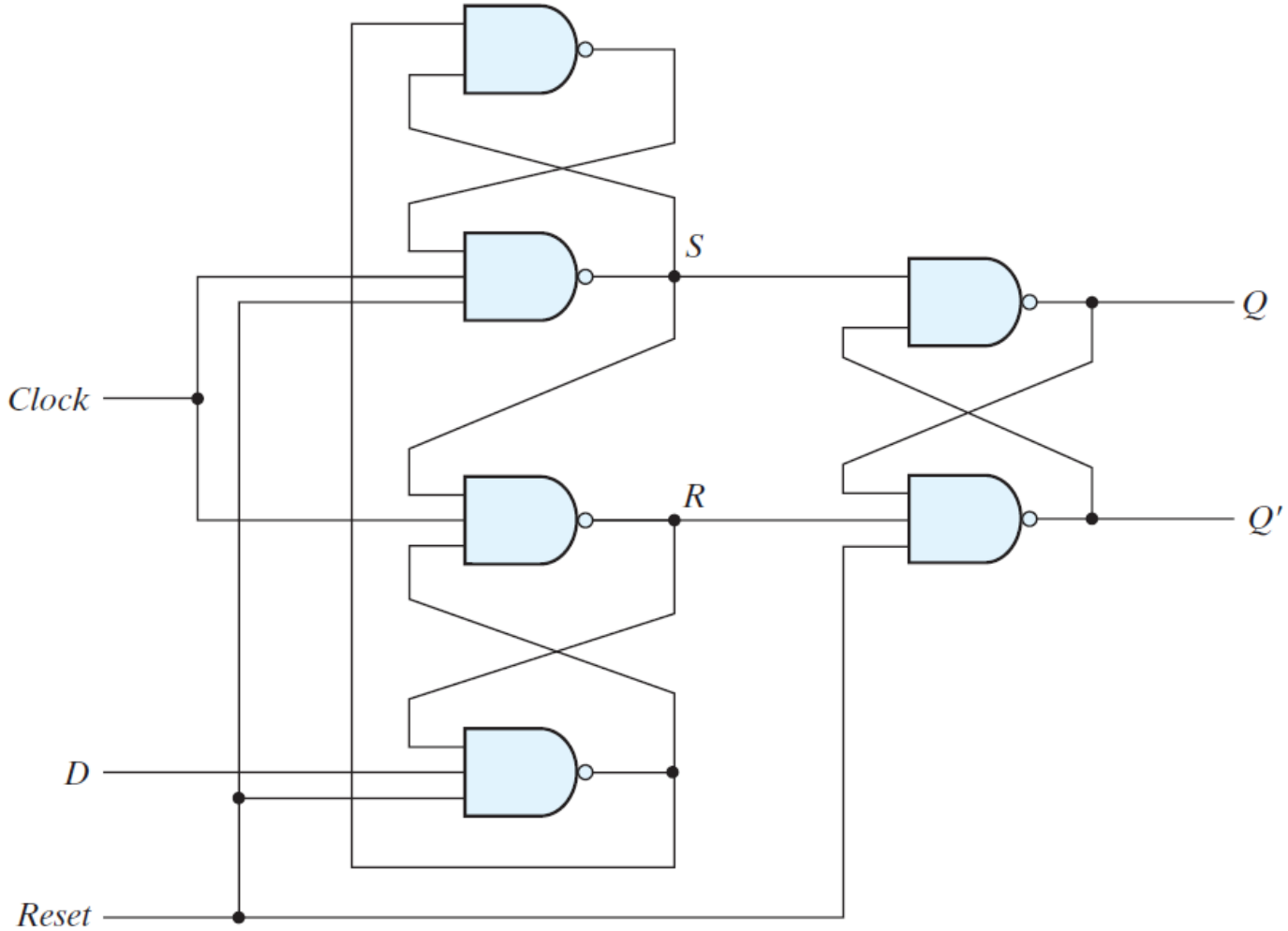
Some flip-flops have asynchronous inputs to force the flip-flop to a particular state independently of the clock.

Direct set/reset: setting flip-flip to 1 or 0.

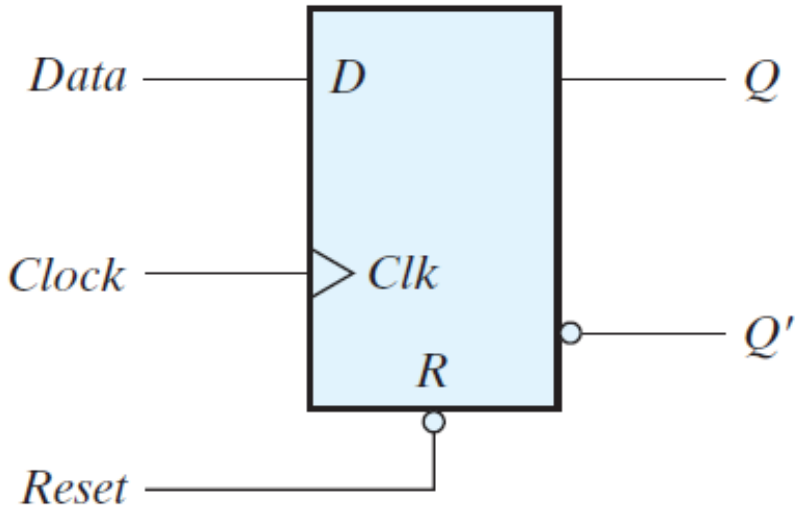
When power is turned on, the state of the flip-flops is unknown.

Direct inputs bring all flip-flops to a known starting state prior to the clocked operation.

Positive-edge-triggered *D* flip-flop with active-low asynchronous reset



(a) Circuit diagram



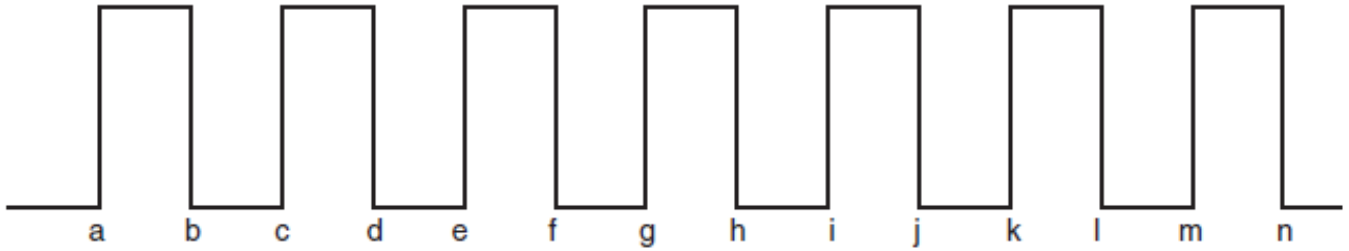
(b) Graphic symbol

R	*Clk*	*D*	*Q*	*Q′*
0	X	X	0	1
1	↑	0	0	1
1	↑	1	1	0

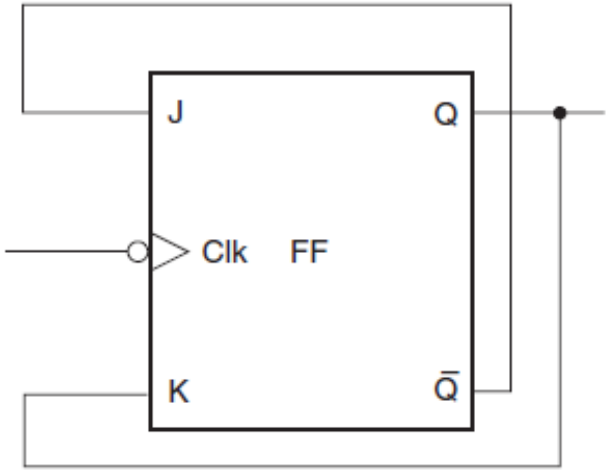
(b) Function table

Question

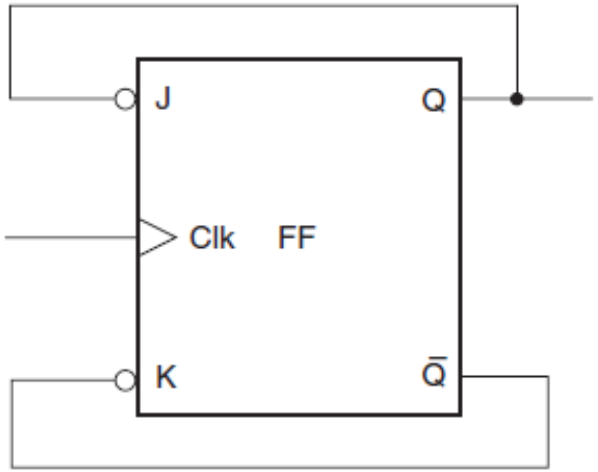
The 100 kHz square waveform is applied to the clock input of the flip-flops. If the Q output is initially '0', draw the Q output waveforms. Also, determine the frequency of the Q output.



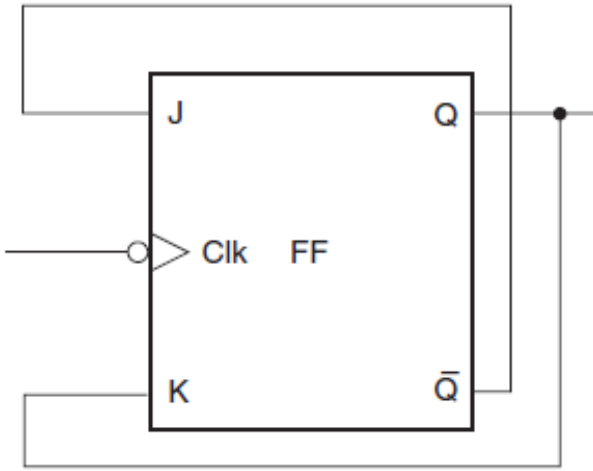
Circuit 1



Circuit 2



Solution of circuit 1



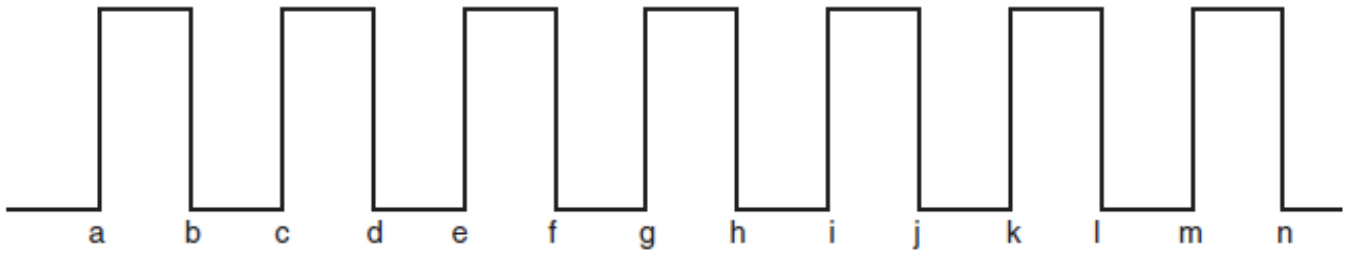
Q is initially '0'. ➔ J=1, K=0.

At first negative edge of clock, Q becomes 1.

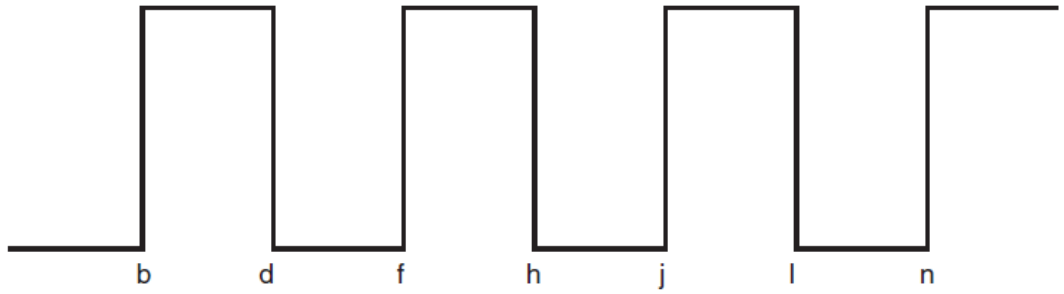
➔J=0, K=1

With the next negative edge, Q=0.

This process continues, and Q alternately becomes '1' and '0'.

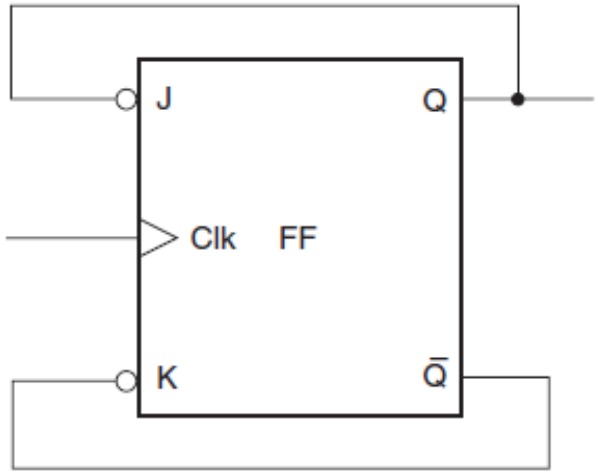


Input



Output

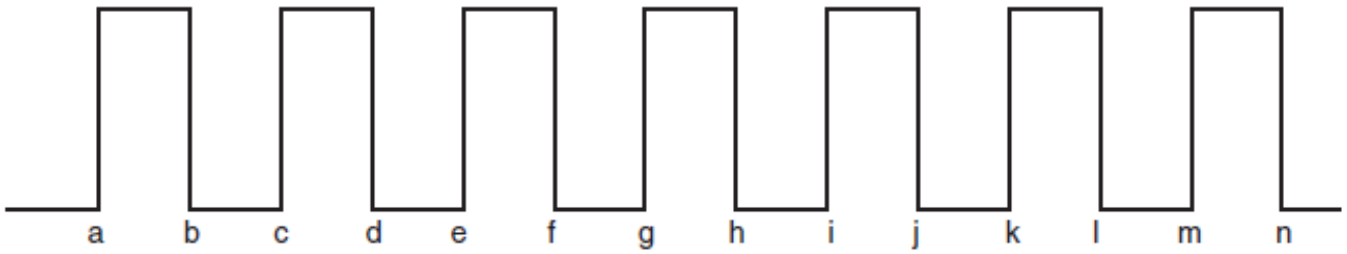
Solution of circuit 2



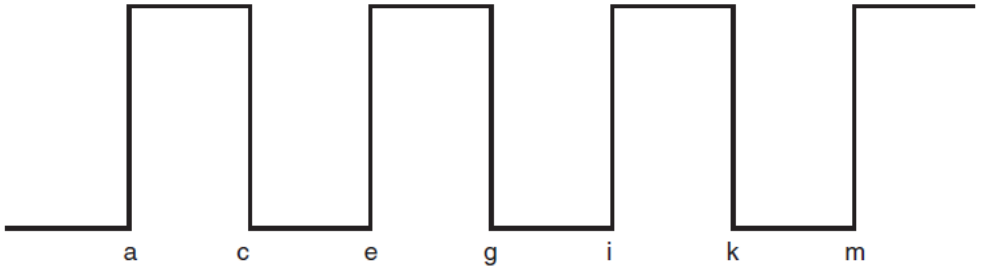
The circuit behaves similarly to first circuit.

Only change: transition happens on positive edge.

In both cases, output frequency is half of input frequency.



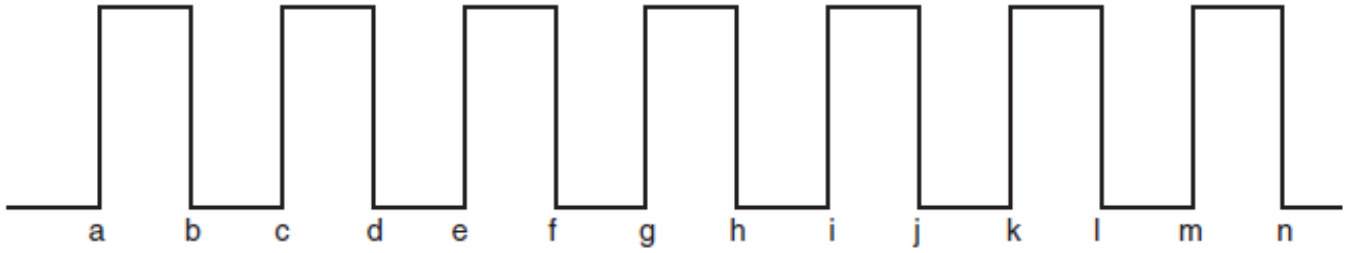
Input

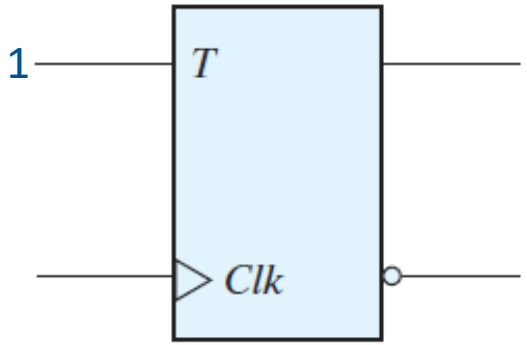


Output

Question

The 100 kHz square waveform is applied to the clock input of T flip-flop. If the Q output is initially '0', draw the Q output waveforms. Also, determine the frequency of the Q output.

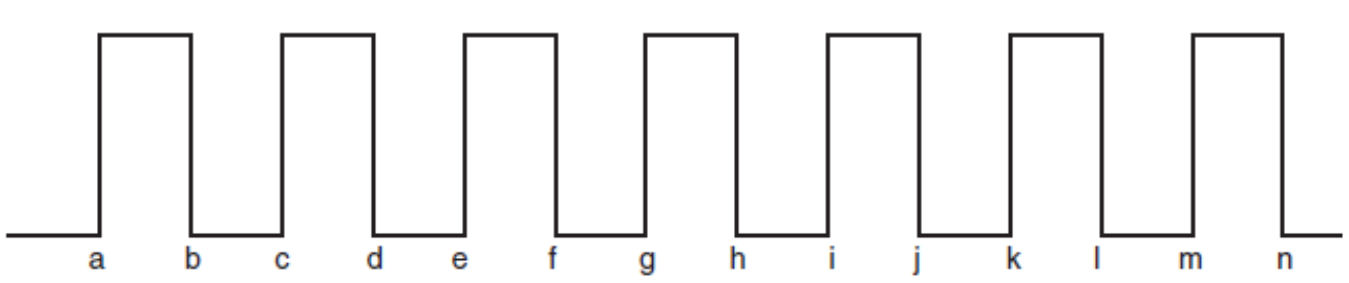




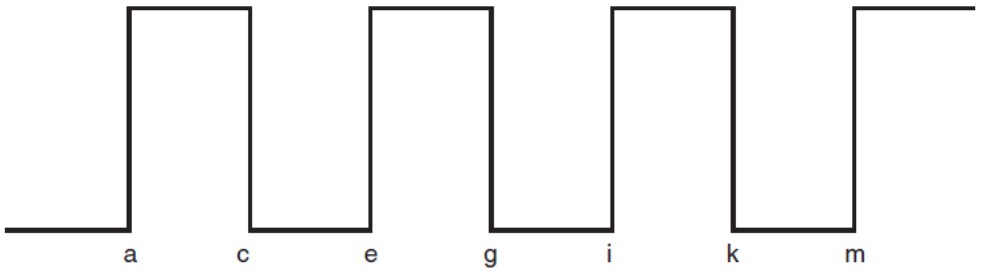
Solution

The circuit acts as a frequency divider.

Transition happens on positive edge.



Input



Output

The Big Picture: Storage Elements

- Latches and Flip-Flops
  - Very fast, parallel access
  - Very expensive (one bit costs tens of transistors)
- Static RAM (SRAM)
  - Relatively fast
  - Expensive (one bit costs 6+ transistors)
- Dynamic RAM (DRAM)
  - Slower, reading destroys content (refresh), needs special process for manufacturing
  - Cheap (one bit costs only one transistor plus one capacitor)
- Other storage technology (flash memory, hard disk, tape)
  - Much slower, access takes a long time,