Memory Decoding

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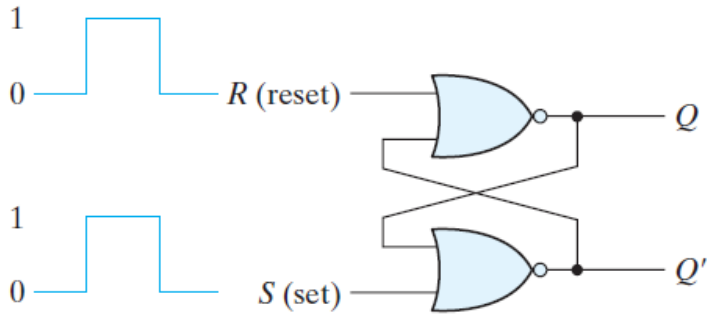
Background: SR Latch

We will use SR Latch with NOR gates

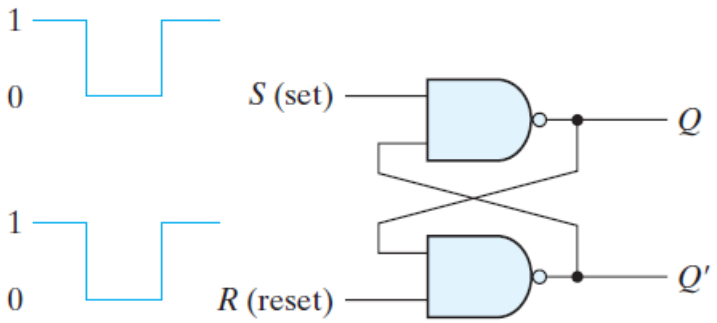


(a) Logic diagram

S	R	Q	Q'	
1	0	1	0	
0	0	1	0	(after $S = 1, R = 0$)
0	1	0	1	
0	0	0	1	(after $S = 0, R = 1$)
1	1	0	0	(forbidden)

(b) Function table

FIGURE 5.3
SR latch with NOR gates



(a) Logic diagram

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0	0	1	1	(forbidden)

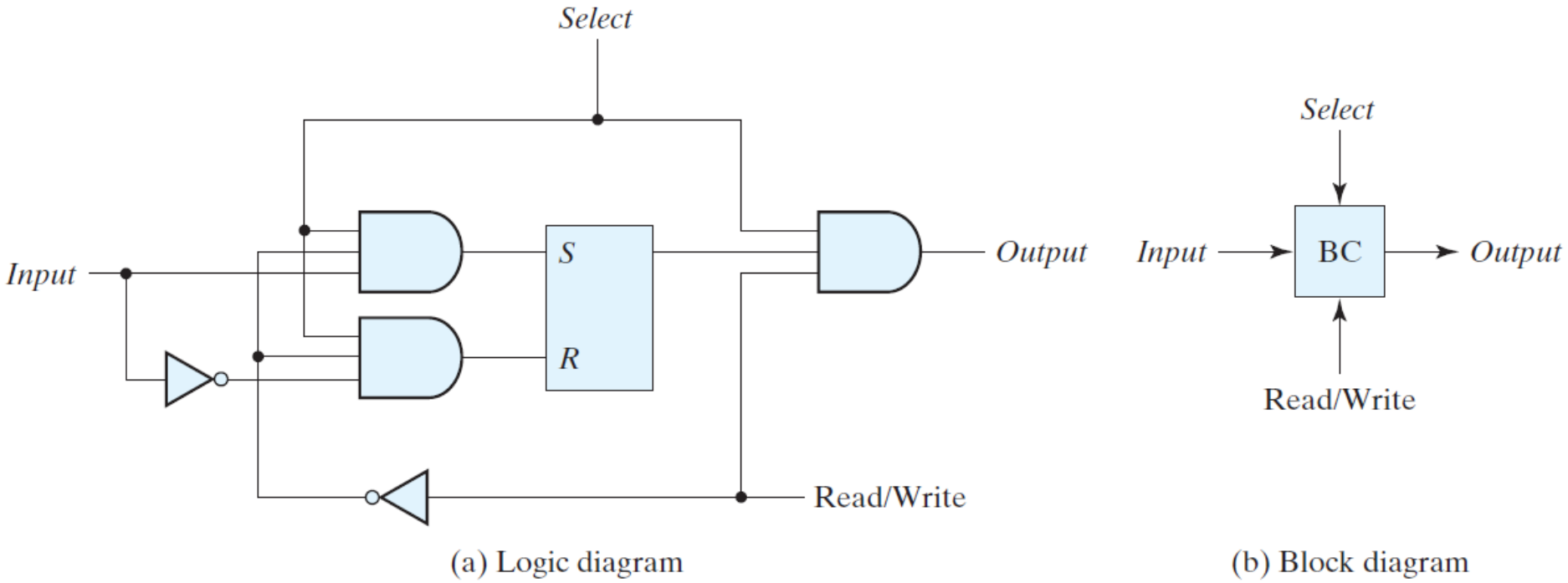
(b) Function table

FIGURE 5.4
SR latch with NAND gates

Binary storage cell (stores 1b data)

The binary storage cell is the basic building block of a memory unit.

Here is equivalent logic of a binary cell that stores one bit of information:



The storage part of the cell is an SR latch with associated gates to form a D latch.

Working

The select input enables the cell for reading or writing, and the read/write input determines the operation of the cell when it is selected.

A 1 in the read/write input provides the read operation by forming a path from the latch to the output terminal.

A 0 in the read/write input provides the write operation by forming a path from the input terminal to the latch.

Design of RAM

A RAM of m words and n bits per word consists of m * n binary storage cells and associated decoding circuits for selecting individual words.

We will show memory decoding for a memory with a capacity of 16 bits, arranged in four words of 4 bits each.

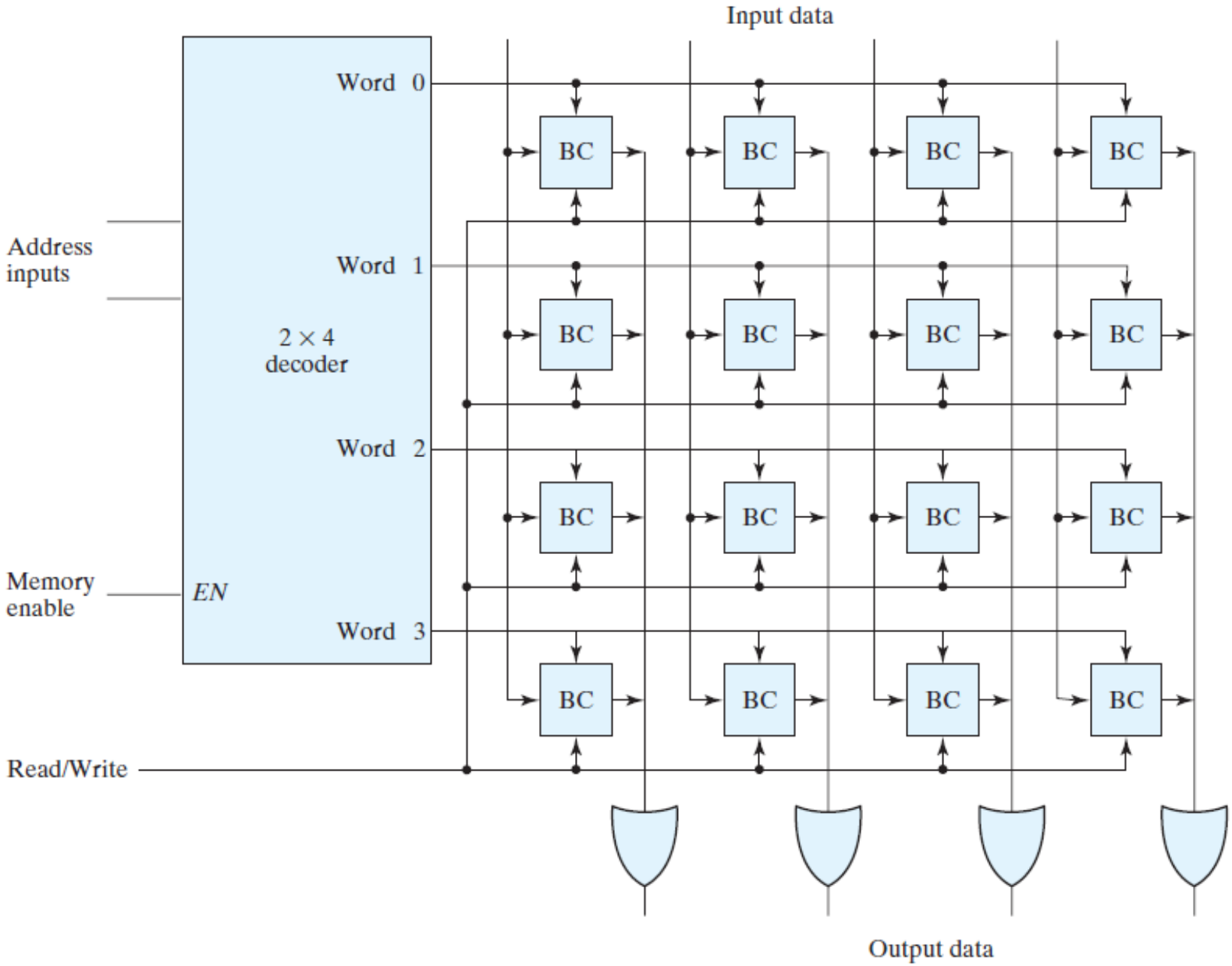
RAM

A memory with four words needs two address lines.

The two address inputs go through a 2 * 4 decoder to select one of the four words.

The decoder is enabled with the memory-enable input.

Memory enable is 0 ==> all decoder outputs are 0. None of the memory words are selected.

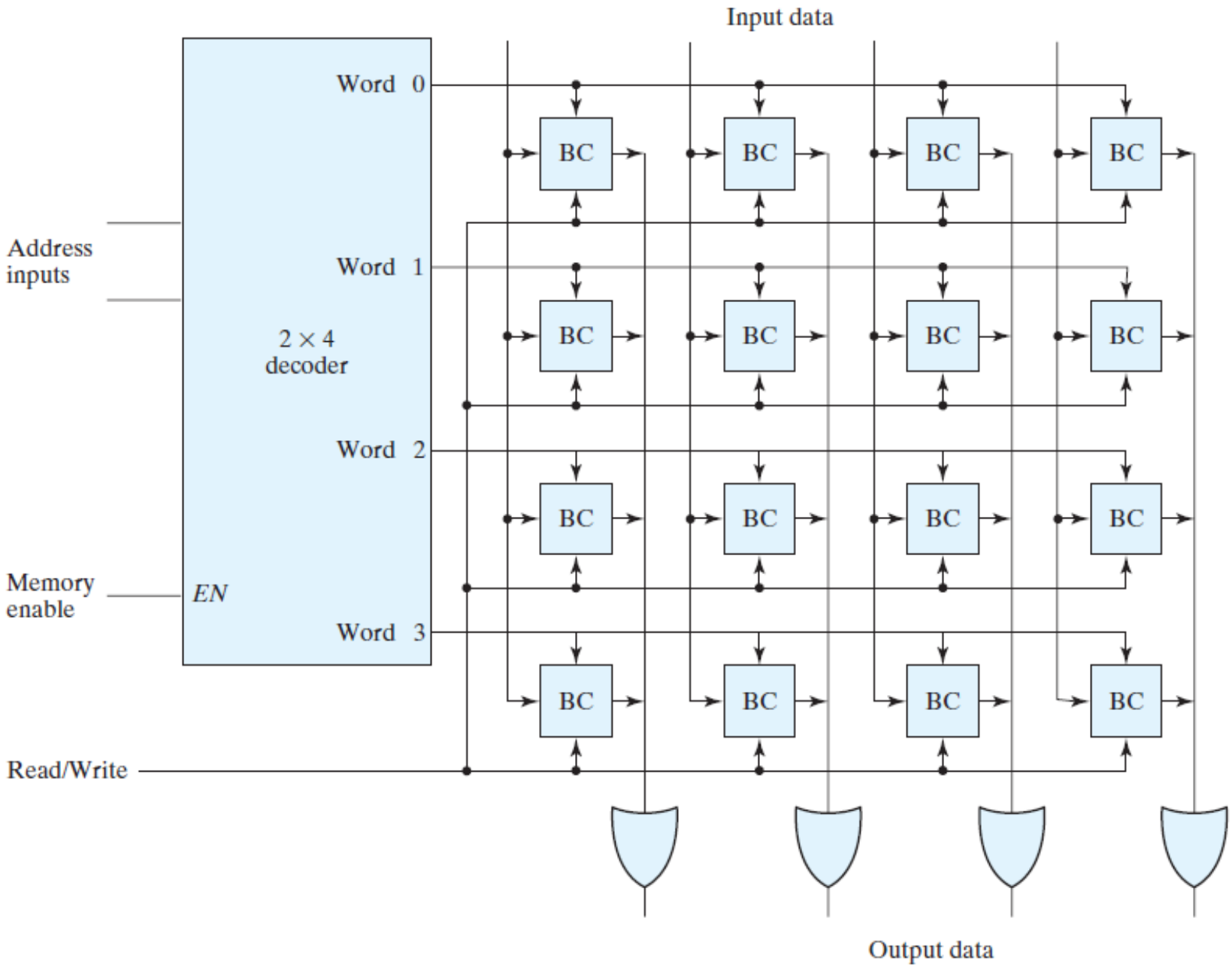


RAM

Memory select at 1==> one of the four words is selected, dictated by the value in the two address lines.

Once a word has been selected, the read/write input determines the operation.

During the read operation, the four bits of the selected word go through OR gates to the output terminals.



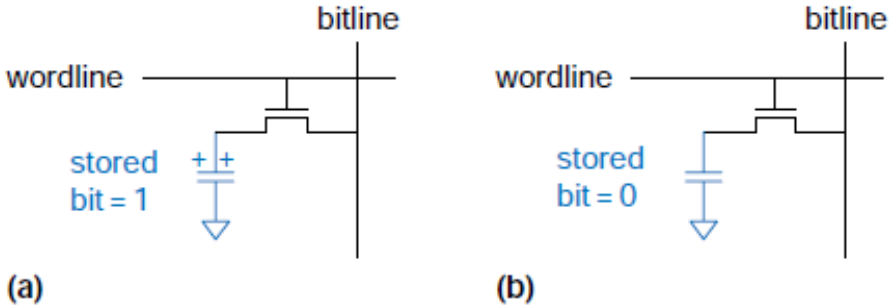


Figure 5.45 DRAM stored values

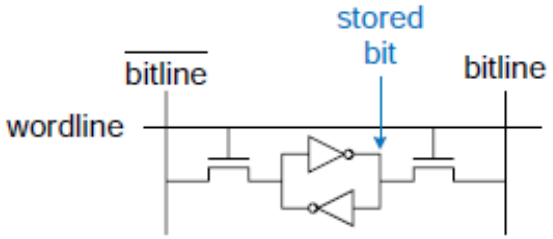
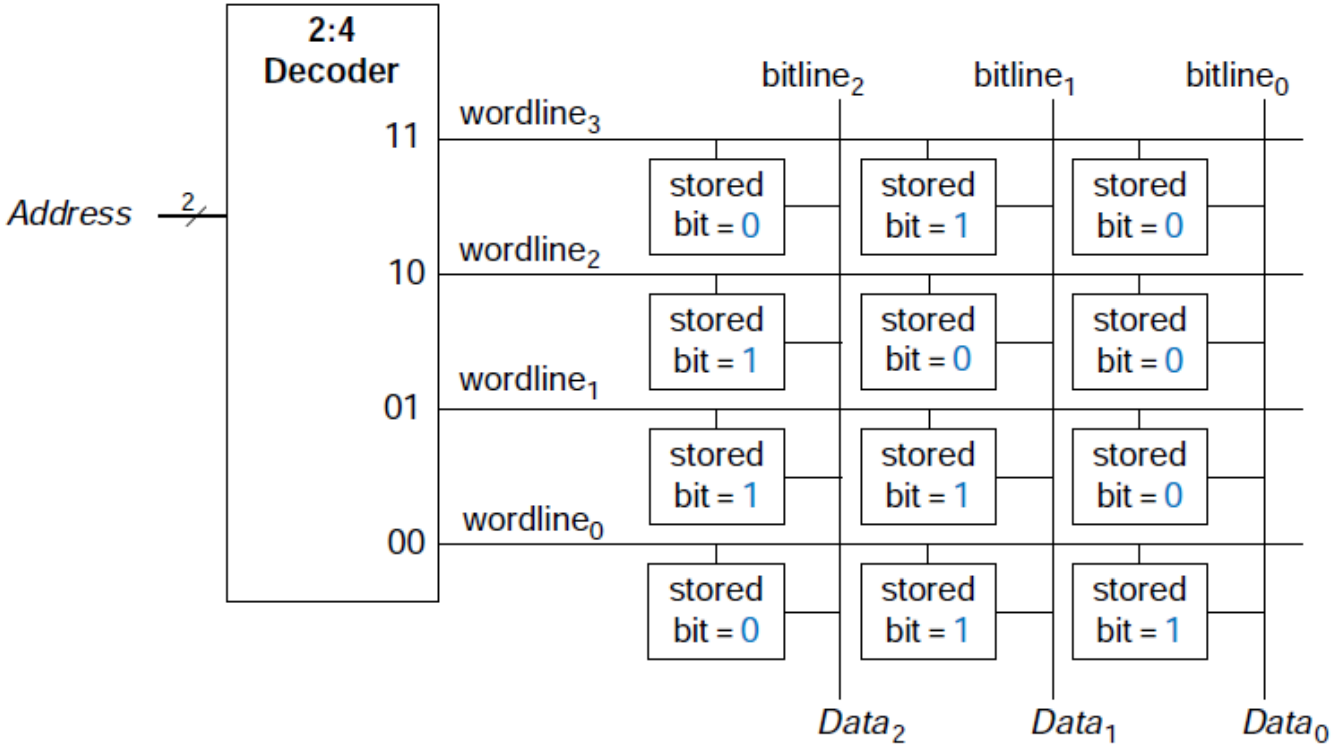
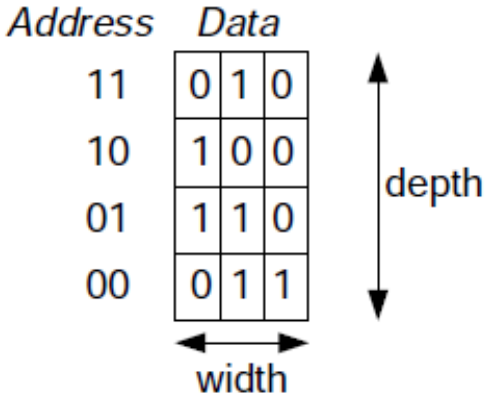


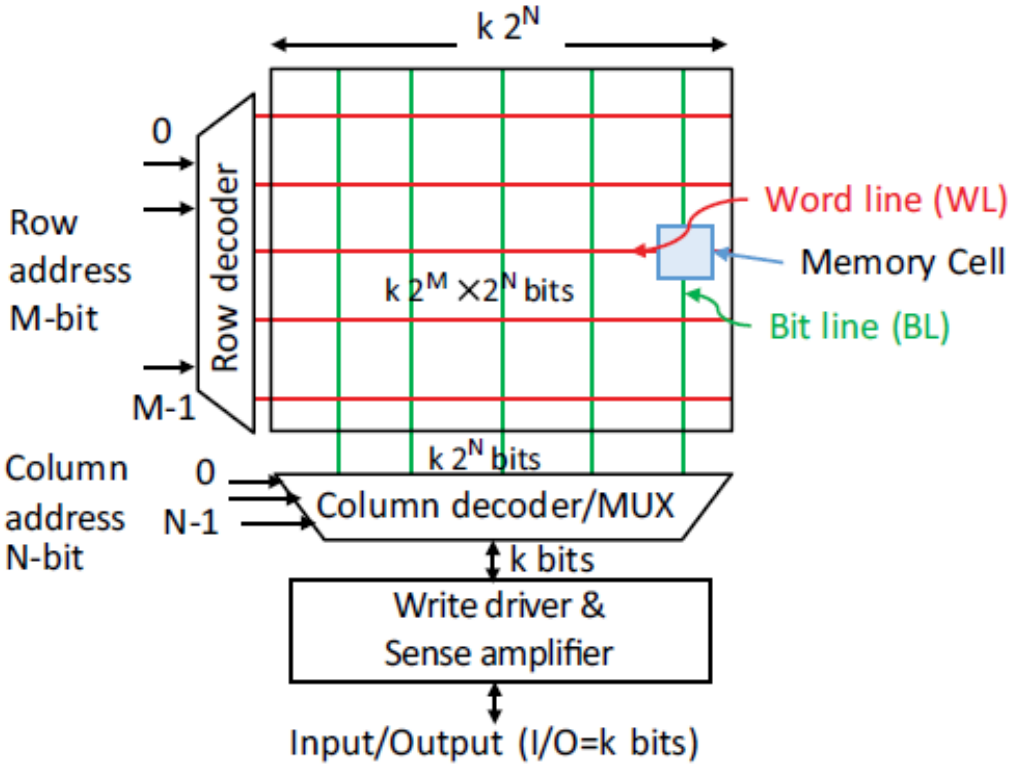
Figure 5.46 SRAM bit cell

Organization of a 4x3 memory array





Stored data



The generic memory sub-array diagram organized in a 2D matrix, showing the memory cell array and its peripheral circuit modules

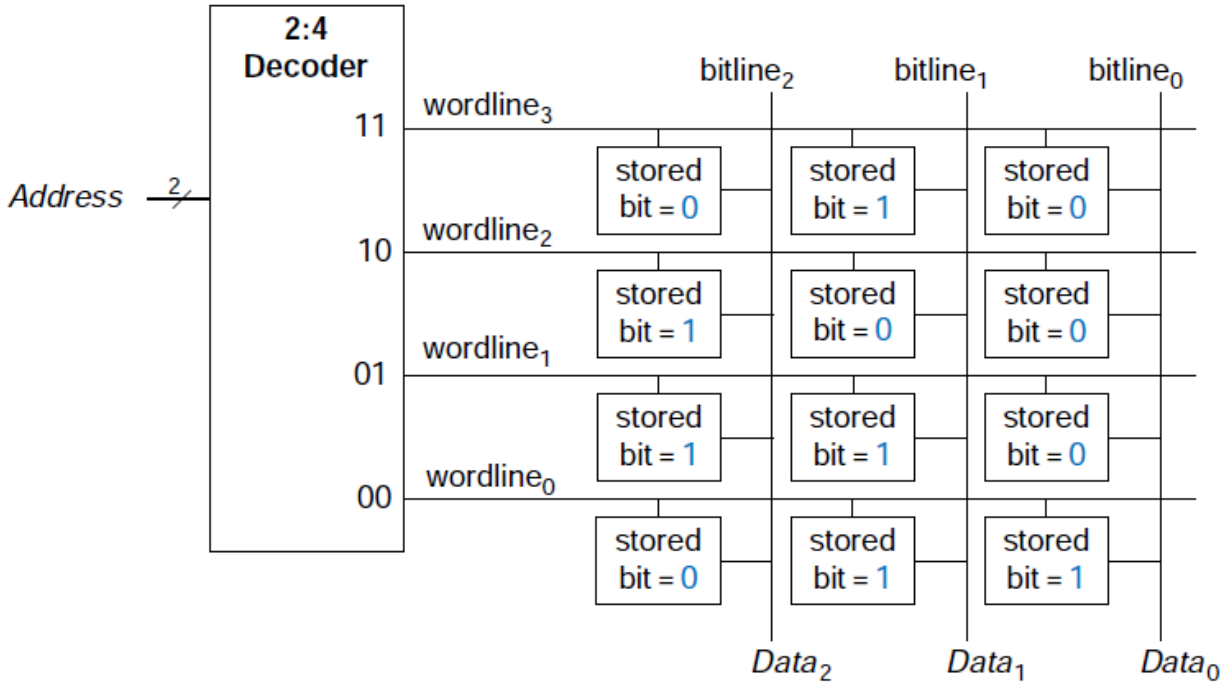
Organization of a 4x3 memory array

Memory read: a wordline is asserted, and the corresponding row of bit cells drives the bitlines HIGH or LOW.

Memory write: the bitlines are driven HIGH or LOW first and then a wordline is asserted, allowing the bitline values to be stored in that row of bit cells.

To read *Address* 10, the bitlines are left floating, the decoder asserts *wordline2*, and the data stored in that row of bit cells, 100, reads out onto the *Data* bitlines.

To write the value 001 to *Address* 11, the bitlines are driven to the value 001, then *wordline3* is asserted and the new value (001) is stored in the bit cells.



Write operation on RAM

During the write operation, the data available in the input lines are transferred into the four binary cells of the selected word.

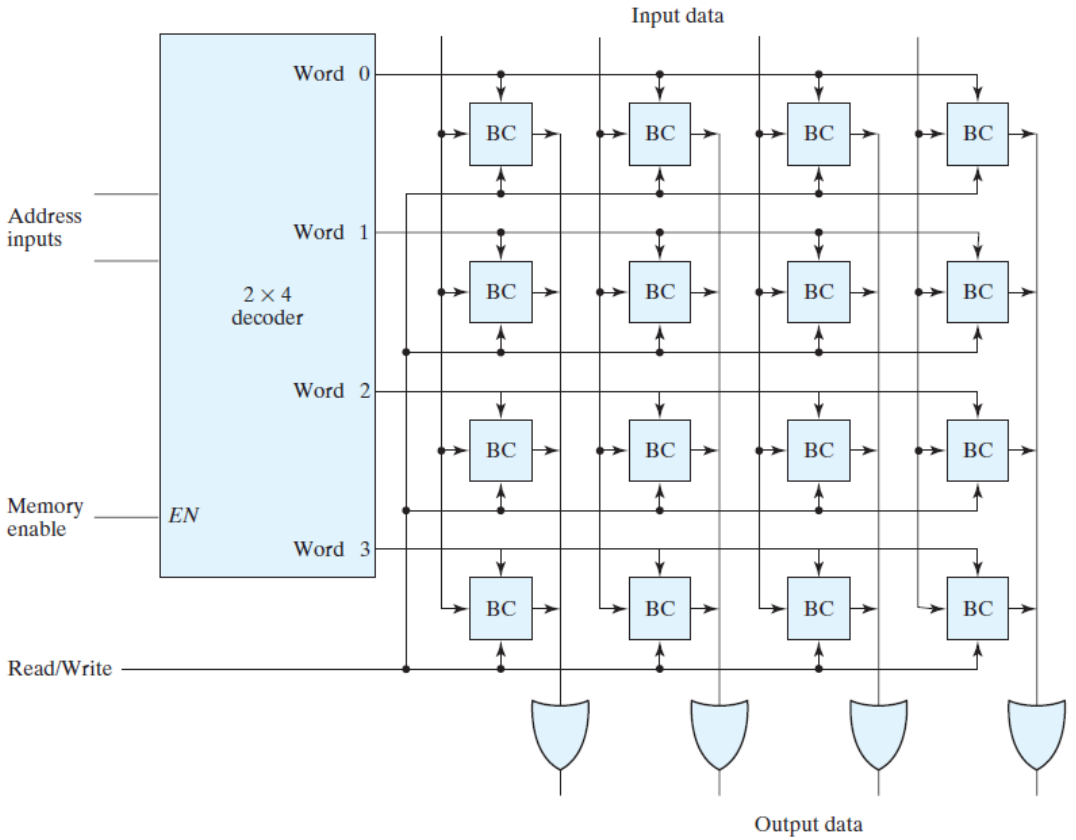
The binary cells that are not selected are disabled, and their previous binary values remain unchanged.

When the memory select input that goes into the decoder is equal to 0, none of the words are selected and the contents of all cells remain unchanged regardless of the value of the read/write input.

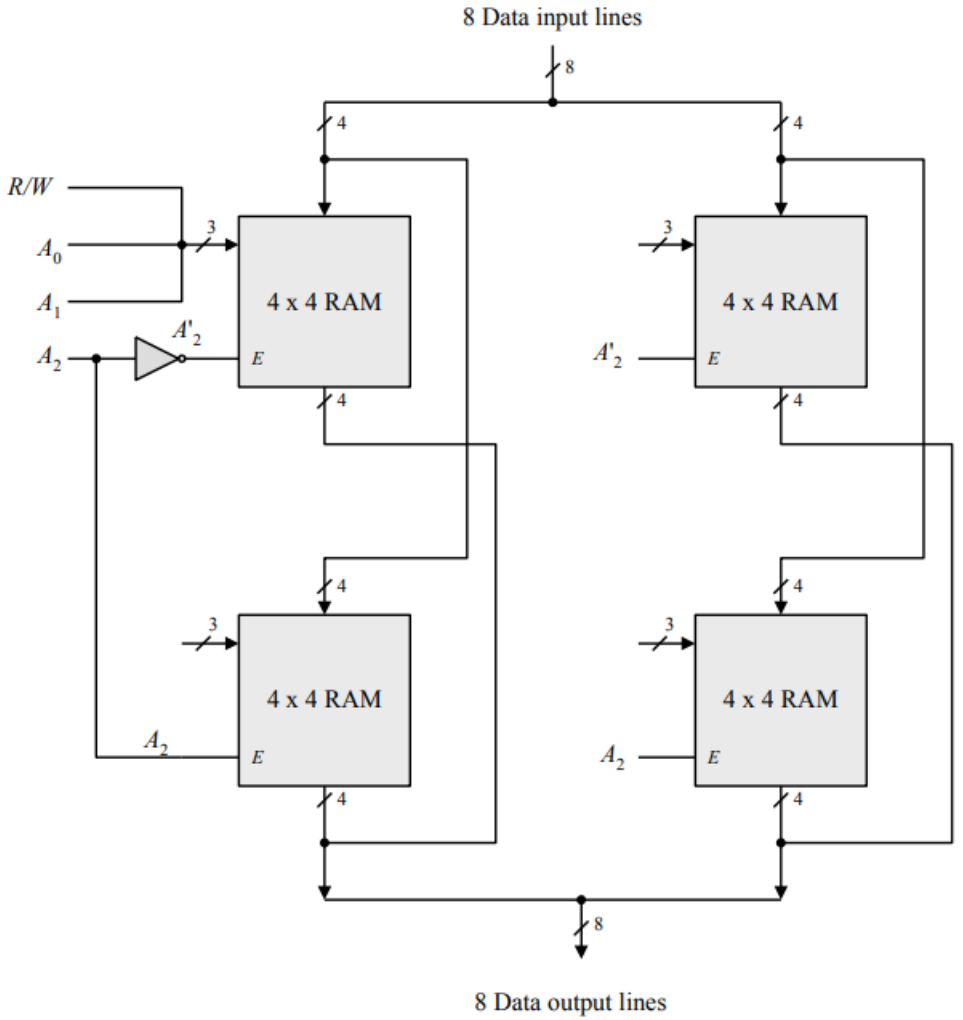
Problem – 7.6

Enclose the 4 × 4 RAM of Fig. 7.6 in a block diagram showing all inputs and outputs. Assuming three-state outputs, construct an 8 × 8 memory using four 4 × 4 RAM units.

Fig. 7.6



Solution – 7.6


8 Data input lines
8
4
4
R/W
A0
A1
3
4 x 4 RAM
A'2
A2
E
4
3
4 x 4 RAM
A'2
E
4
4
3
4 x 4 RAM
A2
E
4
4
3
4 x 4 RAM
A2
E
4
8
8 Data output lines

Problem – 7.8

(a) How many 32K × 8 RAM chips are needed to provide a memory capacity of 256K bytes?
(b) How many lines of the address must be used to access 256K bytes? How many of these lines are connected to the address inputs of all chips?
(c) How many lines must be decoded for the chip select inputs? Specify the size of the decoder.

Solution – 7.8

(a) 256 K / 32 K = 8 chips

(b) 256 K = 2^{18} (18 address lines for memory); 32 K = 2^{15} (15 address pins / chip)

(c) 18 – 15 = 3 lines ; must decode with 3 × 8 decoder

Two-dimensional decoding (Coincident Decoding)

Coincident decoding

A decoder with k inputs and 2^k outputs requires 2^k AND gates with k inputs per gate.

The total number of gates and the number of inputs per gate can be reduced by employing two decoders in a two-dimensional selection scheme.

Key idea in two-dimensional decoding is to arrange the memory cells in an array that is close as possible to square.

Then, two k /2-input decoders are used instead of one k -input decoder.

One decoder performs the row selection and the other the column selection in a two-dimensional matrix configuration.

Example: 1K memory

1D decoding: We need a 10 * 1,024 decoder. It needs 1,024 AND gates with 10 inputs in each.

2D decoding: we need 2*32 AND gates with 5 inputs in each.

Five MSBs of the address go to input X and the five least significant bits go to input Y.

Each word within the memory array is selected by the coincidence of one X line and one Y line.

Thus, each word in memory is selected by the coincidence between 1 of 32 rows and 1 of 32 columns, for a total of 1,024 words.

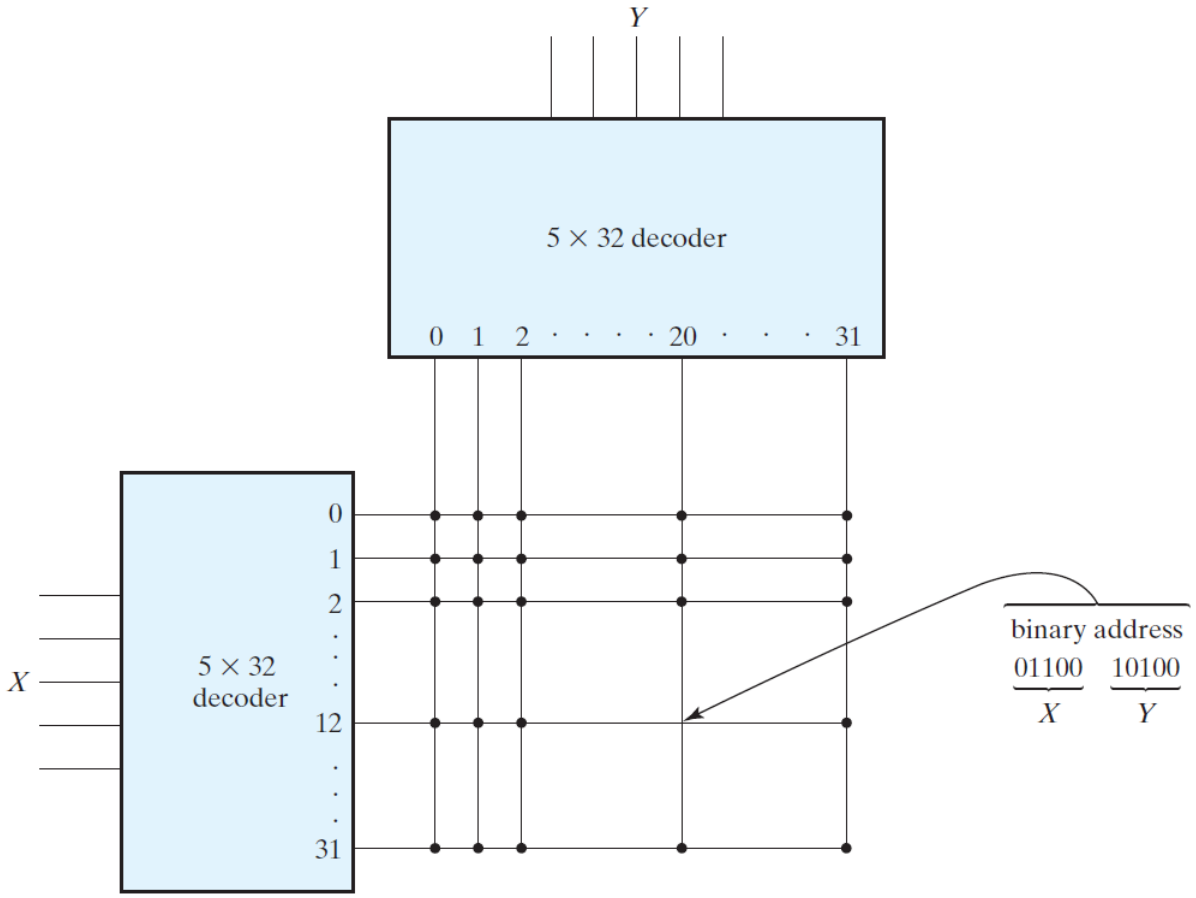


FIGURE 7.7
Two-dimensional decoding structure for a 1K-word memory

Example (continued)

Consider the word whose address is 404 (01100 10100 in binary).

Hence, X = 01100 (binary 12) and Y = 10100 (binary 20).

The n-bit word that is selected lies in the X decoder output number 12 and the Y decoder output number 20.

All the bits of the word are selected for reading or writing.

Problem – 7.7

A 16K × 4 memory uses coincident decoding by splitting the internal decoder into X -selection and Y -selection.

(a) What is the size of each decoder, and how many AND gates are required for decoding the address?

(b) Determine the X and Y selection lines that are enabled when the input address is the binary equivalent of 6,000.

Solution – 7.7

(a) $16\ K = 2^{14} = 2^7 \times 2^7 = 128 \times 128$

Each decoder is 7×128. Decoders require 256 AND gates, each with 7 inputs

(b) 6,000 = 0101110_1110000

x = 46 y = 112

Address multiplexing

Address multiplexing

Because of their large capacity, the address decoding of DRAMs is arranged in a two-dimensional array.

In a two-dimensional array, the address is applied in two parts at different times, with the row address first and the column address second.

Since the same set of pins is used for both parts of the address, the size of the package is decreased significantly

Example: 64K word memory

The memory has a 2D array of cells arranged into 256 rows by 256 columns, for a total of

$2^8 * 2^8 = 2^{16} = 64K$ words.

There is single data input line, a single data output line, and a read/write control.

There is an eight-bit address input, a row address strobe and a column address strobe. These strobes are used for enabling the row and column address into their respective registers.

The bar on top of RAS and CAS indicates that registers are enabled on the zero level of the signal.

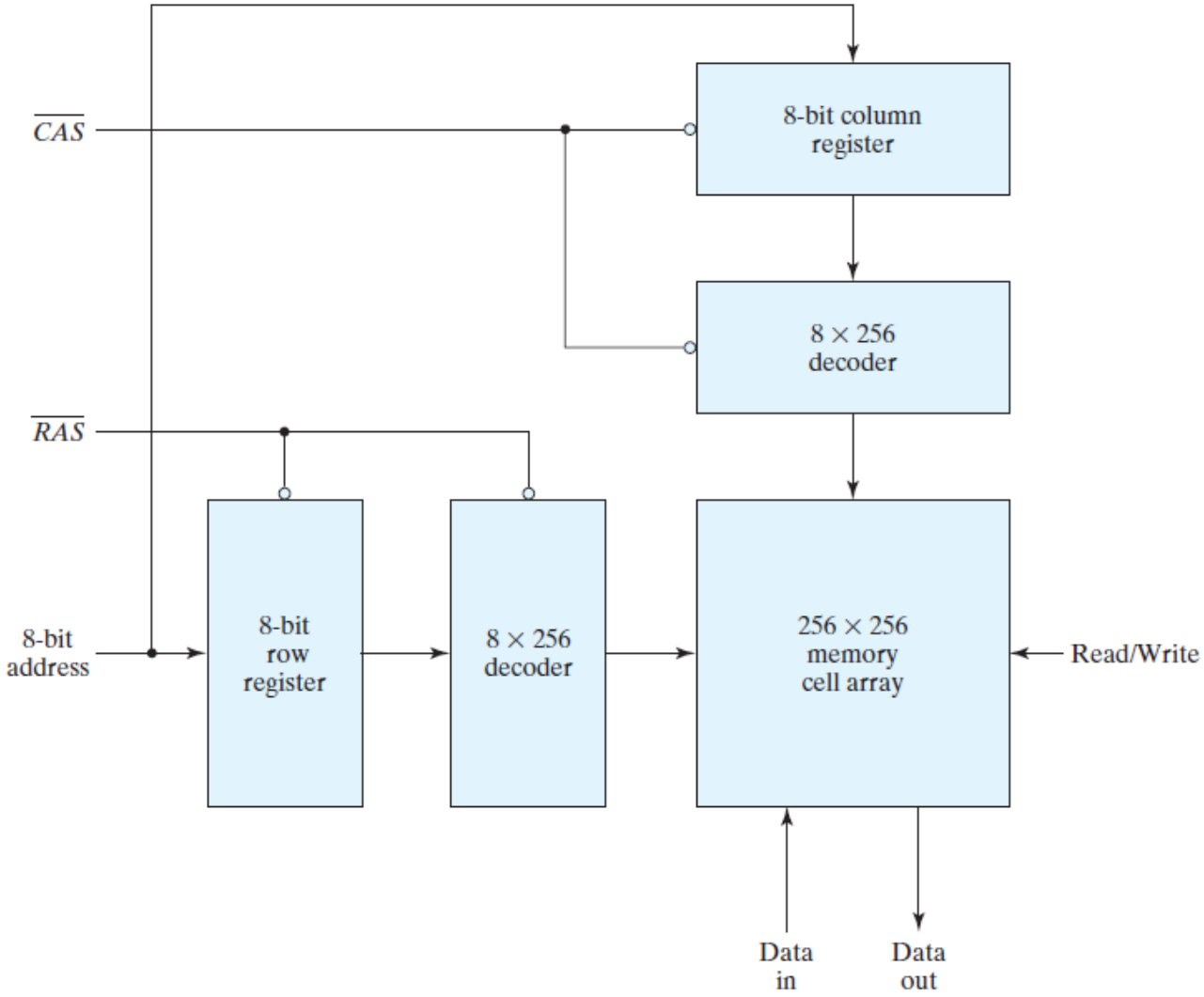


FIGURE 7.8
Address multiplexing for a 64K DRAM

Example (continued)

The 16-bit address is applied to the DRAM in two steps using RAS and CAS.

Initially, both strobes are in the 1 state.

Step 1: The 8-bit row address is applied to the address inputs and RAS is changed to 0. This loads the row address into the row address register.

RAS also enables the row decoder so that it can decode the row address and select one row of the array.

After a time equivalent to the settling time of the row selection, RAS goes back to the 1 level.

Example (continued)

Step 2: Then, 8-bit column address is applied to address inputs, and CAS is driven to 0 state.

This transfers column address into the column register and enables the column decoder.

Now the two parts of the address are in their respective registers, the decoders have decoded them to select the one cell corresponding to the row and column address, and a read or write operation can be performed on that cell.

CAS must go back to the 1 level before initiating another memory operation.

Problem – 7.9

A DRAM chip uses two-dimensional address multiplexing. It has 13 common address pins, with the row address having one bit more than the column address. What is the capacity of the memory?

Solution – 7.9

13 + 12 = 25 address lines. Memory capacity = 2^{25} words.