Decoder and Demultiplexer

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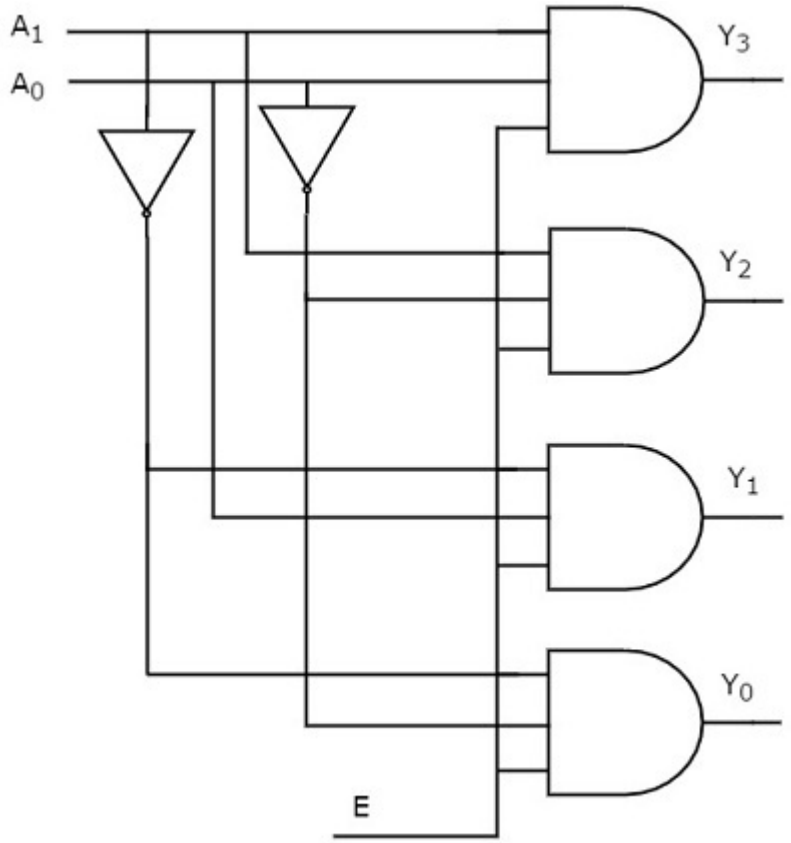
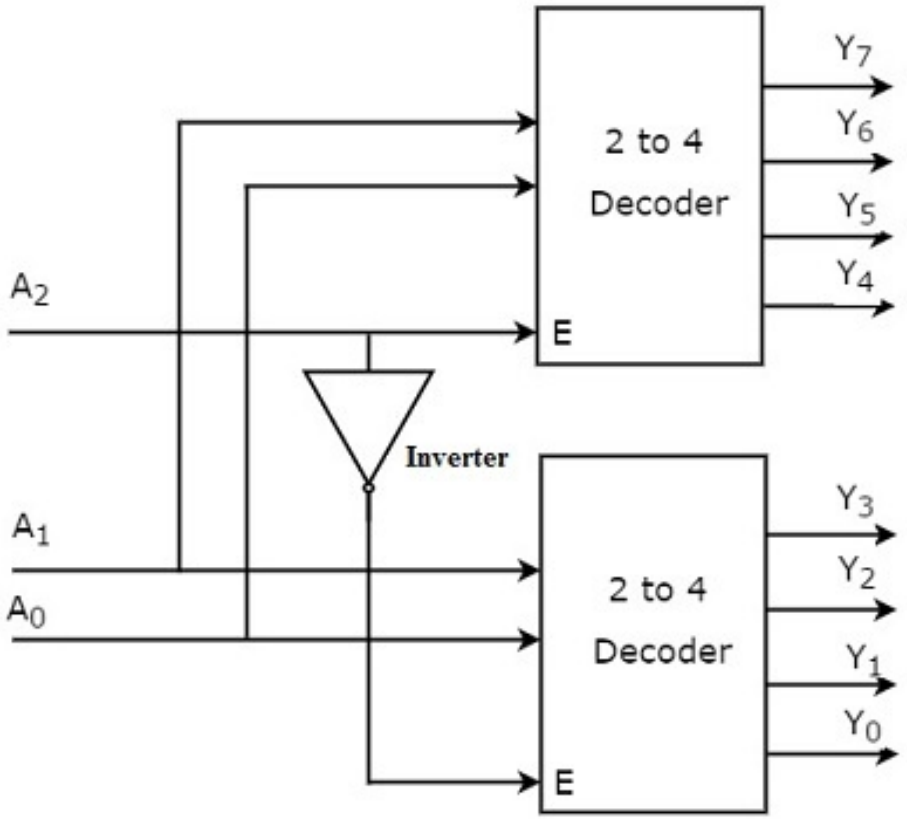
Definition

- An n-bit code can represent up to 2^n distinct elements.
- Decoder: converts binary information from n input lines to a maximum of 2^n unique output lines.
- If the n-bit coded information has unused combinations, the decoder may have fewer than 2^n outputs.
- Decoders are called n-to- m -line decoders, where m <= 2^n.
- They generate 2^n (or fewer) minterms of n input variables.
- Each combination of inputs will assert a unique output.

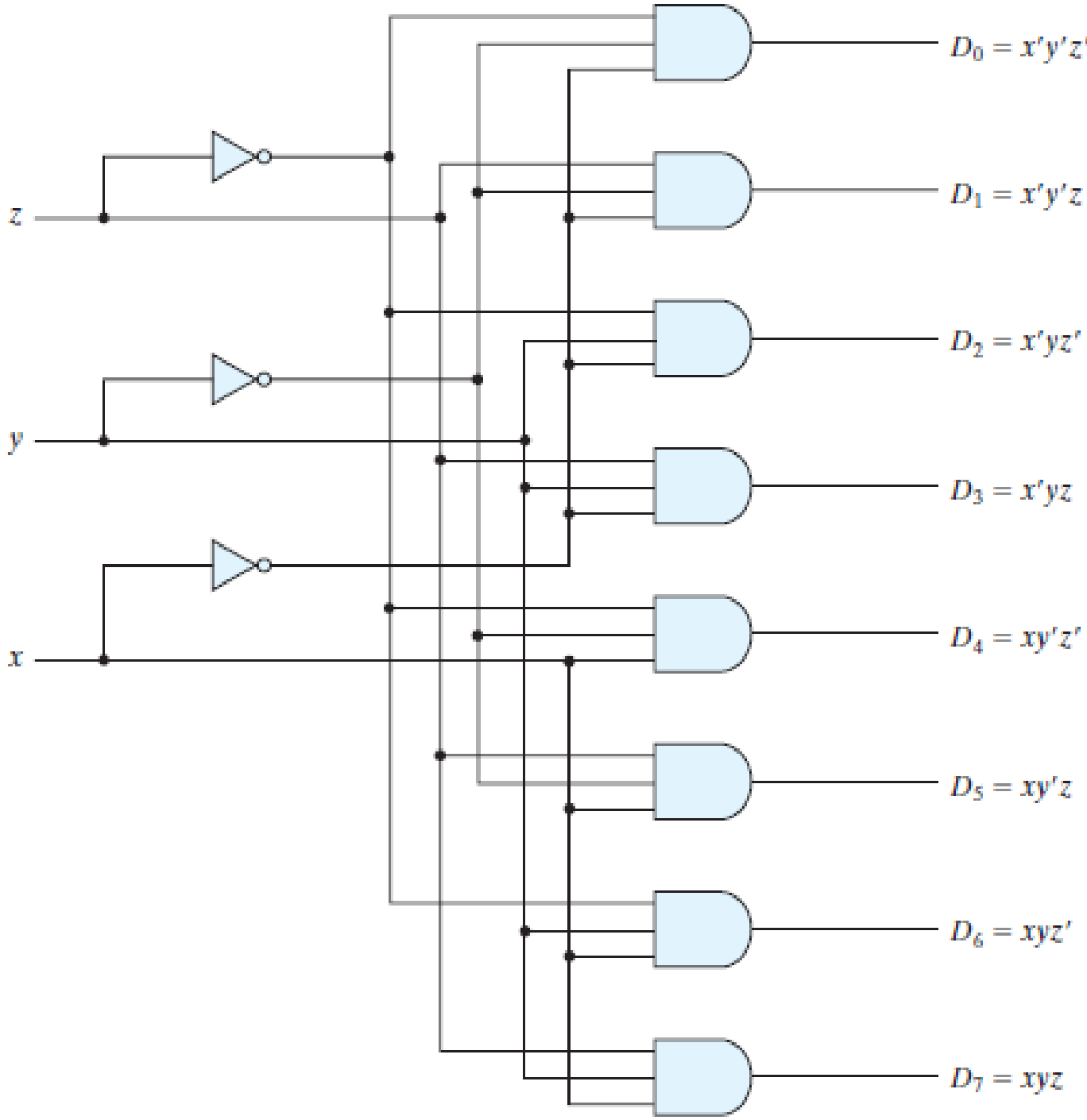
2-to-4 Decoder



3-to-8 decoder using 2-to-4 decoder



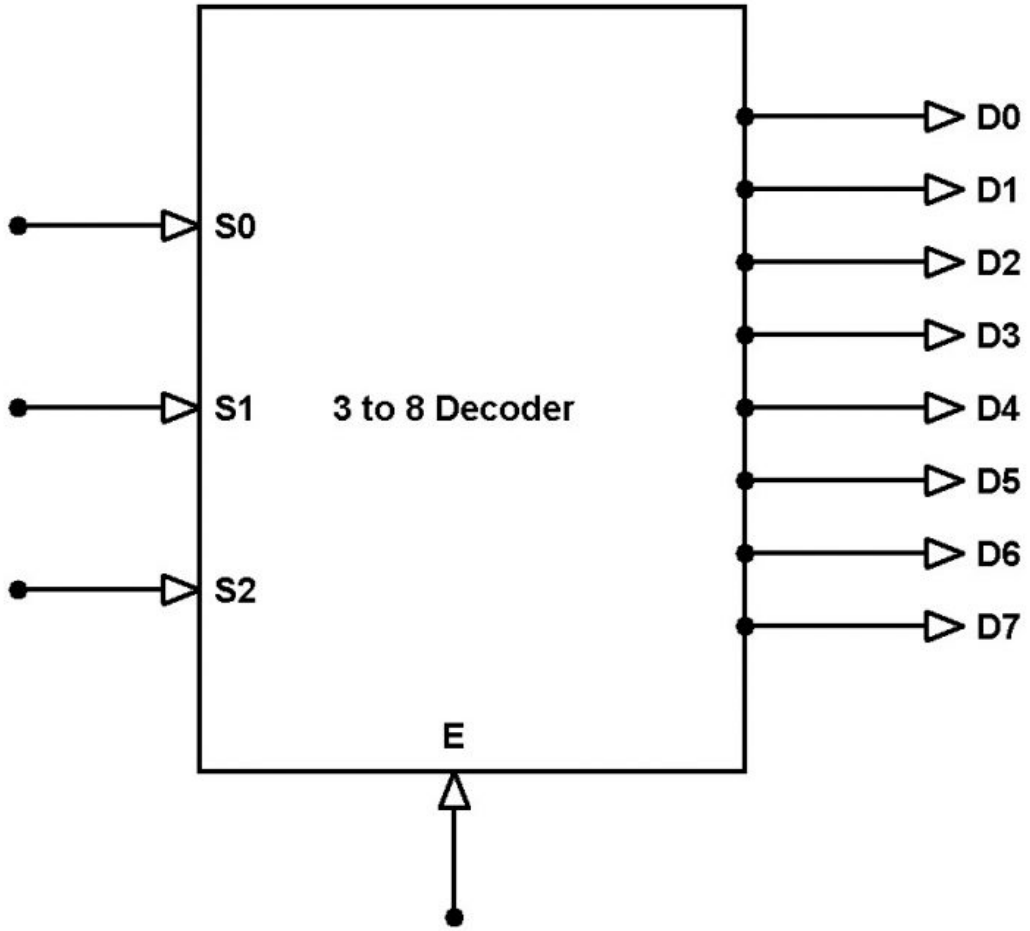
Three-to-eight-line decoder



Truth Table of a Three-to-Eight-Line Decoder

Inputs			Outputs							
x	y	z	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1

Block diagram



Three-to-eight-line decoder

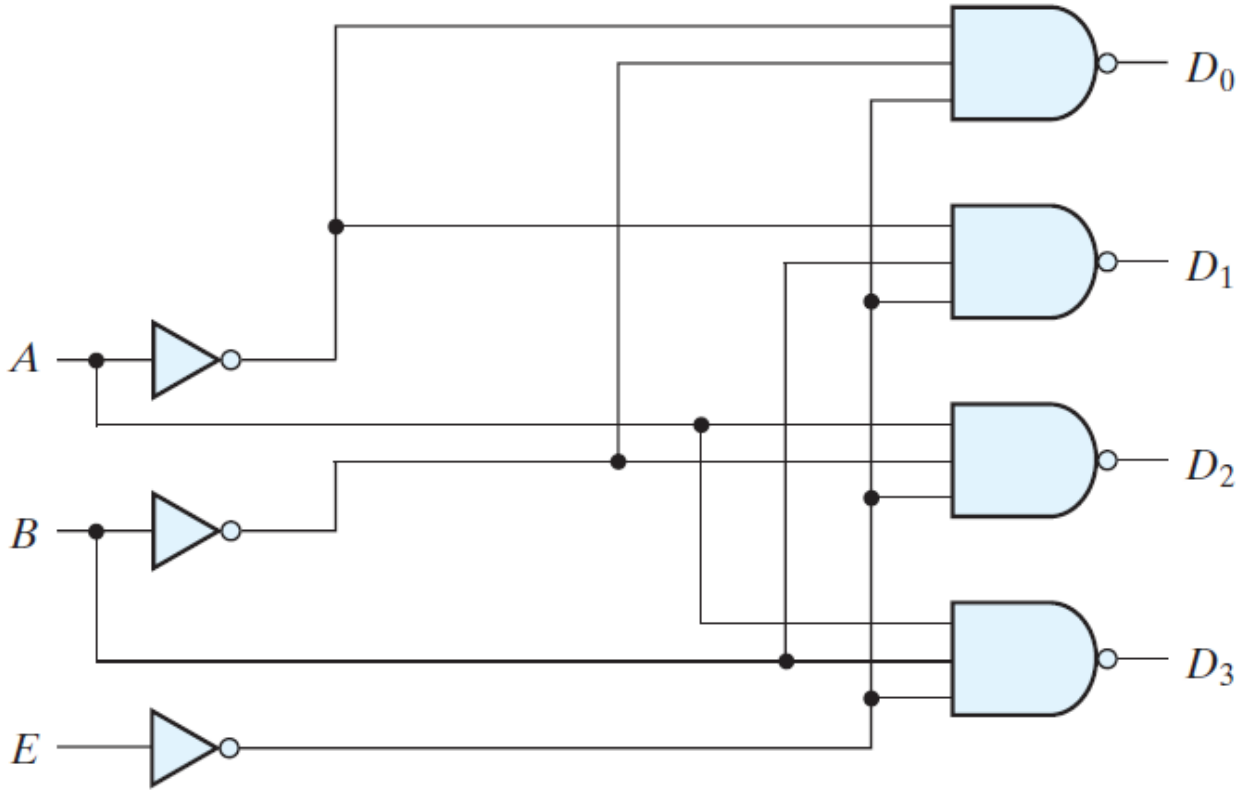
- A particular application of this decoder is binary-to-octal conversion.
- The input variables represent a binary number, and the outputs represent the eight digits of a number in the octal number system.
- A three-to-eight-line decoder can be used for decoding any three-bit code to provide eight outputs, one for each element of the code.

Example: Convert binary 1101100_2 to octal:
Convert every 3 binary bits (from bit0) to octal digit:
$1101100_2 = 1\ 101\ 100 = 1\ 5\ 4 = 154_8$

Constructing Decoder with NAND gates

- Since a NAND gate produces the AND operation with an inverted output, it becomes more economical to generate the decoder minterms in their complemented form.
- Furthermore, decoders include one or more *enable* inputs to control the circuit operation.

- This circuit operates with complemented outputs and a complement enable input.
- Only one output can be equal to 0 at any given time: corresponding to the selected minterm.
- The decoder is enabled when *E* is equal to 0 (i.e., active-low enable). The circuit is disabled when *E* is equal to 1, regardless of the values of the other two inputs.
- When the circuit is disabled, none of the outputs are equal to 0 and none of the minterms are selected.



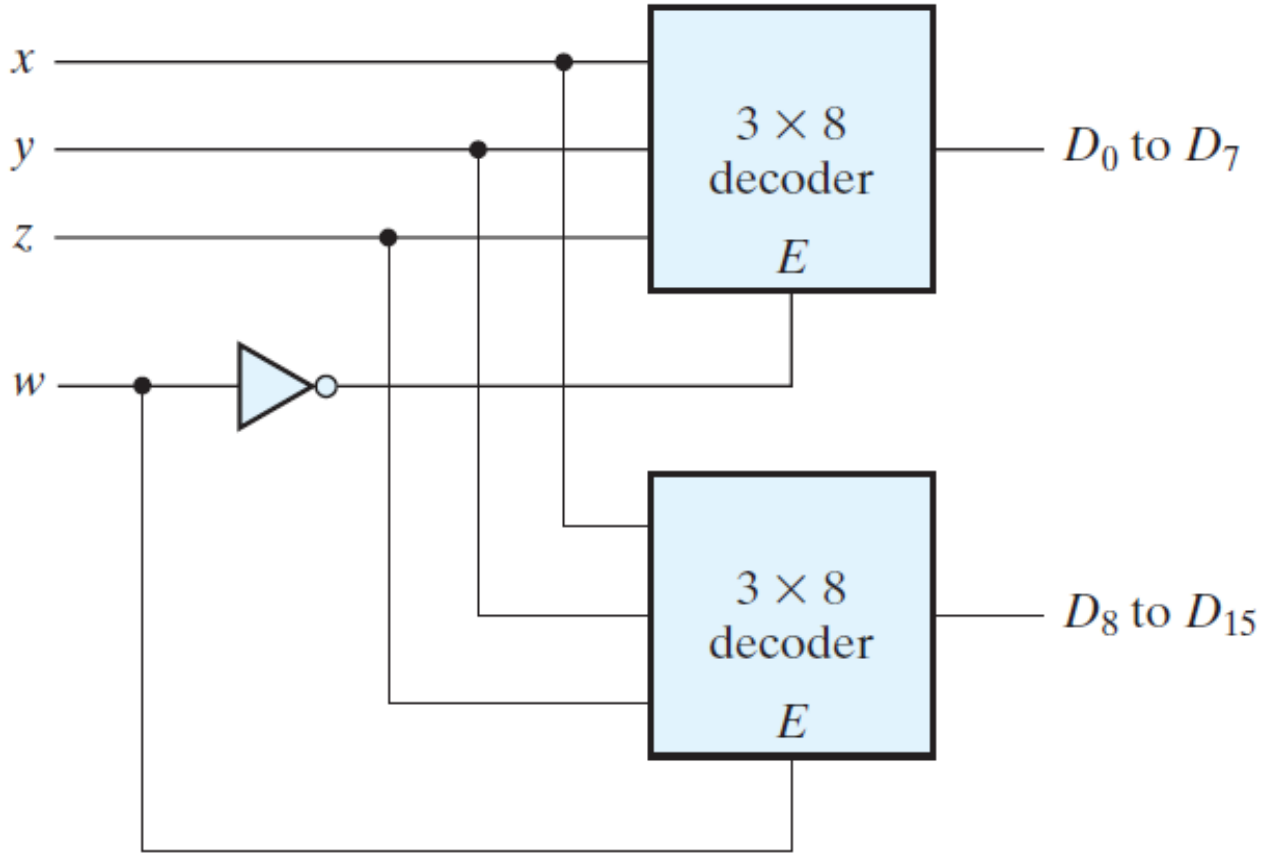
(a) Logic diagram

E	A	B	D_0	D_1	D_2	D_3
1	X	X	1	1	1	1
0	0	0	0	1	1	1
0	0	1	1	0	1	1
0	1	0	1	1	0	1
0	1	1	1	1	1	0

(b) Truth table

4 * 16 decoder constructed with two 3 * 8 decoders

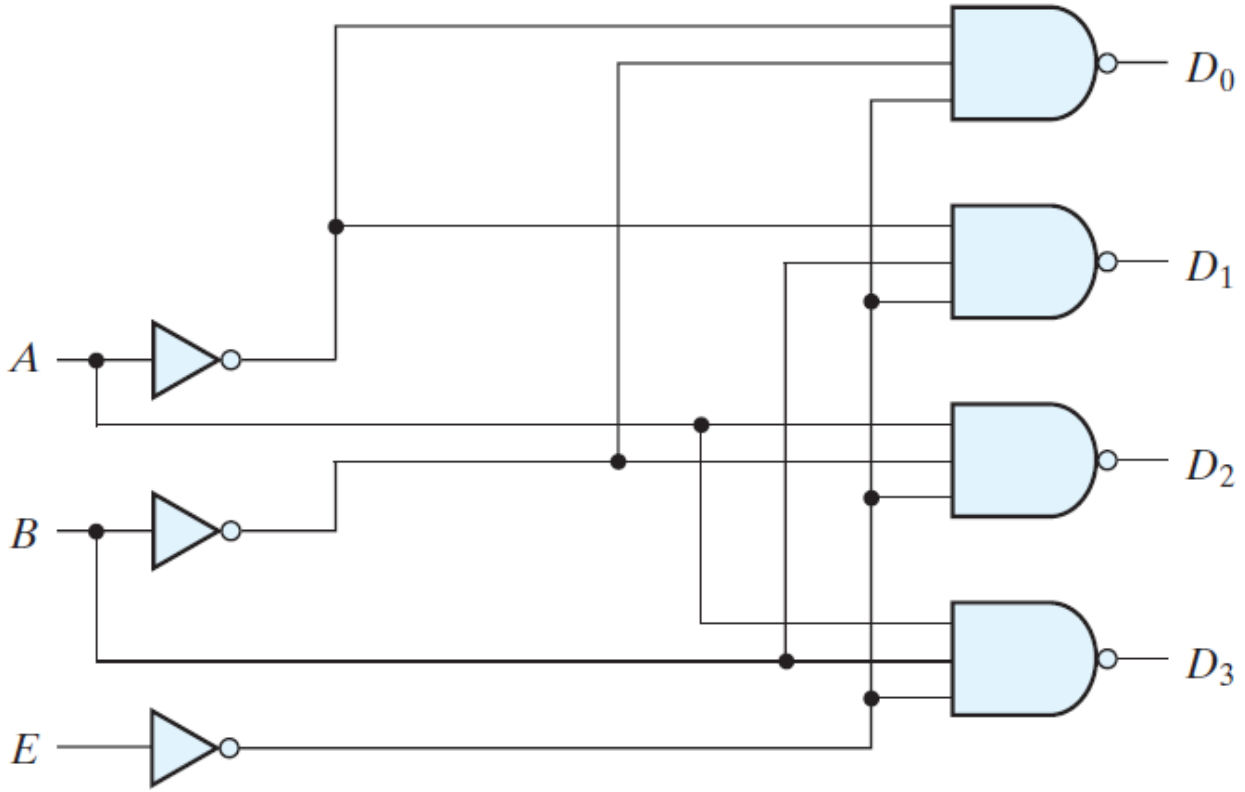
- **When *w*=0**, top decoder is enabled and the other is disabled.
- The bottom decoder outputs are all 0's, and the top eight outputs generate minterms 0000 to 0111.
- **When *w*=1**, the enable conditions are reversed.
- The bottom decoder outputs generate minterms 1000 to 1111, while the outputs of the top decoder are all 0's.



Decoder – Demultiplexer

- Demultiplexer: It receives information from a single line and directs it to one of 2^n possible output lines.
- A decoder with enable input can function as a demultiplexer.
- A specific output is selected by the bit combination of n selection lines.
- The decoder discussed earlier can function as a one-to-four-line demultiplexer when E is taken as a data input line and A and B are taken as the selection inputs.
- The single input variable E has a path to all four outputs, but the input information is directed to only one of the output lines, as specified by the binary combination of the two selection lines A and B.

Truth table for demultiplexer



(a) Logic diagram

E	A	B	D_0	D_1	D_2	D_3
1	X	X	1	1	1	1
0	0	0	0	1	1	1
0	0	1	1	0	1	1
0	1	0	1	1	0	1
0	1	1	1	1	1	0

(b) Truth table

Using decoder to implement a combinational logic circuit

Using decoder to implement a function

- A decoder provides the 2^n minterms of n input variables. Each asserted output of the decoder is associated with a unique pattern of input bits.
- Any Boolean function can be expressed in sum-of-minterms form
- ➔ A decoder that generates the minterms of the function, together with an external OR gate that forms their logical sum, provides a hardware implementation of the function.
- ➔ Any combinational circuit with n inputs and m outputs can be implemented with an n -to-2^n -line decoder and m OR gates.

Example: Full adder

$$S = x'y'z + x'yz' + xy'z' + xyz$$
$$C = xy + xz + yz$$

$$S(x, y, z) = \Sigma(1, 2, 4, 7)$$
$$C(x, y, z) = \Sigma(3, 5, 6, 7)$$

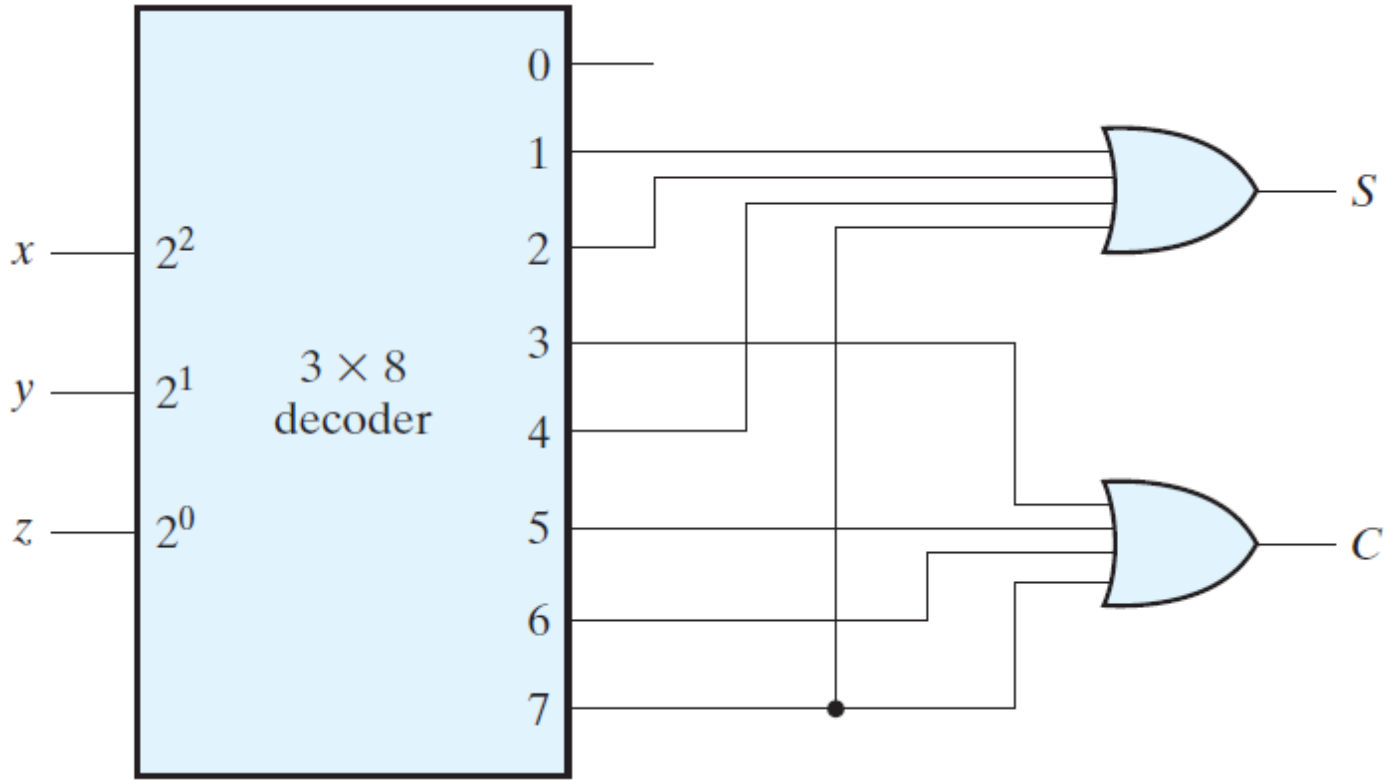
- Since there are three inputs and a total of eight minterms, we need a three-to-eight-line decoder.

Full Adder

x	y	z	C	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

Full adder

- The decoder generates the eight minterms for x , y , and z .
- The OR gate for output S forms the logical sum of minterms 1, 2, 4, and 7.
- The OR gate for output C forms the logical sum of minterms 3, 5, 6, and 7.



Function with long list of minterms

- A function with a long list of minterms requires an OR gate with a large number of inputs.
- A function having a list of k minterms can be expressed in its complemented form F' with 2^n - k minterms.
- In such a case, it is advantageous to use a NOR gate to sum the minterms of F.
- The output of the NOR gate complements this sum and generates the normal output F.

Solved Example

- A combinational circuit is defined by F = ∑ 0, 2, 5, 6, 7. Implement the Boolean function F with a suitable decoder and an external OR/NOR gate having the minimum number of inputs.
- Implementing F will require an OR gate with 5 inputs. Hence, we can implement F' = ∑ 1,3,4. It requires a NOR gate with 3 inputs only.