Logic Family Parameters

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NAND and NOR gates

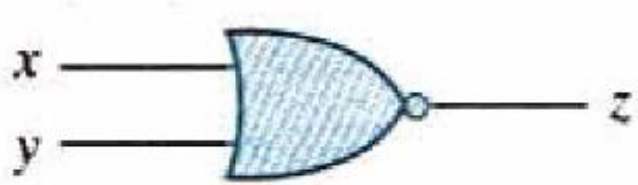
- The basic circuit in each IC digital logic family is a NAND or NOR gate.
- We must investigate their input-output relationships in terms of two voltage levels: a high level, designated by H,and a low level, designated by L.
- **NAND summary:**
- If any input of a NAND gate is low, the output is high.
- If all inputs of a NAND gate are high, the output is low.

Inputs		Output
x	y	z
L	L	H
L	H	H
H	L	H
H	H	L

NAND and NOR gates

- **NOR summary:**
- If any input of a NOR gate is high, the output is low.
- If all inputs of a NOR gate are low, the output is high.

Inputs		Output
x	*y*	*z*
L	*L*	*H*
L	*H*	*L*
H	*L*	*L*
H	*H*	*L*



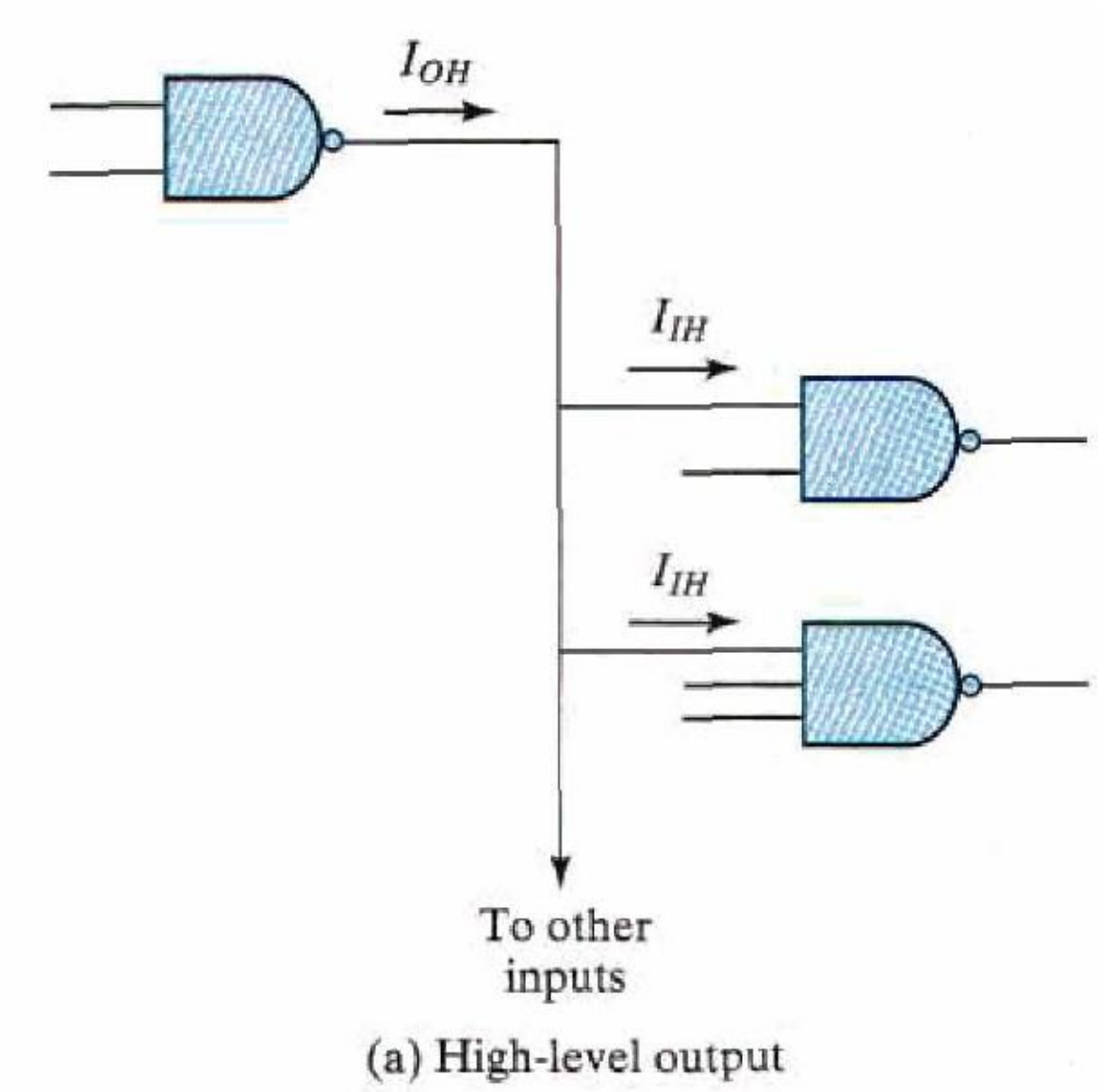
Fan out

- Fanout of a gate (also called loading): number of standard loads that can be connected to gate output without degrading its normal operation.
- A standard load is usually defined as the amount of current needed by an input of another gate in the same logic family.

- The output of a gate is usually connected to the inputs of other gates.
- Each input requires a certain amount of current from the gate output, so that each additional connection adds to the load of the gate.
- The output of a gate can supply a limited amount of current, above which it ceases to operate properly and is said to be overloaded.

Computing fan-out

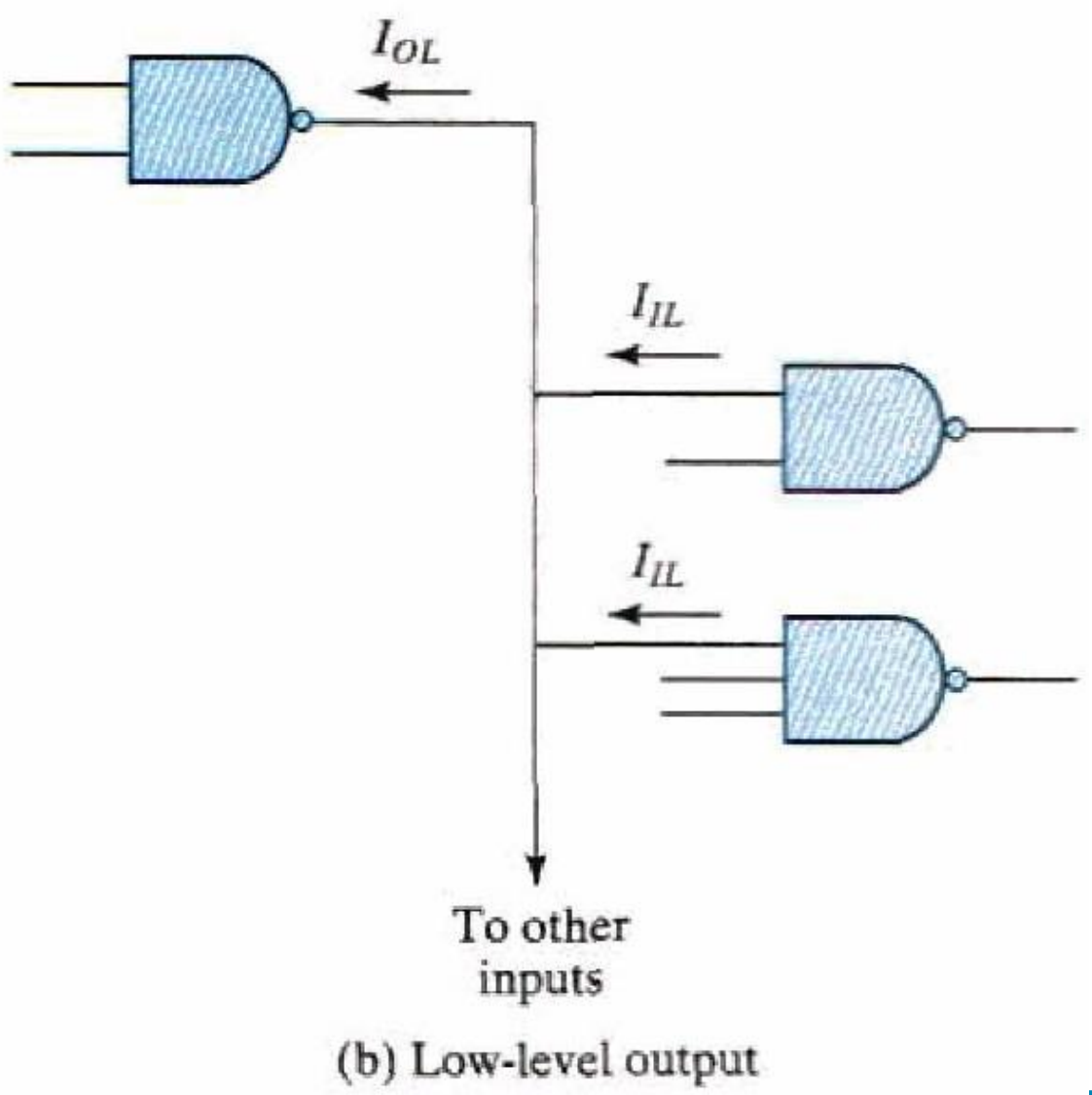
- The fan-out is calculated from the amount of current available in the output of a gat and the amount of current needed in each input of a gate.
- **Right-side figure:** Gate output is in the high-voltage level.
- It provides I_{OH} current output.
- The connected input gates require I_{IH} for proper operation.



(a) High-level output

Computing fan-out

- **Right-side figure:** The gate output is in the low-voltage level.
- It provides a current sink I_{OL} for all the gate inputs connected to it.
- Each gate input supplies a current I_{IL}.



(b) Low-level output

Computing fanout

- Fanout is lower out of the I_{OH}/I_{IH} and I_{OL}/I_{IL}
- For TTL

$$I_{OH} = 400\ \mu A$$
$$I_{IH} = 40\ \mu A$$
$$I_{OL} = 16\ mA$$
$$I_{IL} = 1.6\ mA$$

- ➔ Ratio = 10.
- The fan-out of standard TTL is 10.
- ➔ TTL gate output gate can be connected to no more than 10 inputs of other gates in the same logic family.

Power

- Digital systems draw both *dynamic* and *static* power.
- Dynamic power is the power used to charge capacitance as signals change between 0 and 1.
- Static power is the power used even when signals do not change and the system is idle.

Static Power dissipation

- Amount of power required for gate operation
- It shows the power delivered to the gate from the power supply.
- Use four gates ==> four times the power dissipation
- Static Power = Vcc X Icc
- Vcc = supply voltage
- Icc = current drawn by the circuit

Static Power dissipation

- The current drawn depends on the logic state.
- IccH = current drawn when output is in high-voltage level.
- IccL = current drawn when output is in low-voltage level.
- Icc(avg) = (IccH+IccL)/2
- Power = Vcc X Icc(avg)
- For TTL, Vcc =5V, IccH = 1mA, IccL = 3mA
- Power = 10mW

Dynamic Power

- Logic gates and the wires that connect them have capacitance.
- The energy drawn from the power supply to charge a capacitance C to voltage V_{DD} is CV_{DD}^2.
- If the voltage on the capacitor switches at frequency f (i.e., f times per second), it charges the capacitor $f/2$ times and discharges it $f/2$ times per second.
- Discharging does not draw energy from the power supply, so the dynamic power consumption is

$$P_{\text{dynamic}} = \frac{1}{2} C V_{DD}^2 f$$

Example

- A particular cell phone has a 6 watt-hour (W-hr) battery and operates at 1.2 V.
- **When it is in use**, the cell phone operates at 300 MHz and the average amount of capacitance in the chip switching at any given time is 10 nF. When in use, it also broadcasts 3 W of power out of its antenna.
- **When the phone is not in use**, the dynamic power drops to almost zero because the signal processing is turned off. But the phone also draws 40 mA of quiescent current whether it is in use or not.
- Determine the battery life of the phone
  (a) if it is not being used, and
  (b) if it is being used continuously.

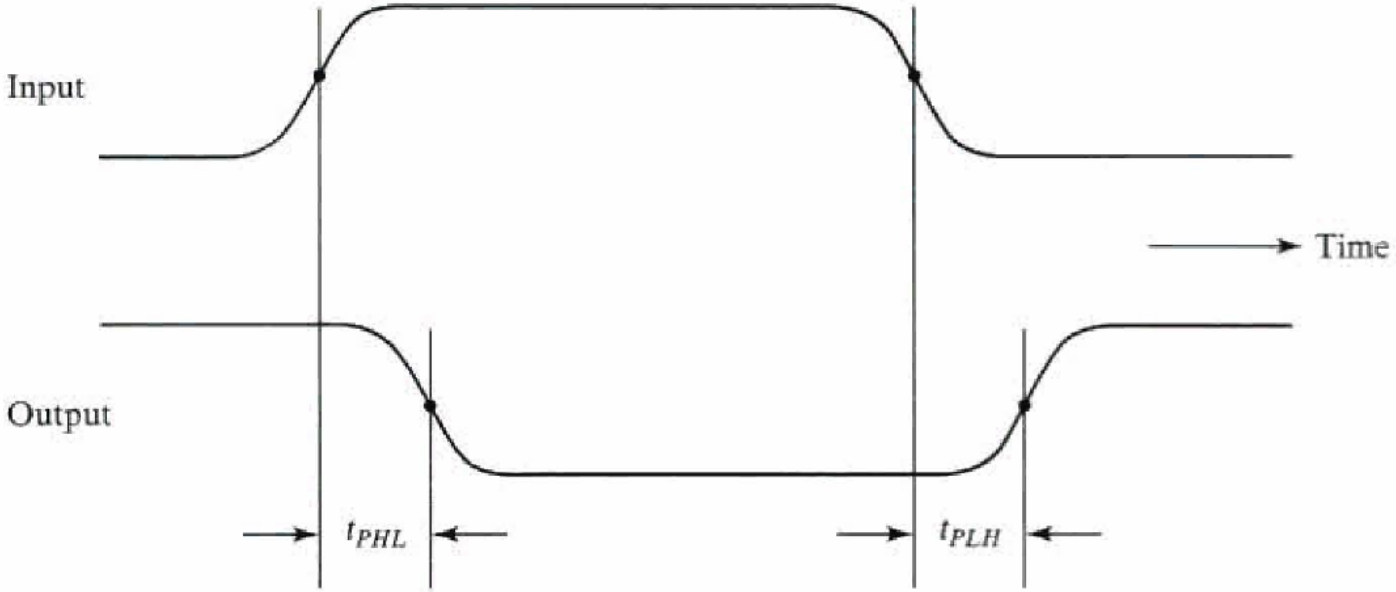
Solution

- The static power is Pstatic = (0.040 A)(1.2 V) = 48 mW.
- **When not used**, this is the only power consumption, so the battery life is (6 Whr)/(0.048 W) = 125 hours.
- **If the phone is being used**,
- Pdynamic = $(0.5)(10^{-8}\ \text{F})(1.2\ \text{V})^2(3*10^8\ \text{Hz})$ = 2.16 W.
- Together with the static and broadcast power, the total active power is 2.16 W+0.048 W +3W = 5.2W,
- So the battery life is 6 W-hr/5.2 W = 1.15 hours.

Propagation Delay

- The propagation delay of a gate is the average transition-delay time for the signal to propagate from input to output when the binary input signal changes in value.
- The total delay of the circuit is the sum of the propagation delays through the gates.
- More the number of levels, more the delay
- The average propagation delay is calculated from the input and output waveforms of the gate.

- Signal-delay between the input and the output when the output changes from
  - high to low level = t_{PHL}.
  - low to high level = t_{PLH}



- It is customary to measure the time between the 50 percent point on the input and output transitions.
- In general, the two delays are not the same, and both vary with loading conditions.
- The average propagation delay is the average of the two delays.

- For TTL
- t_{PHL} = 7ns
- t_{PLH} = 11ns
- ➔ Average delay is 9 ns

- Sometimes, maximum delay is more important than average delay.
- For standard NAND gates in TTL, t_{PHL} = 15ns and t_{PLH} = 22ns.

Noise

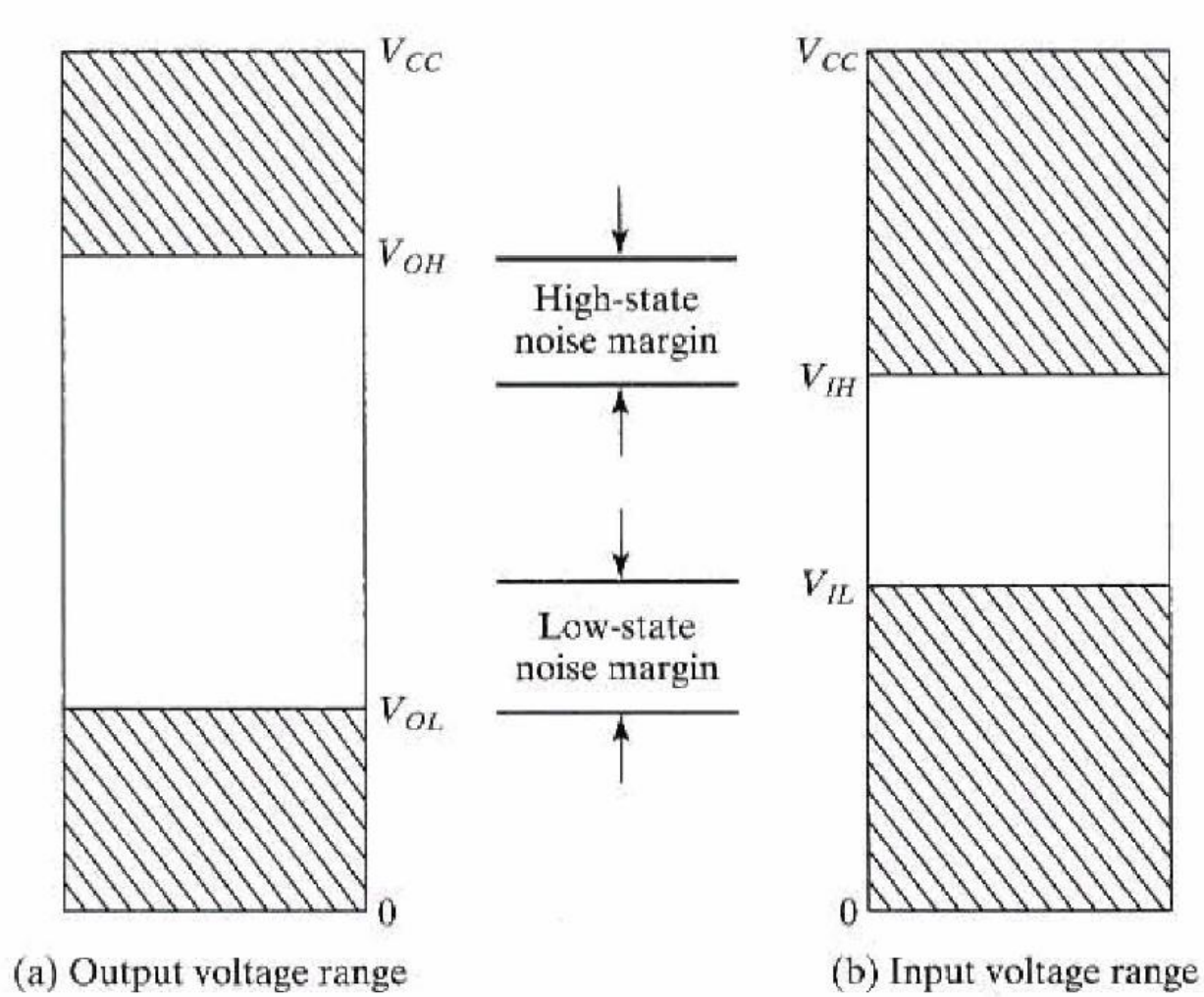
- Noise is undesired signal
- DC noise is caused by a drift in the voltage levels of a signal.
- AC noise is a random pulse that may be created by other switching signals.

Noise margin

- Noise margin: maximum noise voltage added to an input signal of a digital circuit that does not cause an undesirable change in the circuit's output.
- Noise margin is the amount of noise that a circuit could withstand without compromising the operation of circuit.
- Noise margin makes sure that any signal which is logic ‘1’ with finite noise added to it, is still recognized as logic ‘1’ and not logic ‘0’.
- The noise margin is calculated from knowledge of the voltage signal available in the output of the gate and the voltage signal required in the input of the gate.

Signals used in computing noise margin

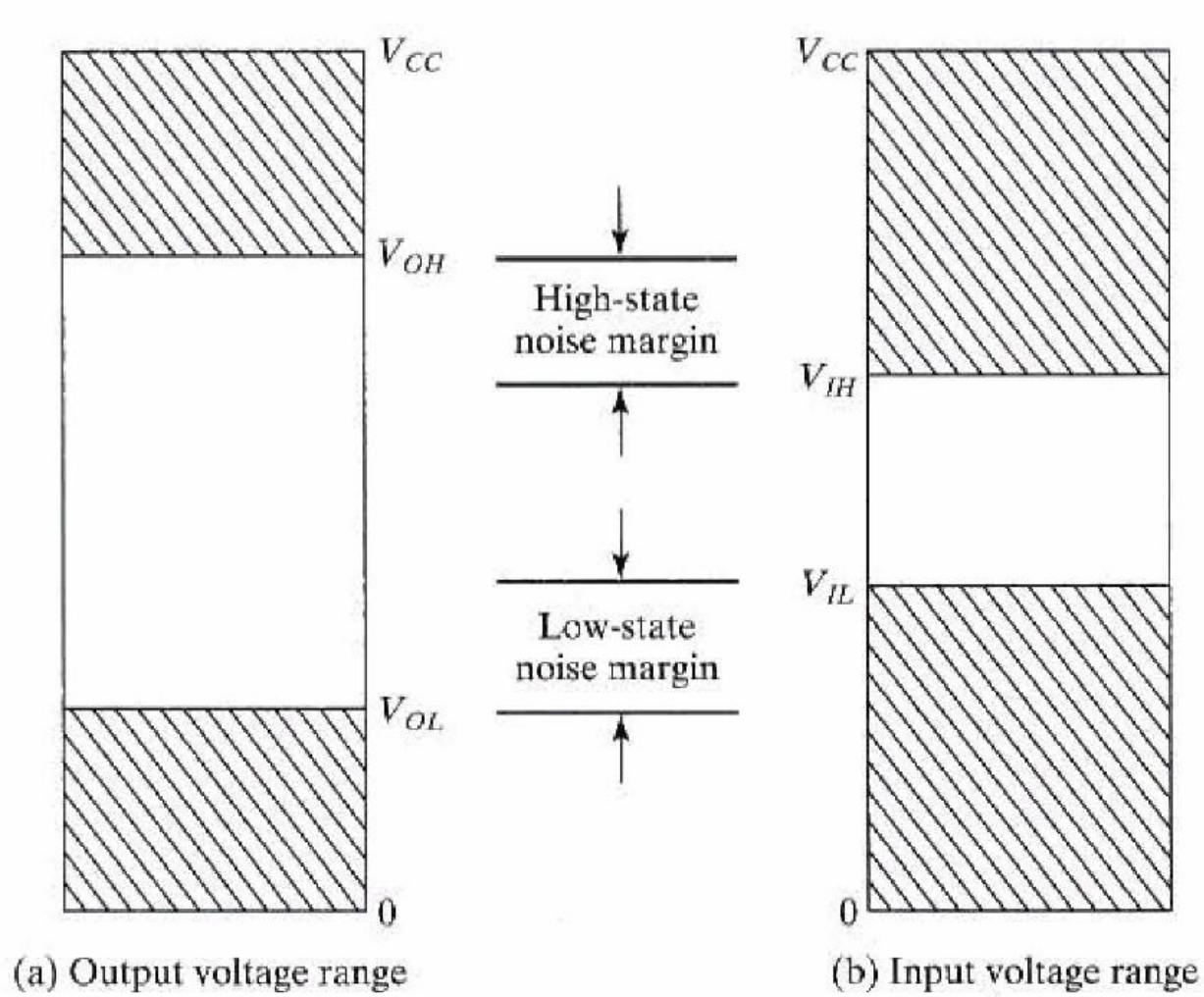
- Any voltage in the gate output between V_{CC} and V_{OH} is considered to be the high-level state.
- Any voltage between 0 and V_{OL} in the gate output is considered to be the low-level state.
- Voltages between V_{OL} and V_{OH} are indeterminate and do not occur under normal operating conditions, except during transition between two levels.



(a) Output voltage range

(b) Input voltage range

- The corresponding two voltage ranges that are recognized by the gate input are shown in figure (b).
- To compensate for any noise signal, the circuit must be designed so that V_{IL} is greater than V_{OL} and V_{IH} is less than V_{OH}.
- The **noise margin** is the difference V_{OH} - V_{IH}, or V_{IL} - V_{OL}, whichever is smaller.



Understanding noise margin

- V_{OL} is the maximum voltage that the output can be in the low-level state.
- The circuit can tolerate any noise signal that is less than the noise margin (V_{IL} - V_{OL}) because the input will recognize the signal as being in the low-level state.
- Any signal greater than V_{OL} plus the noise-margin will send the input voltage into the indeterminate range, which may cause an error in the output of the gate.
- Similarly, a negative-voltage noise greater than V_{OH} - V_{IH} will send the input voltage into the indeterminate range.

Noise margin values for TTL NAND gate

The parameters for the noise margin in a standard TTL NAND gate are $V_{OH} = 2.4$ V, $V_{OL} = 0.4$ V, $V_{IH} = 2$ V, and $V_{IL} = 0.8$ V. The high-state noise margin is $2.4 - 2 = 0.4$ V, and the low-state noise margin is $0.8 - 0.4 = 0.4$ V. In this case, both values are the same.