Flip-flop

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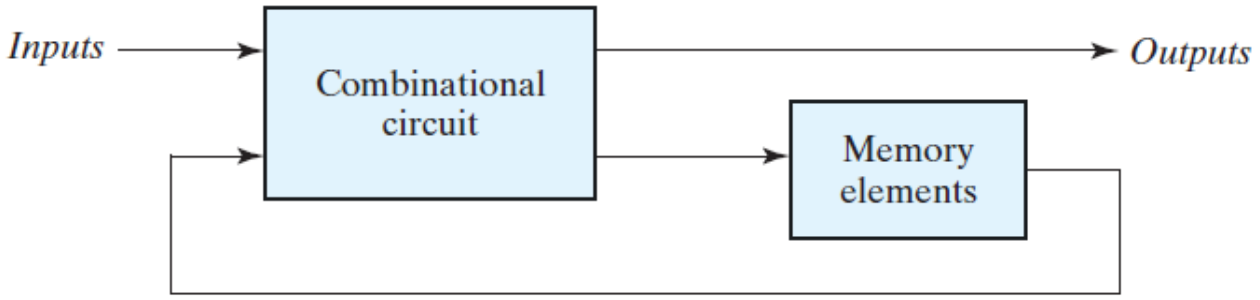
Challenge with latch

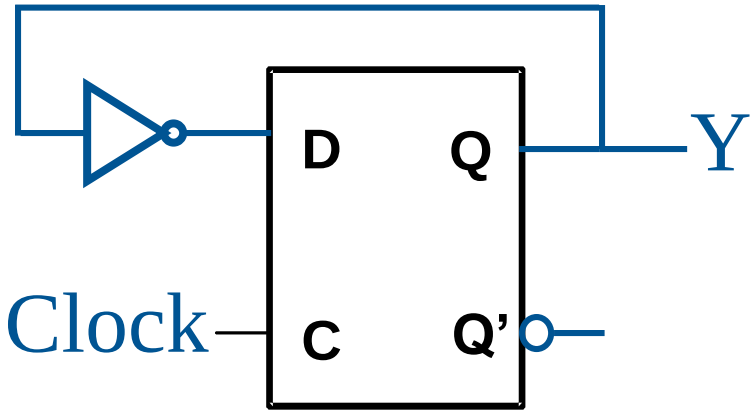
A sequential circuit has a feedback path from the outputs of the flip-flops to the input of the combinational circuit.

Consequently, the inputs of the flip-flops are derived in part from the outputs of the same and other flip-flops.

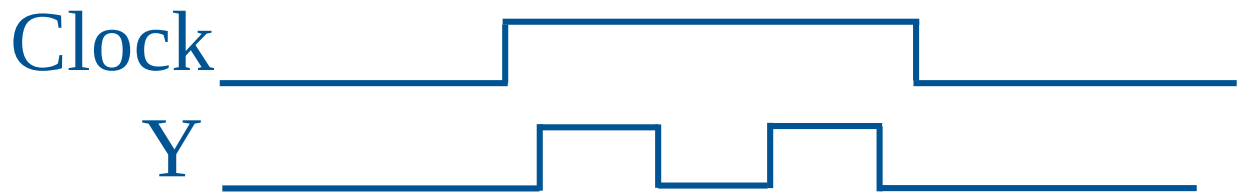


The Latch Timing Problem

- Consider the following circuit:



- Suppose that initially Y = 0.



- As long as C = 1, the value of Y continues to change!
- The changes are based on the delay present on the loop through the connection from Y back to Y.
- This behavior is clearly unacceptable.
- Desired behavior: Y changes only once per clock pulse

Challenge with latch

The state transitions of the latches start as soon as the clock pulse changes to the logic-1 level.

The new state of a latch appears at the output while the pulse is still active.

This output is connected to the inputs of the latches through the combinational circuit.

If the inputs applied to the latches change while the clock pulse is still at the logic-1 level, the latches will respond to new values and a new output state may occur.

Challenge with latch

The result is an unpredictable situation, since the state of the latches may keep changing for as long as the clock pulse stays at the active level.

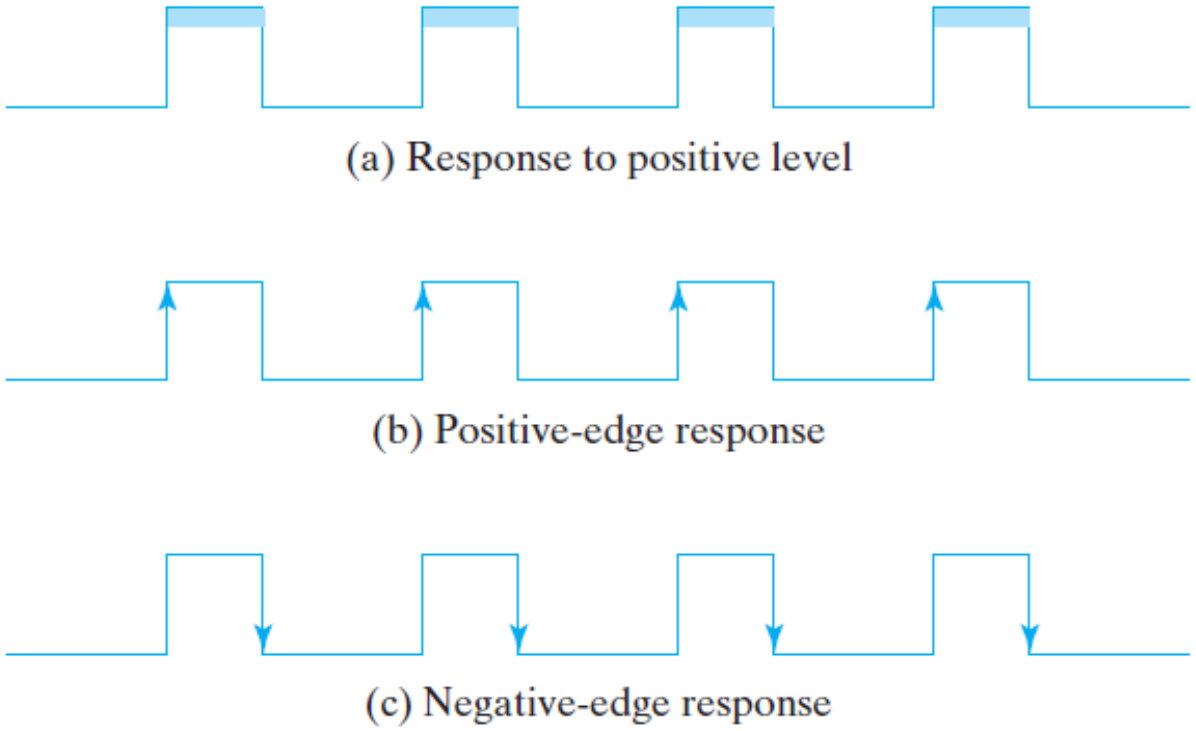
Because of this unreliable operation, the output of a latch cannot be applied directly or through combinational logic to the input of the same or another latch when all the latches are triggered by a common clock source.

Flip-flop to solve Latch issues

The problem with the latch: it responds to a change in the level of a clock pulse.

Solution: Flip-flop is triggered only during a signal transition.

For this, eliminate the feedback path that is inherent in the operation of the sequential circuit using latches.



Flip-flop

The storage elements (memory) used in clocked sequential circuits are called *flip-flops*.

A flip-flop stores one bit of information.

In a stable state, the output of a flip-flop is either 0 or 1.

The new value is stored (i.e., the flip-flop is updated) when a pulse of the clock signal occurs.

When a clock pulse is not active, the feedback loop between the value stored in the flip-flop and the value formed at the input to the flip-flop is effectively broken.

This is because the flip-flop outputs cannot change even if the outputs of the combinational circuit driving their inputs change in value.

Flip-flop vs latch

Flip-flop

- Operate with signal-transition
- Edge-sensitive devices

Latch

- Operate with signal levels
- Called level-sensitive device

Two ways to modify a latch to form a flip-flop

1. Employ two latches in a special configuration that isolates the output of the flip-flop and prevents it from being affected while the input to the flip-flop is changing.

2. Produce a flip-flop that triggers only during a signal transition (from 0 to 1 or from 1 to 0) of the synchronizing signal (clock) and is disabled during the rest of the clock pulse.

Master-slave D flip-flop: An Edge-Triggered Flip-Flop

The circuit samples the D input and changes its output Q only at the negative edge of the clock.

Clock=0 ==> The slave latch is enabled, and its output Q is equal to the master output Y. The master latch is disabled.

When clock changes to 1, the data D is transferred to the master. The slave is disabled as long as clock=1.

As long as clock remains 1, any change in the input changes the master output at Y, but cannot affect the slave output.

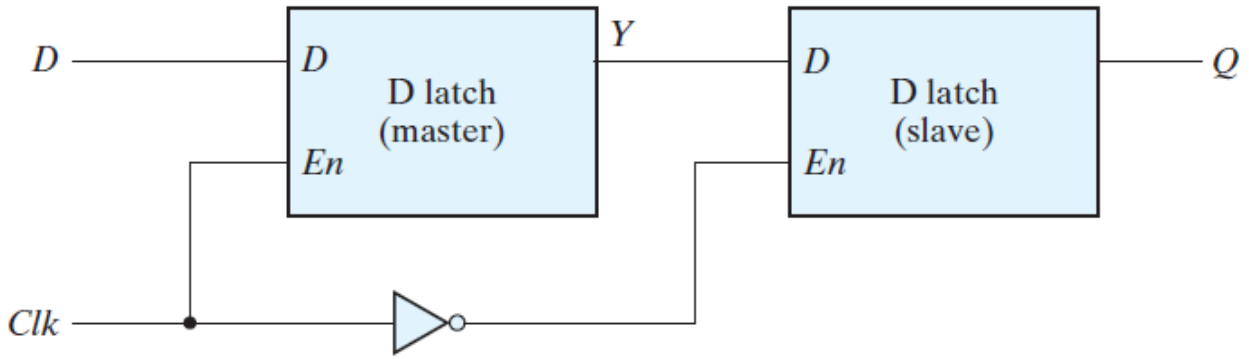


FIGURE 5.9
Master–slave *D* flip-flop

Master-slave D flip-flop (continued)

Clock changes to 0, the master is disabled and is isolated from the D input.

But slave is enabled and the value of Y is transferred to the output of the flip-flop at Q.

Thus, a change in the output of the flip-flop can be triggered only by and during the transition of the clock from 1 to 0.

The value that is produced at the output of the flip-flop is the value that was *stored in the master stage immediately before the negative edge occurred* .

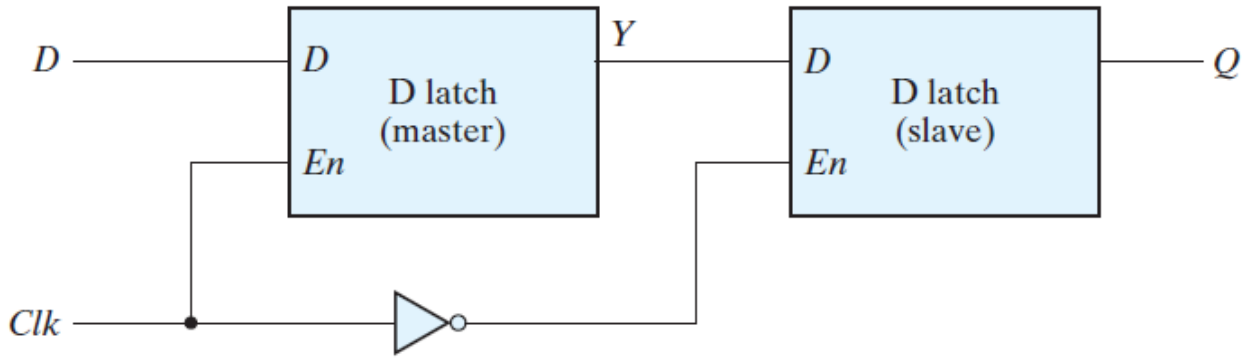
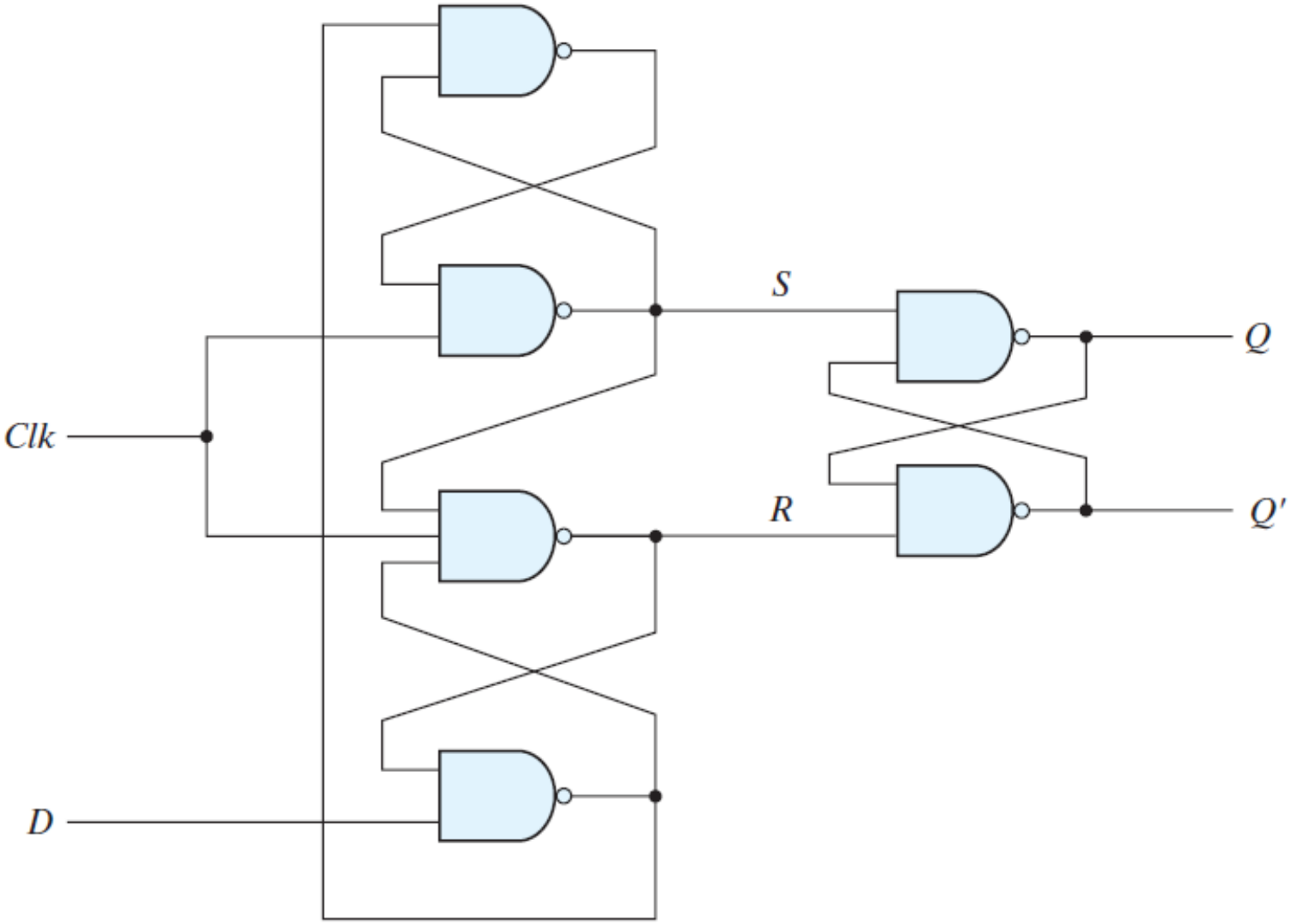


FIGURE 5.9
Master–slave *D* flip-flop

Designing Edge-Triggered Flip-Flop using 3 SR Latches



Two latches respond to the external D (data) and Clk (clock) inputs.

The third latch provides the outputs for the flip-flop.

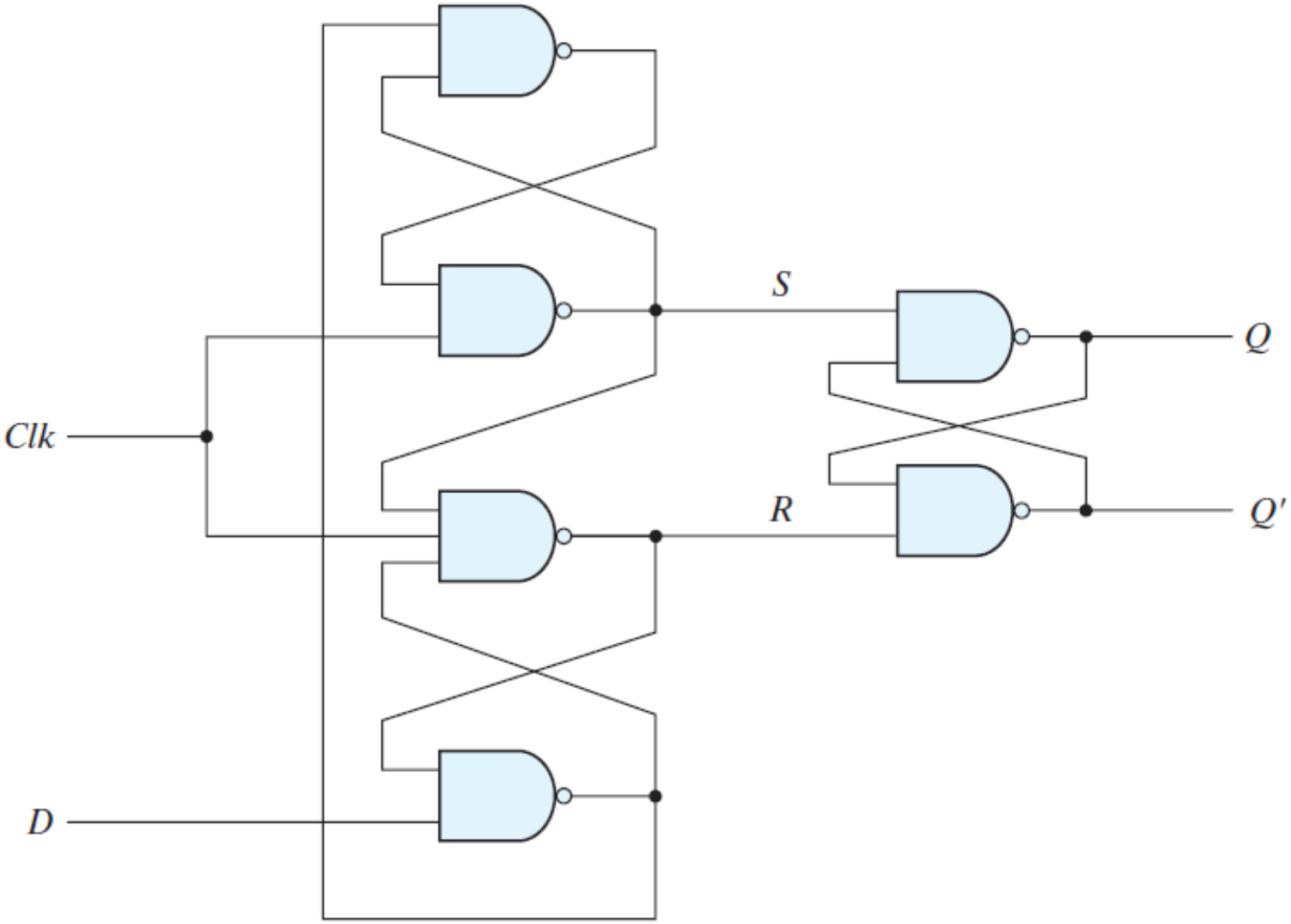
The S and R inputs of the output latch are maintained at the logic-1 level when Clk = 0.

This causes the output to remain in its present state.

Function table of NAND-based Latch

S	R	Q	Q'	
1	0	0	1	
1	1	0	1	(after $S = 1, R = 0$)
0	1	1	0	
1	1	1	0	(after $S = 0, R = 1$)
0	0	1	1	(forbidden)

Designing Edge-Triggered Flip-Flop using 3 SR Latches



When Clk becomes 1
If D = 0, R changes to 0. 3rd flip-flop goes to reset state, making Q = 0.
If there is a change in the D input while Clk = 1, terminal R remains at 0 because Q is 0.
Thus, the flip-flop is locked out and is unresponsive to further changes in the input.

When Clk becomes 1,
If D = 1, S changes to 0.
This causes the circuit to go to the set state, making Q = 1.

Any change in D while Clk = 1 does not affect the output.

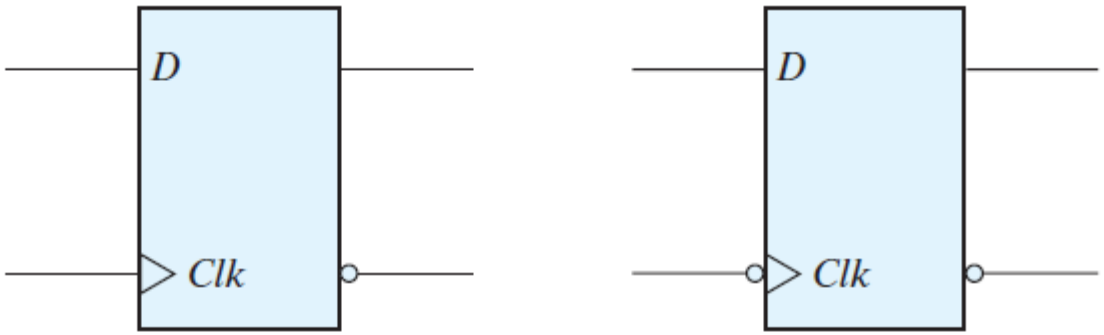


FIGURE 5.11
Graphic symbol for edge-triggered *D* flip-flop

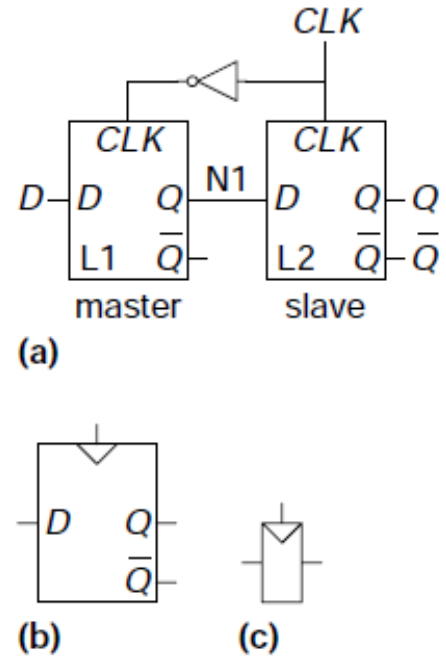
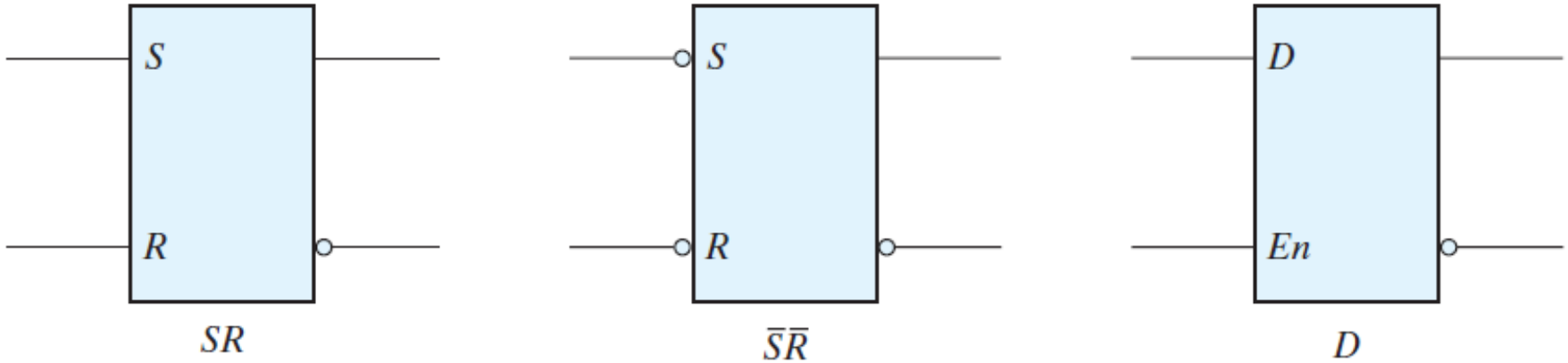


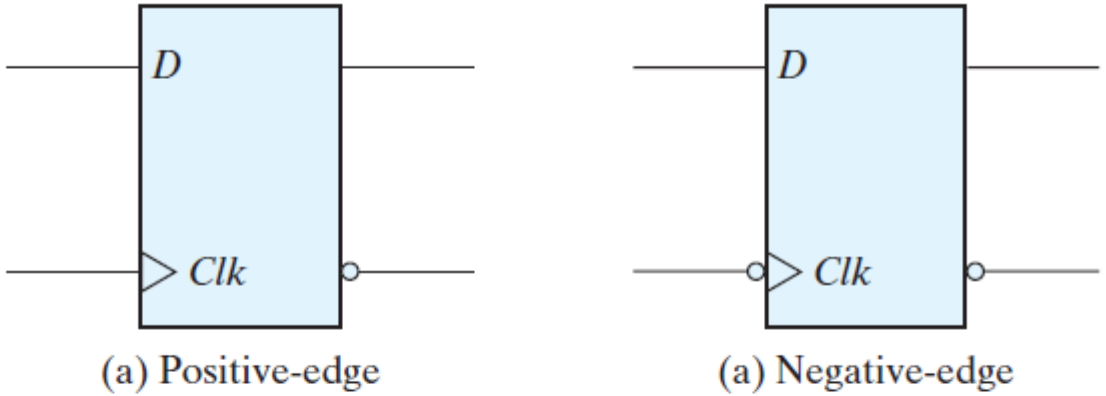
Figure 3.8 D flip-flop: (a) schematic, (b) symbol, (c) condensed symbol

Comparison of latch vs FF symbol

Latch



FF



The *dynamic indicator* (>) denotes the fact that the flip-flop responds to the edge transition of the clock.