Tri State Buffer

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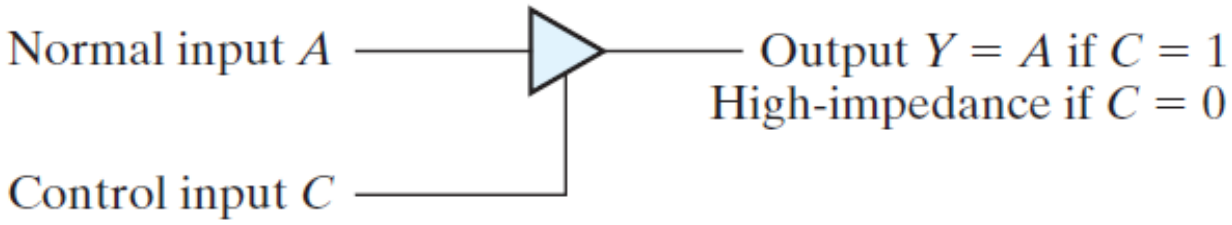
Three-State Gates

- It has 3 states: Two of the states are signals equivalent to logic 1 and logic 0.
- The third state is a *high-impedance* state in which
- ✓ the logic behaves like an open circuit, which means that the output appears to be disconnected
- ✓ the circuit has no logic significance,
- ✓ the circuit connected to the output of the three-state gate is not affected by the inputs to the gate.
- Three-state gates may perform any conventional logic, such as AND or NAND.
- However, the one most commonly used is the buffer gate.

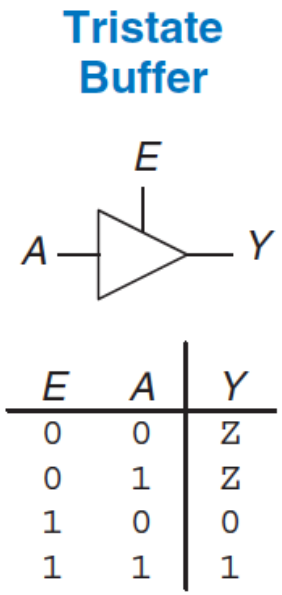
Three-State Gates as a buffer



It is distinguished from a normal buffer by an input control line entering the bottom of the symbol.

- The buffer has a normal input, an output, and a control input that determines the state of the output.
- Control input=1: the output is enabled and the gate behaves like a conventional buffer, with the output equal to the normal input.
- Control input=0, the output is disabled and the gate goes to a high-impedance state, regardless of the value in the normal input.

Tri-State Buffer



E	A	Y
0	0	Z
0	1	Z
1	0	0
1	1	1

Figure 2.40 Tristate buffer

A tri-state buffer acts like a switch

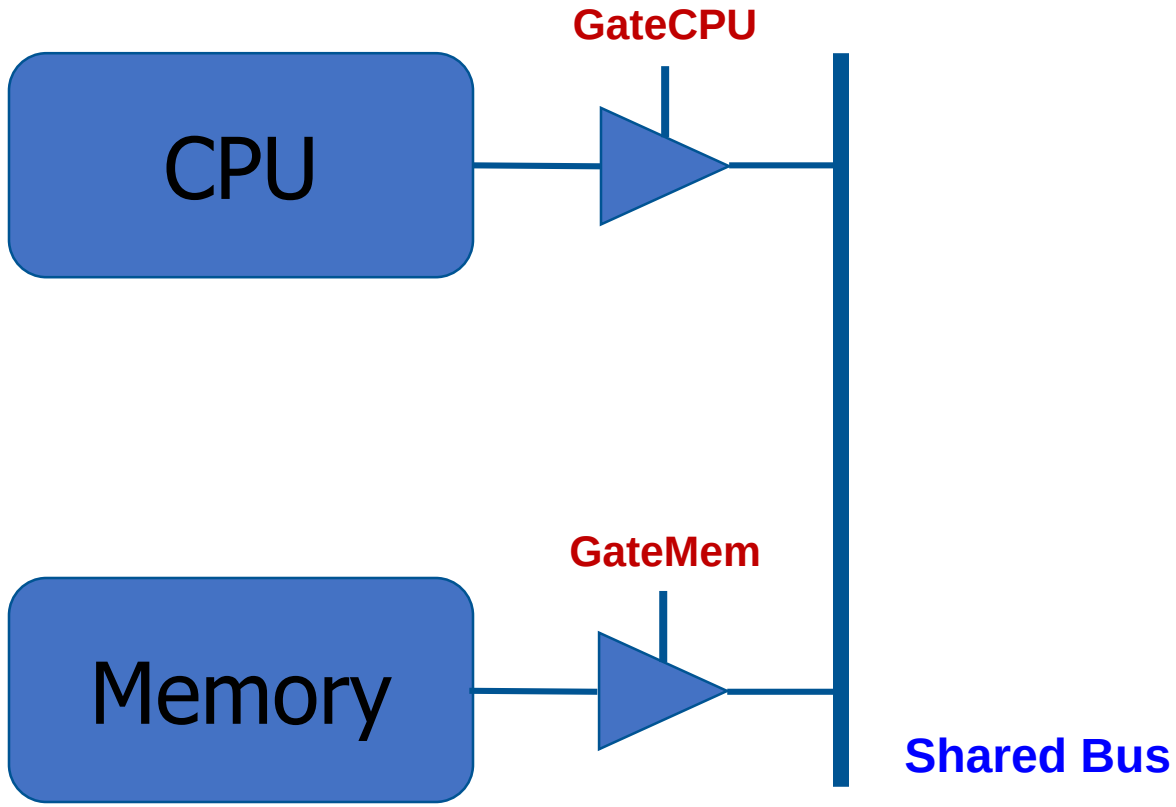
Example: Use of Tri-State Buffers

- Imagine a wire connecting the CPU and memory

  At any time only the CPU or the memory can place a value on the wire, both not both

  You can have two tri-state buffers: one driven by CPU, the other memory; and ensure at most one is enabled at any time

Example Design with Tri-State Buffers

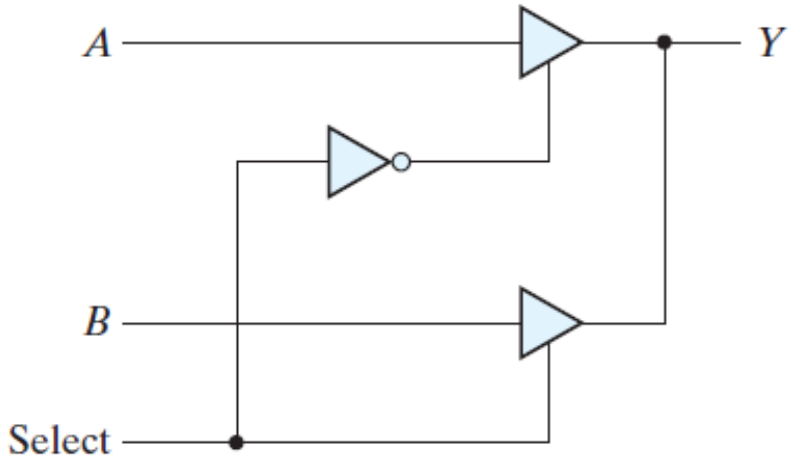


Benefit of high-impedance state

- The high-impedance state of a three-state gate provides a special feature not available in other gates.
- Because of this feature, a large number of three-state gate outputs can be connected with wires to form a common line without endangering loading effects.

Designing MUX using 3-state gate

- A multiplexer can be constructed with three-state gates



- The two outputs are connected together to form a single output line.
- **This type of connection cannot be made with gates that do not have three-state outputs.**
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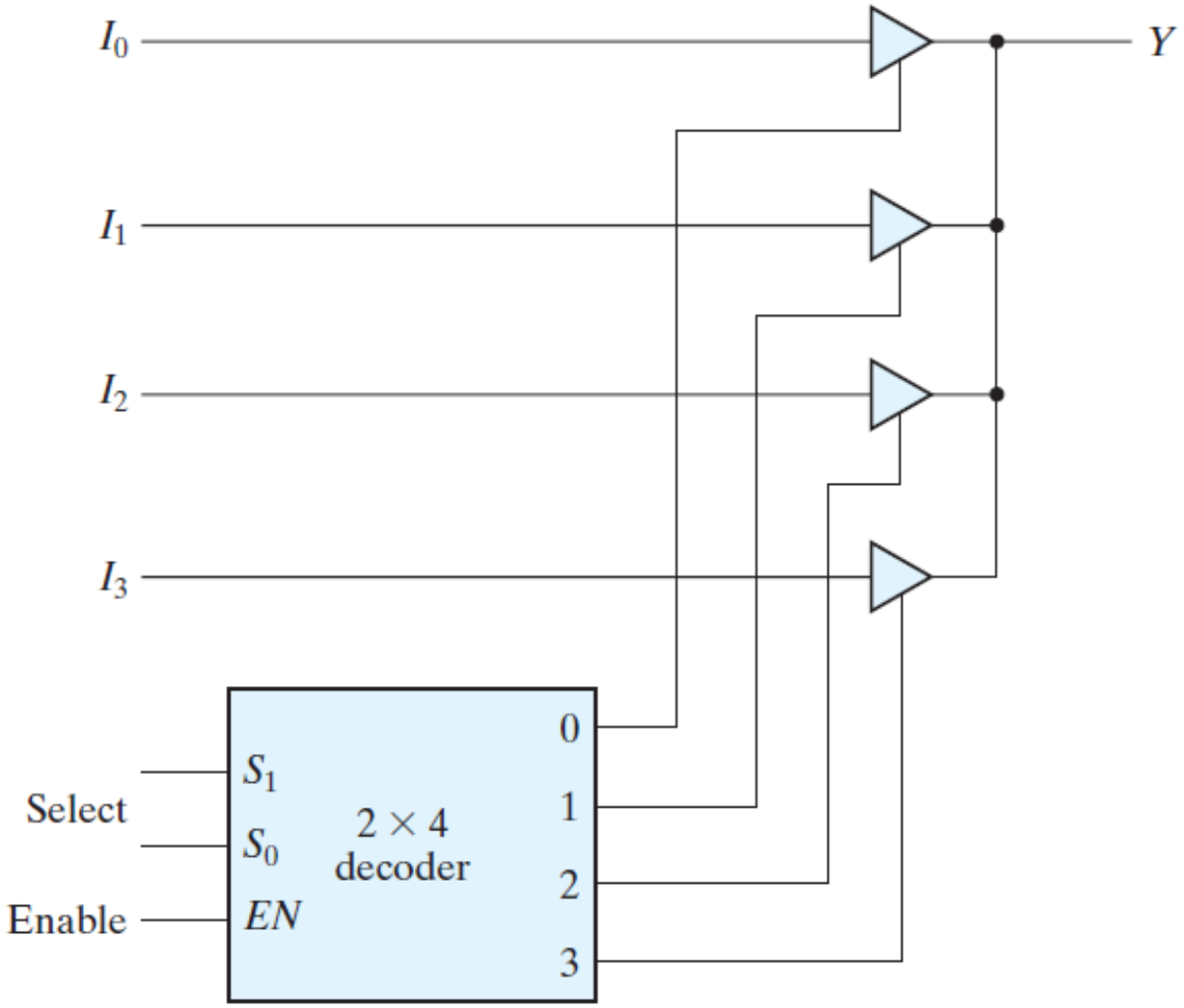
- Select=0 ➔ Upper buffer is enabled by its control input and the lower buffer is disabled. Y=A
- Select =1 ➔ Y=*B* .

4-to-1 MUX



- No more than one buffer may be in the active state at any given time. Remaining stay in high impedance state.
- For this, use a decoder.