Bilkent University Electrical and Electronics Department
EE102-03 Lab 3 Report:
Combinational Logic Circuit

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Purpose:

This lab aimed to get students to design a combinational circuit by using real-life gates on a breadboard. Furthermore, reading the datasheet of the components to design the circuit accordingly was one of the main targets.

Methodology:

The target design was the same as the design of the 2nd lab. In the original design, there were 2 AND and 1 NOR gate. However, there were not enough gates to construct the exact design. Thus, the design is improvised by using available gates: NAND and NOT gates. The output is simulated with the green LED as well as an oscilloscope. Finally, it is verified that the truth table is achieved.

Design Specifications:

The design included in this lab aims to achieve the following scenario: The nuclear crisis is about to happen, and four people will decide the future of humanity. They are grouped into two, and the group decision must be collaborative. If at least one of the groups decides to launch the missiles, the world is doomed; else, world peace is sustained. To simulate this case, the design includes 1 NAND(SN74HC00N), 1 NOT(SN74HC04N), and 1

NOR(SN74HC02N) logic IC's. Furthermore, all the combinations for the inputs are generated by a 4-bit counter(74HC163). Finally, the output from the NOR gate is connected to an LED.

Results:

The initial task was to generate four waveforms from the 4-bit counter successfully. According to the 74HC163 datasheet, for the "clock" operating mode(Figure1.1), the following inputs should be set to HIGH, which is 5V (the operating voltage of the counter): MR, CEP, CET, PE. The data entries (D_n) inputs were designated as "don't care"; thus, they are connected to the ground for clearance.

OPERATING MODE	INPUTS						OUTPUTS	
	$\overline{MR}$	CP	CEP	CET	$\overline{PE}$	D_n	Q_n	TC
reset (clear)	l	↑	X	X	X	X	L	L
parallel load	h h	↑ ↑	X X	X X	l l	l h	L H	L (1)
count	h	↑	h	h	h	X	count	(1)
hold (do nothing)	h h	X X	l X	X l	h h	X X	q_n q_n	(1) L

Figure 1.1 The Function Table

For the clock input, a 5Vpk-pk 1Hz square wave is generated by the signal generator. The data outputs are the Q_n pins. Hence the final pin set can be summarized as:

MR (Pin 1): HIGH
CP (Pin 2): Clock
D_0 – D_3 (Pin 3 – 6): LOW
CEP (Pin 7): HIGH
Ground (Pin 8): Ground
PE (Pin 9): HIGH
CET (Pin 10): HIGH
Q_0 – Q_3(Pin11- 14)
TC(Pin 15): LOW
Vcc(Pin 16): 5V

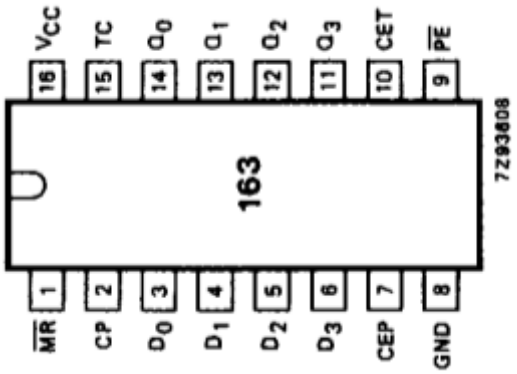

Figure 1.2 The Pin Configuration

The counter counts up to 16 in binary and resets into 0. The counting sequence can be observed via. LEDs. For a more rapid clock rate, the clock input frequency for the CP pin can be increased.

The rest of the design is constructed by logic IC's. For this implementation 1 NAND(SN74HC00N), 1 NOT(SN74HC04N) and 1 NOR(SN74HC02N) gates are used(Figure 1.3). According to their datasheets, 5V input is supplied, and the outputs from the counter are connected to the input pins of logic gates accordingly.

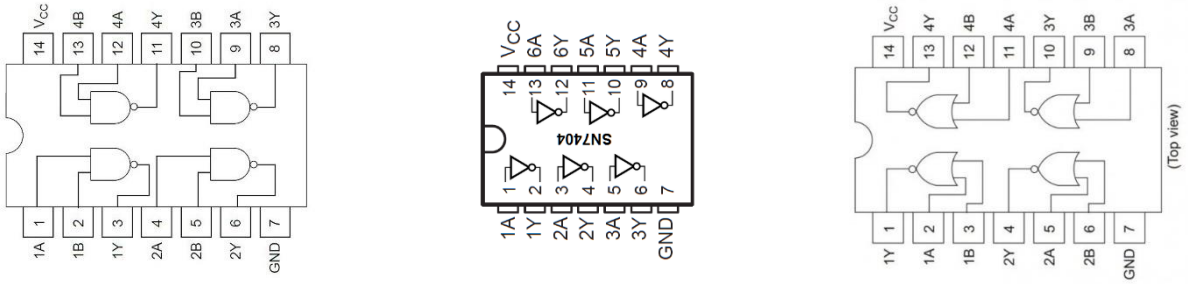

Figure 1.3 The Pinouts for the NAND, NOT and NOR gates in order

First, the Q_0 and Q_1 pins are inputted to 2 input NAND gates; then, the output is inverted via. NOT gate. Hence AND gate is achieved. The same procedure is applied to Q_2 and Q_3. The outputs from those two groups are sent to the NOR gate. The final output is connected to a green LED, and in order to observe the truth table as a waveform, an oscilloscope is used. The schematic of the breadboard design can be seen in Figure 1.4.

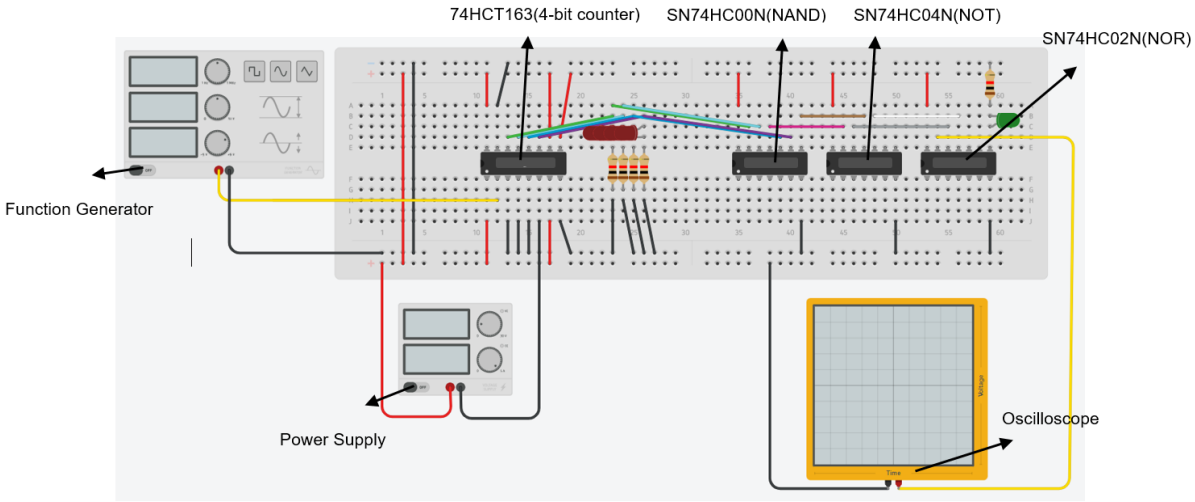

Figure 1.4 Breadboard Schematic of the design

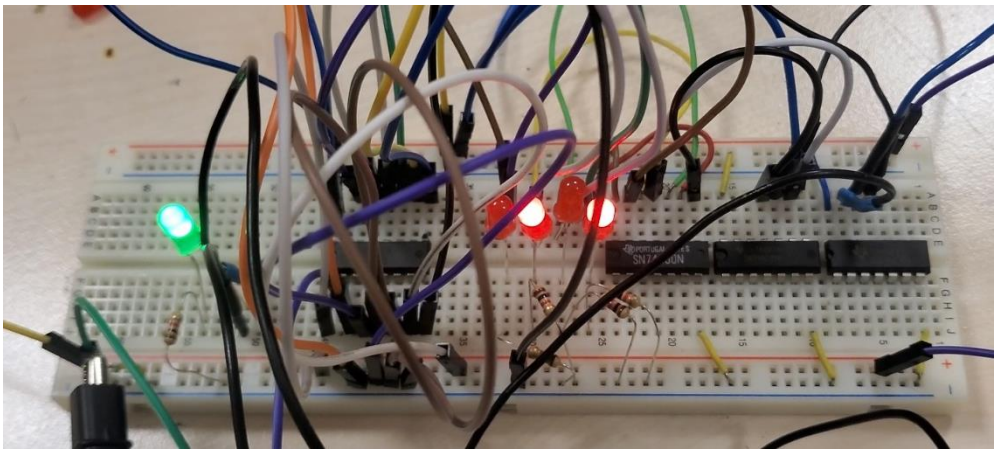

Figure 1.5 The actual breadboard design

For the final step, the waveform is generated on the oscilloscope(Figure 1.6) and verified; indeed, it is the same as the truth table given in Figure 1.7.

Q_3	Q_2	Q_1	Q_0	F
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

Figure 1.7 The Truth Table

The “0000” Point

The “1111” Point

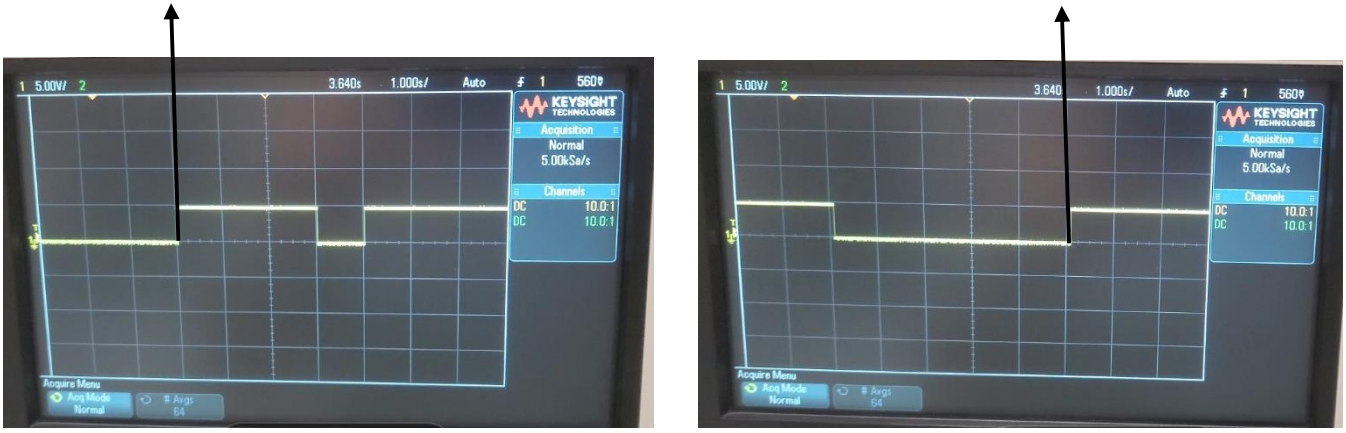

Figure 1.6 The Waveform

After each second, the counter adds +1 to the output. HIGH voltage is 5V, and LOW voltage is 0V.

Conclusion:

This lab was a general introduction to designing a combinational circuit on a breadboard. The designing section included reading the individual datasheets for the logic IC’s. The aim was to simulate the truth table of the logic design and verify the results as a form of a waveform. The waveform is generated via. 4-bit counter. There was little to no error in the counting part except ns error in a second scale (which can be disregarded). Furthermore, NAND, NOT, and NOR gates had also contributed to the delay since each of the gates has an internal capacitance, hence contributing to the overall delay. In the initial testing, the circuit did not function. After the troubleshoot, it is figured out that the NOT gate was not functional anymore (possibly burned from the previous experiments). Thus, after replacing the faulty IC, the circuit worked and gave the correct results without any problems.