Supplementary Materials for

Strain Tuning of Individual Atomic Tunneling Systems Detected by a Superconducting Qubit

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Theoretical model

The Hamiltonian of a TLS in the localized representation is given by Eq. (1) including a possible perturbation $\delta\Delta$ of its asymmetry by a strain field. In the diagonalized representation of the eigenstates, the perturbation is non-diagonal with diagonal elements describing phonon-induced changes of the energy splitting E and off-diagonal elements describing transitions between the eigenstates caused by resonant absorption or emission of phonons with frequency E/h. This is the dynamic interpretation of Eq. (1) accounting e.g. for acoustic properties of disordered solids. For static strain the diagonal terms of the Hamiltonian may be added, leading to Eq. (2). In fact, this simple dependence was applied for 40 years to interpret the behavior of TLSs in amorphous solids, but it was never measured for any individual TLS. In our experiments, this fundamental $E(\varepsilon)$ dependence is verified with surprising precision for single coherent TLSs.

In earlier experiments (*30,31*) static strain was used to influence the dwell time of individual incoherent two-level fluctuators. There, random tunneling events of TLSs with $\Delta_0 \ll \Delta \approx k_\mathrm{B}T$ caused random telegraph noise in the conductance of mesoscopic metallic wires. The strain dependence of the potential well asymmetry Δ was inferred indirectly from an analysis of the dwell times in either well, and tunneling energies Δ_0/k_B of the order of 10^{-7} K were extracted from the temperature dependence of dwell times. For that analysis, Eq. (2) was taken for granted, whereas in the present study we proved the correctnes of this relation.

Several alternative theoretical models, such as Andreev fluctuators (*25*) and Kondo traps (*26*) aim primarily to explain additional sources of noise limiting the coherence of JJ qubits. More recently developed models, e.g. Andreev bound states (*27*) seem to be adequate to account for the observed avoided level crossings in qubit spectroscopy data. Type and strength of coupling, however, are still under debate (*28*). Moreover, it has to be investigated to what extent these models can explain the data from this work. Most consistently, the microscopic origin of the anti-crossings seems to be explained by atomic two-level tunneling systems carrying an electric dipole moment and being located inside the aluminum oxide tunnel barrier of the junction. Within the barrier, the electric field is strong enough to couple these microscopic charge dipoles to the qubit. The microscopic charge dipole mechanism is experimentally supported by the scaling of the number of avoided level crossings with the TLS densities of different dielectric materials (*29*) and with the JJ area (*24*).

The sample holder

For the investigation of the dependence of TLS energies on mechanical strain, we designed a sample holder illustrated in Fig. S1. The silicon chip with the phase qubit is suspended in a notch of a copper beryllium plate. It is fixed from the rear side by a self-adhesive copper foil (not shown in the illustration), which is also considered to provide electrical shielding of the qubit circuit against the static voltage of the piezo (*32*) actuator. The piezo is glued onto a support plate which is located inside a copper beryllium frame and can be shifted coarsely by a metric fine thread. To ensure that the force acts on the center of the chip, a gold-plated zirconia sphere is glued on top of the piezo.

Calibration of the piezo actuator at low temperatures

Although the dependence of the displacement of the piezo is known at room temperature, it has to be calibrated at cryogenic temperatures. Therefore, we measured the resultant capacitance formed by the zirconia sphere and the copper foil as a function of the applied piezo voltage at room temperature and at 4.2 K. It is apparent from Fig. S2 that at 4.2 K, the piezo coefficient is reduced to 20% of its value at room temperature, resulting in an effective displacement of approximately 13 nm/V. A similar reduction factor was found for a similar type of a stacked piezo actuator (*33*). At millikelvin temperatures, further reduction of displacement is not significant, so that we can use this experimentally verified value for the following considerations.

Thermal contraction

Before cooling the system, the zirconia sphere and the copper foil are brought into contact with the help of the fine thread, which is why we have to consider the difference in the thermal contraction of the piezo actuator and the housing. According to the article of Taylor *et al.* (*33*), the integral thermal contraction factors of copper and of the piezo stack amount to $4 \cdot 10^{-3}$ and $1.2 \cdot 10^{-3}$, respectively, when reducing the temperature from 300 K to 40 K and result in a displacement of the chip center by approximately 50 μm. In numerical simulations (see next section), the spring constant of the silicon chip is calculated to be 0.7 N/μm. Thus, the load on the piezo actuator is approximately 35 N, which is considerably smaller than the specified load limit and, hence, does not affect the piezo displacement.

Evaluation of the strain field

For an 'on the back of an envelope' estimate of the strain field in the vicinity of the Josephson junction, we may consider the silicon substrate of thickness d and width a to be uniformly deformed as sketched in Fig. S3(A). In this simple model, the chip takes the shape of a circular arc with radius r when its center is displaced by l. The upper side of the chip is lengthened by δa (the lower side shortened) and the respective (dimensionless) strain at the surface is given by $\varepsilon = \delta a/a$. The relation $2\alpha = a/r = (a + \delta a)/(r + d/2)$ yields $r = d/2\varepsilon = 2$ km for $d = 400$ μm and $\varepsilon = 10^{-7}$. The displacement is $l = r(1 - \cos\alpha) \approx r\alpha^2/2$ for small angles, or $l \approx a^2/8r \approx 2.4$ nm for $a = 6.2$ mm. This corresponds to a strain of $0.42 \cdot 10^{-7}$ per 1 nm displacement.

For a more precise estimate of the deformation, we performed a numerical simulation (*34*) of the silicon chip mounted and bent in its special sample holder. The result is shown in Fig. S3(B), where the color code represents the strength of the strain field. As the force acts on a tiny area, the strain field is not uniform, but has its highest value in the center of the chip and decreases rapidly in all directions. For the region of interest where the qubit is located (marked by a black dot in Fig. S3(B)), the simulation yields a strain ranging between 0.55 and $0.65 \cdot 10^{-7}$ per 1 nm displacement in the center of the chip, which translates to $\varepsilon \simeq 7.2 \ - \ 8.4 \cdot 10^{-7}$ per 1 V piezo voltage. Due to these estimates, we consider a value of $\varepsilon/V_{\mathrm{p}} \simeq 7.8 \cdot 10^{-7}$/V reasonable for evaluations in the paper.

The studied sample

The studied phase qubit belongs to the first generation of flux-biased phase qubits (*7*) and has a rather short energy relaxation time of about 13 ns, which limits the line width of the qubit resonance to approximately 70 MHz. The circuit was fabricated on an oxidized silicon substrate which can be bent easily by applying a relatively small external force.

Evaluation of the deformation potential

The fit of the measured TLS data shown in Fig. 4B to Eq. (2) yields the following values: $\Delta_0 = h \cdot 12.4$ GHz, $\gamma_V = h \cdot 73.6$ MHz/V, and $V_0 = 16.4$ V. Applying the calibration $\varepsilon/V_\mathrm{p} = 7.8{\cdot}10^{-7}/\mathrm{V}$ we obtain the deformation potential of this particular TLS to be $\gamma = h{\cdot}4.72{\cdot}10^{13}$ Hz or 0.20 eV.

Results from a more coherent qubit

For verification of our experimental setup and of our observations, we performed the same experiment on a phase qubit with a newer design (*35*). The main differences between the two samples are sapphire as the new substrate and a much smaller Josephson junction which is shunted by a plate capacitor to pull down the junction plasma frequency. The dielectric inside the capacitor is SiN which is known to be very weakly dissipative (*8*). Due to these changes, the coherence times T_1 and T_2 of the qubit have increased by a factor of 10 to approximately 100 ns. Al and AlO_x were used as the superconductor and the tunneling barrier, respectively, as it was also the case with the older samples. Figure S4 shows the TLS traces of the newer sapphire sample. The experimental technique is exactly the same as explained in the main paper. As expected, the number of TLSs has decreased significantly. Moreover, the resonance frequency of various TLSs shows a hyperbolic dependence on strain as indicated by the fitted dashed lines in the Figure. This strongly supports our interpretation. The reason for the high number of almost symmetric TLSs in comparison to the number of visible TLSs might be a completely different fabrication process of the Josephson junction and the smaller qubit operation frequency. Furthermore, the reduction of the junction area from 30 $\mu\mathrm{m}^2$ to 1 $\mu\mathrm{m}^2$ makes it difficult to compare the defects inside the junction to the "standard" TLSs described and observed in glasses.

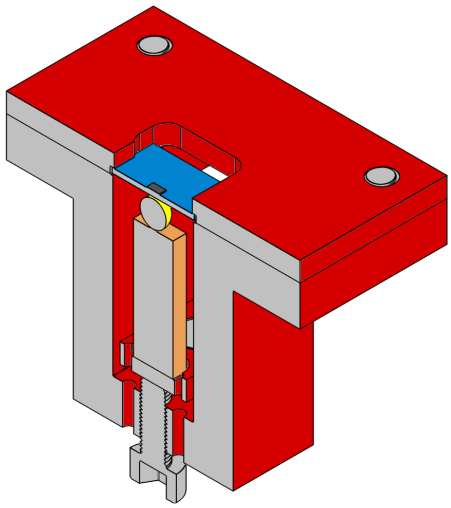

Fig. S1. Cut-away drawing of the sample holder. Main parts are: Body (red) made of copper beryllium, piezo actuator (orange), gold-plated zirconia sphere (yellow), silicon substrate (blue) and position of the qubit (dark gray). The silicon chip is supported by two opposite rims partly shortened to give room for bonding wires.

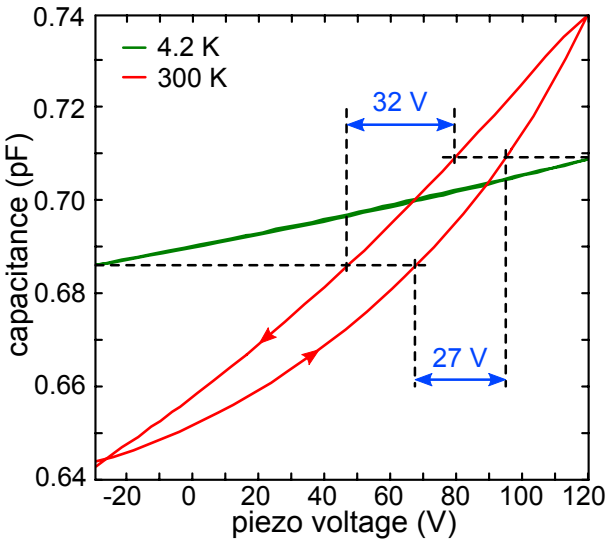

Fig. S2. Calibration of the piezo actuator. Variation with piezo voltage V_{p} of the capacitance formed by the gold-plated zirconia sphere and the copper foil on the rear side of the silicon substrate. The same capacitance change from 0.686 pF to 0.708 pF required a variation of V_{p} of about 30 V (averaging the values of the two shown traces) at room temperature and about 150 V at 4.2 K.

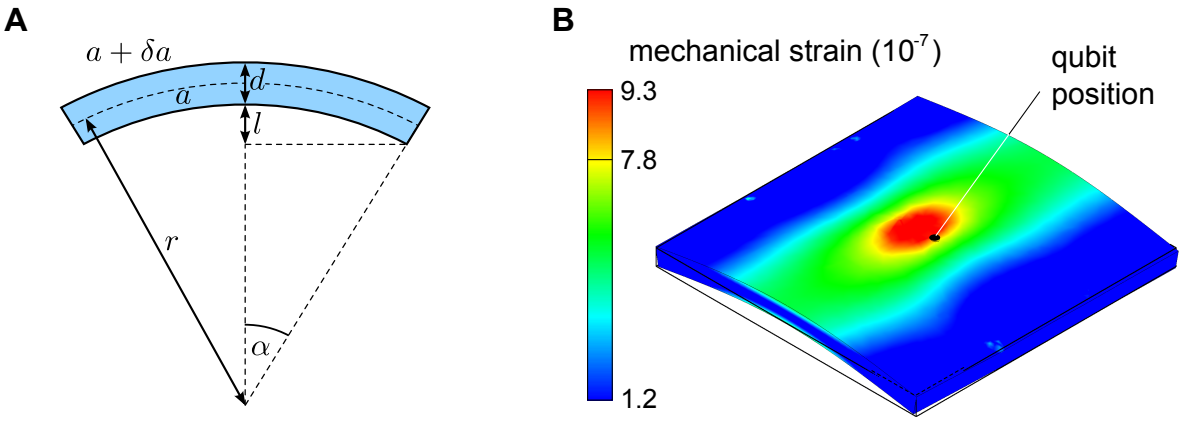

Fig. S3. Estimates of the strain field. **(A)** Geometry of a uniformly bent plate. **(B)** Result of a numerical simulation of the deformation of our silicon substrate in its real mounting. The color code represents the strain field at 13 nm displacement in the center obtained with 1 V applied to the piezo.

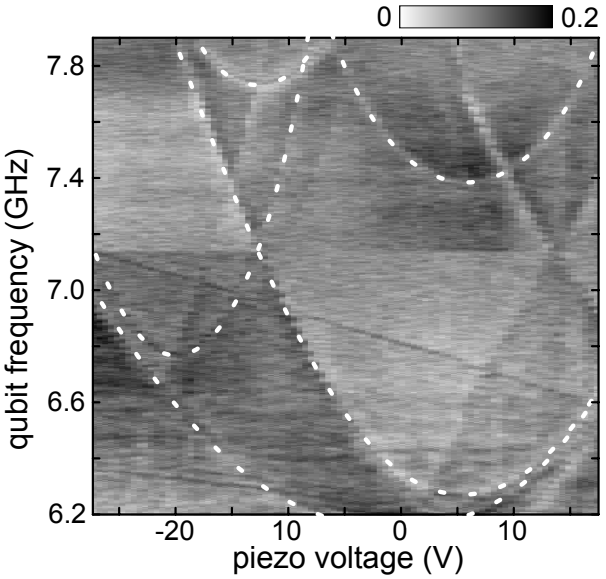

Fig. S4. Measurement of a phase qubit with a newer design on sapphire as substrate. The qubit shows less TLSs in number but the bending of the chip reveals that the resonance frequencies of many TLSs follow a hyperbola, as it is predicted by the tunneling model.

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