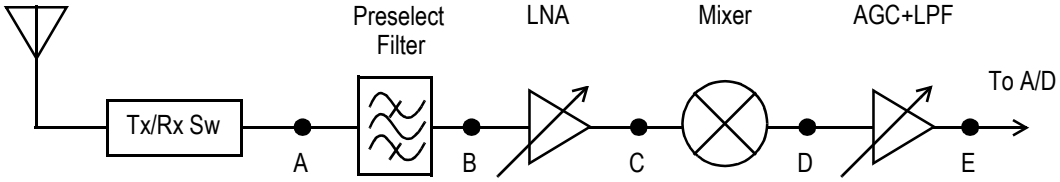
The front-end for a low-IF GSM receiver is shown below. Assume max. gain of 43dB for the AGC+LPF stage when completing the table and questions.

Component	Tx/Rx Switch	Preselect Filter	LNA	Mixer	AGC+LPF
Gain, dB	-1	-3	20	5	4-43dB
Noise Fig, dB	1	3	1.25		7
Input IP_3, dBm	+100	+100		+8	+10 (at max gain)



Signal Point	A	B	C	D	E
ΣNoise Factor					
ΣGain (dB)					
Signal, in dBm	-107				
Noise, in dBm	-121				
S/N Ratio, in dB					
Third-order intercept (IP_3), in dBm					
Minimum detectable signal, in dBm					

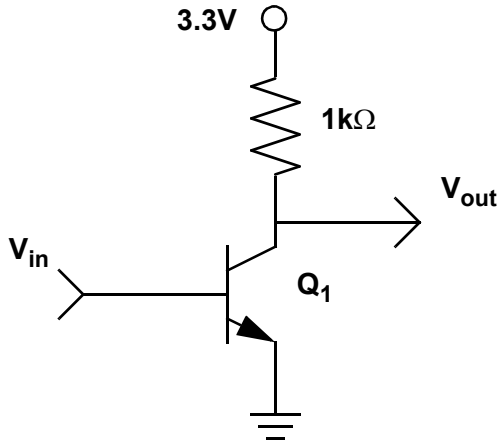
Figure 1: GSM receiver link budget summary.

1. Determine the mixer noise figure and LNA IIP_3 that gives an overall receiver noise figure of 5.5dB and IIP_3 of -15dBm (10 marks total).

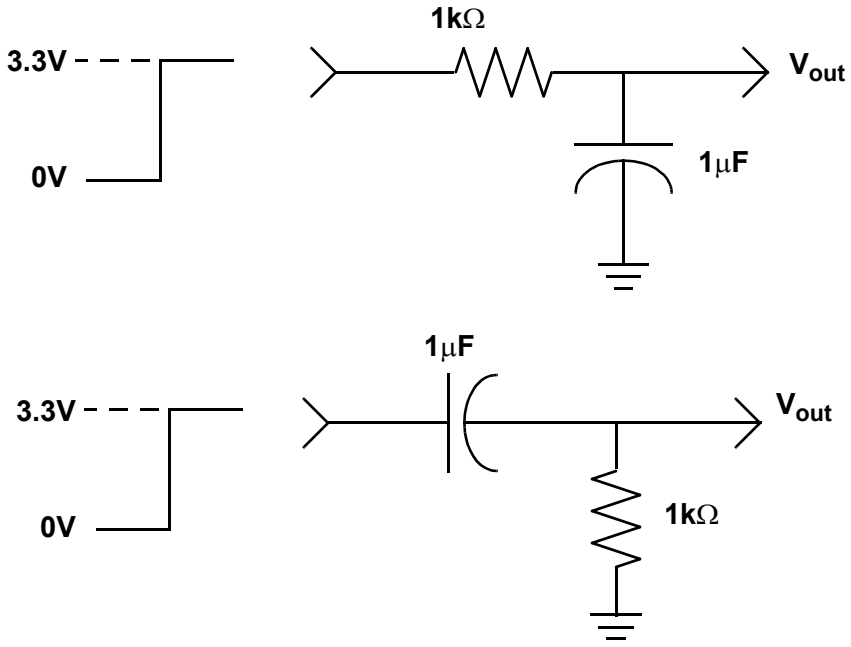
2. Complete the table in the lower part of Figure 1 (35 marks). Assume Eb/No of 14dB for the demodulator when calculating the minimum detectable signal.

Note: 5 of the following problems will be graded (5 marks/question)

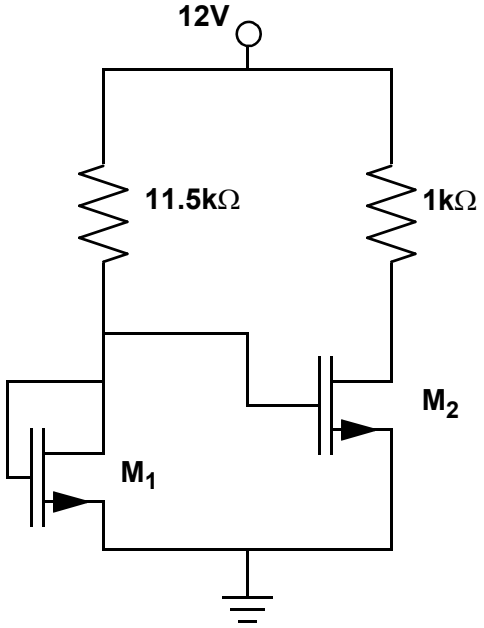
3. The base-emitter voltage of the bipolar transistor Q1 is increased from 0V to +5V. Sketch the voltage at the output, Vout.



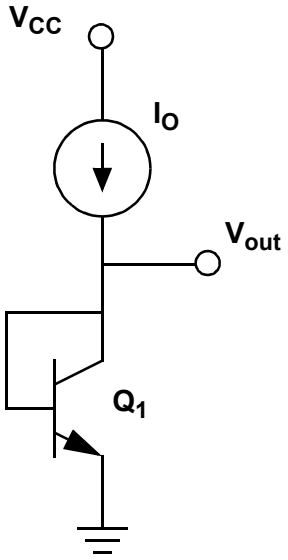
4. If a 0 to 3.3V step voltage (referenced to ground) is applied to each circuit shown below. Sketch the waveforms you expect to see at the output.



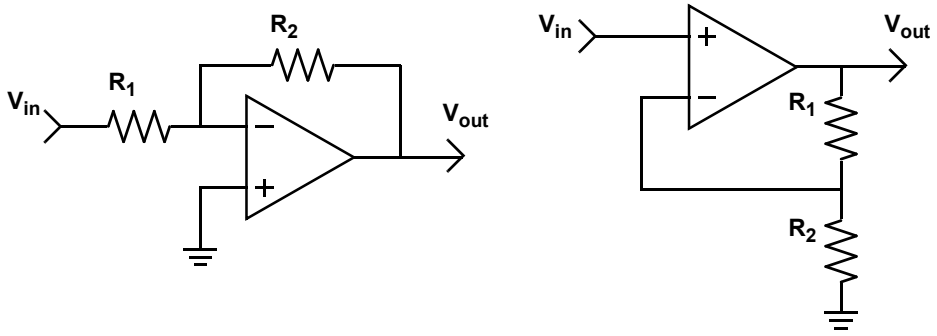
5. The diode-connected MOSFET and the transistor shown below are a matched pair. If the transistor parameters are μC_{ox} = 190 μA/V², V_{TH} = 0.6 V and both transistors have the same gate length (L), approximate the drain current in M2.



6. A constant current source Io is fed into diode-connected transistor Q1. What happens to the output voltage Vout as the temperature increases?

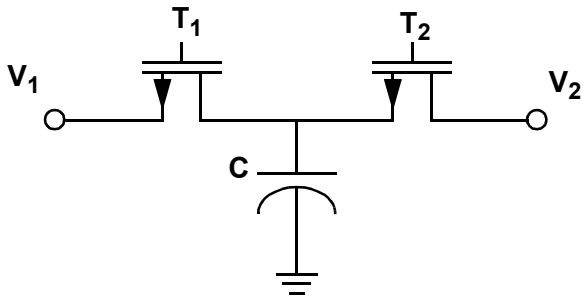


7. The ideal op amps shown below are connect with feedback resistors R1 and R2. What is the closed loop gain of each configuration?

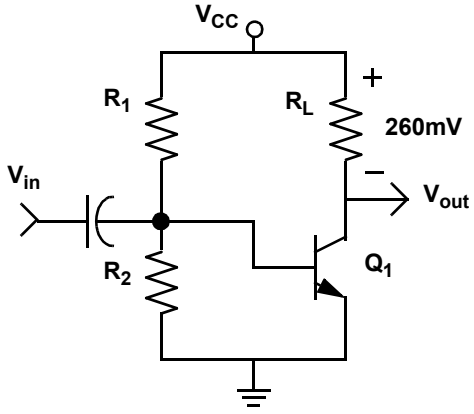


8. Assume that the op amps from question 7 have finite gain A0. What is the closed loop gain of each configuration now that the op amps are non-ideal?

9. A capacitor is connected to two MOS switches as shown below. Switches T1 and T2 are turned on alternately at frequency fc. What is the average current flowing between node 1 and node 2? What is the equivalent impedance between nodes 1 and 2?

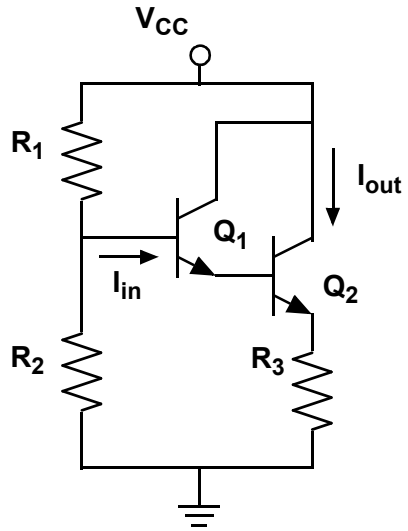


10. The bipolar transistor shown below is biased so that the voltage across RL is 260mV. A small AC signal is applied to the input. Qualitatively describe what the voltage at the output (Vout) looks like. Calculate the small-signal gain.

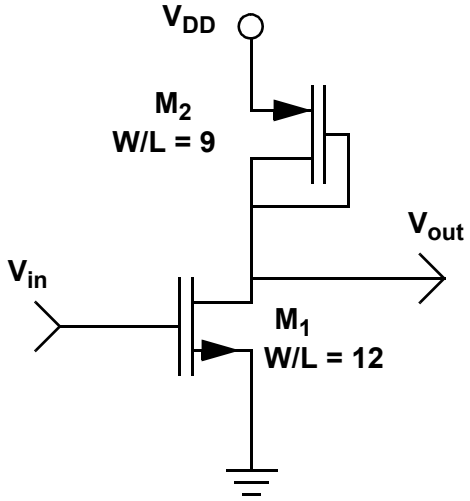


11. A two-pole amplifier is found to have an open-loop DC gain of 100dB, gain-bandwidth product of 10MHz, and 45^o of phase margin. Sketch the Bode plot for the open-loop amplifier, showing the gain response, phase response and location of the poles.

12. The Darlington pair of npn transistors Q1 and Q2 shown below have current gain β. What is the approximate current gain of the pair?



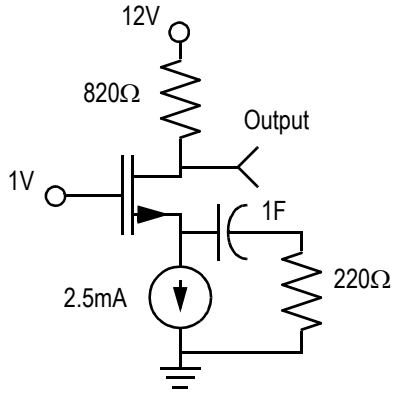
13. A CMOS amplifier consists of PMOS device M1 and NMOS transistor M2 as shown below. Assuming that both transistors have the same gate oxide thickness, what is the approximate gain of the amplifier?



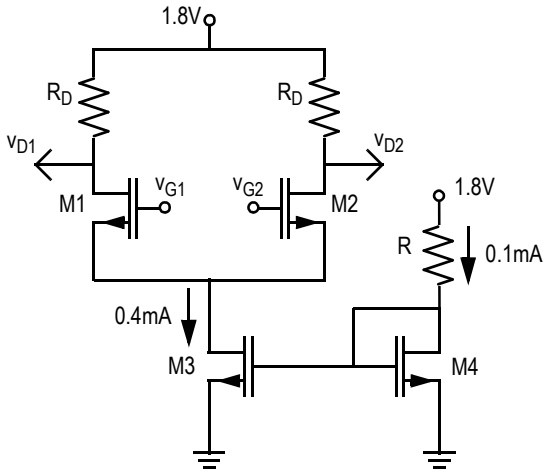
14. You are probing a square wave pulse in the lab that has a risetime of 5ns and a falltime of 2ns. Assuming a first-order lowpass response, what is the minimum bandwidth of the oscilloscope required to measure the signal properly?

15. What is the thermal rms noise voltage of a 1kOhm resistor at 300K?

16. Find the low-frequency output impedance of the MOSFET stage shown below assuming that the output resistance of the transistor is rds. The small-signal parameters of the transistor are: gm = 20mS, Cgs = 0.1pF, Cgd = 39fF, rds = 750Ohms. How does the output impedance change at low frequency if the load resistor at the drain is doubled to 1640Ohms?



17. Design the NMOS differential amplifier shown below to obtain a DC voltage of +1V at each drain of M1 and M2 when $V_{G1} = V_{G2} = 0.9V$. Operate all transistors at $V_{OV} = 0.15V$ and assume that $V_{tn} = 0.5V$ and $\mu_n C_{ox} = 500\mu A/V^2$ for the process technology. Neglect channel length modulation.



The following questions (problems 23-27) relate to your design from problem 22:

18. Compute R, R_D, and W/L ratios for M1, M2, M3 and M4.

19. What is the input common mode range for your design?

20. Find g_m for transistors M1 and M2.

21. Draw a complete small-signal equivalent circuit for the amplifier.

22. For $v_{out} = v_{d1} - v_{d2}$ and $v_{sig} = v_{g1} - v_{g2}$, find v_{out}/v_{sig}.