

**SDI deserializer**

U2A GS2971A Semtech

U2B GS2971A Semtech

U2C GS2971A Semtech

**Programming interface**

J6 GRP8052VWVN-RC

**GS\_I2C**

J5 GRP8041VWVN-RC

**Logotypes**

N1 antmicro\_logo

N2 osthw\_logo

**SDI output**

U3 GS2988-INE3 Semtech

**SDI input**

J2 112740-13

**Filtering**

R30 105R

C58 33u

**RESET**

R84 2k2

S1 B3U-1000P

**Place close to GS2971A**

C59 16p

C60 16p

**MIPI connector**

J3 WL68715014522\_ONE-SIDE

**I2C to SPI bridge**

U5 SC18IS602BIPW

**I2S connector**

J4 GRP8052VWVN-RC

**Pull-up resistors**

R85-R94 2k2

The figure displays three circuit diagrams, each showing a different power supply rail and its associated components:

- Top Diagram (+3V3):** Shows a circuit with a +3V3 supply rail. It includes capacitors C19 (10nF) and C24 (1uF) connected to GNDREF, and capacitors C28 (1uF) and C32 (10nF) connected to GND. Resistors R21 and R22 are shown in series between the two ground planes.
- Middle Diagram (+1V2):** Shows a circuit with a +1V2 supply rail. It includes capacitors C20 (10nF) and C25 (1uF) connected to GNDREF, and capacitors C29 (1uF) and C33 (10nF) connected to GND. Resistor R23 is shown in series between the two ground planes.
- Bottom Diagram (+3.3V):** Shows a circuit with a +3.3V supply rail. It includes capacitors C21 (10nF) and C26 (1uF) connected to GNDREF, and capacitors C30 (1uF) and C34 (10nF) connected to GND. Resistor R24 is shown in series between the two ground planes.

The top diagram shows the connection of the BLM18PG121SH1D component to the +3.3V (VCC\_IO) and +1V2 (VCCA\_DPHY) power pins. The component is connected to GNDREF and GNDREF. The bottom diagram shows the connection of the BLM18PG121SH1D component to the +1V2 (VCCGPLL) and GNDREF power pins. The component is connected to GNDREF and GNDREF.

LOCKED

R31

100R

D1

1

2

LG\_L29K-G2J1-24-Z

GNDREF

LOCKED\_CL

R88

100R

D2

1

2

LG\_L29K-G2J1-24-Z

GNDREF

CDONE

R93

100R

D4

1

2

LG\_L29K-G2J1-24-Z

GNDREF

USER\_LED

R64

100R

D5

1

2

LG\_L29K-G2J1-24-Z

GNDREF

DATA\_ERROR

Diagram showing the connections for pins 1 through 16 of the ADXL345 module:

- Pin 1:** USER\_SW
- Pin 2:** SDO\_EN\_DIS
- Pin 3:** Audio\_EN\_DIS
- Pin 4:** IOPAD0\_EN\_DIS
- Pin 5:** 20Hz\_10Hz
- Pin 6:** SMPTE\_BYPASS
- Pin 7:** GND
- Pin 8:** SW1 (SW\_DIP\_x06)
- Pin 9:** SW2 (SW\_DIP\_x06)
- Pin 10:** 10\_VDD
- Pin 11:** DVB\_ASI
- Pin 12:** SW\_EN
- Pin 13:** TIM\_861
- Pin 14:** RC\_BYP
- Pin 15:** STANDBY
- Pin 16:** /TAQ\_HOST

[illegible]