Silicon Optronics, Inc.

JX-F37: 1/3" Full HD CMOS Image Sensor With MIPI Interface

General Description:

JX-F37 is a high performance 2.0MP CMOS image sensor designed and fabricated with SOI's 2.7um pixel technology. It can deliver images at 30fps in full HD mode.

The JX-F37 consists of a 1928 x 1088 active pixel sensor (APS) array with on-chip 10-bit ADC, programmable gain control (PGA), and correlated double sampling (CDS) to significantly reduce fixed pattern noise (FPN). The sensor also has many standard programmable and automatic functions. It has both the industry compliant DVP parallel and MIPI CSI2 dual-data lane serial interfaces. The external host controller can access this device through a standard serial interface.

It is available in wafer-level packaged CSP.

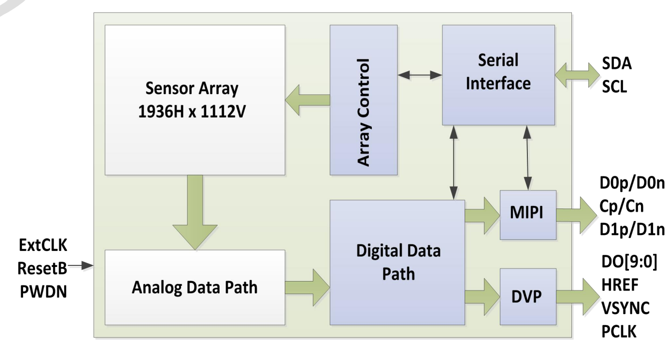
Features:

- Automatic functions:
  - ABLC – Automatic Black Level Calibration
- Programmable controls:
  - Gain, exposure, frame rate and size
  - Image mirror and flip
  - Window panning and cropping
  - I2C slave ID
- Output formats:
  - DVP parallel interface
  - MIPI CSI2 (dual lane)
- Data formats:
  - 10-bit RAW RGB
- Others
  - 50/60Hz flick noise cancellation
  - Frame sync
  - Register group write capability
  - Black sun spot cancellation

Key Specifications:

Optical format		1/3"
Active Pixels		1928H x 1088V
Pixel size		2.7 x 2.7 µm
Color filter array		RGB Bayer pattern
Chief Ray Angle		12.5 degrees linear
Shutter type		Electronic rolling shutter
Maximum Frame Rate		FHD: 1920x1080 @30fps
Supply voltage	**Analog**	2.6 – 3.0V (2.8V nominal)
	I/O	1.7 – 3.45V (1.8V nominal)
Power consumption	**Active**	TBD
	Standby	Typ.: 300 uA
Output Formats		10-bit RGB Raw Data
Sensitivity		TBD mV/lux-sec
Max SNR		TBD db
Dynamic range		TBD db
Dark Current		TBD mV/sec @ 45 ˚C
Operating junction temperature		-30 ˚C to 85 ˚C
Stable image junction temperature		60 ˚C

Functional Block:



Component Order Information:

Part Number	Description
JX-F37-C1-D3	CSP, DVP interface
JX-F37-C1-M3	CSP, MIPI interface

Contents

Pin Diagram:

JX-F37's pin diagram is shown in Figure 1 and each pin's description is shown in Table 1:

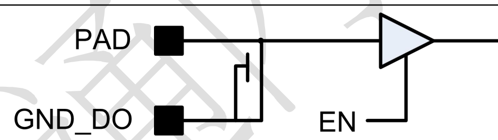
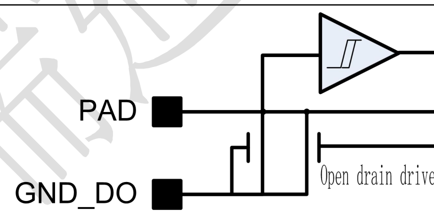
Figure 1: JX-F37 CSP top view

Table 1: Pin Description

Pin number	Pin name	Pin type	Description
A1	PCLK	I/O	DVP Pixel clock output.
A2	DOGND	Supply	Digital I/O ground
A3	DOVDD	Supply	Digital I/O supply voltage.
A4	PWDN	Input	System power down control. High active.
A5	NC		No Connection.
A6	DOGND	Supply	Digital I/O ground
A7	VR	Reference	Analog Reference
A8	DVDD	Supply	Digital core supply voltage. With embedded 1.5V regulator
A9	AGND	Supply	Analog ground
B1	AGND	Supply	Analog ground
B2	HREF	I/O	Line data valid signal output.
B3	VSYNC	I/O	Vertical synchronize signal, drive high when last frame end and drive low before next frame start. Also, can be programmed as frame synchronize input
B4	SDA	I/O	Serial data, pull to DOVDD with a 4.3k Ω resistor
B5	DVDD	Supply	Digital core supply voltage. With embedded 1.5V regulator
B6	NC		No Connection.
B7	DOGND	Supply	Digital I/O ground
B8	DOVDD	Supply	Digital I/O supply voltage.
B9	AVDD	Supply	Analog supply voltage.
C1	AVDD	Supply	Analog supply voltage.
C2	DVDD	Supply	Digital core supply voltage. With embedded 1.5V regulator
C3	SCL	Input	Serial interface clock input.
C4	RSTB	Input	System synchronize reset when driven low, it resumes normal operation with all configuration register set to factory default
C5			
C6			
C7			
C8	VH	Reference	Internal analog reference.
C9	VN	Reference	Internal analog reference.
D1	AVDD	Supply	Analog supply voltage.
D2	D7	I/O	DVP data output bit 7
D3	DOVDD	Supply	Digital I/O supply voltage.
D4	D4	I/O	DVP data output bit 4
D5	D1/SID1	I/O	DVP data output bit 1. I2C Slave ID programming bit<1>, default pull down internally. I2C slave ID can be programmed as "80/81", "84/85", "88/89" or "8C/8D" for write and read.
D6	AGND	Supply	Analog ground
D7	MCN	I/O	MIPI clock lane negative output.
D8	MCP	I/O	MIPI clock lane positive output.
D9	DOGND	Supply	Digital I/O ground
E1	D9	I/O	DVP data output bit 9
E2	D6	I/O	DVP data output bit 6
E3	DVDD	Supply	Digital core supply voltage. With embedded 1.5V regulator
E4	D3	I/O	DVP data output bit 3
E5	D0/SID0	I/O	Pixel data output bit 0. I2C Slave ID programming bit<0>, default pull down internally.

E6	MDN1	I/O	MIPI data lane 1 negative output.
E7	MDP1	I/O	MIPI data lane 1 positive output.
E8	MDP0	I/O	MIPI data lane 0 positive output.
E9	MDN0	I/O	MIPI data lane 0 negative output.
F1	D8	I/O	DVP data output bit 8
F2	D5	I/O	DVP data output bit 5
F3	DOGND	Supply	Digital I/O ground
F4	D2	I/O	DVP data output bit 2
F5	EXCLK	Input	System clock input.
F6	MVDD	Supply	MIPI supply voltage. Connect to DVDD.
F7	DOGND	Supply	Digital I/O ground
F8	MVDD	Supply	MIPI supply voltage. Connect to DVDD.
F9	DOVDD	Supply	Digital I/O supply voltage.

Table2: I/O Equivalent Circuit Diagram

<table>
<tr><th>Symbol</th><th>Equivalent Circuit</th></tr>
<tr><td>EXCLK</td><td>
</td></tr>
<tr><td>SDA</td><td>
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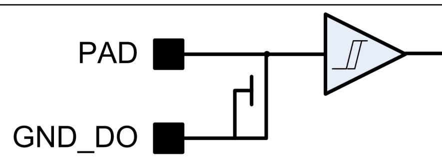
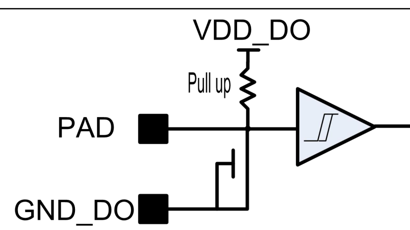
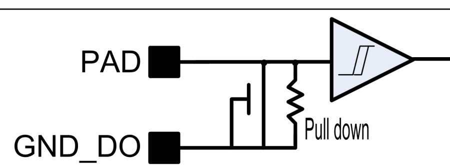
<tr><td>SCL</td><td>
</td></tr>
<tr><td>RSTB</td><td>
</td></tr>
<tr><td>PWDN</td><td>
</td></tr>
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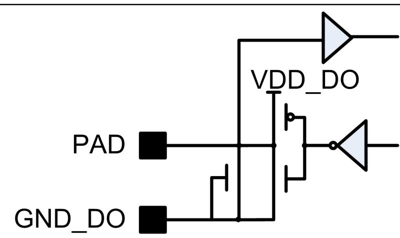
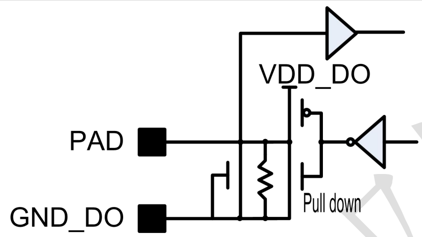
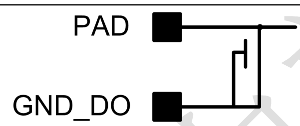
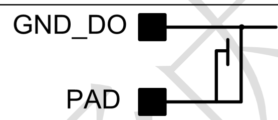
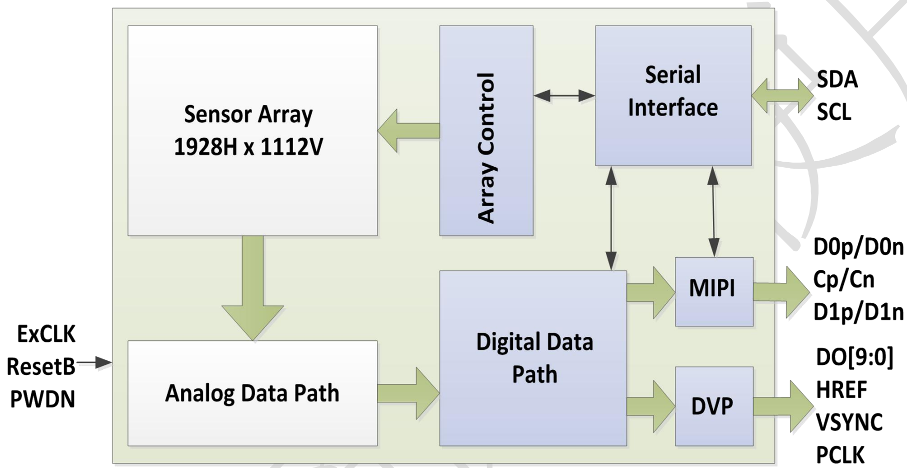
D9,D8,D7,D6,D5, D4,D3,D2,HREF,VS, PCLK	
D1,D0	
MDP1,MDN1, MDP0,MDN0,MCP, MCN,VH,VR	
VN	

Functional Overview:

The JX-F37 is a progressive-scan CMOS image sensor. It has an on-chip, phase-locked loop (PLL) to generate internal clocks from a single master input clock running between 6 and 27MHz. Its analog data process and digital data process can handle up to 81.6Mp/s at corresponding pixel clock 81.6MHz. Figure 2 illustrates the sensor's block diagram.

Figure 2. Functional Block Diagram



User can access and program JX-F37 sensor internal registers through the two-wire serial bus. The core of the sensor is a 1928x1088 pixel array. The timing and control circuitry sequences through the rows of the array, resetting and then reading each row in turn. In the time interval between resetting and reading that row, the pixels in the row integrate the incident light. The exposure is controlled by varying the time interval between reset and readout. Once a row has been read, the data from the columns is sequenced through an analog signal path to apply gain and analog signal to digital signal converter (ADC). The ADC output passes through a digital processing path for black level calibration. Then the data will output though a DVP port or MIPI CSI-2 standard interface.

Pixel Array Format:

The JX-F37 pixel array consists of a 1928-column by 1112-row matrix of pixels addressed by column and row. The address (column 0, row 0) represents the upper-right corner of the entire array (please refer to Figure 3,4 for JX-F37's Pixel array structure). The first 24 rows are optical black row for black level calibration. Outside of the 1920x1080 active pixels, there are several boundary pixels:4 rows on top, 4 rows at the bottom, 4 columns on the right, and 4 columns on the left. The detailed pixel array arrangement and default read out direction is noted in the following two figures:

Figure 3: Pixel array structure

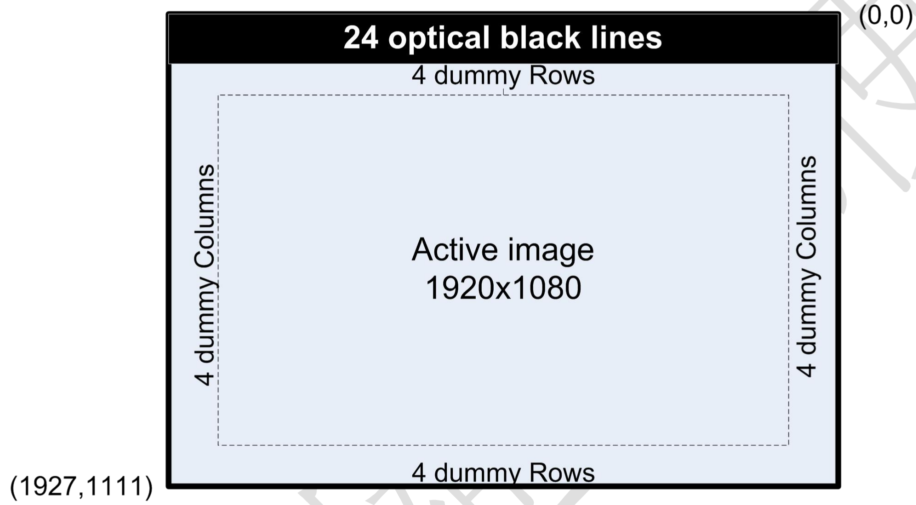
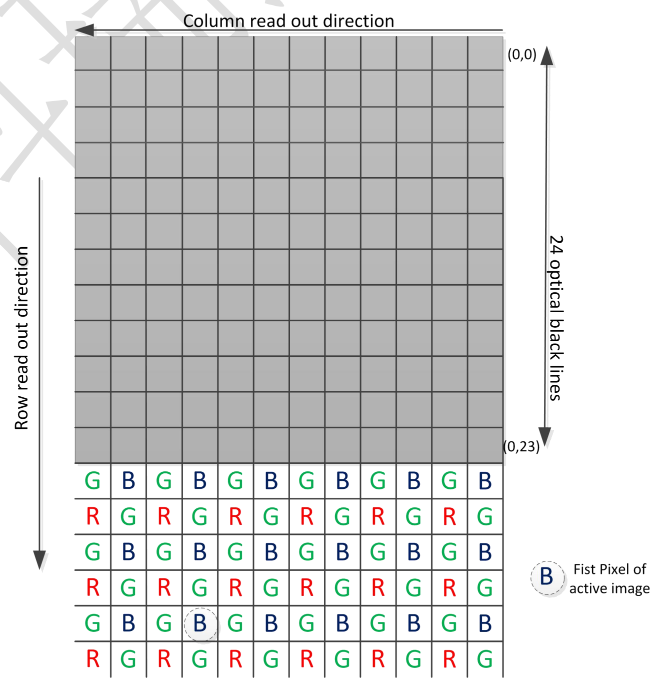


Figure 4: Pixel array detail with default read out direction.



Data Output Format:

The output images are divided into frames, which are further divided into lines. By default, the sensor produces 1088 lines (rows) of 1928 columns each. The VSYNC and HREF signals indicate the boundaries between frames and lines, respectively. PCLK can be used as a clock to latch the data. For each PCLK cycle, one 10-bit pixel data outputs on the D[9:0] pins (Figure 5). The pixel data is valid when HREF signal is asserted. The VSYNC signal indicates frame end and new frame start. JX-F37 default frame timing is illustrated as figure 6.

Figure 5: Row data output timing

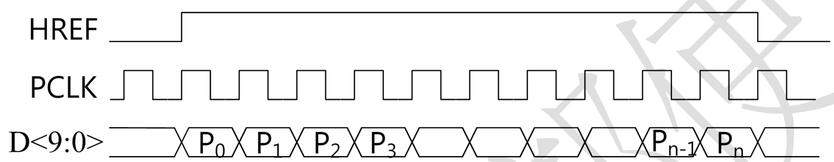
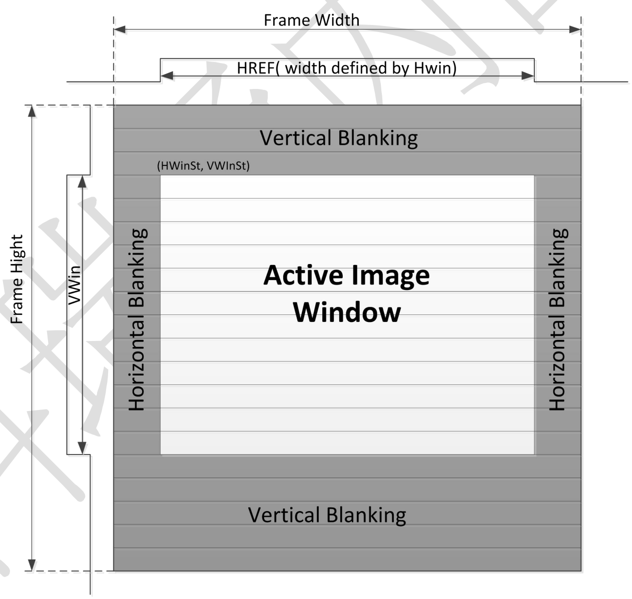


Figure 6: Default frame timing



As shown above in Figure 6, a line (row) period can be calculated as Trow = Frame_width * Thclk, and frame rate can be calculated as fps=1/(Frame_hight * Trow).

As default configuration, VSYNC, PCLK and Data are all valid at PCLK rising edge. For user convenience, JX-F37 provides register bits to control HREF, VSYNC and PCLK polarity. In addition, PCLK also have adjustable delay control.

For pixel Bayer pattern data output, several settings can have effect on pixel output sequences. These registers include HWIn_St, VWin_St, Haddr_St, Mirror, V_Flip. Please consult your SOI AE for further information.

Test Pattern Output:

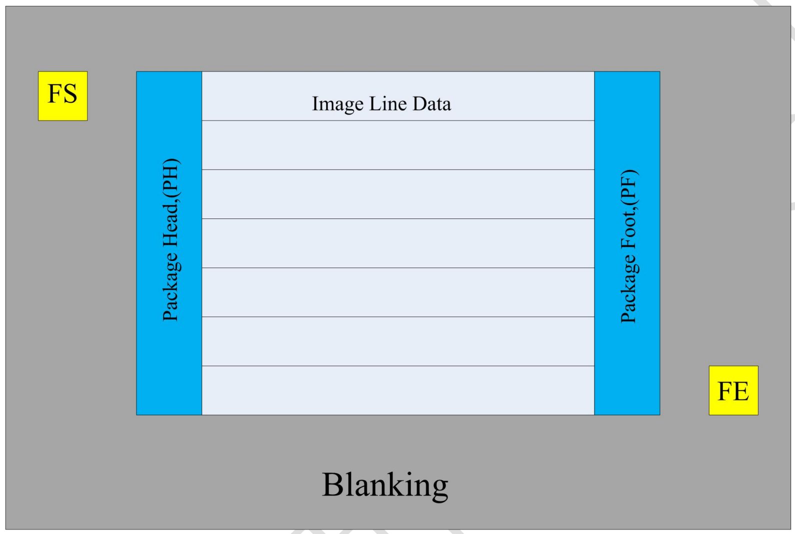
JX-F37 can output following test patterns as described below:

1) Walking “1” test pattern: for most sensor module connectivity test, JX-F37 provides walking “1” test pattern.

MIPI interface:

JX-F37 supports MIPI CSI-2 compliant interface. It has one pair of differential clock lane and two pairs of differential data lane. JX-F37 can output raw8 or raw10 mode through the MIPI interface. In raw8 mode, only 8 MSBs of 10-bit data will output and user needs to set MIPI clock speed at 8x parallel port pixel clock. In raw10 mode, user needs to set MIPI PHY clock as 10x parallel port pixel clock.

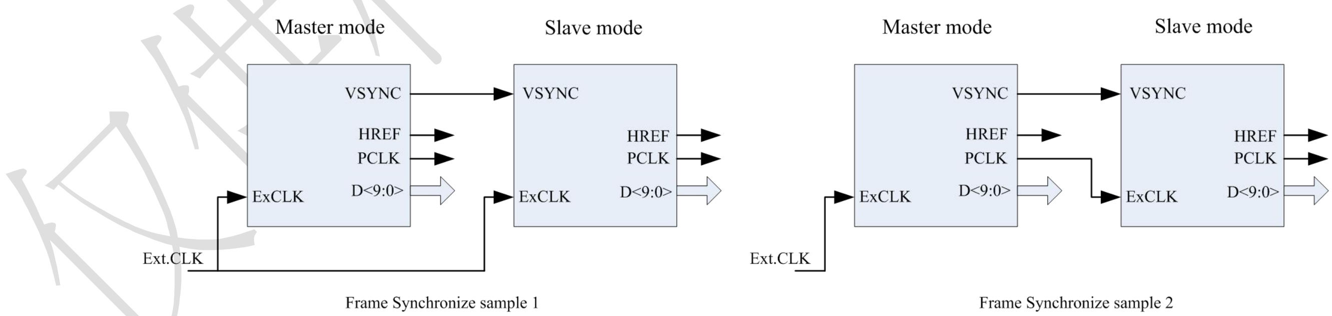
Figure 7: MIPI interface frame timing



Frame Synchronization:

JX-F37 provides the capability of frame synchronization. By setting VSYNC pin as input and enable frame-sync option, JX-F37 will work as slave device and synchronized with an external VSYNC. If all master devices and slave devices use same timing setting, all devices frame timing mismatch will be less than few pixel clocks. Figure 8 shows 2 ways to realize frame synchronization.

Figure 8: Frame Synchronization illustration



In the above 2 frame synchronize configurations, sample 2 will have more accurate synchronization than sample 1 because the slave device will have exactly same pixel clock as the master.

Serial Interface:

The serial interface is a two-wire bi-directional bus. Both wires (Serial Clock –SCL and Serial Data – SDA) are connected to DOVDD via a pull-up resistor, and when the bus is free both lines are high. The two-wire serial interface defines several different transmission stages as follows:

- A start bit
- The slave device 7-bit address
- An (No) acknowledge bit coming from slave
- An 8-bit or 16-bit message (address and/or data)
- A stop bit (or another 8bit or 16bit message in multiple Read/Write access)

Figure 9: I2C Timing chart

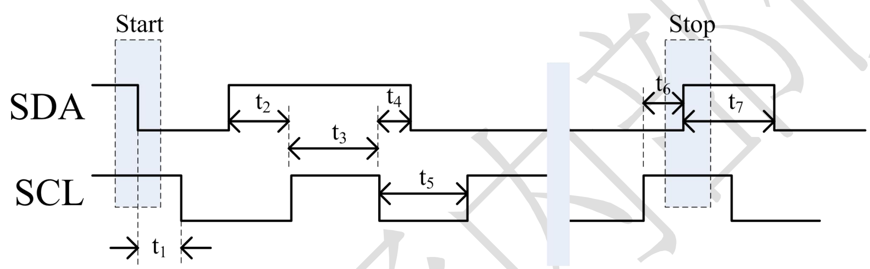


Table 3: I2C timing characteristic

Symbol	Description	Min	Max	Units
	SCL clock frequency	0	400k	Hz
t1	Hold time for START condition	0.6	-	μs
t2	Data setup time	160	-	ns
t3	High period of the SCL clock	0.6	-	μs
t4	Data hold time	0.3	0.9	μs
t5	Low period of the SCL clock	1.3	-	μs
t6	Setup time for STOP condition	0.6	-	μs
t7	Bus free time between STOP and START condition	1.3	-	μs
	Rise time for both SDA and SCL signals		300	ns
	Fall time for both SDA and SCL signals		300	ns
Cb	Capacitive load for each bus line		400	pF

Single Write Mode operation

S	**Slave-ID**	**W**	**A**	**Address (8bit)**	**A**	**DATA**	**P**

Multiple Write Mode (Register address is increased automatically) operation

S	**Slave-ID**	**W**	**A**	**Address (8bit)**	**A**	**DATA**	**P**	**…**

…	**DATA**	**A**	**…**	**DATA**	**A**	**P**

Single Read Mode operation

S	**Slave-ID**	**W**	**A**	**Address (8bit)**	**A**	**P**

S	**Slave-ID**	**R**	**A**	**DATA**	**NA**	**P**

Multiple Read Mode (Register address is increased automatically) operation

S	**Slave-ID**	**W**	**A**	**Address (8bit)**	**A**	**P**

S	**Slave-ID**	**R**	**A**	**DATA**	**A**	**…**

…	**DATA**	**A**	**DATA**	**NA**	**P**	**…**

S: start conditions, A: acknowledge bit, NA: no acknowledge, DATA: 8 bit data, P: stop condition.
JX-F37 slave ID is programmable, default is 0x80/81 for write and read. User can program DVP data bit<1:0> for other configuration. The slave ID program table is list below:

D[1]	D[0]	Read/Write
X	X	81/80
X	Pull high	85/84
Pull high	X	89/88
Pull high	Pull high	8D/8C

Register Group Write Function:

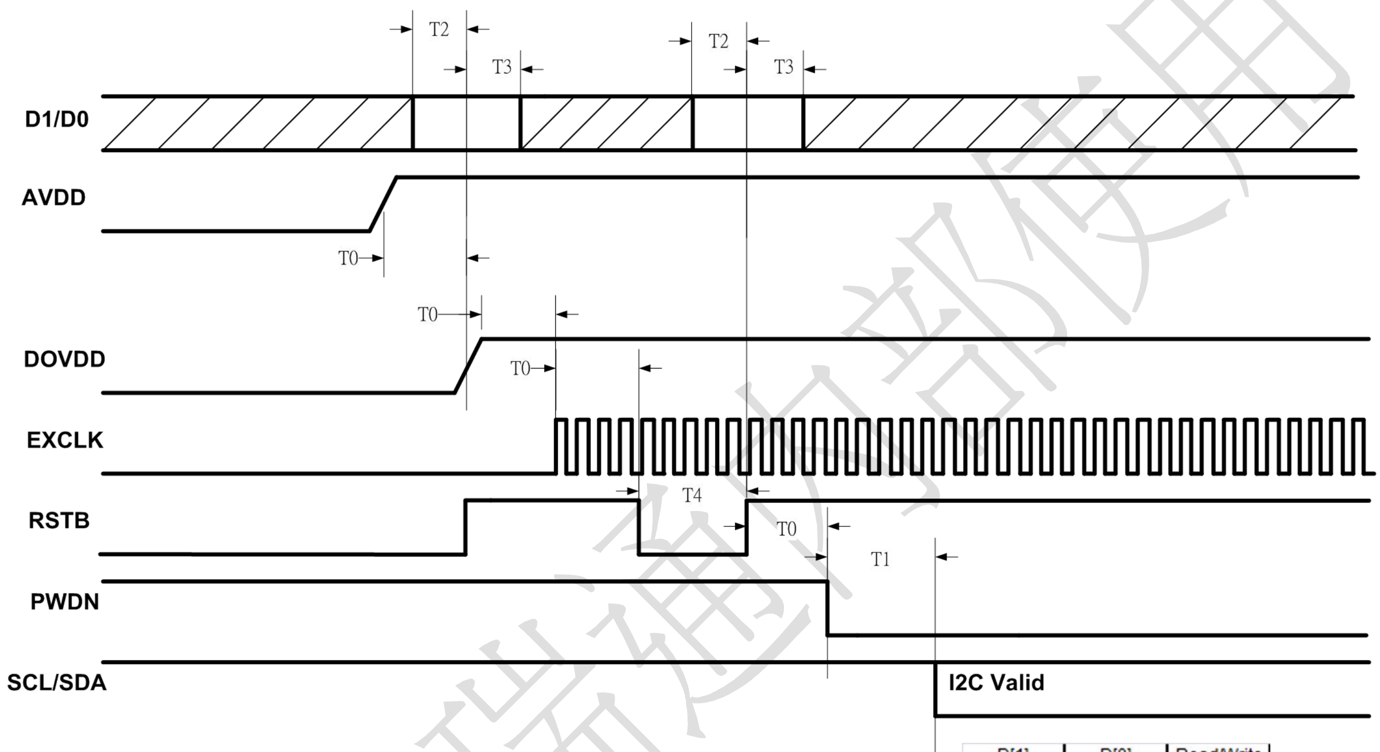
JX-F37 provides register group write function, user can pre-load address and data from register 0xC0 to 0xFF, then trigger this function by setting Reg0x1F[7], normally JX-F37 will auto write back group register content at next vertical blanking period and reset Reg0x1F[7] JX-F37 can update up to 32bytes of registers.

User can always monitor Reg0x1F[7] to make sure group write procedure is finished or not.

Power on/off sequence:

Figure 10 shows a reference power up sequence of JX-F37.

Figure 10. Power up sequence for JX-F37



Note:
1. T0 >= 0 us
2. T1 >= 8192 EXCLK cycles
3. T2>= 1ms
4. T3>= 1ms
5. T4>= 10ms

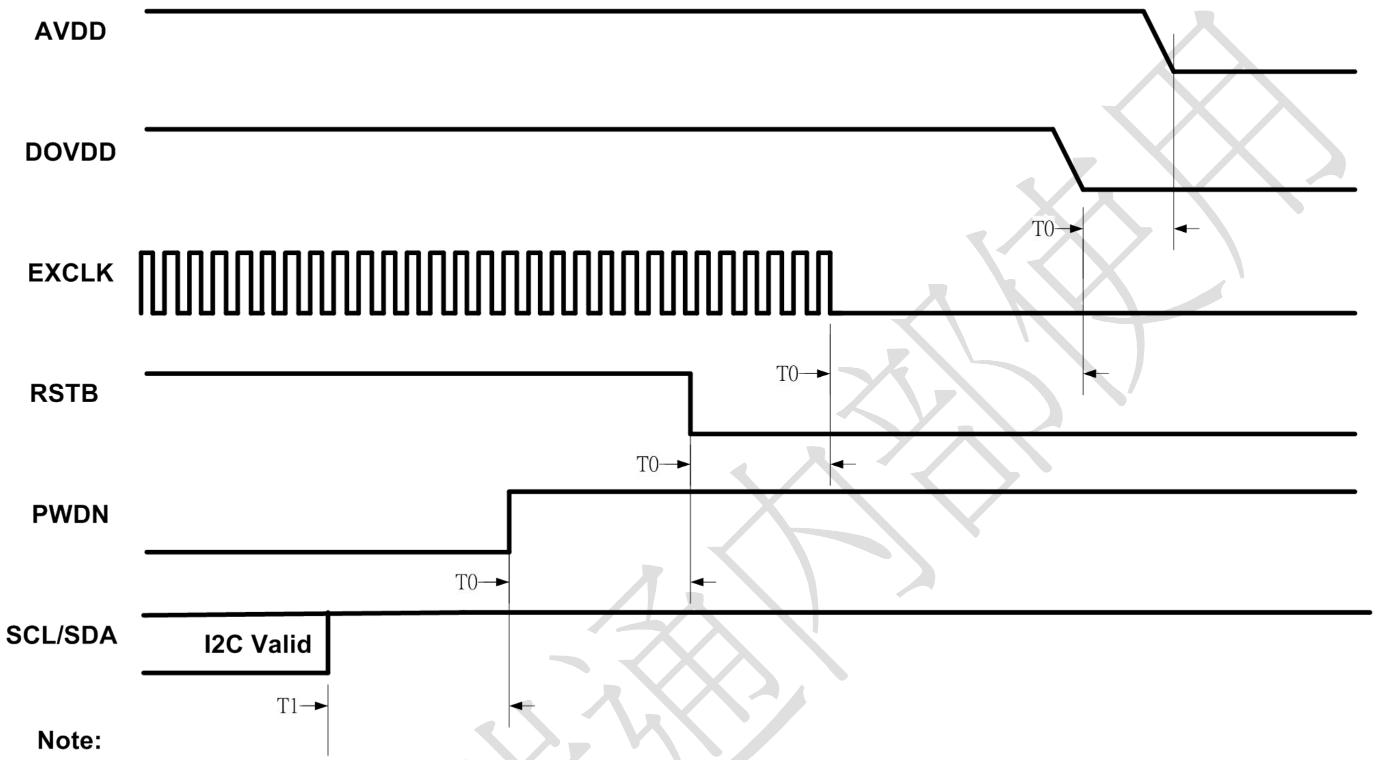
Slave ID will be updated when:
1. Power up (DVDD/DOVDD)
2. Hardware reset pin: Low -> High
3. Software reset : Reg0x12[7]=" 1"

Please stable D1/D0 when issue above commands.

D[1]	D[0]	Read/Write
X	X	81/80
X	Pull high	85/84
Pull high	X	89/88
Pull high	Pull high	8D/8C

Figure 11 shows a reference power down sequence of JX-F37.

Figure 11. Power down sequence for JX-F37



Note:
1. T0 >= 0 ns
2. T1 >= 512 EXCLK cycle

Electrical Characteristics:

Table 4. Absolute maximum ratings

Symbol	Descriptions	Absolute maximum rating	Units
V_{DD-IO}	I/O Digital Power	4.5	V
V_{DD-A}	Analog Power	4.5	V
V_{DD-D}	Core Digital Power	3.0	V
V_I	Input voltages	-0.3v to V_{DD-IO} + 1V	V
T_{AS}	Ambient Storage Temperature	-40 ~ 125	ºC

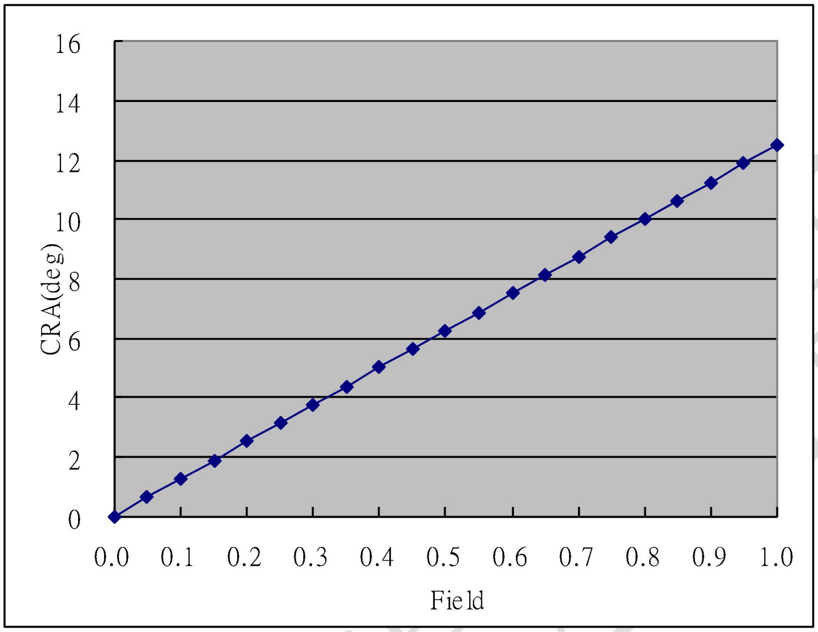
Table 5. DC Characteristics (0°C ≤ TA ≤ 85°C, Voltages referenced to GND)

Symbol	Descriptions	Max	Typ	Min	Units
supply					
V_{DD-IO}	Supply voltage (DOVDD)	3.45	1.8	1.7	V
V_{DD-A}	Supply voltage (AVDD)	3.0	2.8	2.6	V
Digital Inputs					
V_{IL}	Input voltage LOW	0.2* V_{DD-IO}	-	-	V
V_{IH}	Input voltage HIGH			0.7*V_{DD-IO}	V
C_{IN}	Input capacitor	10			pF
Digital Outputs (loading 20pF)					
V_{OH}	Output voltage HIGH			V_{DD-IO} – 0.2	V
V_{OL}	Output voltage LOW	0.2			V
Power consumption (Internal DVDD, MVDD short to DVDD; DVP output mode; AVDD=2.8V, DOVDD=1.8V)					
I_{DD-IO}	Supply current (V_{DD-IO}=1.8V@30fps FHD without digital I/O loading)		TBD		mA
I_{DD-A}	Supply current (V_{DD-A}=2.8V@30fps FHD)		TBD		mA
Power consumption (Internal DVDD, MVDD short to DVDD; MIPI output mode; AVDD=2.8V, DOVDD=1.8V)					
I_{DD-IO}	Supply current (V_{DD-IO}=1.8V@30fps MIPI2L FHD)		TBD		mA
I_{DD-A}	Supply current (V_{DD-A}=2.8V@30fps MIPI2L FHD)		TBD		mA
Ipwrdn	HW PWDN Pin active		TBD		uA

CRA Specifications:

JX-F37 is designed with a linear chief ray angle curve as shown in Figure 12. The shifting of the color filter and micro lenses on the sensor is critical to accommodate the ever-shorter height of the camera module as well as minimizing shading at the corner of the image.

Figure 12. CRA Curve for JX-F37



Field	CRA
0.00	0.000
0.05	0.625
0.10	1.250
0.15	1.875
0.20	2.500
0.25	3.125
0.30	3.750
0.35	4.375
0.40	5.000
0.45	5.625
0.50	6.250
0.55	6.875
0.60	7.500
0.65	8.125
0.70	8.750
0.75	9.375
0.80	10.000
0.85	10.625
0.90	11.250
0.95	11.875
1.00	12.500

Mechanical Specifications:

JX-F37 is available in CSP packaged component. Figure 13 shows top view and bottom view of the CSP component. Table 5 shows the nominal dimensions for the packaged chip.

Figure 13. CSP Top, Bottom, Side View

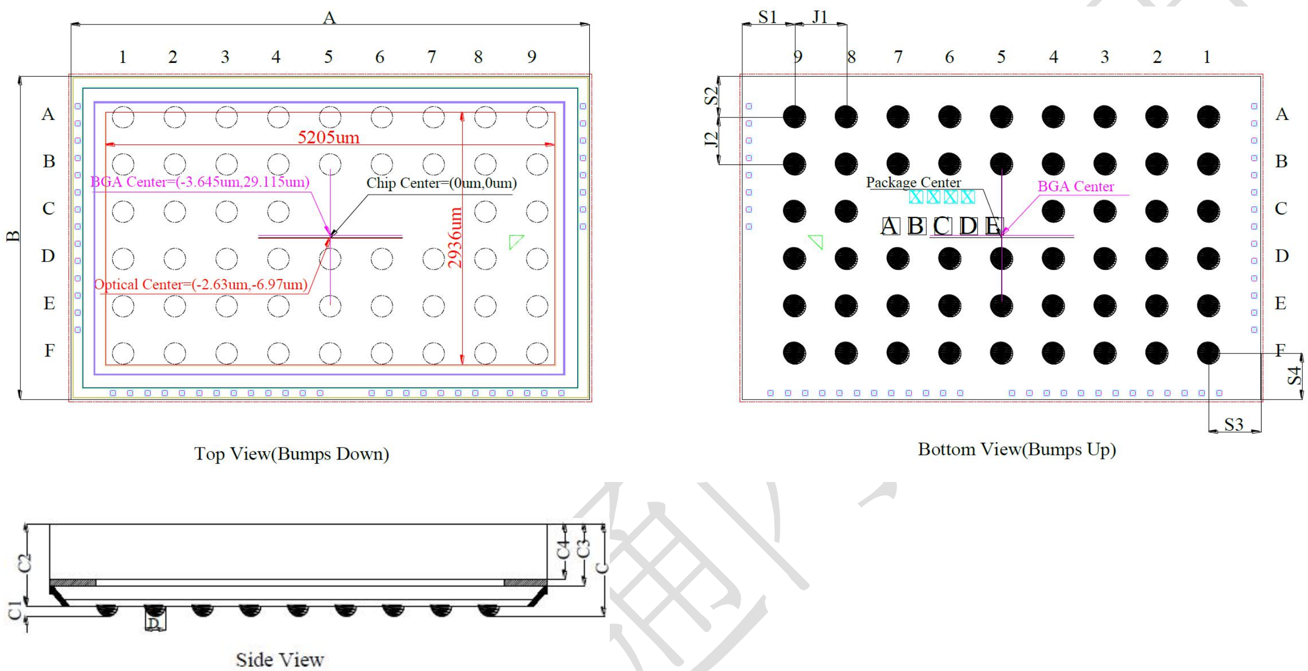


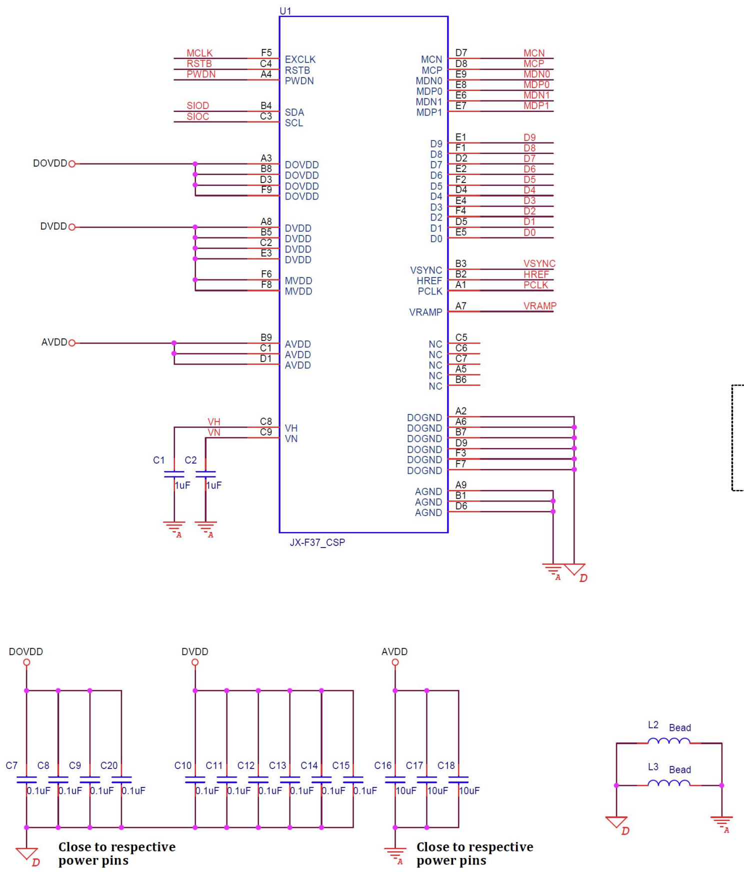
Table 6. Dimensions for JX-F37 CSP package (in mm)

	Symbol	Nominal	Min	Max	Nominal	Min	Max
		Millimeters			Inches		
Package Body Dimension X	A	6.012	5.987	6.037	0.23669	0.23571	0.23768
Package Body Dimension Y	B	3.764	3.739	3.789	0.14819	0.14720	0.14917
Package Height	C	0.770	0.710	0.830	0.03031	0.02795	0.03268
Ball Height	C1	0.130	0.100	0.160	0.00512	0.00394	0.00630
Package Body Thickness	C2	0.640	0.605	0.675	0.02520	0.02382	0.02657
Thickness from top glass surface to wafer	C3	0.445	0.425	0.465	0.01752	0.01673	0.01831
Glass Thickness	C4	0.400	0.385	0.415	0.01575	0.01516	0.01634
Ball Diameter	D	0.250	0.220	0.280	0.00984	0.00866	0.01102
Total Ball Count	N	51（2NC）					
Pins pitch X axis	J1	0.6					
Pins pitch Y axis	J2	0.55					
Edge to Pin Center Distance along X1	S1	0.609645	0.579645	0.639645	0.02400	0.02282	0.02518
Edge to Pin Center Distance along Y1	S2	0.477885	0.447885	0.507885	0.01881	0.01763	0.02000
Edge to Pin Center Distance along X2	S3	0.602355	0.572355	0.632355	0.02371	0.02253	0.02490
Edge to Pin Center Distance along Y2	S4	0.536115	0.506115	0.566115	0.02111	0.01993	0.02229

CSP Module Schematic (Reference):

Figure 14 shows reference schematics for CSP module.

Figure 14. Reference schematic for CSP module



Register Descriptions:

Write Slave ID:0x80/84/88/8C Read Slave ID:0x81/85/89/8D

Address (Hex)	Register Name	Default (Hex)	R/W	Description
00	PGA	00	RW	Programmable gain, valid 00 to 3F, Total gain = 2^PGA[6:4]*(1+PGA[3:0]/16)
01	EXP	FF	RW	Exposure line LSBs, EXP [7:0]
02	EXP	00	RW	Exposure line MSBs, EXP[15:8].; AEC[15:8] Exposure time is defined by EXP[15:0] at line period base. T_{EXP}=EXP[15:0]*T_{Line}
03-06				RSVD
07	GainLmt	00	RW	GainLmt[7:4]: Max gain limitation in AEC/AGC auto mode. “00”: 4x; “01”:8x; “10”:16x; “11”:32x; GainLmt[3:0]: HDR mode short exposure frame options.
09				RSVD
0A	PIDH	0F	R	PIDH[7:0]:Product ID MSBs. “0x0F”
0B	PIDL	33	R	PIDL[7:0]: Product ID LSBs. “0x33”
0C	DVP1	44	RW	DVP control 1. DVP1[7]: RSVD DVP1[6]: Sensor sun spot elimination control, “1”: disable sun spot elimination, “0”: enable sun spot elimination. DVP1[5:4]: SRAM read out clock delay control. (after SRAM, before digital FiFo.) DVP1[3:2]: RSVD DVP1[1:0]: DVP test mode output option. “00”: DVP output normal image data. “01”: DVP[9:0] = Output 10-bit walk “1” test pattern.; others: RSVD
0D	DVP2	50	RW	DVP control 2. DVP2[7:4]: P-Pump and N-Pump clock selection. DVP2[3:2]: PAD drive capability. “00”: min, “11”: max. DVP2[1:0]: RSVD
0E	PLL1	10	RW	PLL control 1. PLL1[7]: PLL bypass selection. “1”: PLLclk = Input clock/PLL_Pre_Ratio. “0”: see PLL2[1:0]. PLL1[6:4]: reserved PLL1[3]: Sys_Clk select, “0”:sys normal divider clock before Sys_Clk divider, “1”: select Mipi_HS_Clk before Sys_Clk divider PLL1[2]: external clock input pad circuit option, “0”: internal no Schmitt trigger; “1”: internal has Schmitt trigger. PLL1[1:0]: PLL pre-divider ratio. PLL_Pre_Ratio = 1 + PLL[1:0]
0F	PLL2	04	RW	PLL control 2. PLL2[7:4]: Output FiFo clock ratio; PLL2[3]: “1” : MIPI high speed clock = VCO/2; “0”: MIPI high speed clock = VCO; PLL2[2]: "1": work with MIPI 10bit mode, "0": work with MIPI 8bit mode PLL2[1:0]: PLL clock divider. PLLclk = VCO/(1+PLL2[1:0])
10	PLL3	26	RW	PLL control 3. PLL VCO multiplier. VCO = Input clock*PLL3[7:0]/PLL_Pre_Ratio
11	CLK	80	RW	Digital system clock control CLK[7]: System clock option. “1”: system clock use PLLclk directly. “0”: see system clock equation below. CLK[6]: system clock digital doubler on/off selection. “1”: on, “0”: off

				CLK[5:0]: system clock divide ratio. *Equation:* When CLK[5:0] > 0: System clock = PLLclk *(1+CLK[6])/(2*CLK[5:0]) When CLK[5:0] = 0: System clock = PLLclk*(1+CLK[6])/2
12	SYS	00	RW	System status set up SYS[7]: Soft reset initialize, “1”: initial system reset, it will reset whole sensor to factory default status, and this bit will clear after reset. Default : “0”: normal mode SYS[6]: Sleep mode on/off selection, “1”: sensor into sleep mode. No data output and all internal operation stops. External controller can stop sensor clock, while I2C interface still can work. Default : “0” : normal mode SYS[5]: mirror image on/off, “1”: mirrored image output, “0”: normal image output SYS[4]: flip image on/off, “1”: flipped image output, “0”: normal image output. SYS[3]: HDR mode on/off selection. “0”: normal mode, “1”: HDR mode. SYS[2]: horizontal skip or binning mode select; “0” : H-binning mode; 1: H-skip mode SYS[1]: vertical skip or full mode selection. “0” : full mode,"1":vertical skip mode SYS[0]: Horizontal down sample mode enable.
13	LCCtrl1	81	RW	Luminance control register 1. LCCtrl1[7:1]:RSVD. LCCtrl1[0]: automatic luminance control on/off selection, “0”: auto, “1”: manual
14 – 18	LCCtrl2	80	RW	RSVD
19	LCCtrl17	44	RW	Luminance control register 7 LCCtrl7[7:6]: PCLK delay option. LCCtrl7[5]: AGC delay 1 frame valid option. “0”: manual gain will apply at next VSYNC;“1”: manual gain will delay 1 frame to apply. LCCtrl7[4]: RSVD LCCtrl[3]: Enable AE change every frame. LCCtrl[2:0]: RSVD
1A	LCCtrl8	80	RW	Luminance control register 8 LCCtrl8[7:0]: RSVD
1B	LCCtrl9	4F	RW	Luminance control register 9 LCCtrl9[7:3]: RSVD LCCtrl9[2:1]: pre-precharge line selection, “00”: 1 line, “01:2lines, “10”: 3 lines, “11”: 4 lines. LCCtrl9[0]: pre-precharge option on/off selection, “0”: off, “1”: on.
1C	LCCtrl10	00	R	Luminance control register 10 LCCtrl10[7:0]: image luminance average value.
1D	DVP3	00	RW	DVP control 3 DVP3[7:0]: GPIO direction control for data output port D[7:0]. “1”: enable output. “0”: tri-state output.
1E	DVP4	1C	RW	DVP control 4 DVP4[7]: PCLK polarity control. “0”: data output at rising edge of PCLK, “1”:data output at falling edge of PCLK DVP4[6]: HREF polarity control. “0”: positive, “1”: negative DVP4[5]: VSYNC polarity control. . “0”: positive, “1”: negative DVP4[4:0]: GPIO direction control for output port: PCLK, HREF, VSYNC and D[9:8] . “1”: enable output. “0”: tri-state output.
1F	Glat	00	RW	Group latch control Glat[7]: Group write trigger. “1”: system will write reg0xC0 to 0xFF content to proper register. This bit will clear after group write. “0”: inactive group write function. Glat[6]: Group latch trigger time option, “0”: trigger at vertical blanking period. “1”: group latch trigger immediately. Glat[5:0]: reserved
20	FrameW	B0	RW	Sensor frame time width LSBs; FrameW[7:0]

21	FrameW	04	RW	Sensor frame time width MSBs; FrameW[15:8] FrameW[15:0]: sensor frame width
22	FrameH	56	RW	Sensor frame time high LSBs ;FrameH[7:0]
23	FrameH	04	RW	Sensor frame time high MSBs. FrameH[15:8] FrameH[15:0]: sensor frame high. Sensor frame rate is defined as Fpclk / (FrameW*FrameH). Fpclk: frequency of pixel clock.
24	Hwin	C0	RW	Image horizontal output window width LSBs: Hwin[7:0]
25	Vwin	38	RW	Image vertical output window high LSBs: Vwin[7:0]
26	HVWin	43	RW	Image output window horizontal and vertical MSBs. { Vwin[11:8],Hwin[11:8]}
27	HwinSt	D0	RW	Image horizontal output window start position LSBs. HwinSt[7:0]
28	VwinSt	14	RW	Image vertical output window start position LSBs. VwinSt[7:0]
29	HVWinSt	01	RW	Image output window horizontal and vertical start position MSBs. {VwinSt[11:8],HwinSt[11:8]}
2A	Cshift1	C0	RW	Column shift control 1 Cshift1[7:0]: Column SRAM data shift start position LSBs. Cshift[7:0]
2B	Cshift2	21	RW	Column shift control 2 Cshift2[7:6]: SRAM read out start address MSBs. SenHASt[9:8] Cshift2[5:4]: RSVD Cshift2[3:0]: Column SRAM data shift timing start position MSBs, Cshift[9:8]
2C	SenHASt	00	RW	SRAM read out start address LSBs, SenHASt[7:0]; each bit represent 2 pixels
2D	SenVSt	00	RW	Sensor physical vertical start address, LSBs. SenVSt[7:0]; each bit represent 4 lines
2E	SenVEnd	14	RW	Sensor physical vertical end address, LSBs. SenVEnd[7:0] ;each bit represent 4 lines
2F	SenVadd	44	RW	Sensor vertical address settings. SenVadd[7:4]: RSVD SenVadd[3:2]: SenVEnd[9:8] SenVadd[1:0]: SenVSt[9:8]
30 -40			RW	RSVD
41	SenT12	C8	RW	Sensor timing control 12 SenT12[7:0]: Array SRAM shift out pixel number LSBs, in 2 pixels step.
42	SenT13	03	RW	Sensor timing control 13 SenT13[7:2]: RSVD SenT13[1:0]: Array SRAM shift out pixel number MSBs.
43	VS_POS1	00	RW	VSYNC position LSBs: VS_POS[7:0];
44	VS_POS2	40	RW	VS_POS2[7:4]: VSYNC width selection. VS_POS2[3:0]: VSYNC position MSBs VS_POS[11:8];
45-47		C9	RW	RSVD
48	BLCOpt1	00	RW	BLC control option 1 BLCopt1[7:4]: RSVD BLCopt1 [3:2]: "00": HCLK = SYS_CLK / 4 "01": HCLK = SYS_CLK / 2 "10" or "11": HCLK = SYS_CLK. BLCopt1[1:0]:

				"00": SRAM_CLK = SYS_CLK /4, FiFo_CLK = FiFo_SYS_CLK/4 "01": SRAM_CLK = SYS_CLK /2, FiFo_CLK = FiFo_SYS_CLK/2 "10" or "11": SRAM_CLK = SYS_CLK, , FiFo_CLK = FiFo_SYS_CLK
49	BLC_TGT	04	RW	Black level calibration target level. BLC_TGT[7]: sign bit."0" positive; "1" negative BLC_TGT[6:0]: target level.
4A	BLCCtrl	03	RW	BLC control BLCCtrl[7]: BLC_B bit 10 BLCCtrl[6]: BLC_Gb bit 10 BLCCtrl[5]: BLC_Gr bit 10 BLCCtrl[4]: BLC_R bit 10 BLCCtrl[3:2]: reserved BLCCtrl[1]: BLC action option. "0": Sensor do BLC only when triggered. "1": always do BLC. BLCCtrl[0]: auto BLC function on/off selection. "0": sensor stop calculate black value. "1": sensor calculates black value automatically.
4B	BLC_B	00	RW	B channel black value LSBs. BLC_B[7:0]
4C	BLC_Gb	00	RW	Gb channel black value LSBs. BLC_Gb[7:0]
4D	BLC_Gr	00	RW	Gr channel black value LSBs. BLC_Gr[7:0]
4E	BLC_R	00	RW	R channel black value LSBs. BLC_R[7:0]
4F	BLC_H	00	RW	Black value MSBs. {BLC_R[9:8],BLC_Gr[9:8],BLC_Gb[9:8],BLC_B[9:8]}
50-5E			RW	RSVD
5F	DAC_Pll0	01	RW	DAC PLL control 0 DACPLL0[7]: DAC PLL bypass on/off selection; 1: Bypass on, 0: By pass off DACPLL0[6:4]: RSVD DACPLL0[3:2]: DAC PLL post divider bypass on/off selection; 1: Bypass on, 0: By pass off DACPLL0[1:0]: DAC PLL pre- divider DAC_CLK=input clock/(DAC PLL pre-divider + 1) * DAC PLL VCO multiplier / (DAC PLL post divider + 1)
60	DAC_Pll1	1C	RW	DAC PLL control 1 DACPLL1[7:6]: RSVD DACPLL1[5:0]:DAC PLL VCO multiplier
61 – 64			RW	RSVD
65	RAMP3	07	RW	RAMP3 [7:4]: reserved. RAMP3 [3:0]: Second stage black sun reference control. Strength: (Strong) 1,0,F,E,D,C,B,A,9,8,7,6,5,4,3,2. (Weak)
66	PWC0	08	RW	PWC5[7:6]: RSVD PWC5[5:4]: D-phy Lp high voltage reference voltage control; 00- min, 11- max. PWC5[3:0]: RSVD;
67-68	RSVD		RW	RSVD
69	PWC3	74	RW	PWC3[7:4]: RSVD; PWC3[3]: Second stage black sun switch on/off enable, "0": always off. "1": Black sun will switch to second stage when analog gain greater than 2x. PWC3[2:0]: RSVD;
6A	PWC4	3A	RW	Power control 4 PWC4[7:4]: reserved PWC4[3:0]: first stage black sun control. Strength : (Strong) 1,0,F,E,D,C,B,A,9,8,7,6,5,4,3,2. (Weak)

6B	DPHY1	00	RW	Mipi PHY control 1 DPHY1[7:6]: MPCKSkew[1:0] DPHY1[5:4]:HSCKSkew[1:0] DPHY1[3:2]CKSkew[1:0] Clock Lane Skew Control : 00:Min, .. 11:max. DPHY1[1:0]:D0Skew[1:0]
6C	DPHY2	00	RW	DPHY2[7]: Mipi interface power down. “0”: enable ;”1” normal mode DPHY2[6:5]:RSVD DPHY2[4]: Second data lane disable on/off selection “0”: enable “; 1”: disable; DPHY2[3:2]Pg_Vcm[1:0] D-phy Hs Tx output voltage control 01:min, 00,11,10 : max DPHY2[1:0]:D1Skew[1:0]
6D	DPHY3	02	RW	DPHY3[7:3]:RSVD DPHY3[2]: Mipi data lane 1 disable on/off selection; 1” :disable; “0”: enable DPHY3[1:0]: RSVD
6E -6F	DPHY4	0C	RW	RSVD
70	Mipi1	49	RW	Mipi timing control 1 Mipi1[7:5]: Tlpx Mipi1[4:2]: Tck-pre Mipi1[1]: Mipi 8/10 bit mode switch, “0”: 10-bit, “1”: 8-bit mode Mipi1[0]: reserved
71	Mipi2	8A	RW	Mipi timing control 2 Mipi2[7:5]: Ths-zero Mipi2[4:0]: Tck-zero
72	Mipi3	68	RW	Mipi timing control 3 Mipi3[7:5]: Ths-prepare Mipi3[4:0]: Tck-post
73	Mipi4	33	RW	Mipi timing control 4 Mipi4[7]: Mipi pixel clock option Mipi4[6:4]: Ths-trail Mipi4[3:0]: Tck-trail
74	Mipi5	53	RW	Mipi timing control 5 Mipi5[7:3]: reserved Mipi5[2]: Mipi byte clock revise Mipi5[1]: Mipi continues mode or strobe mode selection “1” free run; “0” Normal; Mipi5[0]: Mipi interface sleep on/off Mipi should wait a complete frame than enter sleep mode. “1” Sleep mode enable; “0” Normal;
75	Mipi6	2B	RW	Mipi data type ID;
76	Mipi7	60	RW	Mipi word count LSBs
77	Mipi8	09	RW	Mipi word count MSBs
78	Mipi9	14	RW	Mipi timing control 9 Mipi9[7]: CK-pre-timing option 0: Auto; 1 Manual Mipi9[6:0]: Mipi TX start point adjust related to DVP HREF and internal FIFO
79-7F				RSVD
80	DigData	00	RW	DigData[7]: frame sync function enable DigData[6]: DVP data output sequence adjust DigData[5:0]: RSVD
81-85				RSVD
86	DPHY5	00	RW	DPHY5[7:6]: Mipi high speed clock input skew adjust

				DPHY5[5:4]: Mipi data lane 1 clock delay adjust DPHY5[3:2]: Mipi data lane 0 clock delay adjust DPHY5[1:0]: Mipi clock lane clock delay adjust
87-89				RSVD
8A		00	RW	[7:2]: RSVD [1]: Precharge off/on, “0”: normal, “1”: no precharge [0]: RSVD
8B-8F				RSVD
C0	Group0	0A	RW	Group write 1st data address
C1	Group1	0A	RW	Group write 1st data value.
C2	Group2	0A	RW	Group write 2nd data address
C3	Group3	0A	RW	Group write 2nd data value.
…	…	…	…	…
FE	Group62	0A	RW	Group write 32nd data address
FF	Group63	0A	RW	Group write 32nd data value.

Document Revision Control

Version Number #	Date Released	Comments
R0.0	Jan 06,2019	Initial release of JX-F37 preliminary datasheet
R0.1	Mar 05,2019	Update TSV package, Register info.