



# SSC338D/SSC338Q High-Integrated IP Camera SoC Processor

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Preliminary Product Brief Version 0.8



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## REVISION HISTORY

Revision No.	Description	Date
0.1	<ul style="list-style-type: none"> <li>Initial release</li> </ul>	01/17/2020
0.2	<ul style="list-style-type: none"> <li>Added DLA function</li> </ul>	03/02/2020
0.3	<ul style="list-style-type: none"> <li>Updated Features</li> <li>Updated Mechanical Dimensions</li> </ul>	05/11/2020
0.4	<ul style="list-style-type: none"> <li>Updated CA7 Spec.</li> </ul>	05/29/2020
0.5	<ul style="list-style-type: none"> <li>Updated Features</li> <li>Added Interface Characteristics and Thermal Resistance Data</li> </ul>	09/28/2020
0.6	<ul style="list-style-type: none"> <li>Added Minimum Order Quantity and Moisture Sensitivity Level</li> </ul>	01/21/2021
0.7	<ul style="list-style-type: none"> <li>Updated audio spec. and I2C SDA Hold Time min. value</li> <li>Added Ambient Temperature during OTP programming</li> </ul>	04/26/2021
0.8	<ul style="list-style-type: none"> <li>Updated Recommended Operating Conditions</li> </ul>	06/30/2021

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## 1. CHIP OVERVIEW

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The SSC338D/SSC338Q series products are highly integrated multimedia System-on-Chip (SoC) products for high-resolution intelligent video recording applications like IP camera, CAR camera, and USB camera.

The chip includes a 32-bit dual-core RISC processor, advanced Image Signal Processor (ISP), high performance MJPEG/H.264/H.265 video encoder, Deep Learning Accelerator (DLA), Intelligent Video Engine (IVE), as well as high speed I/O interfaces like MIPI, and Ethernet.

Advanced low-power, low-voltage architecture and optimized design flow are implemented to fulfill long time usage applications. Hardwired AES/DES/3DES cipher engines are integrated to support secure boot, authentication, and video/audio stream encryption in security system.

The SSC338D/SSC338Q, powered by SigmaStar Technology, comes with a complete hardware platform and software SDK, allowing customers to speed up "Time-to-Market."

## 2. BLOCK DIAGRAM

Figure 2-1 shows the major functional blocks of SSC338D/SSC338Q series chip.

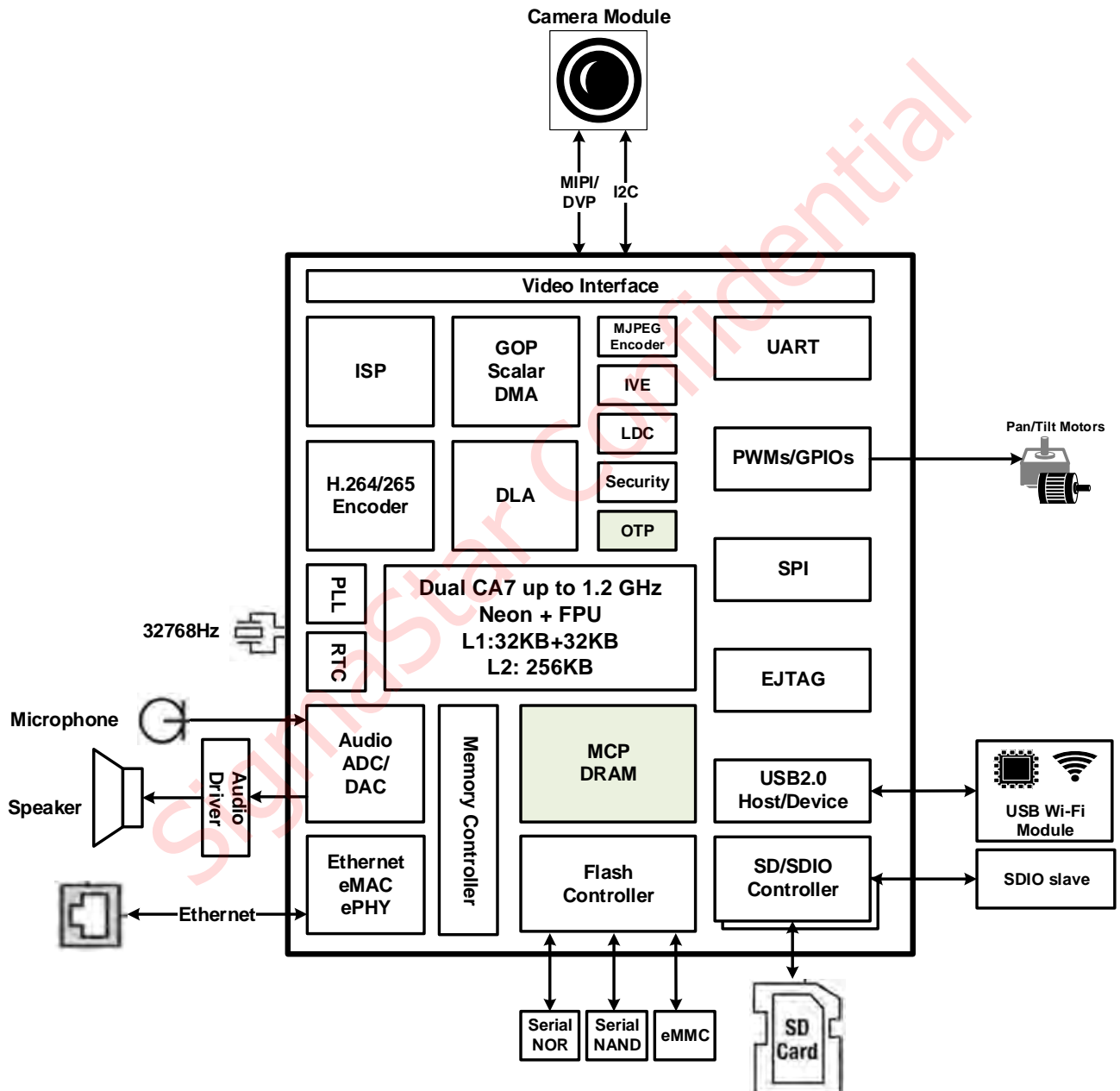


Figure 2-1: SSC338D/SSC338Q Block Diagram

### 3. FEATURES

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#### ■ High Performance Processor Core

- ARM Cortex-A7 Dual Core
- Clock rate up to 1.2GHz
- Neon and FPU
- Memory Management Unit for Linux support
- DMA Engine

#### ■ Image/Video Processor

- Supports 8/10/12-bit parallel interface for raw data input
- Supports MIPI interface with 2/4 data lanes and 1 clock lane
- Supports one MIPI interface
- Supports sensor interface with both parallel and MIPI
- Supports 8/10-bit CCIR656 interface
- Supports max. 4K (3840x2160) pixels video recording and image snapshot
- Bad pixel compensation
- Temporal-domain Noise Reduction (3DNR)
- Bayer domain Spatial-domain Noise Reduction (2DNR)
- Bayer domain filter to remove purple false color in highlight regions
- Optical black correction
- Lens shading compensation
- Auto White Balance (AWB) / Auto Exposure (AE) / Auto Focus (AF)
- CFA color interpolation
- Color correction
- Gamma correction
- Video stabilization
- High Dynamic Range (HDR) with two exposure frames and de-ghost function
- Frame buffer data compression and de-compression to save memory bandwidth
- Wide Dynamic Range (WDR) with local tone mapping

- Flip, Mirror, and Rotation with 90 or 270 degree
- Lens distortion correction (LDC/FishEye)
- Rolling shutter compensation
- Fully programmable multi-function scaling engines

#### ■ Advanced Color Engine

- Luma gain/offset adjustment
- Supports 2D peaking with user definition filter
- Horizontal noise masking
- Direct Luma Correction (DLC)
- Black/White Level Extension (BLE/WLE)
- IHC/ICC/IBC for chroma adjustment
- Histogram statistics
- Spatial domain IIR filter to reduce noise

#### ■ H.265/HEVC

- Supports H.265/HEVC main profile
- Supported Prediction Unit (PU) size: 32x32, 16x16, 8x8
- Supported Transform Unit (TU) size: 32x32 to 4x4
- Search range [H: +/-128, V: +/-64]
- Supports up to quarter-pixel
- Supports frame level and MB level rate control
- Supports ROI encoding with custom QP map
- Supports max. 4K with 20 fps encoding

#### ■ H.264 Encoder

- Supports H.264 baseline, constrained baseline, main, and high profile
- Supports 16x16, 8x8 and 4x4 block sizes
- Search range [H: +/-64, V: +/-32]
- Supports up to quarter-pixel
- Supports frame level and MB level rate control
- Supports ROI encoding with custom QP map
- Supports max. 4K with 20 fps encoding

#### ■ JPEG Encoder

- Supports JPEG baseline encoding
- Supports YUV422 or YUV420 formats
- Supports max. 4K with 20 fps encoding
- Supports real-time mode and frame encode mode

#### ■ Video Encoding Performance

- Supports 4K + HD + D1 20fps H.265/HEVC encoding
- Supports 4K + HD + D1 20fps H.264 encoding
- Supports MJPEG up to 4K 20 fps encoding

#### ■ Deep Learning Accelerator

- Pure hardwired accelerator
- Supports various video analysis functions like FD/FR, human detection, MD/OD, object tracking, etc.

#### ■ Audio Processor

- One stereo ADC for microphone input
- 2-pin DMIC input
- One mono DAC for lineout
- Supports 8K/16K/32KHz/48KHz sampling rate audio recording
- Digital and analog gain adjustment
- I2S digital audio input and output with TDM up to 8-ch input and 2-ch output

#### ■ NOR/NAND Flash Interface

- Compliant with standard, dual and quad SPI Flash memory components
- High speed clock/data rate up to 108MHz

#### ■ SD Card/eMMC Interface

- Compatible with SD spec. 2.0, data bus 1/4 bit mode
- Supports eMMC 4.3 interface

#### ■ SDIO 2.0 Interface

- Compatible with SDIO spec. 2.0, data bus 1/4 bit mode
- Compatible with SD spec. 2.0, data bus 1/4 bit mode

#### ■ USB Interface

- One USB 2.0 configurable host or device
  - Host mode supports EHCI specification
  - Device mode supports up to 8 endpoints
- Supports suspend/hibernation/wake-up power saving mode

#### ■ DRAM Memory

- Embedded 1Gb or 2Gb 16-bit DDR3 memory with max. 2133Mbps

#### ■ Connectivity

- Built-in 10/100M Ethernet MAC and Ethernet PHY
- USB 2.0 Host Controller could be used for USB Wi-Fi Dongle or Module
- **One** SDIO 2.0 Host Controller could be used for SDIO Wi-Fi module
- Supports Wake-on-LAN (WOL)
- Supports BT.656 8-bit output with max. 75MHz clock rate (single clock edge)
- Supports BT.656 YUV422 format and progressive mode

#### ■ Security Engines

- Supports AES/DES/3DES/RSA/SHA-1/SHA-256
- Supports secure booting

#### ■ Real Time Clock (RTC)

- Built-in RTC working with 32.768 KHz crystal
- Alarm interrupt for wakeup
- Tick time interrupt (millisecond)
- Built-in regulator
- Supports low leakage RTC-mode for long battery application

#### ■ Peripherals

- Dedicated GPIOs for system control
- Supports max. 11 PWM outputs
- Three generic UARTs and one fast UART with flow control
- Three generic timers and one watchdog timer
- Two SPI masters
- Four I2C Masters
- Built-in SAR ADC with 4-channel analog inputs for different kinds of applications
- Supports internal temperature sensor

#### ■ Operating Voltage Range

- Core: Typ. 0.9V
- I/O: 1.8/3.3V
- DRAM: 1.5V (DDR3) or 1.35V (DDR3L)
- Power Consumption: TBD

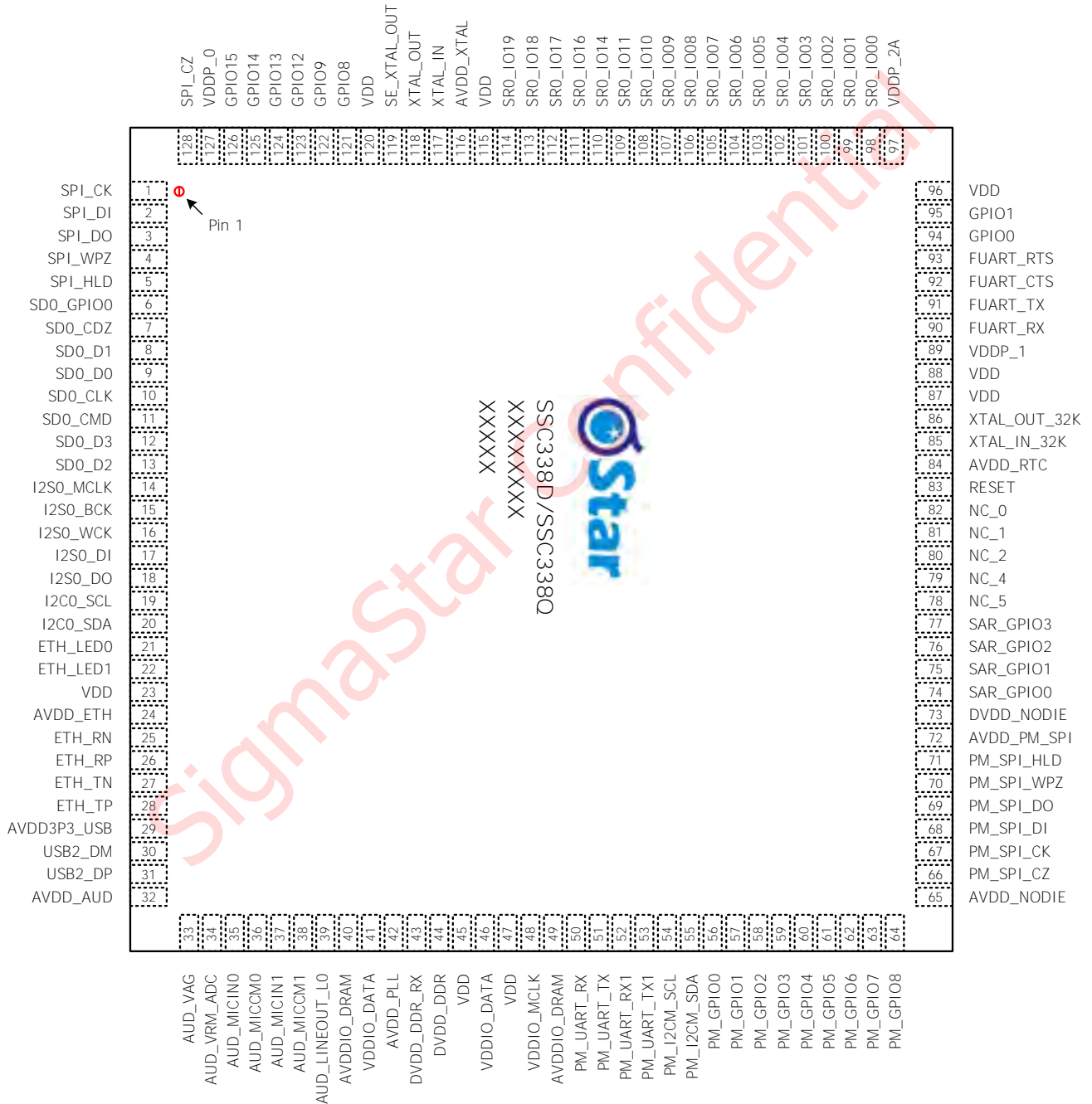
#### ■ Package

- QFN with 128 pins, 12.3mm x 12.3mm
- Moisture Sensitivity Level: 3



## 4. PACKAGE DESCRIPTION

### 4.1. Pin Diagram



## 4.2. Signal Description

Signal Name	Signal Type	Function	QFN128 Pin Location
System Reset Interface			
RESET	I	System Reset (Active High)	83
Debug UART Interface			
PM_UART_RX	I	Debug UART Receive Data Input with Pull Up Resistor / Slave I2C Serial Clock	50
PM_UART_TX	O	Debug UART Transmit Data Output with Pull Up Resistor / Slave I2C Serial Data	51
PM_UART_RX1	I	PM_UART1 Receive Data Input with Pull Up Resistor in Power Manage group domain	52
PM_UART_TX1	O	PM_UART1 Transmit Data Output with Pull Up Resistor in Power Manage group domain	53
System Interface			
XTAL_IN	I	24MHz Crystal Input	117
XTAL_OUT	O	24MHz Crystal Output	118
XTAL_IN_32K	I	32.768KHz Crystal Input	85
XTAL_OUT_32K	O	32.768KHz Crystal Output	86
SE_XTAL_OUT	O	24MHz Clock Output	119
8051 SPI Flash Interface			
PM_SPI_CZ	O	SPI Flash Chip Select (Active Low)	66
PM_SPI_CK	O	SPI Flash Clock	67
PM_SPI_DI	O	SPI Flash Serial Data To Device (MOSI)	68
PM_SPI_DO	I	SPI Flash Serial Data From Device (MISO)	69
PM_SPI_WPZ	O	SPI Flash Write Protect	70
PM_SPI_HLD	O	SPI Flash Hold	71
GPIO Interface			
GPIO0	I/O	General Purpose Input/Output 0	94
GPIO1	I/O	General Purpose Input/Output 1	95
GPIO8	I/O	General Purpose Input/Output 8	121
GPIO9	I/O	General Purpose Input/Output 9	122
GPIO12	I/O	General Purpose Input/Output 12	123
GPIO13	I/O	General Purpose Input/Output 13	124

Signal Name	Signal Type	Function	QFN128 Pin Location
GPIO14	I/O	General Purpose Input/Output 14	125
GPIO15	I/O	General Purpose Input/Output 15	126
PM GPIO Interface			
PM_GPIO0	I/O	Power Manage Group General Purpose Input/Output 0	56
PM_GPIO1	I/O	Power Manage Group General Purpose Input/Output 1	57
PM_GPIO2	I/O	Power Manage Group General Purpose Input/Output 2	58
PM_GPIO3	I/O	Power Manage Group General Purpose Input/Output 3	59
PM_GPIO4	I/O	Power Manage Group General Purpose Input/Output 4	60
PM_GPIO5	I/O	Power Manage Group General Purpose Input/Output 5	61
PM_GPIO6	I/O	Power Manage Group General Purpose Input/Output 6	62
PM_GPIO7	I/O	Power Manage Group General Purpose Input/Output 7	63
PM_GPIO8	I/O	Power Manage Group General Purpose Input/Output 8	64
SAR ADC Interface			
SAR_GPIO0	I	General Purpose Input/Output or Muxed to SARADC Input Channel 0	74
SAR_GPIO1	I	General Purpose Input/Output or Muxed to SARADC Input Channel 1	75
SAR_GPIO2	I	General Purpose Input/Output or Muxed to SARADC Input Channel 2	76
SAR_GPIO3	I	General Purpose Input/Output or Muxed to SARADC Input Channel 3	77
CA7 SPI Flash Interface			
SPI_CZ	O	Master SPI Chip Select (Active Low)	128
SPI_CK	O	Master SPI Serial Clock	1
SPI_DI	I/O	Master SPI Serial Data To Device (MOSI) / SDIO0 - 4x IO mode	2
SPI_DO	I/O	Master SPI Serial Data From Device (MISO) / SDIO1 - 4x IO mode	3
SPI_WPZ	I/O	Master SPI Write Protect (Active Low) / SDIO2 - 4x IO mode	4
SPI_HLD	I/O	Master SPI Hold input (Active Low) / SDIO3 - 4x IO mode	5

Signal Name	Signal Type	Function	QFN128 Pin Location
I2S Interface			
I2S0_MCLK	O	I2S Master Clock	14
I2S0_BCK	O	I2S Bit Clock	15
I2S0_WCK	O	I2S Word Clock	16
I2S0_DI	I	I2S Data Input	17
I2S0_DO	O	I2S Data Output	18
Master I2C Interface			
I2C0_SCL	O	Non-PM Domain I2C 0 Master I2C Clock	19
I2C0_SDA	I/O	Non-PM Domain I2C 0 Master I2C Data	20
PM_I2CM_SCL	O	PM Domain I2C Master I2C Clock	54
PM_I2CM_SDA	I/O	PM Domain I2C Master I2C Data	55
Fast UART Interface			
FUART_RX	I	Fast UART Receive Data Input	90
FUART_TX	O	Fast UART Transmit Data Output	91
FUART_CTS	I	Fast UART Clear to Send	92
FUART_RTS	O	Fast UART Request to Send	93
Image Sensor Interface			
SR0_IO00	I/O	Sensor General Purpose Input/Output 0	98
SR0_IO01	I/O	Sensor General Purpose Input/Output 1	99
SR0_IO02	I/O	Sensor General Purpose Input/Output 2	100
SR0_IO03	I/O	Sensor General Purpose Input/Output 3	101
SR0_IO04	I/O	Sensor General Purpose Input/Output 4	102
SR0_IO05	I/O	Sensor General Purpose Input/Output 5	103
SR0_IO06	I/O	Sensor General Purpose Input/Output 6	104
SR0_IO07	I/O	Sensor General Purpose Input/Output 7	105
SR0_IO08	I/O	Sensor General Purpose Input/Output 8	106
SR0_IO09	I/O	Sensor General Purpose Input/Output 9	107
SR0_IO10	I/O	Sensor General Purpose Input/Output 10	108
SR0_IO11	I/O	Sensor General Purpose Input/Output 11	109
SR0_IO14	I/O	Sensor General Purpose Input/Output 14	110
SR0_IO16	I/O	Sensor General Purpose Input/Output 16	111

Signal Name	Signal Type	Function	QFN128 Pin Location
SR0_IO17	I/O	Sensor General Purpose Input/Output 17	112
SR0_IO18	I/O	Sensor General Purpose Input/Output 18	113
SR0_IO19	I/O	Sensor General Purpose Input/Output 19	114
10/100M Ethernet Interface			
ETH_RN	I	10/100M Ethernet Differential Pair of Receiver Signal Negative	25
ETH_RP	I	10/100M Ethernet Differential Pair of Receiver Signal Positive	26
ETH_TN	O	10/100M Ethernet Differential Pair of Transmitter Signal Negative	27
ETH_TP	O	10/100M Ethernet Differential Pair of Transmitter Signal Positive	28
ETH_LED0	O	10/100M Ethernet LED0 Control Driven Active When Linked	21
ETH_LED1	O	10/100M Ethernet LED1 Control Driven Active When Linked in 100 Base-TX and Blinking When Transmitting or Receiving Data	22
SD 2.0 Card Interface			
SD0_CLK	O	SD 2.0 Clock	10
SD0_CMD	O	SD 2.0 Command	11
SD0_D0	I/O	SD 2.0 Data Bus 0	9
SD0_D1	I/O	SD 2.0 Data Bus 1	8
SD0_D2	I/O	SD 2.0 Data Bus 2	13
SD0_D3	I/O	SD 2.0 Data Bus 3	12
SD0_CDZ	I	Power Manage SD 2.0 Card Detect	7
SD0_GPIO0	I/O	SD0 General Purpose Input/Output 0	6
Audio Line Out Interface			
AUD_LINEOUT_L0	O	Audio Left Channel Line Output	39
AUD_VAG	O	Audio Reference Voltage from 1/2 AVDD_AUD	33
AUD_VRM_ADC	I	Audio Reference Voltage for ADC	34
Analog Microphone Interface			
AUD_MICIN0	I	Audio Left Channel Microphone Positive Input	35
AUD_MICCM0	I	Audio Left Channel Microphone Negative Input	36
AUD_MICIN1	I	Audio Right Channel Microphone Positive Input	37
AUD_MICCM1	I	Audio Right Channel Microphone Negative Input	38

Signal Name	Signal Type	Function	QFN128 Pin Location
USB 2.0 Interface			
USB2_DM	I/O	USB 2.0 Differential Pair, Negative	30
USB2_DP	I/O	USB 2.0 Differential Pair, Positive	31
Test Interface			
NC_0	I/O	RTC Test Pin (NC)	82
NC_1	I/O	RTC Test Pin (NC)	81
NC_2	I/O	RTC Test Pin (NC)	80
NC_4	I/O	RTC Test Pin (NC)	79
NC_5	I/O	RTC Test Pin (NC)	78
Power pins			
VDD	Core Power	Digital Core Power	23, 45, 47, 87, 88, 96, 115, 120
VDDP_0	3.3V Power	Digital Input/Output Power for Domain 0	127
VDDP_1	1.8/3.3V Power	Digital Input/Output Power for Domain 1	89
VDDP_2A	1.8/3.3V Power	Digital Input/Output Power for Domain 2A (Sensor IO Group 0 Power)	97
DVDD_DDR_RX	Core Power	Digital Power for DDR RX LDO (0.1uF CAP to GND)	43
DVDD_DDR	Core Power	Digital Power for DDR TX	44
VDDIO_DATA	DDR Power	IO Power for DDR Data	41, 46
VDDIO_MCLK	DDR Power	IO Power for DDR Clock	48
AVDDIO_DRAM	DDR Power	IO Power for embedded DRAM	40, 49
AVDD_NODIE	3.3V Power	Analog Power for PM Domain	65
DVDD_NODIE	Output	PM Domain LDO Output (1uF Cap to GND)	73
AVDD_PM_SPI	3.3V Power	Analog Power for PM SPI Domain	72
AVDD_PLL	3.3V Power	Analog Power for PLL	42
AVDD_XTAL	3.3V Power	Analog Power for XTAL	116
AVDD_RTC	3.3V Power	Analog Power for RTC	84
AVDD3P3_USB	3.3V Power	Analog Power for USB2.0	29
AVDD_ETH	3.3V Power	Analog Power for Ethernet	24
AVDD_AUD	3.3V Power	Analog Power for Audio	32
GND	GND	Ground	ePad

Note: E-pad has to connect to system GND net.

## 5. ELECTRICAL CHARACTERISTIC

### 5.1. Interface Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
DIGITAL INPUTS					
Input Voltage, High	$V_{IH}$	$V_{DDP} \times 0.7$ <sup>Note</sup>			V
Input Voltage, Low	$V_{IL}$			$V_{DDP} \times 0.2$ <sup>Note</sup>	V
Input Current, High	$I_{IH}$			-1.0	uA
Input Current, Low	$I_{IL}$			1.0	uA
Input Capacitance			5		pF
DIGITAL OUTPUTS					
Output Voltage, High	$V_{OH}$	$V_{DDP} - 0.1$ <sup>Note</sup>			V
Output Voltage, Low	$V_{OL}$			0.1	V
SAR ADC Input		0		3.3	V
AUDIO OUTPUTS					
Line-Out			2.54		Vp-p
24MHz XTAL Specifications					
Input Voltage, High	$V_{IH}$	2.0		3.6	V
Input Voltage, Low	$V_{IL}$	-0.3		0.8	V
Clock frequency			24		MHz
Crystal accuracy			+/-30		ppm
Long-term jitter			+/-500		ps
32KHz XTAL Specifications					
XIN Vswing	$V_{swing}$	140			mV
XOUT Vswing	$V_{swing}$	175			mV
Crystal accuracy				20	ppm

Note: VDDP typical voltage is 3.3V or 1.8V



## 5.2. Absolute Maximum Ratings

Parameter	Symbol	Min	Typ.	Max.	Unit
Core Power Supply Voltage	VDD	-0.3		1.26	V
3.3V I/O Supply Voltage	VDDP_0 AVDD_PM_SPI	-0.3		3.63	V
1.8/3.3V I/O Supply Voltage	VDDP_1 VDDP_2A	-0.3		3.63	V
DDR Digital Power Supply Voltage	DVDD_DDR*	-0.3		1.26	V
DDR IO Power Supply Voltage (DDR3/L)	VDDIO_* AVDD*_DRAM	-0.3		1.8	V
PM IO Power Supply Voltage	AVDD_NODIE	-0.3		3.63	V
3.3V Analog Power Supply Voltage	AVDD*	-0.3		3.63	V
0.9V Analog Power Supply Voltage	AVDDL*	-0.3		1.26	V
Storage Temperature	T <sub>STG</sub>	-40		150	°C

Note: Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and does not imply functional operation of device. Exposure to absolute maximum ratings for extended periods may affect device reliability.

## 5.3. Recommended Operating Conditions

Parameter	Description	Min.	Typ.	Max	Unit
VDD	Digital Core Power	0.87	0.9	1.05	V
VDDP_0	Digital Input/Output Power for Domain 0	2.97	3.3	3.63	V
VDDP_1	Digital Input/Output Power for Domain 1	2.97	3.3	3.63	V
	Digital Input/Output Power for Domain 1	1.62	1.8	1.98	V
VDDP_2A	Digital Input/Output Power for Domain 2A (Sensor IO Group 0 Power)	2.97	3.3	3.63	V
	Digital Input/Output Power for Domain 2A (Sensor IO Group 0 Power)	1.62	1.8	1.98	V
DVDD_DDR_RX	Digital Power for DDR RX LDO (0.1uF CAP to GND)	TBD	0.9	TBD	V
DVDD_DDR	Digital Power for DDR TX	TBD	0.9	TBD	V
VDDIO_DATA	(DDR3) IO Power for DDR Data	1.45	1.5	1.55	V
VDDIO_MCLK	(DDR3) IO Power for DDR Clock	1.45	1.5	1.55	V
AVDDIO_DRAM	(DDR3) IO Power for embedded DRAM	1.45	1.5	1.55	V
AVDD_NODIE	Analog Power for PM Domain	2.97	3.3	3.63	V
DVDD_NODIE	PM Domain LDO Output (1uF Cap to GND)	TBD	0.9	TBD	V
AVDD_PM_SPI	External power supply for 3.3V IO	2.97	3.3	3.63	V
AVDD_PLL	Analog Power for PLL	3.14	3.3	3.46	V

Parameter	Description	Min.	Typ.	Max	Unit
AVDD_XTAL	Analog Power for XTAL	3.14	3.3	3.46	V
AVDD_RTC	Analog Power for RTC	1.6	3	3.6	V
AVDD3P3_USB	Analog Power for USB2.0	3.14	3.3	3.46	V
AVDD_ETH	Analog Power for Ethernet	3.14	3.3	3.46	V
AVDD_AUD	Analog Power for Audio	3.14	3.3	3.46	V
Junction Temperature	Main Die			125	°C
	DDR3 Die			125	
Ambient Temperature during OTP programming		0		125	°C

## 6. THERMAL RESISTANCE

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### 6.1. Thermal simulation mode

PCB condition: JEDEC JESD51-5

PCB layers: 4L

PCB dimensions: 76.2 x 114.3 (mm x mm)

PCB thickness: 1.6 (mm)

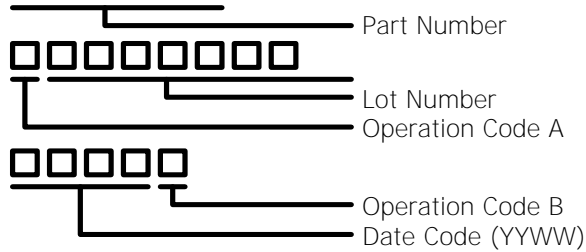
Part Number	Package		Thermal Resistance (°C/W)	
		PCB Layer	$\theta_{JA}$	$\theta_{JC}$
SSC338D/SSC338Q	QFN128_12.3x12.3	4L PCB	25.4	7.6

## 7. ORDERING GUIDE

Part Number	Temperature Range	Package Description	Package Option	Minimum Order Quantity
SSC338D/SSC338Q	-20°C to +60°C	QFN	128	1216ea

### 7.1. Marking Information

SSC338D/SSC338Q



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Electrostatic charges accumulate on both test equipment and human body and can discharge without detection. SSC338D/SSC338Q comes with ESD protection circuitry; however, the device may be permanently damaged when subjected to high energy discharges. The device should be handled with proper ESD precautions to prevent malfunction and performance degradation.