General Description:

JX-H65 is an HD CMOS image sensor designed and fabricated with SOI's 3.75um pixel technology . It can deliver images at 60fps in 960P mode and 30fps in HDR mode.

The JX-H65 consists of a 1292 x 968 active pixel sensor (APS) array with on-chip 10-bit ADC, programmable gain control (PGA), and correlated double sampling (CDS) to significantly reduce fixed pattern noise (FPN). The sensor also has many standard programmable and automatic functions. It has both the industry compliant DVP parallel and MIPI CSI2 dual-data lane serial interfaces. The external host controller can access this device through a standard serial interface.

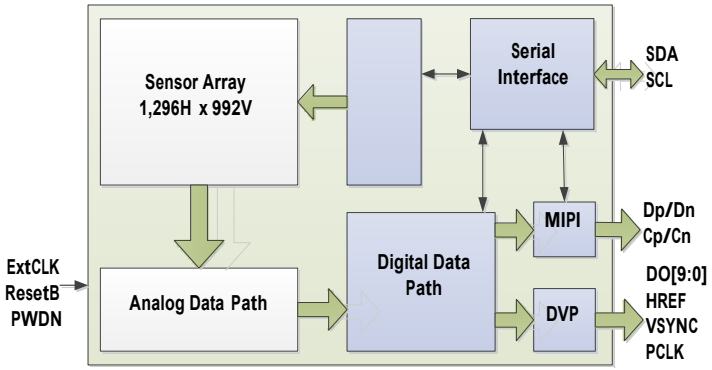
It is available in wafer-level packaged CSP.

Features:

- Automatic functions:
  - o ABLC – Automatic Black Level Calibration
- Programmable controls:
  - o Gain, exposure, frame rate and size
  - o Image mirror and flip
  - o Window panning and cropping
  - o Column and row sub-sampling or binning
  - o I2C slave ID
- Output formats:
  - o DVP parallel interface
  - o MIPI CSI2 (dual lane)
- Data formats:
  - o 10-bit RAW RGB
- HDR mode support
- Others
  - o 50/60Hz flick noise cancellation
  - o Frame sync
  - o Register group write capability
  - o Black sun spot cancellation

Optical format		1/3"
Active Pixels		1292H x 968V
Pixel size		3.75 x 3.75 µm
Color filter array		RGB Bayer pattern
Chief Ray Angle		9 degrees linear
Shutter type		Electronic rolling shutter
Maximum Frame Rate		Full: 1280x960 @60fps HDR: 1280x960@30fps, 2 frame staggered output
Supply voltage	**Digital**	1.35 – 1.65V (1.5V nominal, With embedded 1.5V regulator)
	Analog	2.6 – 3.0V (2.8V nominal)
	I/O	1.7 – 3.45V (1.8V nominal)
Power consumption	**Active**	55 mA
	Standby	TBD uA
Output Formats		10-bit RGB Raw Data
Sensitivity		TBD mV/lux-sec
Max SNR		TBD db
Dynamic range		TBD db
Dark Current		< TBD mV/sec @ 45 ˚C
Operating junction temperature		-30 ˚C to 85 ˚C
Stable image junction temperature		60 ˚C

Functional Block:



Component Order Information:

Part Number	Description
JX-H65-C1-D3	CSP,DVP @ 30fps

Key Specifications:

Contents

Pin Diagram:

JX-H65's pin diagram is shown in Figure 1 and each pin's description is shown in Table 1:

Figure 1: JX-H65 CSP top view

Table 1: Pin Description

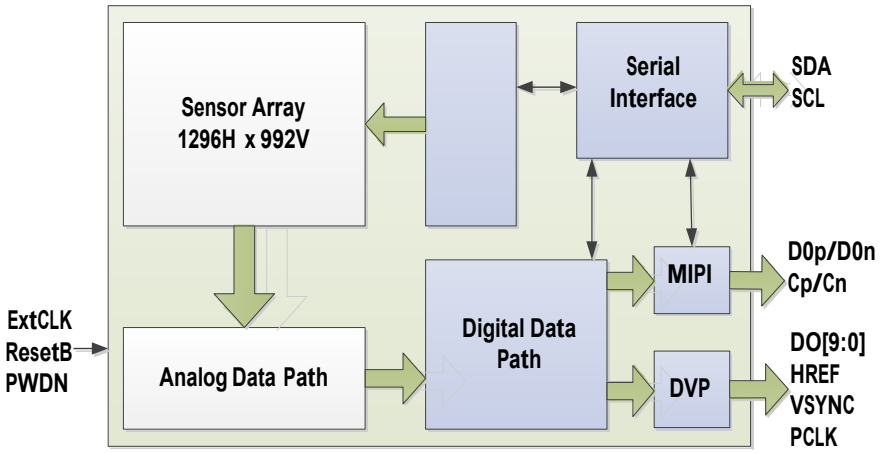
Pin number	Pin name	Pin type	Description
A1	AGND	Supply	Analog ground.
A2	D5	I/O	DVP data output bit 5.
A3	D8	I/O	DVP data output bit 8.
A4	HREF	I/O	Line data valid signal output.
A5	DVDD	Supply	Digital core supply voltage.(with embedded 1.5V regulator)
A6	PWDN	Input	Chip power down initiate pin. High active.
A7	NC		No connection.
A8	AGND	Supply	Analog ground.
B1	AVDD	Supply	Analog supply voltage.
B2	DOGND	Supply	Digital I/O ground.
B3	D7	I/O	DVP data output bit 7.
B4	DOVDD	Supply	Digital I/O supply voltage.
B5	SDA	I/O	Serial data, pull to DOVDD with a 4.3k Ω resistor.
B6	SCL	Input	Serial interface clock input.
B7	DOGND	Supply	Digital I/O ground.
B8	AVDD	Supply	Analog supply voltage.
C1	DVDD	Supply	Digital core supply voltage.(with embedded 1.5V regulator)
C2	D6	I/O	DVP data output bit 6.
C3	D9	I/O	DVP data output bit 9.
C4	VSYNC	I/O	Vertical synchronize signal, drive high when last frame end and drive low before next frame start. Also can be programmed as frame synchronizes input.
C6	RSTB	Input	System synchronize reset when driven low, it resumes normal operation with all configuration register set to factory default.
C7	VH	Reference	Internal analog reference.
C8	VN	Reference	Internal analog reference.
D1	AVDD	Supply	Analog supply voltage.
D2	D4	I/O	DVP data output bit 4.
D3	D2	I/O	DVP data output bit 2.
D4	D1	I/O	DVP data output bit 1.
D5	MVDD	Supply	MIPI block supply voltage, connect to DVDD pin.
D6	DOGND	Supply	Digital I/O ground.
D7	AGND	Supply	Analog ground.
D8	DVDD	Supply	Digital core supply voltage. (with embedded 1.5V regulator)
E1	PCLK	I/O	DVP Pixel clock output.
E2	DVDD	Supply	Digital core supply voltage. (with embedded 1.5V regulator)
E3	DOVDD	Supply	Digital I/O supply voltage.
E4	EXCLK	Input	System clock input.
E5	MDP	I/O	MIPI data lane positive output.
E6	MCP	I/O	MIPI clock lane positive output.
E7	MCN	I/O	MIPI clock lane negative output.
E8	AVDD	Supply	Analog supply voltage.
F1	AGND	Supply	Analog ground.
F2	D3	I/O	DVP data output bit 3.
F3	DOGND	Supply	Digital I/O ground.
F4	D0	I/O	DVP data output bit 0.
F5	MDN	I/O	MIPI data lane negative output.

F6	MVDD	Supply	MIPI block supply voltage, connect to DVDD pin.
F7	DOGND	Supply	Digital I/O ground.
F8	DOVDD	Supply	Digital I/O supply voltage.

Functional Overview:

The JX-H65 is a progressive-scan CMOS image sensor. It has an on-chip, phase-locked loop (PLL) to generate internal clocks from a single master input clock running between 6 and 27MHz. Its analog data process and digital data process can handle up to 88Mp/s at corresponding pixel clock 88MHz. Figure 2 illustrates the sensor's block diagram.

Figure 2. Functional Block Diagram



User can access and program JX-H65 sensor internal registers through the two-wire serial bus. The core of the sensor is a 1296x992 pixel array. The timing and control circuitry sequences through the rows of the array, resetting and then reading each row in turn. In the time interval between resetting and reading that row, the pixels in the row integrate the incident light. The exposure is controlled by varying the time interval between reset and readout. Once a row has been read, the data from the columns is sequenced through an analog signal path to apply gain and analog signal to digital signal converter (ADC). The ADC output passes through a digital processing path for black level calibration. Then the data will output though a DVP port or MIPI CSI-2 standard interface.

Pixel Array Format:

The JX-H65 pixel array consists of a 1296-column by 992-row matrix of pixels addressed by column and row. The address (column 0, row 0) represents the upper-right corner of the entire array (please refer to Figure 3 for JX-H65's Pixel array structure). The first 20 rows are optical black row for black level calibration. Outside of the 1280x960 active pixels, there are several boundary pixels: 6 rows on top, 6 rows at the bottom, 8 columns on the right, and 8 columns on the left. The detailed pixel array arrangement and default read out direction is noted in the following two figures:

Figure 3: Pixel array structure

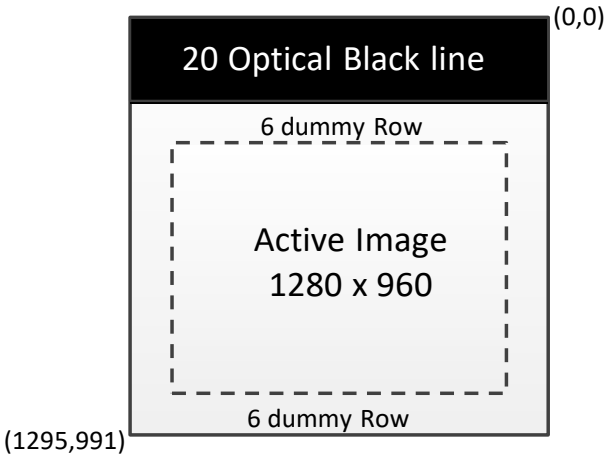
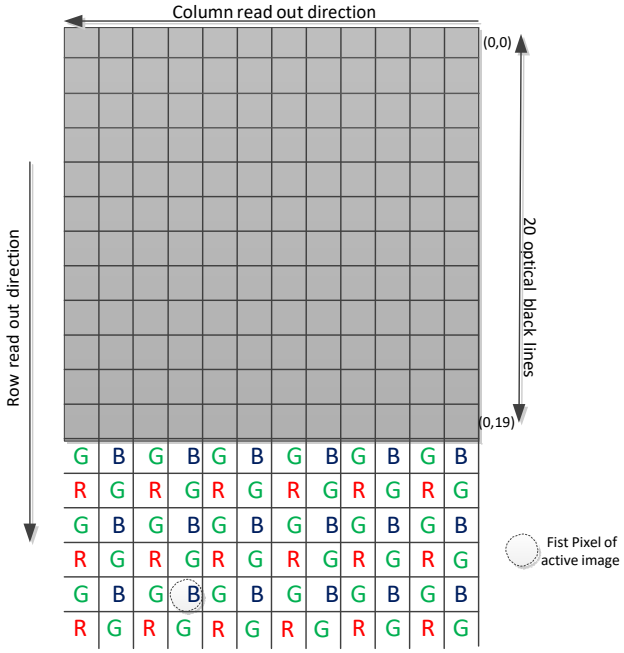


Figure 4: Pixel array detail with default read out direction.



Data Output Format:

The output images are divided into frames, which are further divided into lines. By default, the sensor produces 972 lines (rows) of 1296 columns each. The VSYNC and HREF signals indicate the boundaries between frames and lines, respectively. PCLK can be used as a clock to latch the data. For each PCLK cycle, one 10-bit pixel data outputs on the D[9:0] pins (Figure 5). The pixel data is valid when HREF signal is asserted. The VSYNC signal indicates frame end and new frame start. JX-H65 default frame timing is illustrated as figure 6.

Figure 5: Row data output timing

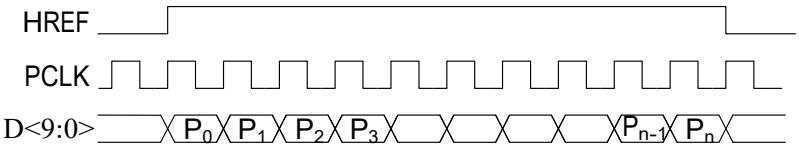
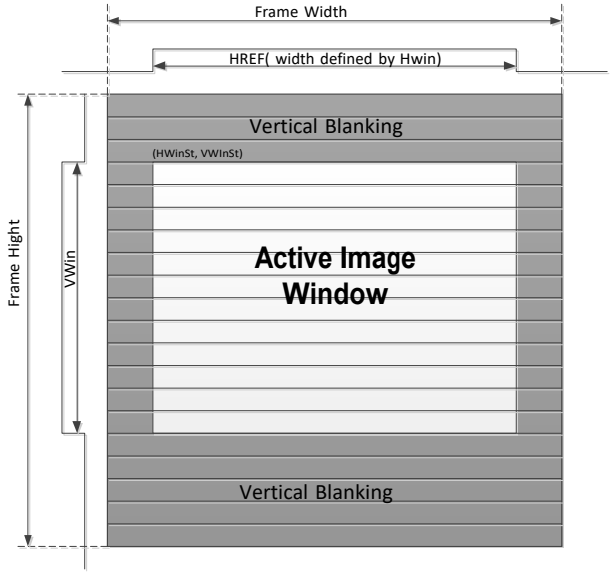


Figure 6: Default frame timing



As shown above in Figure 6, a line (row) period can be calculated as Trow = Frame_width * Thclk, and frame rate can be calculated as fps=1/(Frame_hight * Trow).

As default configuration, VSYNC, PCLK and Data are all valid at PCLK rising edge. For user convenience, JX-H65 provides register bits to control HREF, VSYNC and PCLK polarity. In addition, PCLK also have adjustable delay control.

For pixel Bayer pattern data output, several settings can have effect on pixel output sequences. These registers include HWIn_St, VWin_St, HAddr_St, Mirror, V_Flip. Please consult your SOI AE for further information.

HDR mode

JX-H65 support HDR mode, user can set 2 different exposure times and output 2 frame data (long and short exposure) in staggered output mode. Below is a diagram to illustrate frame output timing under this mode.

Figure 7: HDR frame timing in DVP output

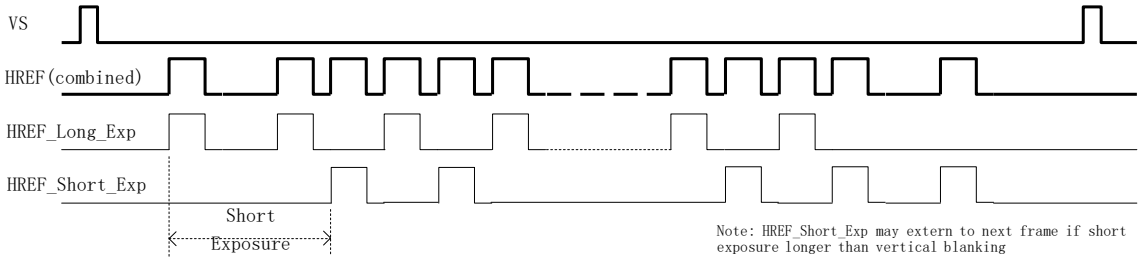
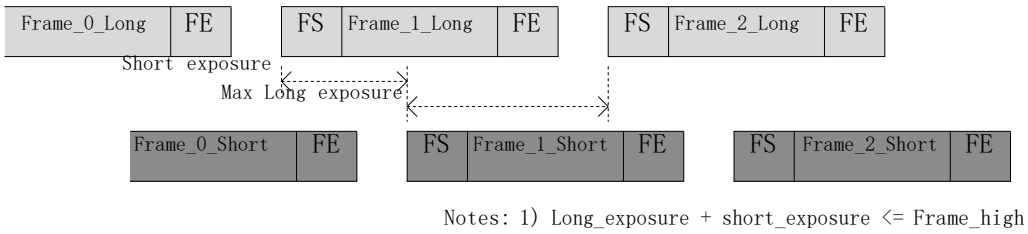


Figure 8: HDR frame timing in MIPI output



Test Pattern Output:

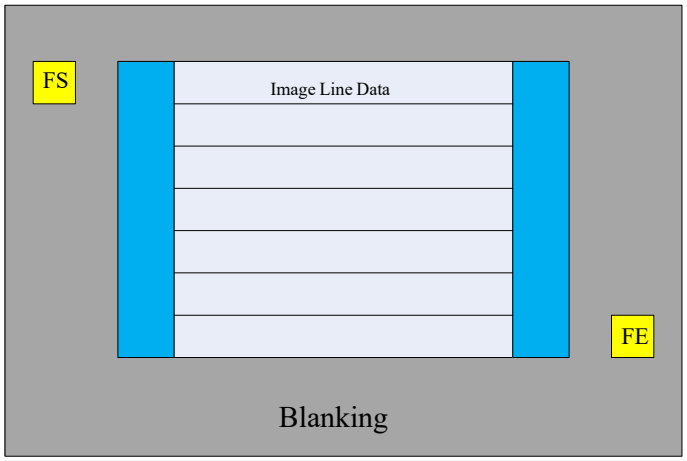
JX-H65 can output test pattern as described below:

1) Walking “1” test pattern: for most sensor module connectivity test, JX-H65 provides walking “1” test pattern.

MIPI interface:

JX-H65 supports MIPI CSI-2 compliant interface. It has one pair of differential clock lane and two pairs of differential data lane. JX-H65 can output raw8 or raw10 mode through the MIPI interface. In raw8 mode, only 8 MSBs of 10-bit data will output and user needs to set MIPI clock speed at 8x parallel port pixel clock. In raw10 mode, user needs to set MIPI PHY clock as 10x parallel port pixel clock.

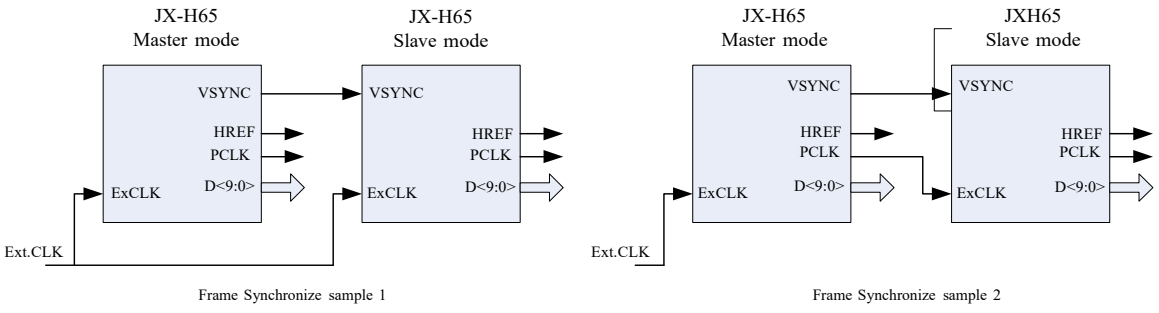
Figure 9: MIPI interface frame timing



Frame Synchronization:

JX-H65 provides the capability of frame synchronization. By setting VSYNC pin as input and enable frame-sync option, JX-H65 will work as slave device and synchronized with an external VSYNC. If all master devices and slave devices use same timing setting, all devices frame timing mismatch will be less than few pixel clocks. Figure 10 shows 2 ways to realize frame synchronization.

Figure 10: Frame Synchronization illustration



In the above 2 frame synchronize configurations, sample 2 will have more accurate synchronization than sample 1 because the slave device will have exactly same pixel clock as the master.

Serial Interface:

The serial interface is a two-wire bi-directional bus. Both wires (Serial Clock -SCL and Serial Data - SDA) are connected to DOVDD via a pull-up resistor, and when the bus is free both lines are high. The two-wire serial interface defines several different transmission stages as follows:

- A start bit
- The slave device 7-bit address
- An (No) acknowledge bit coming from slave
- An 8-bit or 16-bit message (address and/or data)
- A stop bit (or another 8bit or 16bit message in multiple Read/Write access)

Figure 11: I2C Timing chart

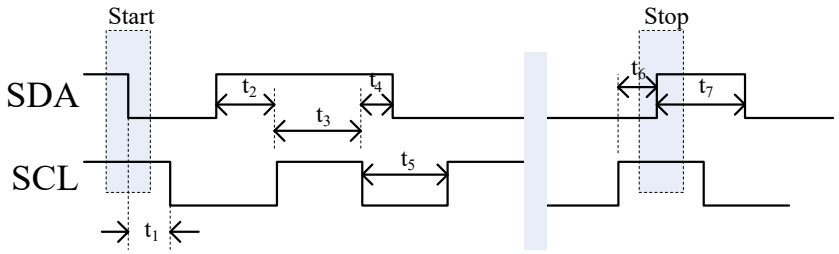
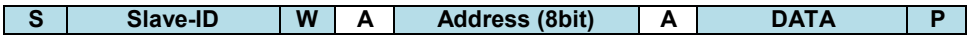


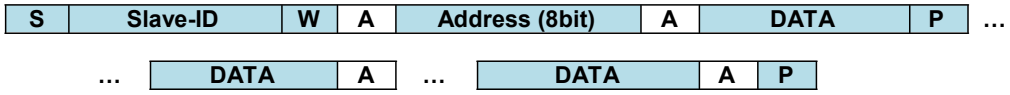
Table 2: I2C timing characteristic

Symbol	Description	Min	Max	Units
	SCL clock frequency	0	400k	Hz
t1	Hold time for START condition	0.6	-	µs
t2	Data setup time	160	-	ns
t3	High period of the SCL clock	0.6	-	µs
t4	Data hold time	0	0.9	µs
t5	Low period of the SCL clock	1.3	-	µs
t6	Setup time for STOP condition	0.6	-	µs
t7	Bus free time between STOP and START condition	1.3	-	µs
	Rise time for both SDA and SCL signals		300	ns
	Fall time for both SDA and SCL signals		300	ns
Cb	Capacitive load for each bus line		400	pF

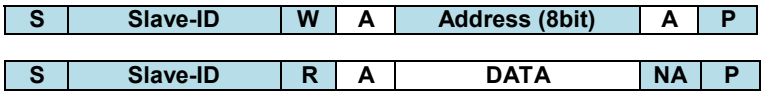
Single Write Mode operation



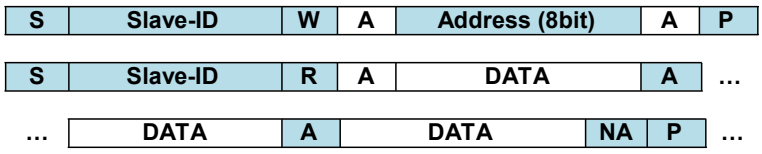
Multiple Write Mode (Register address is increased automatically) operation



Single Read Mode operation



Multiple Read Mode (Register address is increased automatically) operation



S: start conditions, A: acknowledge bit, NA: no acknowledge, DATA: 8 bit data, P: stop condition
JX-H65 slave ID is programmable, default is 0x60/61 for write and read command. User can program DVP data bit<1:0> for other configuration. The slave ID program table is list below:

D[1]	D[0]	Read/Write
X	X	61/60
X	Pull high	65/64
Pull high	X	69/68
Pull high	Pull high	6D/6C

Register Group Write Function:

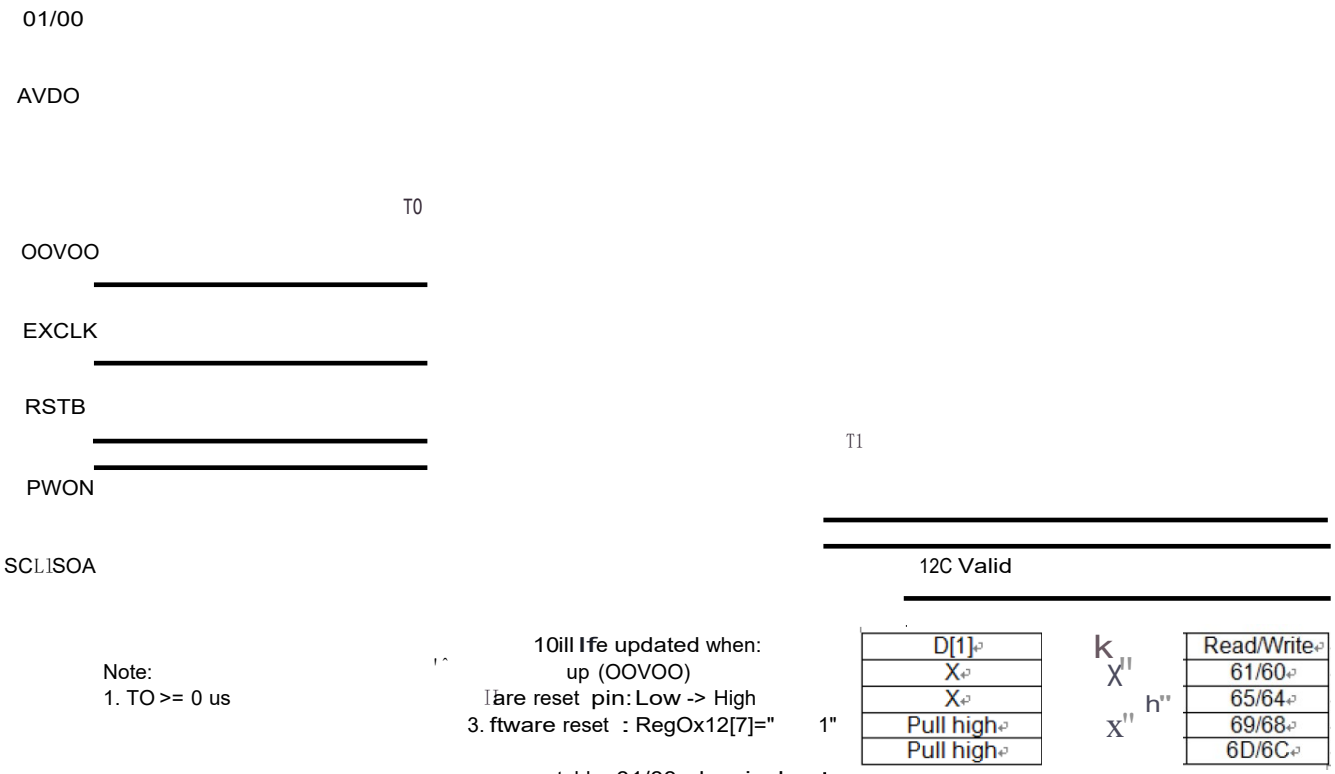
JX-H65 provides register group write function, user can pre-load address and data from register 0xC0 to 0xFF, then trigger this function by setting Reg0x1F[7], normally JX-H65 will auto write back group register content at next vertical blanking period and reset Reg0x1F[7] JX-H65 can update up to 32bytes of registers.

User can always monitor Reg0x1F[7]] to make sure group write procedure is finished or not.

Power *on/off* sequence:

Figure 12 shows a reference pow rup sequ nce of JX-H65

Figure 12. Power up sequence for JX-H65



Note:
1. TO >= 0 us

10ill Ife updated when:
up (OOVOO)
Iare reset pin: Low -> High
3. ftware reset : RegOx12[7]=" 1"

D[1]	Read/Write
X	61/60
X	65/64
Pull high	69/68
Pull high	6D/6C

table 01/00 when issue above commands.

Figur 13 shows a refi nc pow rdownsequ nc ofJX-H65

Figure 13. Power down sequence for JX-H65

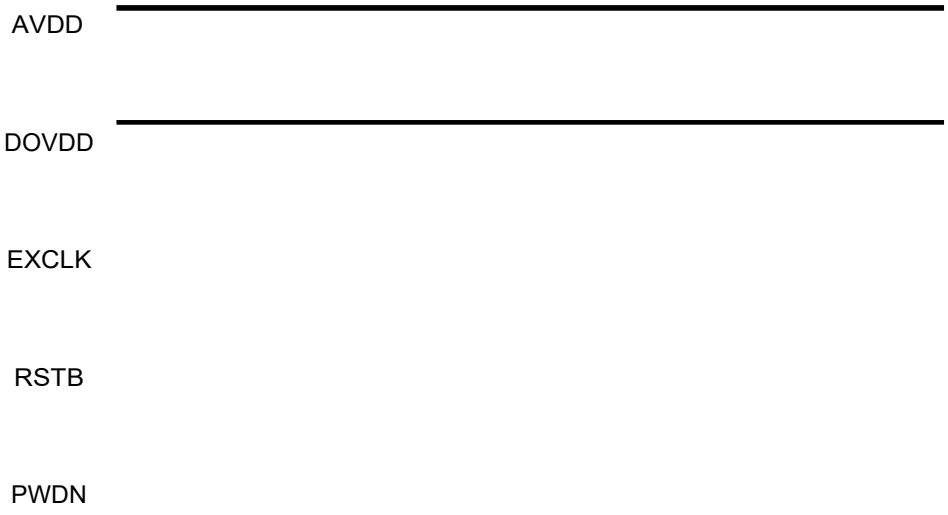


Table 3. Absolute maximum ratings

Symbol	Descriptions	Absolute maximum rating	Units
V_{DD-IO}	I/O Digital Power	4.5	V
V_{DD-A}	Analog Power	4.5	V
V_{DD-D}	Core Digital Power	4.5	V
V_I	Input voltages	-0.3v to V_{DD-IO} + 1V	V
T_A	Ambient Temperature	-40 ~ 125	℃
T_S	Storage Temperature	-40 ~ 125	℃

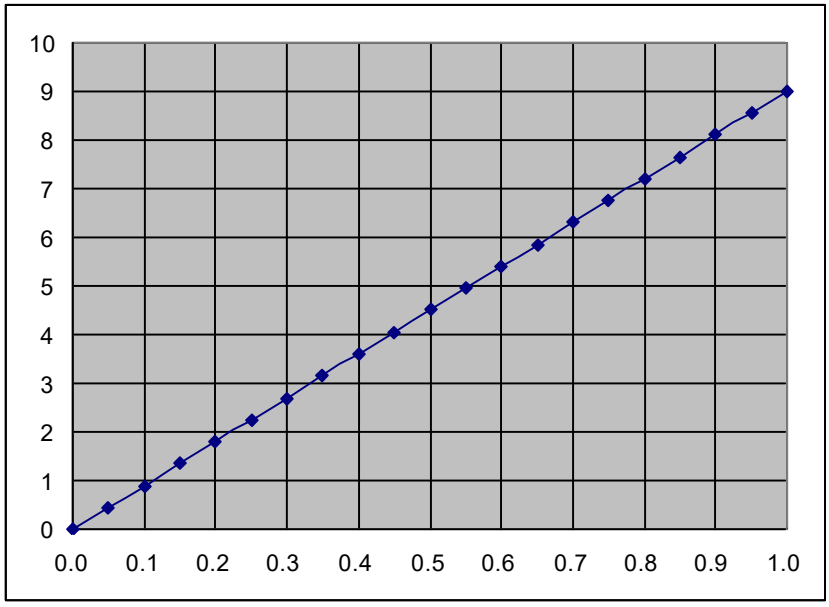
Table 4. DC Characteristics (0°C ≤ TA ≤ 85°C, Voltages referenced to GND)

Symbol	Descriptions	Max	Typ	Min	Units
supply					
V_{DD-IO}	Supply voltage (DOVDD)	3.45	1.8	1.7	V
V_{DD-A}	Supply voltage (AVDD)	3.0	2.8	2.6	V
V_{DD-D}	Supply voltage (DVDD)	1.35	1.5	1.65	V
Digital Inputs					
V_{IL}	Input voltage LOW	0.2* V_{DD-IO}	-	-	V
V_{IH}	Input voltage HIGH			0.7*V_{DD-IO}	V
C_{IN}	Input capacitor	10			pF
Digital Outputs (loading 20pF)					
V_{OH}	Output voltage HIGH			V_{DD-IO} – 0.2	V
V_{OL}	Output voltage LOW	0.2			V
Power consumption (Internal DVDD, MVDD short to DVDD;DVP output AVDD=2.8V, DOVDD=1.8V)					
I_{DD-IO}	Supply current (V_{DD-IO}=1.8V@ 30fps 960P without digital I/O loading)		15		mA
I_{DD-A}	Supply current (V_{DD-A}=2.8V)		35		mA
I_{pwrdn}	HW PWDN Pin active		TBD		uA
Power consumption (Internal DVDD, MVDD short to DVDD;MIPI output AVDD=2.8V, DOVDD=1.8V)					
I_{DD-IO}	Supply current (V_{DD-IO}=1.8V@ 30fps 960P without digital I/O loading)		20		mA
I_{DD-A}	Supply current (V_{DD-A}=2.8V)		35		mA
I_{pwrdn}	HW PWDN Pin active		TBD		uA

CRA Specifications:

JX-H65 is designed with a linear chief ray angle curve as shown in Figure 14. The shifting of the color filter and micro-lenses on the sensor is critical to accommodate the ever shorter height of the camera module as well as minimizing shading at the corner of the image.

Figure 14. CRA Curve for JX-H65



Field	CRA
0.00	0.00
0.05	0.45
0.10	0.90
0.15	1.35
0.20	1.80
0.25	2.25
0.30	2.70
0.35	3.15
0.40	3.60
0.45	4.05
0.50	4.50
0.55	4.95
0.60	5.40
0.65	5.85
0.70	6.30
0.75	6.75
0.80	7.20
0.85	7.65
0.90	8.10
0.95	8.55
1.00	9.00

Mechanical Specifications:

JX-H65 is available in both CSP packaged component or die forms. Figure 15 shows top view and bottom view of the CSP component. Table 5 shows the nominal dimensions for the packaged chip.

Figure 15. CSP Top, Bottom, Side View

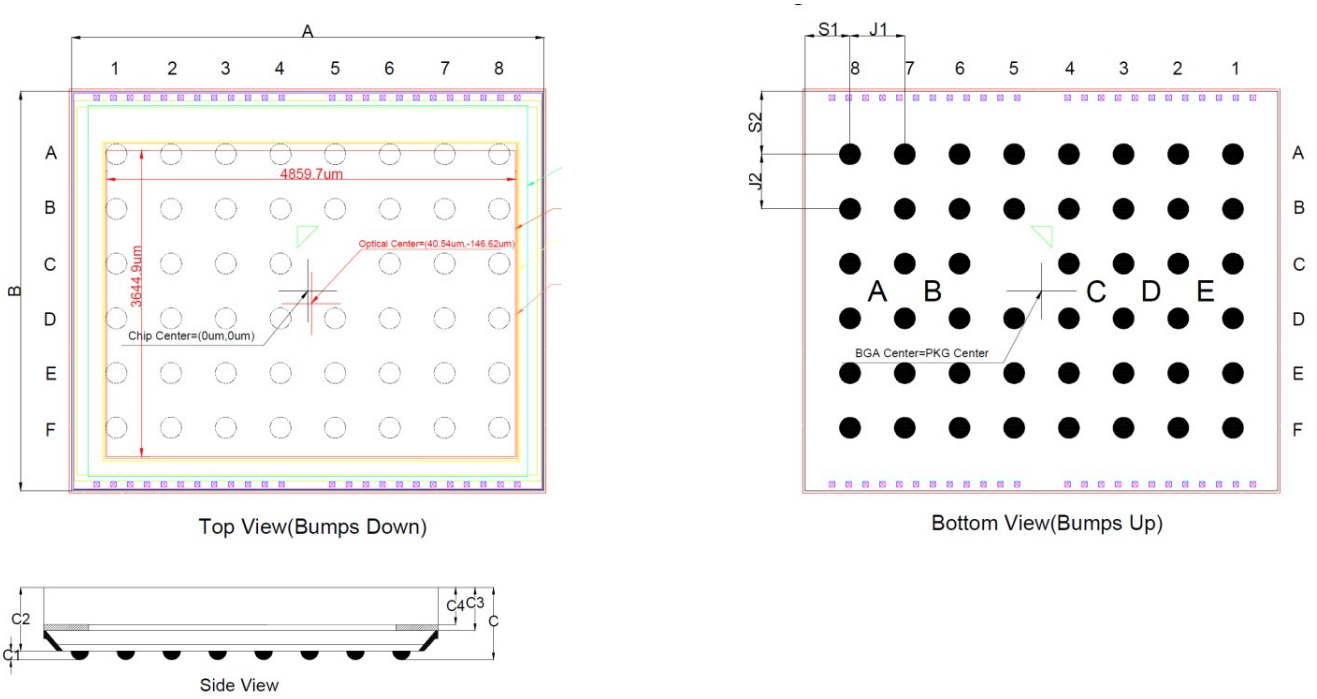


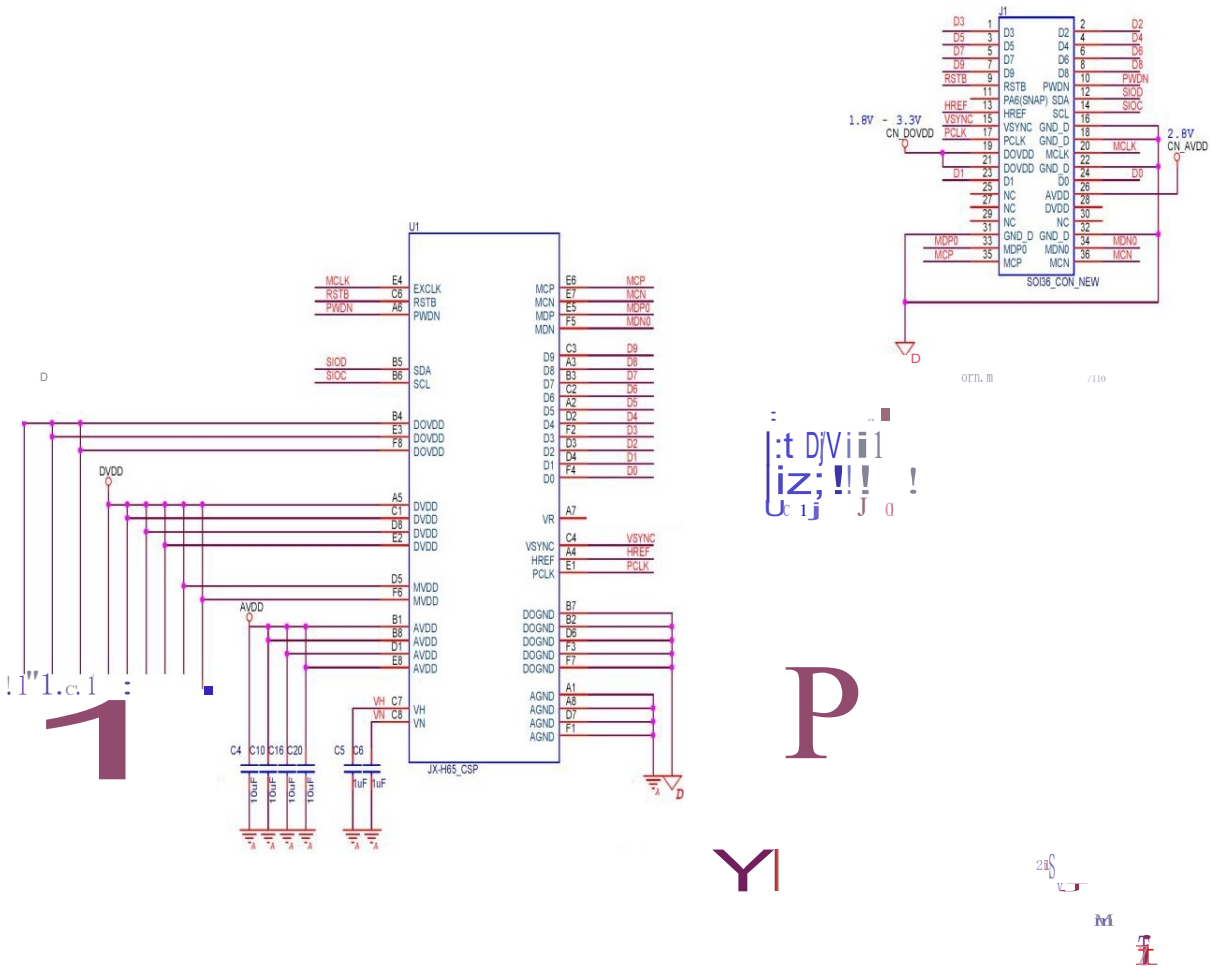
Table 5. Dimensions for JX-H65 CSP package

	Symbo	Nominal	Min	Max	Nominal	Min	Max
		Millimeters			Inches		
Package Body Dimension X	A	5.614	5.589	5.639	0.22102	0.22004	0.22201
Package Body Dimension Y	B	4.749	4.724	4.774	0.18697	0.18598	0.18795
Package Height	C	0.770	0.710	0.830	0.03031	0.02795	0.03268
Ball Height	C1	0.130	0.100	0.160	0.00512	0.00394	0.00630
Package Body Thickness	C2	0.640	0.605	0.675	0.02520	0.02382	0.02657
Thickness from top glass surface to wafer	C3	0.445	0.425	0.465	0.01752	0.01673	0.01831
Glass Thickness	C4	0.400	0.385	0.415	0.01575	0.01516	0.01634
Ball Diameter	D	0.250	0.220	0.280	0.00984	0.00866	0.01102
Total Ball Count	N	47					
Pins pitch X axis	J1	0.65					
Pins pitch Y axis	J2	0.65					
Edge to Pin Center Distance along X	S1	0.5320	0.5020	0.5620	0.02094	0.01976	0.02213
Edge to Pin Center Distance along Y	S2	0.7495	0.7195	0.7795	0.02951	0.02833	0.03069

CSP Module Schematic (Reference):

Figure 16 shows a reference schematic for CSP module.

Figure 16. Reference schematic for CSP module



Register Descriptions:

Write Slave ID:0x60/64/68/6C Read Slave ID:0x61/65/69/6D

Address (Hex)	Register Name	Default (Hex)	R/W	Description
00	PGA	00	RW	Programmable gain, valid 0 to 7F,PGA[7] reserved Total gain = 2^PGA[6:4]*(1+PGA[3:0]/16)
01	EXP	FF	RW	Exposure line LSBs, EXP[7:0]
02	EXP	00	RW	Exposure line MSBs, EXP[15:8]. Exposure time is defined by EXP[15:0] at line period base. T_{EXP}=EXP[15:0]*T_{Line}
03-04	PLEXP	FF	RW	RSVD
05	EXP_S	00	RW	Short exposure lines in HDR mode, EXP_S[7:0]: each bit equals to 2 lines, short_exposure_time = (EXP_S[7:0] *2 + 1) * T_{Line}
06-08				Reserved
09	VER	00	R	Version ID
0A	PIDH	0A	R	Product ID MSBs.
0B	PIDL	65	R	Product ID LSBs.
0C	DVP1	40	RW	DVP control 1. DVP1[7]: RSVD DVP1[6]: Sensor sun spot elimination control, “1”: disable sun spot elimination, “0”: enable sun spot elimination. DVP1[5:2]: RSVD. DVP1[1:0]: DVP test mode output option. “00”: DVP output normal image data. “01”: DVP[9:0] = Output 10-bit walk “1” test pattern. “10”,“11”: RSVD
0D	DVP2	50	RW	DVP control 2. DVP2[7:6]: P_Pump clock frequency selection. DVP2[5:4]: N-Pump clock frequency selction. DVP2[3:2]: PAD drive capability. “00”: min, “11”: max. DVP2[1:0]: Digital gain. “00”:1x, “01” and “10”: 2x, “11”:4x
0E	PLL1	10	RW	PLL control 1. PLL1[7]: PLL bypass selection. “1”: PLLclk = Input clock/PLL_Pre_Ratio. “0”: see PLL2[3:0]. PLL1[6:4]: PLL current adjustment. PLL1[3]: Mipi PLL Powerdown. PLL1[2]: external clock input pad circuit option, “0”: internal no Schmitt trigger; “1”: internal has Schmitt trigger. PLL1[1:0]: PLL pre-divider ratio. PLL_Pre_Ratio = 1 + PLL[1:0]
0F	PLL2	05	RW	PLL control 2. PLL2[7:4]: Mipi clock divider. Mipiclk = VCO/(1+PLL2[7:4]) PLL2[3]: Mipi clock divider. 1 :MIPIPCLK=1/2 VCO., 0 : MIPIPCLK = VCO PLL2[2]: Sys div2. 0: 1/8; 1: 1/10. PLL2[1:0]: PLL clock divider. PLLclk = VCO/(1+PLL2[1:0])
10	PLL3	22	RW	PLL control 3. PLL VCO multiplier. VCO = Input clock*PLL3[7:0]/PLL_Pre_Ratio

11	CLK	80	RW	RSVD
12	SYS	00	RW	System status set up SYS[7]: Soft reset initialize, “1”: initial system reset, it will reset whole sensor to factory default status, and this bit will clear after reset. SYS[6]: Sleep mode on/off selection, “1”: sensor into sleep mode. No data output and all internal operation stops. External controller can stop sensor clock, while I2C interface still can work. SYS[5]: mirror image on/off, “1”: mirrored image output, “0”: normal image output SYS[4]: flip image on/off, “1”: flipped image output, “0”: normal image output. SYS[3]: HDR mode on/off selection. “0”: normal mode, “1”: HDR mode. SYS[2]: horizontal skip or binning mode select SYS[1]: vertical skip or full mode selection. SYS[0]: down sample mode on/off selection. “1”: sensor into down sample mode, “0”: full size mode output.
13	LCCtrl1	81	RW	Luminance control register 1. LCCtrl1[7:1]: RSVD LCCtrl1[0]: automatic luminance control on/off selection, “0”: auto, “1”: manual
14	LCCtrl2	80	RW	Luminance Control register 2. LCCtrl2[7:0]: Image luminance expect target.
15	LCCtrl3	44	RW	Luminance Control register 3 LCCtrl3[7:4]: auto Luminance control adjustment trigger range. LCCtrl3[3:0]: auto luminance control stable range
16	LCCtrl4	C0	RW	Luminance control register 4 LCCtrl[7:0]: Luminance control large step adjustment high threshold
17	LCCtrl5	40	RW	Luminance control register 5 LCCtrl[7:0]: Luminance control large step adjustment low threshold
18	LCCtrl6	99	RW	Luminance control register 6 LCCtrl6[7:0]: Banding filter minimum exposure line LSBs;Band[7:0]
19	LCCtrl17	44	RW	Luminance control register 7 LCCtrl7[7:6]: PCLK delay option. LCCtrl7[5]: AGC delay 1 frame valid option. LCCtrl7[4:2]: RSVD. LLCCtrl7[1:0]: Banding filter minimum exposure line MSBs. Band[9:8]
1A	LCCtrl8	80	RW	Luminance control register 8 LCCtrl8[7:0]: RSVD
1B	LCCtrl9	4F	RW	Luminance control register 9 LCCtrl9[7:0]: RSVD
1C	LCCtrl10	00	R	Luminance control register 10 LCCtrl10[7:0]: image luminance average value.
1D	DVP3	00	RW	DVP control 3 DVP3[7:0]: GPIO direction control for data output port D[7:0]. “1”: enable output. “0”: tri-state output.
1E	DVP4	1C	RW	DVP control 4 DVP4[7]: PCLK polarity control. “0”: data output at rising edge of PCLK, “1”:data output at falling edge of PCLK DVP4[6]: HREF polarity control. DVP4[5]: VSYNC polarity control. DVP4[4:0]: GPIO direction control for output port: PCLK, HREF, VSYNC and D[9:8]
1F	GLat	00	RW	Group latch control GLat[7]: Group write trigger. “1”: system will write reg0xC0 to 0xFF content to proper register. This bit will clear after group write. “0”: inactive group write function.. GLat[6]: Group latch trigger time option, “0”: trigger at vertical blanking period. “1”: group latch trigger immediately. GLat[4]: NoPreChg, No precharge when Gain is bigger than 2X.

				GLat[3:0]: RSVD
20	FrameW	B0	RW	Sensor frame time width LSBs; FrameW[7:0]
21	FrameW	02	RW	Sensor frame time width MSBs; FrameW[15:8] FrameW[15:0]: sensor frame width.
22	FrameH	F0	RW	Sensor frame time high LSBs ;FrameH[7:0]
23	FrameH	03	RW	Sensor frame time high MSBs. FrameH[15:8] FrameH[15:0]: sensor frame high. Sensor frame rate is defined as Fpclk / (FrameW*FrameH). Fpclk: frequency of pixel clock.
24	HWin	80	RW	Image horizontal output window width LSBs: HWin[7:0]
25	VWin	C0	RW	Image vertical output window high LSBs: VWin[7:0]
26	HVWin	32	RW	Image output window horizontal and vertical MSBs. { VWin[11:8],HWin[11:8]}
27	HWinSt	D0	RW	Image horizontal output window start position LSBs. HWinSt[7:0]
28	VWinSt	14	RW	Image vertical output window start position LSBs. VWinSt[7:0]
29	HVWinSt	01	RW	Image output window horizontal and vertical start position MSBs. {VWinSt[11:8],HWinSt[11:8]}
2A	CShift1	C0	RW	Column shift control 1 Cshift1[7:6]: Column SRAM data shift start position LSBs.
2B	Cshift2	25	RW	Column shift control 2 Cshift2[7:6]: Sensor physical column SRAM read out start address, MSBs, SenHASt[9:8] Cshift2[5:2]: reserved Cshift2[1:0]: Column SRAM data shift start position MSBs
2C	SenHASt	0C	RW	Sensor physical column shift start address LSBs, SenHASt[7:0]; each bit represent 2 pixels
2D	SenVSt	00	RW	Sensor physical vertical start address, LSBs. SenVSt[7:0]; each bit represent 4 lines
2E	SenVEnd	F8	RW	Sensor physical vertical end address, LSBs. SenVEnd[7:0] ;each bit represent 4 lines
2F-42	SenVadd	40	RW	RSVD
43	VS_POS1	00	RW	VSYNC position LSBs: VS_POS[7:0];
44	VS_POS2	40	RW	VS_POS2[7:4]: VSYNC width selection. VS_POS2[3:0]: VSYNC position MSBs; VS_POS[11:8];
45	SCAN_Ctrl	89	RW	RSVD
46				RSVD
47	LBLC	62	RW	Line BLC control LBLC[7:2]: RSVD. LBLC[1]: HDR mode short exposure delay 1 frame valid LBLC[0]: HDR mode short exposure pre-charge on/off selection.
48	BLCOpt1	0A	RW	BLC control option 1 BLCopt1[7:0]: Reserved.
49	BLC_TGT	04	RW	Black level calibration target level. BLC_TGT[7]: sign bit. BLC_TGT[6:0]: target level.
4A	BLCCtrl	03	RW	BLC control BLCCtrl[7]: BLC_B bit 10 BLCCtrl[6]: BLC_Gb bit 10 BLCCtrl[5]: BLC_Gr bit 10

				BLCCtrl[4]: BLC_R bit 10 BLCCtrl[3:2]: BLC_Dly[1:0]: ABLC do continue frames after AE stable, '00': 8 frames, '01': 4 frames, '10': 2 frames, '11': 1 frames. BLCCtrl[1]: BLC action option. “0”: Sensor do BLC only when triggered. “1”: always do BLC. BLCCtrl[0]: auto BLC function on/off selection. “0”: sensor stop calculate black value. “1”: sensor calculate black value automatically.
4B	BLC_B	00	RW	B channel black value LSBs. BLC_B[7:0]
4C	BLC_Gb	00	RW	Gb channel black value LSBs. BLC_Gb[7:0]
4D	BLC_Gr	00	RW	Gr channel black value LSBs. BLC_Gr[7:0]
4E	BLC_R	00	RW	R channel black value LSBs. BLC_R[7:0]
4F	BLC_H	00	RW	Black value MSBs. {BLC_R[9:8],BLC_Gr[9:8],BLC_Gb[9:8],BLC_B[9:8]}
50	SBLCCtrl	03	RW	Short exposure BLC control in HDR mode SBLCCtrl[7]: SBLC_B bit 10 SBLCCtrl[6]: SBLC_Gb bit 10 SBLCCtrl[5]: SBLC_Gr bit 10 SBLCCtrl[4]: SBLC_R bit 10 SBLCCtrl[3:0]: RSVD
51	SBLC_B	00	RW	Short exposure B channel black value LSBs. SBLC_B[7:0]
52	SBLC_Gb	00	RW	Short exposure Gb channel black value LSBs. SBLC_Gb[7:0]
53	SBLC_Gr	00	RW	Short exposure Gr channel black value LSBs. SBLC_Gr[7:0]
54	SBLC_R	00	RW	Short exposure R channel black value LSBs. SBLC_R[7:0]
55	SBLC_H	00	RW	Short exposure black value MSBs. {SBLC_R[9:8],SBLC_Gr[9:8],SBLC_Gb[9:8],SBLC_B[9:8]}
56 - 6B	SenT14	A2	RW	RSVD
6C	DPHY2	00	RW	DPHY2[7]: Mipi interface power down. DPHY2[6:0]: RSVD
6D-6F	DPHY3	02	RW	RSVD
70	Mipi1	49	RW	Mipi timing control 1 Mipi1[7:5]: Tlpx,Length of any Low-Power state mode. Mipi1[4:2]: Tck-pre, Time to drive LP-00 to prepare for HS clock transmission Mipi1[1]: Mipi 8/10 bit mode switch, “0”: 10-bit, “1”: 8-bit mode Mipi1[0]: reserved
71	Mipi2	8A	RW	Mipi timing control 2 Mipi2[7:5]: Ths-zero,Time to drive HS-0 before Sync sequence. Mipi2[4:0]: Tck-zero,Time for lead HS-00 period before starting clock.
72	Mipi3	68	RW	Mipi timing control 3 Mipi3[7:5]: Ths-prepare,Time to drive LP-00 to prepare for HS transmission. Mipi3[4:0]: Tck-post,Time that transmitter shall continue sending HS clock after the last associated data lane has transisted to LP mode.
73	Mipi4	33	RW	Mipi timing control 4 Mipi4[7]: Mipi pixel clock option Mipi4[6:4]: Ths-trail,Time to drive flipped differential state after last payload data bit of a HS transmission burst. Mipi4[3:0]: Tck-trail
74	Mipi5	53	RW	Mipi timing control 5 Mipi5[7:4]: reserved Mipi5[3]: Mipi virtual channel ID revise Mipi5[2]: Mipi byte clock revise Mipi5[1]: Mipi continues mode or strobe mode selection

				Mipi5[0]: Mipi interface sleep on/off
75	Mipi6	2B	RW	Mipi data type ID
76	Mipi7	40	RW	Mipi word count LSBs
77	Mipi8	06	RW	Mipi word count MSBs
78	Mipi9	14	RW	Mipi timing control 9 Mipi9[7]: CK-pre timing option Mipi9[6:0]: Mipi TX start point adjust related to DVP HREF and internal FIFO
79-BF				RSVD
C0	Group0	0A	RW	Group write 1st data address
C1	Group1	0A	RW	Group write 1st data value.
C2	Group2	0A	RW	Group write 2nd data address
C3	Group3	0A	RW	Group write 2nd data value.
…	…	…	…	…
FE	Group62	0A	RW	Group write 32nd data address
FF	Group63	0A	RW	Group write 32nd data value.

Document Revision Control

Version Number #	Date Released	Comments
R0.0	8/17/2016	Initial release of JX-H65 datasheet
R0.1	10/28/2016	Modify CSP info, Pixel array info, App ckt info
R0.2	11/08/2016	Change optical format: 1/3"
R0.3	1/08/2017	Modify Component order info, Register description.