1/7-Inch System-on-a-Chip (SOC) CMOS Digital Image Sensor

ASX370 Die Data Sheet, Rev. C

For the product data sheet, refer to Aptina's Web site at www.aptina.com

Features

- Superior low-light performance
- Ultra low power, low cost
- Internal master clock generated by on-die phase-lock-loop (PLL) oscillator
- Electronic rolling shutter (ERS), progressive scan
- Integrated image flow processor (IFP) for single-die camera module
- Automatic image correction and enhancement, including four-channel lens shading correction
- Arbitrary image scaling with anti-aliasing
- Two-wire serial interface providing access to registers and microcontroller memory
- Selectable output data format: YCbCr, 565RGB, 555RGB, 444RGB, processed Bayer, RAW8- and RAW10-bit
- Programmable I/O slew rate
- Parallel and serial MIPI data output
- Independently configurable gamma correction

General Physical Specifications

Die thickness: 200µm ±12µm
(Consult factory for other thickness)

- Back side die surface of bare silicon
- Typical metal 1 thickness: 3.1kÅ
- Typical metal 2 thickness: 3.2kÅ
- Typical metal 3 thickness: 3.2kÅ
- Typical metal 4 thickness: 4.0kÅ
- Metallization composition: 99.5 percent Al and 0.5 percent Cu over Ti
- Typical topside passivation: 2.2kÅ nitride over 5.0kÅ of undoped oxide
- Passivation openings (MIN): 75µm x 90µm

Order Information

ASX370CSSC27SUD20

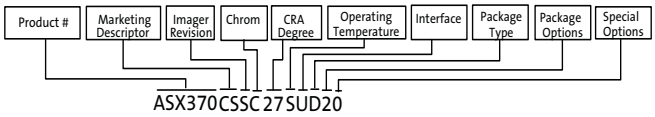
ASX370CSSC27SUD20-E

Note: Consult die distributor or factory before ordering to verify long-term availability of these die products.

Die Database

- Die outline, see Figure 3 on page 10
- Singulated die size (example dimension): 4,137.8µm ±25µm x 4,033.3µm ±25µm
- Bond Pad Location and Identification Tables, see pages 5–7

Options	Designator
• Form	
– Die	D
• Testing	
– Standard (level 1) probe	C1



Key Performance Parameters

- Optical format: 1/7-inch (4:3)
- Full resolution: 640 x 480 pixels (VGA)
- Pixel size: 3.0µm x 3.0µm
- Dynamic range: 72.46 dB
- Responsivity: 3.7 V/lux-sec
- Chief ray angle: 27.61° Max at 90% image height
- Color filter array: RGB Bayer pattern
- Active pixel array area: 1.94mm x 1.46mm
- Shutter type: electronic rolling shutter (ERS)
- Input clock frequency: 6–44 MHz (PLL-enabled)
- Maximum frame rate: 30 fps at full resolution
- Maximum pixel data output: 14 Mp/s
- Maximum pixel clock frequency: 28 MHz
- Supply voltage: analog: 2.5–3.1V
  - Digital: 1.70–1.95V
  - I/O: 1.70–1.95V or 2.5–3.1V
  - PLL: 2.5–3.1V
  - PHY: 1.70–1.95V (MIPI physical layer)
- ADC resolution: 10-bit, on-die
- Typical power consumption: 78mW at 30 fps, full resolution; 29 µW, standby
- Operating temperature: –30°C to +70°C

General Description

Aptina's ASX370 die is a 1/7-inch VGA CMOS digital image sensor with an integrated advanced camera system. The camera system features a micro controller (MCU), a sophisticated image flow processor (IFP), and both parallel and serial mobile industry processor interface (MIPI) ports. The micro controller manages all functions of the camera system and sets key operation parameters for the sensor core to optimize the quality of raw image data entering the IFP. The sensor core consists of an active pixel array of 648 x 488 pixels with programmable timing and control circuitry. It also includes an analog signal chain with automatic offset correction, programmable gain, and 10-bit analog-to-digital converter (ADC).

The entire system-on-a-chip (SOC) has an ultra-low power operational mode and a superior low-light performance that is particularly suitable for mobile applications. The ASX370 die features Aptina's breakthrough low-noise CMOS imaging technology that achieves near-CCD image quality (based on signal-to-noise and low-light sensitivity) while maintaining the inherent size, cost, and integration advantages of CMOS.

Die Testing Procedures

Aptina® die products are tested with a standard probe (C1) test level. Wafer probe is performed at an elevated temperature to test product functionality in Aptina's standard package. Because the package environment is not within Aptina's control, the user must determine the necessary heat sink requirements to ensure that the die junction temperature remains within specified limits.

Image quality is verified through various imaging tests. The probe functional test flow provides test coverage for the on-die ADC, logic, serial interface bus, and pixel array. Test conditions, margins, limits, and test sequence are determined by individual product yields and reliability data.

Aptina retains a wafer map of each wafer as part of the probe records, along with a lot summary of wafer yields for each lot probed. Aptina reserves the right to change the probe program at any time to improve the reliability, packaged device yield, or performance of the product.

Die users may experience differences in performance relative to Aptina's data sheets. This is due to differences in package capacitance, inductance, resistance, and trace length.

Functional Specifications

The specifications provided here are for reference only. For target functional and parametric specifications, refer to the packaged product data sheet found on Aptina's Web site.

Bonding Instructions

The ASX370 die has 48 bond pads. Refer to Tables 1 and 2 on pages 5–7 for a complete list of bond pads and coordinates.

The ASX370 die does not require the user to determine bond option features.

The die also has several pads defined as "No connection." These pads are reserved for engineering purposes and should not be used. Bonding these pads could result in a nonfunctional die.

To ensure proper device operation, all power supply bond pads must be bonded.

Figure 1 on page 4 shows typical ASX370 device connections. For low-noise operation, the ASX370 requires separate supplies for analog and digital sections of the die. Both power supply rails should be decoupled to ground using capacitors as close as possible to the die. The use of inductance filters is not recommended on the power supplies or output signals.

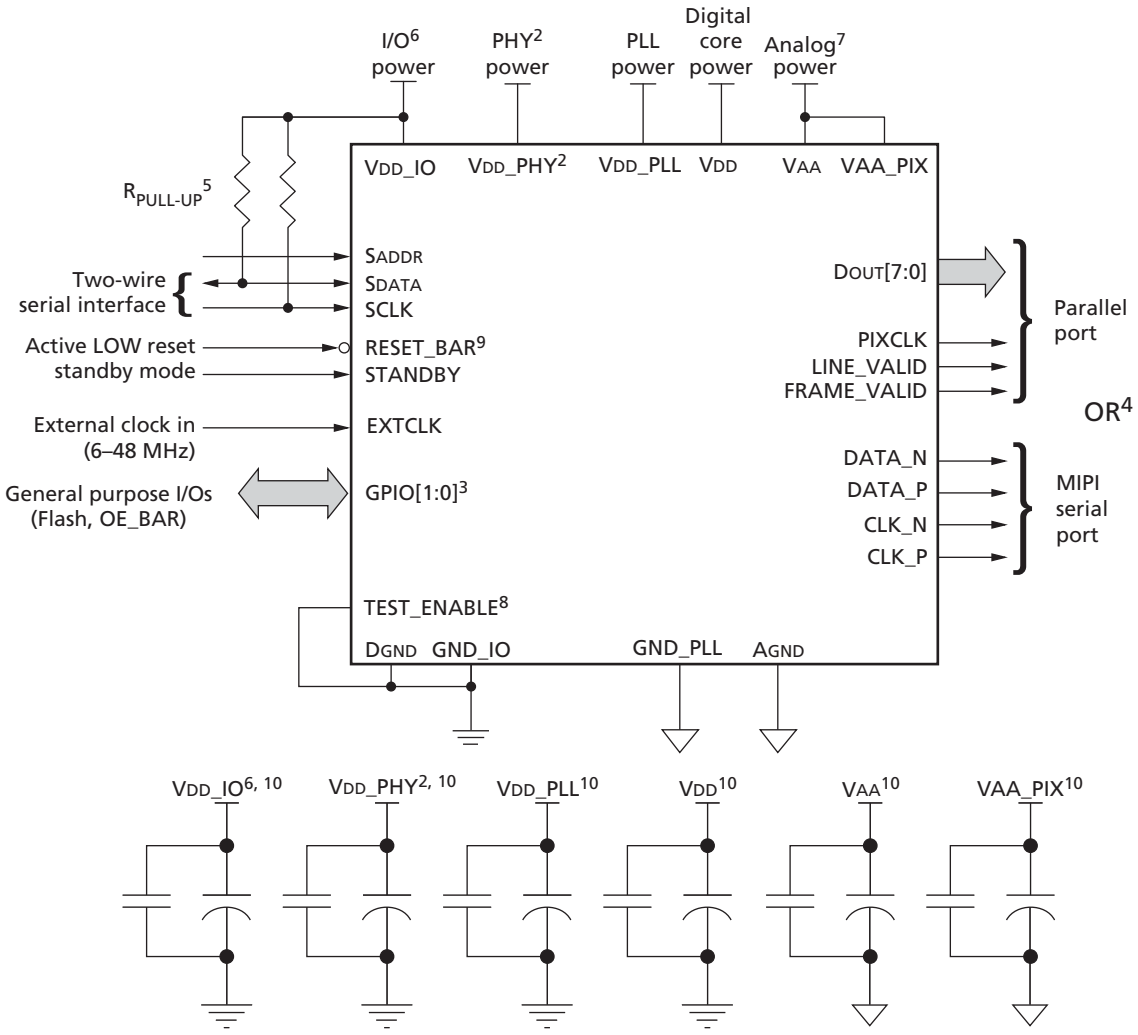
The ASX370 provides dedicated signals for digital core, PHY, and I/O power domains that can be at different voltages. The PLL and analog circuitry require clean power sources.

Storage Requirements

Aptina die products are packaged for shipping in a cleanroom environment. Upon receipt, the customer should transfer the die to a similar environment for storage. Aptina recommends the die be maintained in a filtered nitrogen atmosphere until removed for assembly. The moisture content of the storage facility should be maintained at 30 percent relative humidity ±10 percent. ESD damage precautions are necessary during handling. The die must be in an ESD-protected environment at all times for inspection and assembly.

Typical Connection

Figure 1: Typical Configuration (Connection)



Notes:
1. This typical configuration shows only one scenario out of multiple possible variations for this sensor.
2. If a MIPI interface is not required, the following pads must be left floating: DATA_P, DATA_N, CLK_P, and CLK_N. The VDD_PHY pad must always be connected to 1.8V supply.
3. The GPIO pads have multiple features that can be reconfigured. The function and direction will vary by application. No internal pull-up or pull-down resistors are provided for GPIO pins. An external source needs to drive GPIO pins when GPIO pins are configured as inputs.
4. Only one of the output modes (serial or parallel) can be used at any time.
5. Aptina recommends a 1.5kΩ resistor value for the two-wire serial interface RPULL-UP; however, greater values may be used for slower transmission speed.
6. All inputs must be configured with VDD_IO.
7. VAA and VAA_PIX must be tied together.
8. TEST_ENABLE has an internal pull-down resistor.
9. RESET_BAR has an internal pull-up resistor.
10. Aptina recommends that 0.1µF and 1µF decoupling capacitors for each power supply are mounted as close as possible to the pad. Actual values and numbers may vary depending on layout and design considerations.

Bond Pad Location and Identification Tables

Table 1: ASX370 Bond Pad Location from Center of Die (0, 0)

Pad Number	Pad Name	"X"[1] Microns	"Y"[1] Microns	"X"[1] Inches	"Y"[1] Inches
1	GND_IO1	-1973.300	1856.830	-0.0776890	0.0731035
2	VAA_PIX	-890.685	1918.300	-0.0350663	0.0755236
3	VAA0	-720.685	1918.300	-0.0283734	0.0755236
4	NC[2]	-610.485	1918.300	-0.0240348	0.0755236
5	NC	-500.285	1918.300	-0.0196963	0.0755236
6	AGND	-390.085	1918.300	-0.0153577	0.0755236
7	GND_IO3	1973.300	1856.810	0.0776890	0.0731028
8	TEST_ENABLE[3]	1973.300	1683.820	0.0776890	0.0662921
9	RESET_BAR	1973.300	1514.820	0.0776890	0.0596386
10	SCLK	1973.300	1345.820	0.0776890	0.0529850
11	STANDBY	1973.300	1176.820	0.0776890	0.0463315
12	VDD3	1973.300	1007.820	0.0776890	0.0396780
13	DGND3	1973.300	838.820	0.0776890	0.0330244
14	SDATA	1973.300	670.820	0.0776890	0.0264102
15	GPIO_1	1973.300	489.695	0.0776890	0.0192793
16	PIXCLK	1973.300	316.275	0.0776890	0.0124518
17	SADDR	1973.300	148.270	0.0776890	0.0058374
18	GPIO_0	1973.300	-19.735	0.0776890	-0.0007770
19	VDD_IO3	1973.300	-187.740	0.0776890	-0.0073913
20	GND_IO2	1973.300	-500.950	0.0776890	-0.0197224
21	FRAME_VALID (FV)	1973.300	-668.955	0.0776890	-0.0263368
22	LINE_VALID (LV)	1973.300	-842.375	0.0776890	-0.0331644
23	DGND2	1973.300	-1010.380	0.0776890	-0.0397787
24	DOUT7	1973.300	-1178.385	0.0776890	-0.0463931
25	VDD2	1973.300	-1346.390	0.0776890	-0.0530075
26	DOUT6	1973.300	-1515.395	0.0776890	-0.0596612
27	DOUT5	1973.300	-1688.815	0.0776890	-0.0664888
28	VDD_IO2	1973.300	-1856.820	0.0776890	-0.0731031
29	GND_PLL	-1973.300	-1761.690	-0.0776890	-0.0693579
30	VDD_PLL	-1973.300	-1599.190	-0.0776890	-0.0629602
31	DATA_P	-1973.300	-1371.090	-0.0776890	-0.0539799
32	DATA_N	-1973.300	-1141.090	-0.0776890	-0.0449248
33	CLK_P	-1973.300	-911.085	-0.0776890	-0.0358695
34	CLK_N	-1973.300	-681.085	-0.0776890	-0.0268144
35	VDD_PHY	-1973.300	-419.470	-0.0776890	-0.0165146
36	VDD0	-1973.300	-256.970	-0.0776890	-0.0101169
37	DGND0	-1973.300	-94.470	-0.0776890	-0.0037193
38	EXTCLK	-1973.300	68.030	-0.0776890	0.0026783
39	VDD_IO0	-1973.300	230.530	-0.0776890	0.0090760
40	DOUT0	-1973.300	394.285	-0.0776890	0.0155230
41	GND_IO0	-1973.300	556.790	-0.0776890	0.0219209
42	DOUT1	-1973.300	719.295	-0.0776890	0.0283187
43	VDD_IO1	-1973.300	881.800	-0.0776890	0.0347165

Table 1: ASX370 Bond Pad Location from Center of Die (0, 0)

Pad Number	Pad Name	"X"[1] Microns	"Y"[1] Microns	"X"[1] Inches	"Y"[1] Inches
44	DOUT4	-1973.300	1044.305	-0.0776890	0.0411144
45	DGND1	-1973.300	1206.810	-0.0776890	0.0475122
46	DOUT3	-1973.300	1369.315	-0.0776890	0.0539100
47	VDD1	-1973.300	1531.820	-0.0776890	0.0603079
48	DOUT2	-1973.300	1694.325	-0.0776890	0.0667057

Notes:
1. Reference to center of each bond pad from center of die (0, 0).
2. NC = "No connection."
3. Connect to DGND or leave floating for normal operation.
4. To ensure proper device operation, all power supply bond pads must be bonded.

Table 2: ASX370 Bond Pad Location from Center of Upper left Pad1 (X, Y)

Pad Number	Pad Name	"X"[1] Microns	"Y"[1] Microns	"X"[1] Inches	"Y"[1] Inches
1	GND_IO1	0.000	0.000	0.0000000	0.0000000
2	VAA_PIX	1082.615	61.470	0.0426226	0.0024201
3	VAA0	1252.615	61.470	0.0493156	0.0024201
4	NC[2]	1362.815	61.470	0.0536541	0.0024201
5	NC	1473.015	61.470	0.0579927	0.0024201
6	AGND	1583.215	61.470	0.0623313	0.0024201
7	GND_IO3	3946.600	-0.020	0.1553780	-0.0000008
8	TEST_ENABLE[3]	3946.600	-173.010	0.1553780	-0.0068114
9	RESET_BAR	3946.600	-342.010	0.1553780	-0.0134650
10	SCLK	3946.600	-511.010	0.1553780	-0.0201185
11	STANDBY	3946.600	-680.010	0.1553780	-0.0267720
12	VDD3	3946.600	-849.010	0.1553780	-0.0334256
13	DGND3	3946.600	-1018.010	0.1553780	-0.0400791
14	SDATA	3946.600	-1186.010	0.1553780	-0.0466933
15	GPIO_1	3946.600	-1367.135	0.1553780	-0.0538242
16	PIXCLK	3946.600	-1540.555	0.1553780	-0.0606518
17	SADDR	3946.600	-1708.560	0.1553780	-0.0672661
18	GPIO_0	3946.600	-1876.565	0.1553780	-0.0738805
19	VDD_IO3	3946.600	-2044.570	0.1553780	-0.0804949
20	GND_IO2	3946.600	-2357.780	0.1553780	-0.0928260
21	FRAME_VALID (FV)	3946.600	-2525.785	0.1553780	-0.0994404
22	LINE_VALID (LV)	3946.600	-2699.205	0.1553780	-0.1062679
23	DGND2	3946.600	-2867.210	0.1553780	-0.1128823
24	DOUT7	3946.600	-3035.215	0.1553780	-0.1194967
25	VDD2	3946.600	-3203.220	0.1553780	-0.1261110
26	DOUT6	3946.600	-3372.225	0.1553780	-0.1327648
27	DOUT5	3946.600	-3545.645	0.1553780	-0.1395923
28	VDD_IO2	3946.600	-3713.650	0.1553780	-0.1462067
29	GND_PLL	0.000	-3618.520	0.0000000	-0.1424614
30	VDD_PLL	0.000	-3456.020	0.0000000	-0.1360638
31	DATA_P	0.000	-3227.920	0.0000000	-0.1270835
32	DATA_N	0.000	-2997.920	0.0000000	-0.1180283

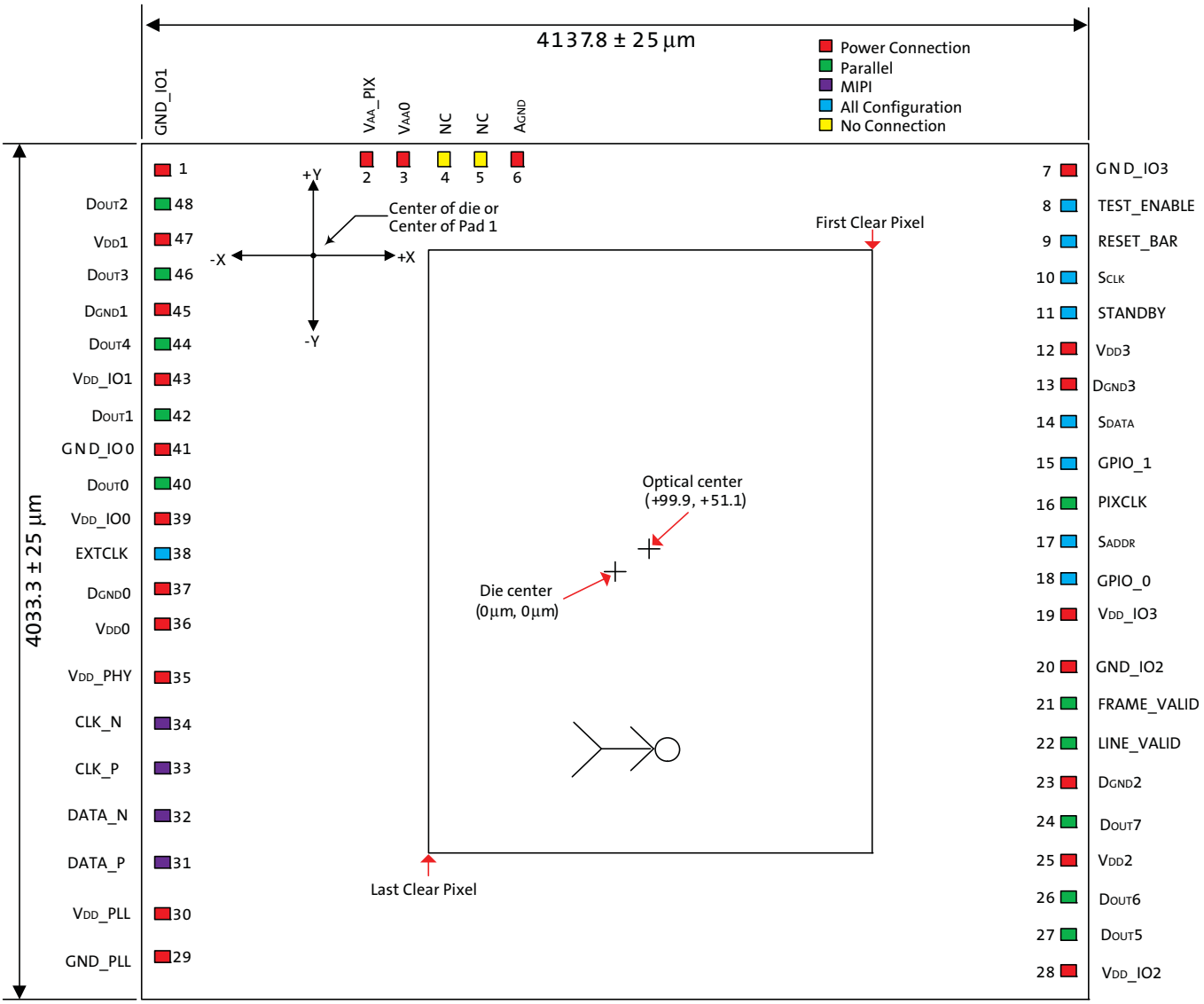
Table 2: ASX370 Bond Pad Location from Center of Upper left Pad1 (X, Y)

Pad Number	Pad Name	"X"[1] Microns	"Y"[1] Microns	"X"[1] Inches	"Y"[1] Inches
33	CLK_P	0.000	-2767.915	0.0000000	-0.1089730
34	CLK_N	0.000	-2537.915	0.0000000	-0.0999179
35	VDD_PHY	0.000	-2276.300	0.0000000	-0.0896181
36	VDD0	0.000	-2113.800	0.0000000	-0.0832205
37	DGND0	0.000	-1951.300	0.0000000	-0.0768228
38	EXTCLK	0.000	-1788.800	0.0000000	-0.0704252
39	VDD_IO0	0.000	-1626.300	0.0000000	-0.0640276
40	DOUT0	0.000	-1462.545	0.0000000	-0.0575805
41	GND_IO0	0.000	-1300.040	0.0000000	-0.0511827
42	DOUT1	0.000	-1137.535	0.0000000	-0.0447848
43	VDD_IO1	0.000	-975.030	0.0000000	-0.0383870
44	DOUT4	0.000	-812.525	0.0000000	-0.0319892
45	DGND1	0.000	-650.020	0.0000000	-0.0255913
46	DOUT3	0.000	-487.515	0.0000000	-0.0191935
47	VDD1	0.000	-325.010	0.0000000	-0.0127957
48	DOUT2	0.000	-162.505	0.0000000	-0.0063978

Notes:
1. Reference to center of each bond pad from center of bond pad 1.
2. NC = "No connection."
3. Connect to DGND or leave floating for normal operation.
4. To ensure proper device operation, all power supply bond pads must be bonded.

Die Features

Figure 2: Die Outline (Top View)

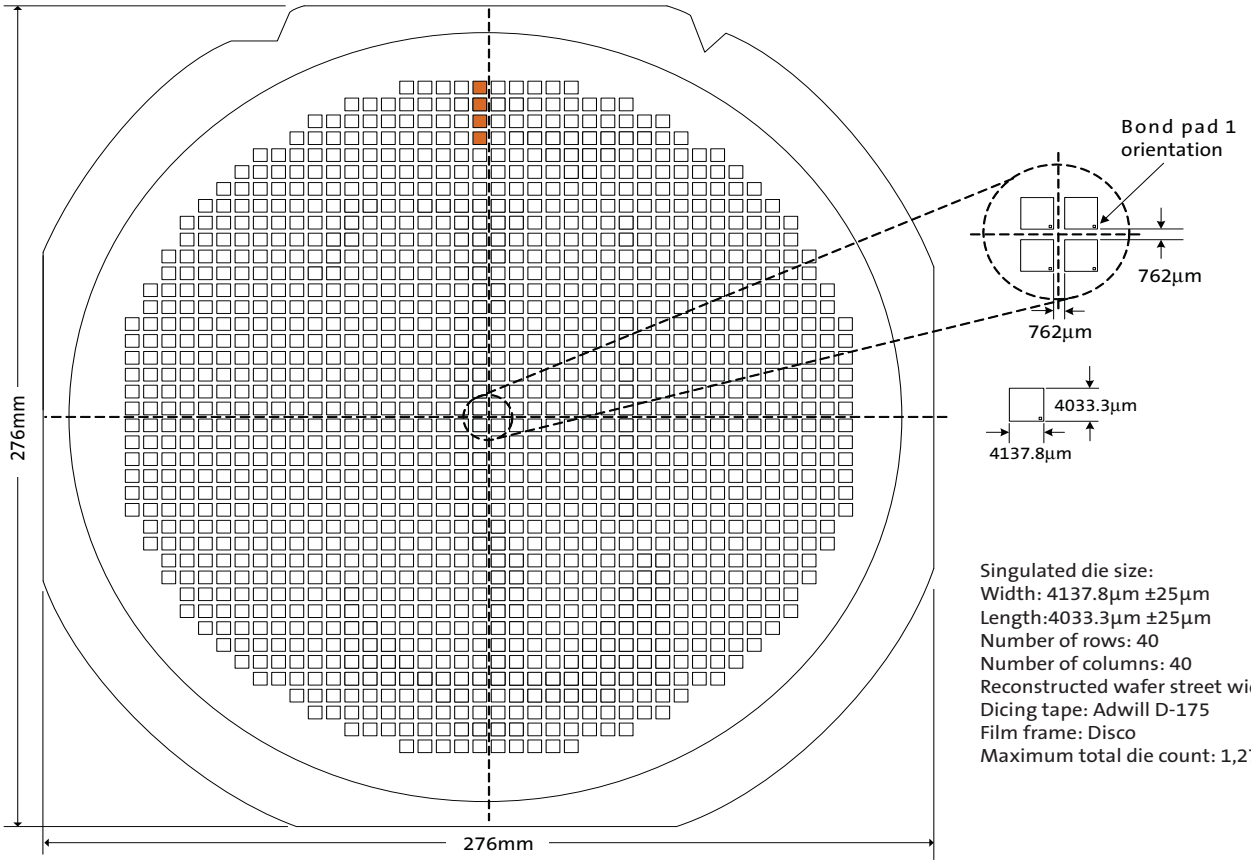


Physical Specifications

Table 3: Physical Dimensions

Feature	Dimensions
Wafer diameter	200mm
Die thickness	200µm ±12µm
Singulated die size (example dimension) Width: Length:	 4137.8µm ±25µm 4033.3µm ±25µm
Bond pad size (MIN)	85µm x 100µm (3.35 mil x 3.94 mil)
Passivation openings (MIN)	75µm x 90µm (2.95 mil x 3.54 mil)
Minimum bond pad pitch	110.2µm (4.34 mil)
Optical array Optical center from die center: Optical center from center of pad 1:	 X = 99.9µm, Y = 51.1µm X = 2073.2µm, Y = –1805.7µm
First clear pixel (col. 88, row 40) From die center: From center of pad 1:	 X = 833.6µm, Y = 1024.6µm X = 2806.9µm, Y = –832.2µm
Last clear pixel (col. 737, row 529) From die center: From center of pad 1:	 X = –633.4µm, Y =–922.4µm X = 1339.9µm, Y = –2779.2µm

Figure 3: Die Orientation in Reconstructed Wafer



Singulated die size:
Width: 4137.8µm ±25µm
Length:4033.3µm ±25µm
Number of rows: 40
Number of columns: 40
Reconstructed wafer street width: 762µm
Dicing tape: Adwill D-175
Film frame: Disco
Maximum total die count: 1,276

Revision History

Rev. C 8/28/13

- Updated to Production
- Applied updated Aptina template

Rev. B 5/15/13

- Updated to Preliminary
- Updated “Key Performance Parameters” on page 1

Rev. A 8/15/12

- Initial release

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