GC1054 CSP

1/4’’720P CMOS Image Sensor

Datasheet

V1.0

2017-12-21

Ordering Information

◆ **GC1054**

(Colored, 40PIN-csp)

GENERATION REVISION HISTORY

REV.	*EFFECTIVE DATE*	*DESCRIPTION OF CHANGES*	*PREPARED BY*
V1.0	*2017-12-21*	*Document Release*	*AE Dept.*

Content

1. Sensor Overview

1.1 General Description

GC1054 is a high quality 720P CMOS image sensor, for mobile phone camera applications and digital camera products. GC1054 incorporates a 1280H x 720V pixel array, on-chip 10-bit ADC, and image signal processor.

The full scale integration of high-performance and low-power functions makes the GC1054 best fit the design, reduce implementation process, and extend the battery life of Motion Camera, Car DVR, and a wide variety of mobile applications.

It provides RAW10 and RAW8 data formats with DVP and MIPI interface. It has a commonly used two-wire serial interface for host to control the operation of the whole sensor.

1.2 Features

- Standard optical format of 1/4 inch
- 3.0um*3.0um
- Output formats: Raw Bayer 10bit/8bit
- Power supply requirement: AVDD33: 3.15~3.45V(Typ.3.3V)
  DVDD: 1.4~1.6(Typ.1.5V)
  IOVDD: 1.7~3.45V(Typ.1.8V)
- PLL support
- DVP@30fps，MIPI@30fps
- Windowing support
- DVP /MIPI (1lane)/ LVDS 1-lane interface support
- Horizontal/Vertical mirror
- Image processing module
- Package: CSP/PLCC

1.3 Application

- Motion camera
- Car DVR
- Monitoring
- Toys
- Digital still cameras and camcorders
- Video telephony and conferencing equipment
- Security systems
- Industrial and environmental systems

1.4 Technical Specifications

Parameter	Typical value
Optical Format	1/4inch
Pixel Size	3.0um x3.0um
Active pixel array	1280 x 720
ADC resolution	10 bit ADC
Max Frame rate	30fps@36MHz,DCLK
Power Supply	AVDD: 3.15~3.45V(Typ.3.3V) DVDD: 1.4~1.6(Typ.1.5V) IOVDD: 1.7~3.45V(Typ.1.8V)
Power Consumption	110mW @30fps,720p
SNR	41.4dB
Dark Current	200 e-/s(60℃)
Sensitivity	18000 e-/lux-sec
Dynamic range	70.7dB
Operating temperature:	-30~80℃
Stable Image temperature	0~50℃
Optimal lens chief ray angle(CRA)	12°(linear)
Package type	CSP/PLCC
Input clock frequency	6~27MHz

2. DC Parameters

2.1 Standby Current

Item	Symbol	Min	Typ	Max	Unit
Analog	I_{AVDD}	—	10	50	uA
Digital	I_{DVDD}	—	40	100	uA
I/O	I_{IOVDD}	—	20	60	uA

INCK: 24MHz, RST: L, PWND: H

Typ. Analog: 3.3V, Digital: 1.5V, I/O:1.8V, Tj=25℃

2.2 Power off Current

Item	Symbol	Min	Typ	Max	Unit
Analog	I_{AVDD}	—	0	0	uA
Digital	I_{DVDD}	—	0	0	uA
I/O	I_{IOVDD}	—	0	0	uA

Power off, T_j=25℃

2.3 Operation current

Full size Operation Current (Parallel mode)

Item	Symbol	Min	Typ	Max	Unit
Analog	I_{AVDD}	—	16	40	mA
Digital	I_{DVDD}	—	25	60	mA
I/O	I_{IOVDD}	—	10	30	mA

Frame rate: 30FPS, RAW 8, Input clock: 24MHz

DCLK: 36MHz

Typ. Analog: 3.3V, Digital: 1.5V, I/O:1.8V, T_j=25℃

Full size Operation Current (MIPI mode @312Mbps / Lane)

Item	Symbol	Min	Typ	Max	Unit
Analog	I_{AVDD}	—	16	40	mA
Digital	I_{DVDD}	—	30	80	mA
I/O	I_{IOVDD}	—	1	10	mA

Frame rate: 30FPS, RAW 10, Input clock: 24MHz

DCLK: 78MHz

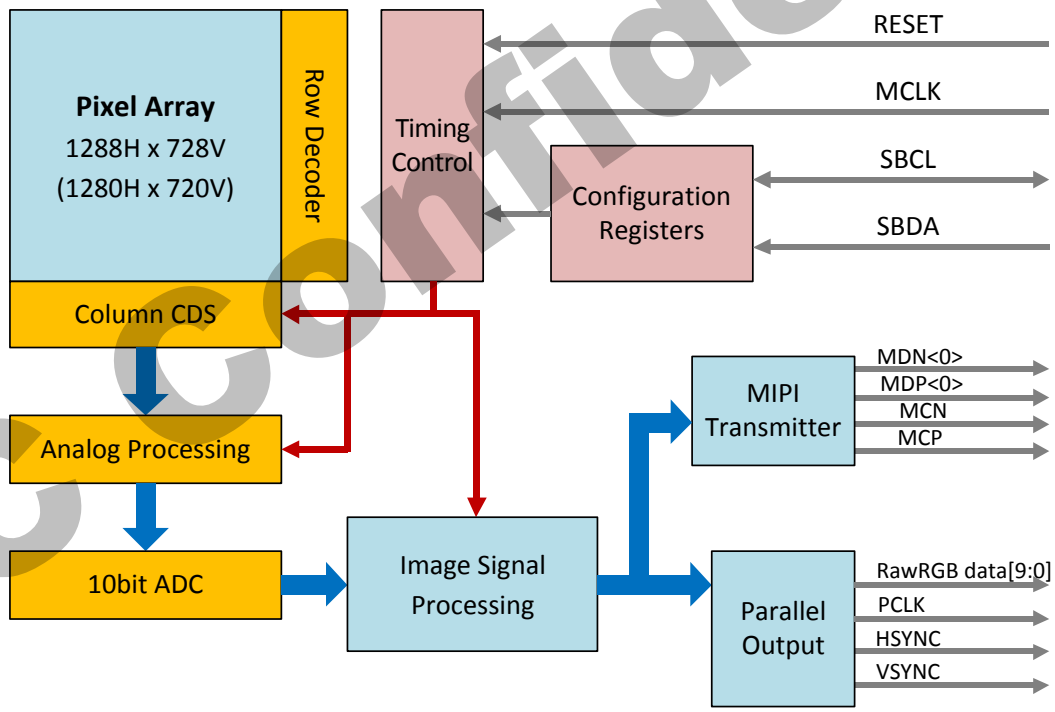
Typ. Analog: 3.3V, Digital: 1.5V, I/O:1.8V, T_j=25℃

2.4 DC Characteristics

Item	Symbol	Min	Typ	Max	Unit
Power supply	V_{AVDD}	3.15	3.3	3.45	V
	V_{DVDD}	1.4	1.5	1.6	V
	V_{IOVDD}	1.7	1.8	3.45	V
Digital Input(Conditions: AVDD = 3.3V, DVDD = 1.5V, IOVDD = 1.8V)					
Input voltage HIGH	V_{IH}	1.4			V
Input voltage LOW	V_{IL}			0.6	V
Digital Output(Conditions: AVDD = 3.3V, IOVDD = 1.8V, standard Loading 25PF)					
Output voltage HIGH	V_{OH}	1.6			V
Output voltage LOW	V_{OL}			0.2	V

3. Block Diagram

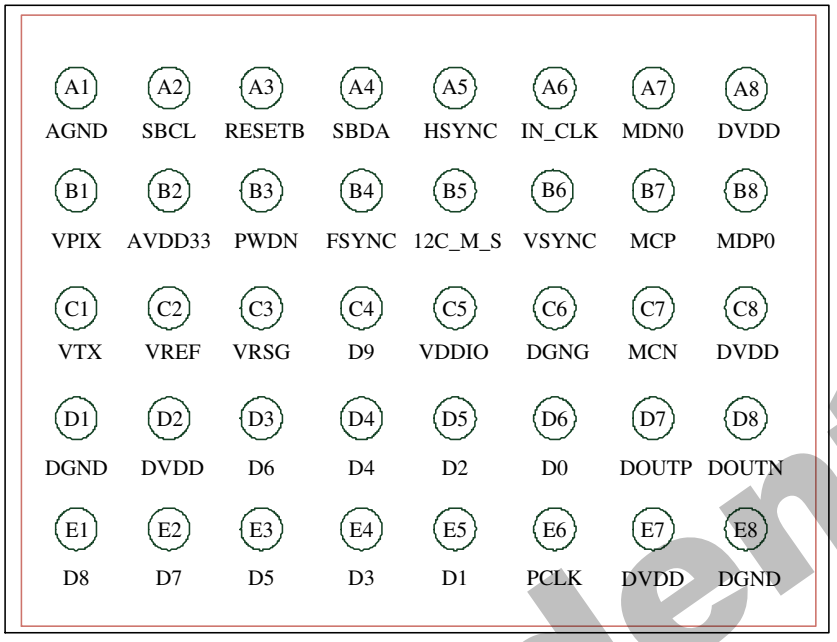
3.1 Block Diagram



GC1054 has an active image array of 1280x720 pixels. The active pixels are read out progressively through column/row driver circuits. In order to reduce fixed pattern noise, CDS circuits are adopted. The analog signal is transferred to digital signal by 10 bit A/D converter. The digital signals are processed in the ISP Block. Users can easily control these functions via two-wire serial interface bus.

4. CSP Package Specifications

4.1 Pin Diagram (CSP)



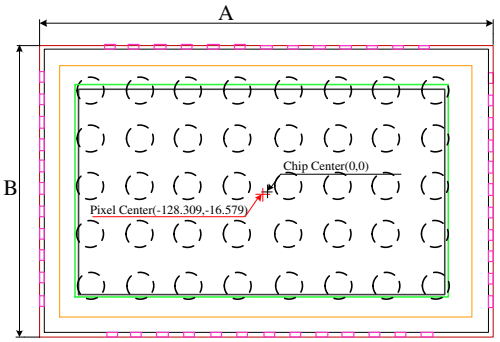
Top View

4.2 Pin Descriptions

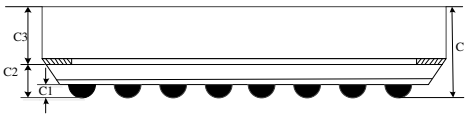
Pin	Name	Pin Type	Description
A1	AGND	Ground	Ground for analog
A2	SBCL	Input	Two-wire serial bus, clock
A3	RESETB	Input	Chip reset control: 0: chip reset 1: normal work
A4	SBDA	I/O	Two-wire serial bus, data
A5	HSYNC	Output	Horizontal sync output
A6	IN_CLK	Input	Sensor input clock
A7	MDN0	Output	MIPI data<0> (-)
A8	DVDD	Power	Digital power supply pin: 1.4~1.6V, please connect capacitor to digital ground.
B1	VPIX	Power	Internal power supply, please connect capacitor to analog ground.
B2	AVDD33	Power	Main power supply pin: 3.3V, Please connect capacitors to analog ground
B3	PWDN	Input	Sensor power down control: 0: normal work 1: standby
B4	FSYNC	I/O	Frame sync signal

B5	I2C_M_S	I/O	0：I2C slave 1：I2C master
B6	VSYNC	Output	Vertical reference output
B7	MCP	Output	MIPI clock (+)
B8	MDP0	Output	MIPI data<0> (+)
C1	VTX	Power	Internal power supply, please connect capacitor to analog ground.
C2	VREF	Power	Internal power supply, please connect capacitor to analog ground.
C3	VRSG	Power	Internal power supply, please connect capacitor to analog ground.
C4	D9	Output	Raw RGB Parallel data output bit[9]
C5	VDDIO	Power	Power supply for I/O circuits: 1.7~3.45V, Please connect capacitor to digital ground.
C6	DGND	Ground	Ground for digital
C7	MCN	Output	MIPI clock (-)
C8	DVDD	Power	Digital power supply pin: 1.4~1.6V, please connect capacitor to digital ground.
D1	DGND	Ground	Ground for digital
D2	DVDD	Power	Digital power supply pin: 1.4~1.6V, please connect capacitor to digital ground.
D3	D6	Output	Raw RGB Parallel data output bit[6]
D4	D4	Output	Raw RGB Parallel data output bit[4]
D5	D2	Output	Raw RGB Parallel data output bit[2]
D6	D0	Output	Raw RGB Parallel data output bit[0]
D7	DOUTP	Output	LVDS data output (+)
D8	DOUTN	Output	LVDS data output (-)
E1	D8	Output	Raw RGB Parallel data output bit[8]
E2	D7	Output	Raw RGB Parallel data output bit[7]
E3	D5	Output	Raw RGB Parallel data output bit[5]
E4	D3	Output	Raw RGB Parallel data output bit[3]
E5	D1	Output	Raw RGB Parallel data output bit[1]
E6	PCLK	Output	Pixel clock output
E7	DVDD	Power	Digital power supply pin: 1.4~1.6V, please connect capacitor to digital ground.
E8	DGND	Ground	Ground for digital

4.3 Package Specification (unit: mm)

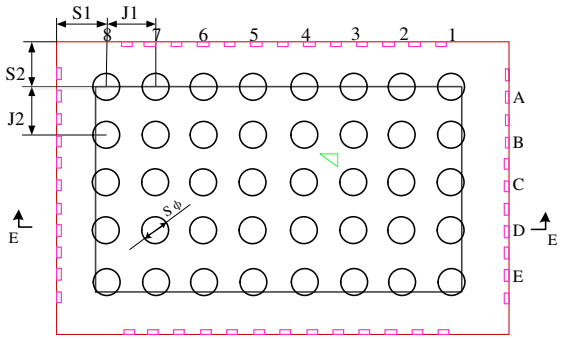


Top View(Image Side)



Cross Section view(E-E)

Notch



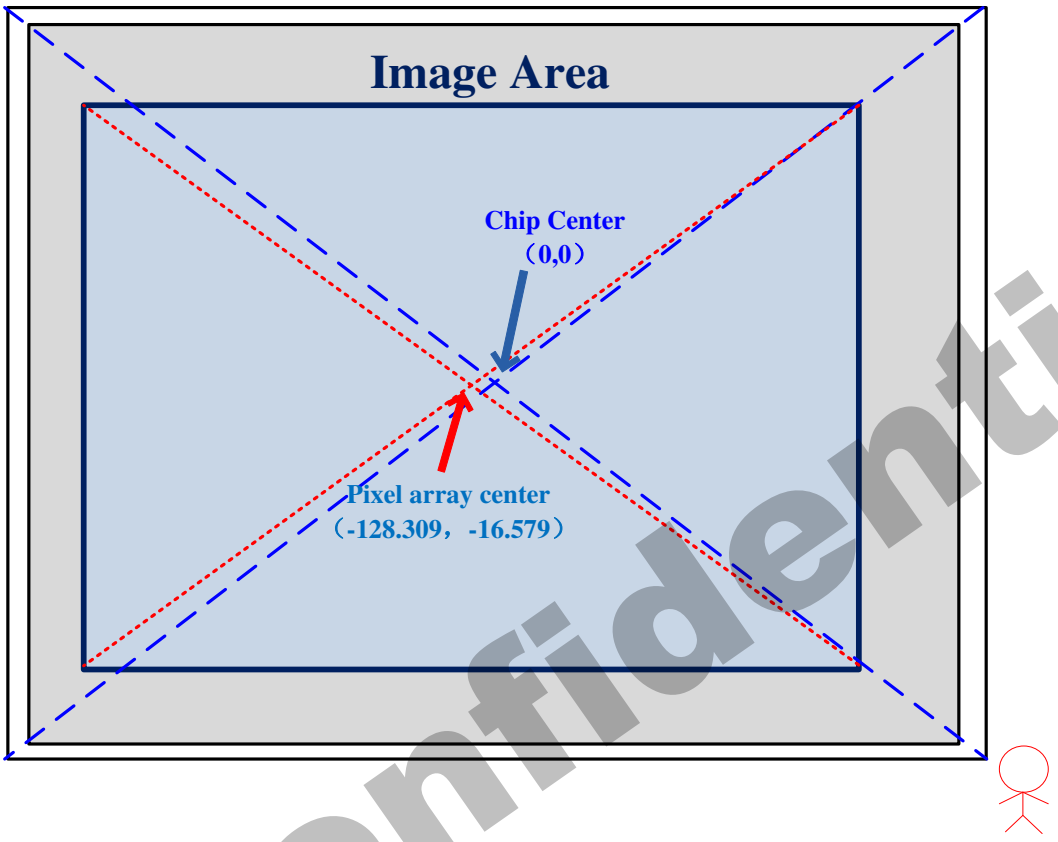
Bottom View(BGA Side)

Package Size:5030*3130
Ball pitch:X:600
Y:590
Ball Diameter:300

Description	Symbol	Nominal	Min.	Max.
		Millimeters		
Package Body Dimension X	A	5.0300	5.0050	5.0550
Package Body Dimension Y	B	3.1300	3.1050	3.1550
Package Height	C	0.7100	0.6550	0.7650
Ball Height	C1	0.1500	0.1200	0.1800
Thickness from ball to wafer surface	C2	0.2775	0.2375	0.3175
Thickness from top glass surface to wafer surface	C3	0.4325	0.4175	0.4475
Ball Diameter	SΦ	0.3000	0.2700	0.3300
Total Ball Count	N	40		
Ball Count X axis	N1	8		
Ball Count Y axis	N2	5		
Pins Pitch X axis	J1	0.6000	0.5900	0.6100
Pins Pitch Y axis	J2	0.5900	0.5800	0.6000
BGA ball center to package center offset in X-direction	X	0.0000	-0.0250	0.0250
BGA ball center to package center offset in Y-direction	Y	0.0000	-0.0250	0.0250
Edge to Ball Center Distance along X	S1	0.4150	0.3850	0.4450
Edge to Ball Center Distance along Y	S2	0.3850	0.3550	0.4150

5. Optical Specifications

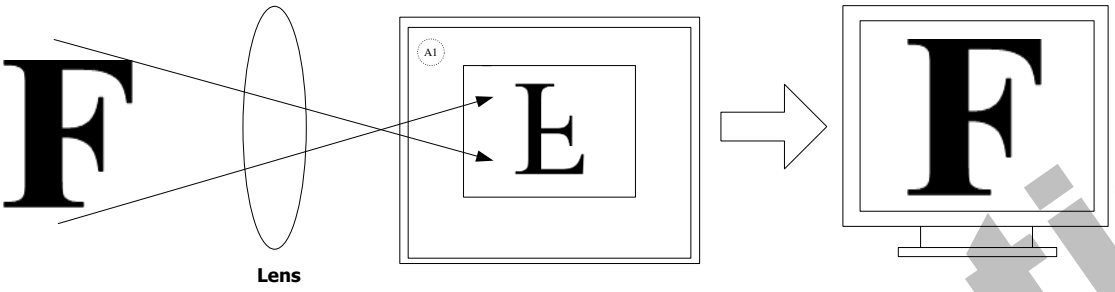
5.1 Optical Center (unit: μm)



Top View

5.2 Readout Position

The GC1054 default status is readout from the lower left corner with pin A1 located in the upper left corner. The proper image output as follow when Pin A1 is located in the upper left corner as the lens inverts image vertically and horizontally.



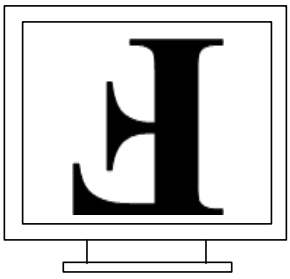
In addition, this system supports up/down and/or right/left inversion, and is capable of following outputs. When using the inversion function, the pixel array reads from the sensor changes, but this is processed adaptively within the ISP, so there is no need for users to be aware of it. However, care must be taken in RAW output mode, as the sensor data is output as is.

Readout direction can be set by the registers.

Function	Register Address	Register Value	First Pixel
Normal	P0:0x17[1:0]	00	R
Horizontal mirror	P0:0x17[1:0]	01	Gr
Vertical Flip	P0:0x17[1:0]	10	Gb
Horizontal Mirror and Vertical Flip	P0:0x17[1:0]	11	B

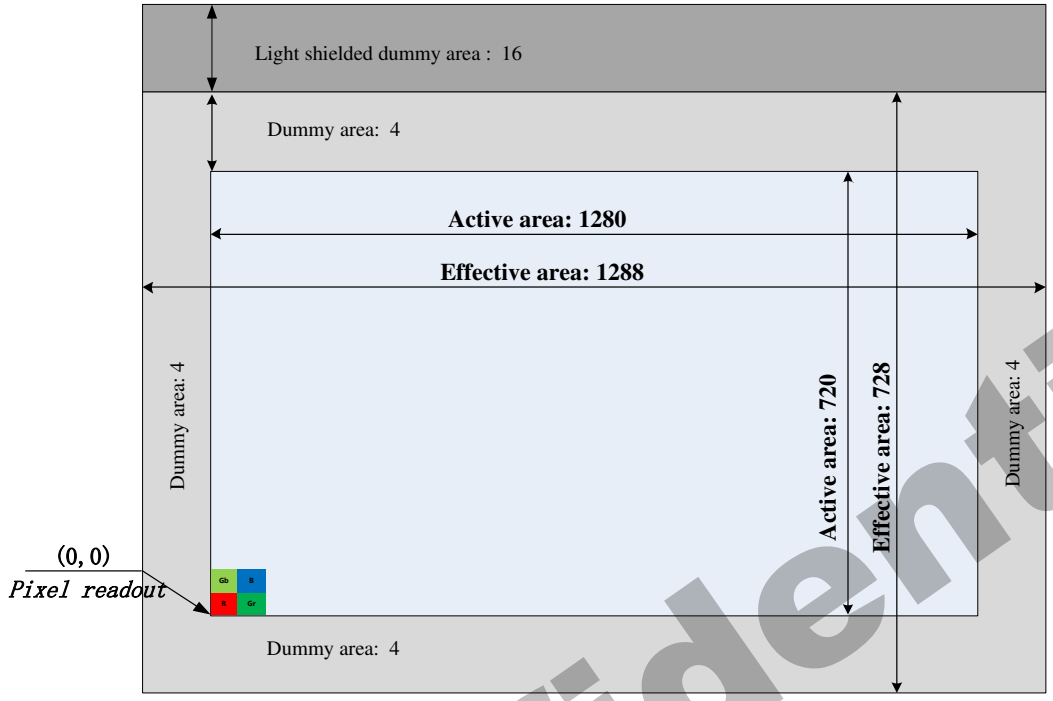
Horizontal Mirror

Vertical Flip



Horizontal Mirror and Vertical Flip

5.3 Pixel Array



Pixel array is covered by Bayer pattern color filters. The primary color BG/GR array is arranged in line-alternating way.

If no flip in column, column is read out from 0 to 1279. If flip in column, column is read out from 1279 to 0.

If no flip in row, row is read out from 0 to 719.If flip in row, row is read out from 719 to 0.

5.4 Lens Chief Ray Angle (CRA)

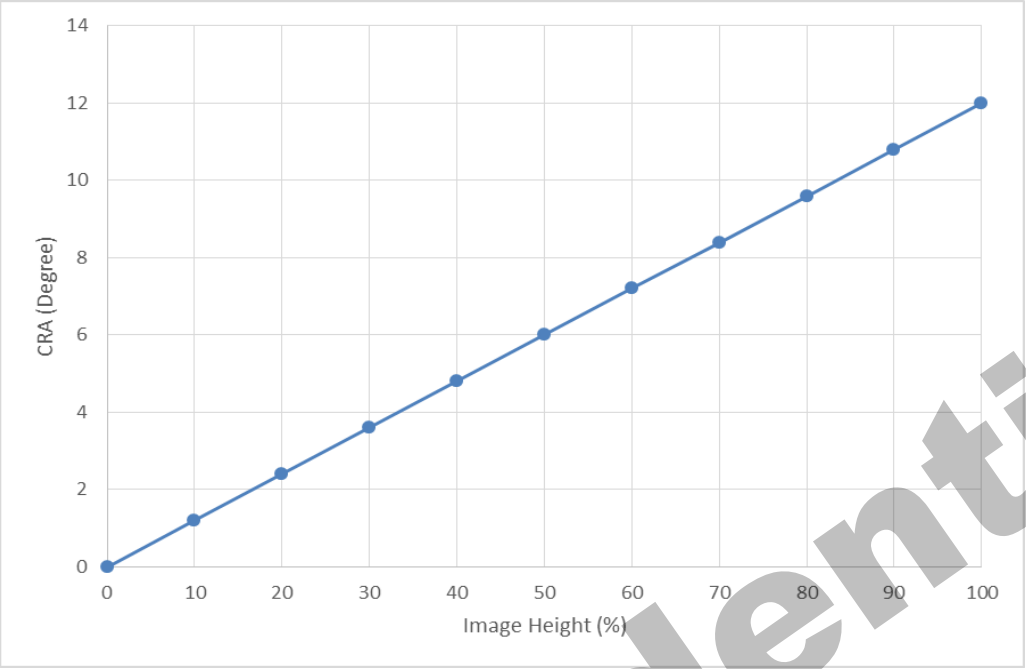
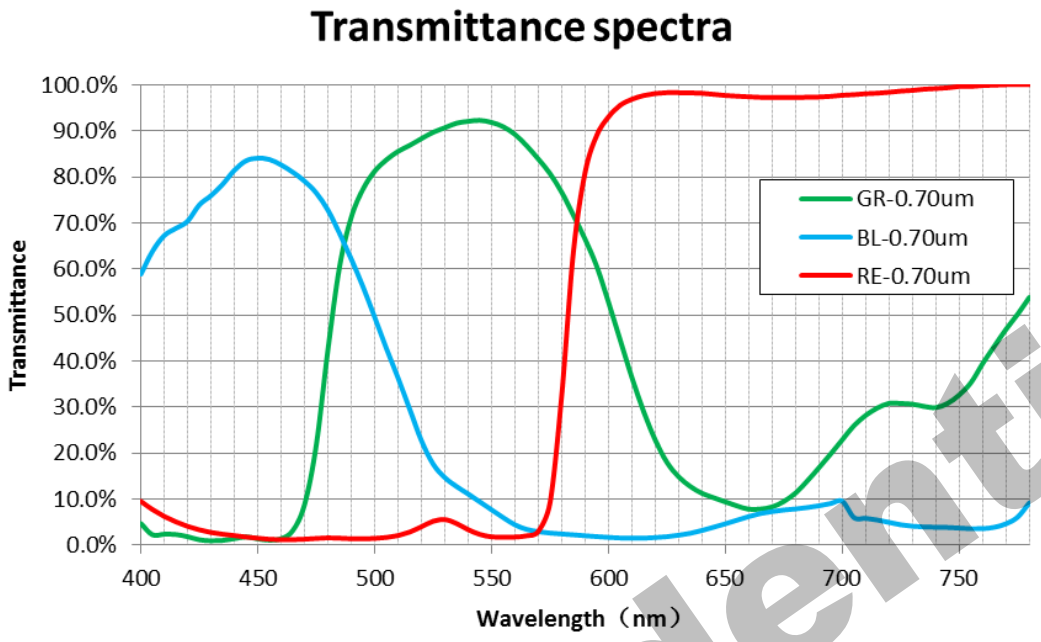


Image Height (%)	Image Height (mm)	CRA (degree)
0	0	0
10	0.2197	1.2
20	0.4394	2.4
30	0.6591	3.6
40	0.8788	4.8
50	1.0985	6
60	1.3182	7.2
70	1.5379	8.4
80	1.7576	9.6
90	1.9773	10.8
100	2.197	12

5.5 Color Filter Spectral Characteristics

The optical spectrum of color filters is shown below



6. Two-wire Serial Bus Communication

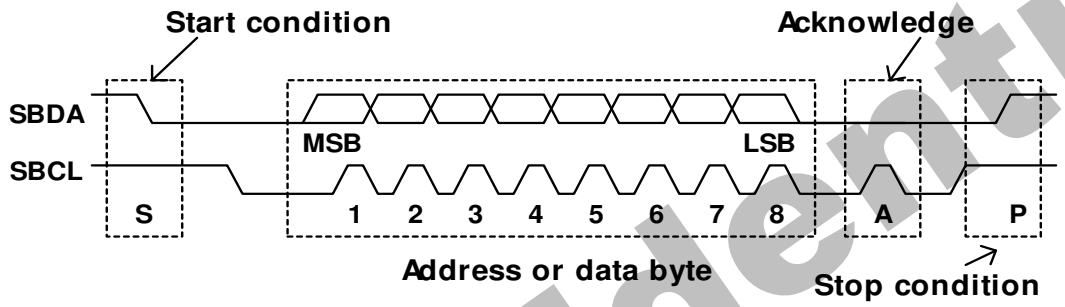
GC1054 Device Address:

Serial bus write address = 0x42 Serial bus read address = 0x43

6.1 Protocol

The host must perform the role of a communications master and GC1054 acts as either a slave receiver or transmitter. The master must do

- Generate the **Start(S)/Stop(P)** condition
- Provide the serial clock on **SBCL**.



Single Register Writing:

S	42H	A	Register Address	A	Data	A	P

Incremental Register Writing:

S	42H	A	Register Address	A	Data(1)	A	……	Data(N)	A	P

Single Register Reading:

S	42H	A	Register Address	A	S	43H	A	Data	NA	P

Notes:

From master to slave From slave to master

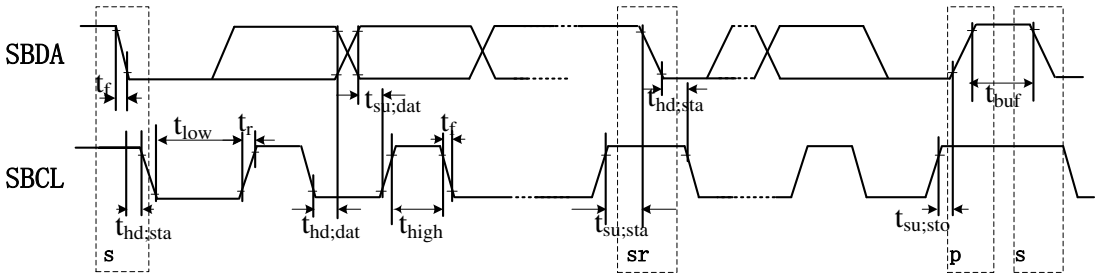
S: Start condition **P:** Stop condition

A: Acknowledge bit **NA:** No acknowledge

Register Address: Sensor register address

Data: Sensor register value

6.2 Serial Bus Timing

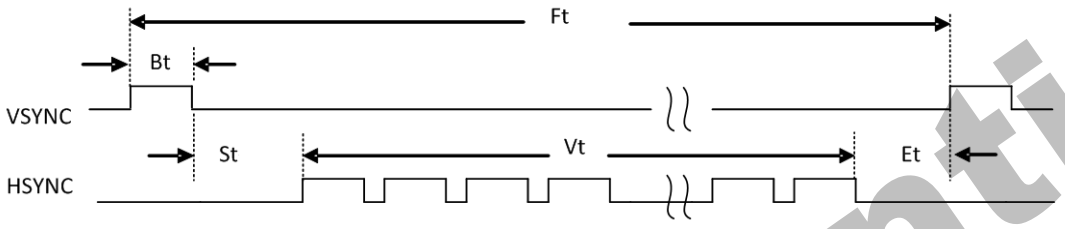


Parameter	Symbol	Min.	Typ.	Max.	Unit
SBCL clock frequency	F_{scl}	0	--	400	KHz
Bus free time between stop and start condition	t_{buf}	1.3	--	--	μs
Hold time for a repeated start	$t_{hd;sta}$	0.6	--	--	μs
LOW period of SBCL	t_{low}	1.3	--	--	μs
HIGH period of SBCL	t_{high}	0.6	--	--	μs
Set-up time for a repeated start	$t_{su;sta}$	0.6	--	--	μs
Data hold time	$t_{hd;dat}$	0	--	0.9	μs
Data Set-up time	$t_{su;dat}$	100	--	--	Ns
Rise time of SBCL, SBDA	t_r	--	--	300	Ns
Fall time of SBCL, SBDA	t_f	--	--	300	Ns
Set-up time for a stop	$t_{su;sto}$	0.6	--	--	μs
Capacitive load of bus line (SBCL, SBDA)	C_b	--	--	--	Pf

7. Applications

7.1 DVP timing

Suppose Vsync is low active and Hsync is high active, and output format is RAW Bayer 10bit/8bit, then the timing of Vsync and Hsync is bellowing (take capture mode for example, preview mode is the same):



Ft =VB+ Vt +16 (dark line) (unit is row_time)

VB+16 = Bt + St + Et, Vblank/Dummy line, setting by register P0:0x07 and P0:0x08.

Ft -> Frame time, one frame time.

Bt -> Blank time, Vsync no active time.

St -> Start time, setting by register P0:0x13.

Et –> End time, setting by register P0:0x14.

Vt -> valid line time. Vt = win_height, win_height is setting by register P0:0x0d and P0:0x0e.

When exp_time ≤ win_height + VB+16, Bt = VB+16 – St - Et. Frame rate is controlled by window_height + VB+16.

When exp_time > win_height + VB+16, Bt = exp_time - win_height – St - Et. Frame rate is controlled by exp_time.

The following is row_time calculate:

row_time = (Hb+16+INT((win_width+Sh_delay)/4))/QWPCLK

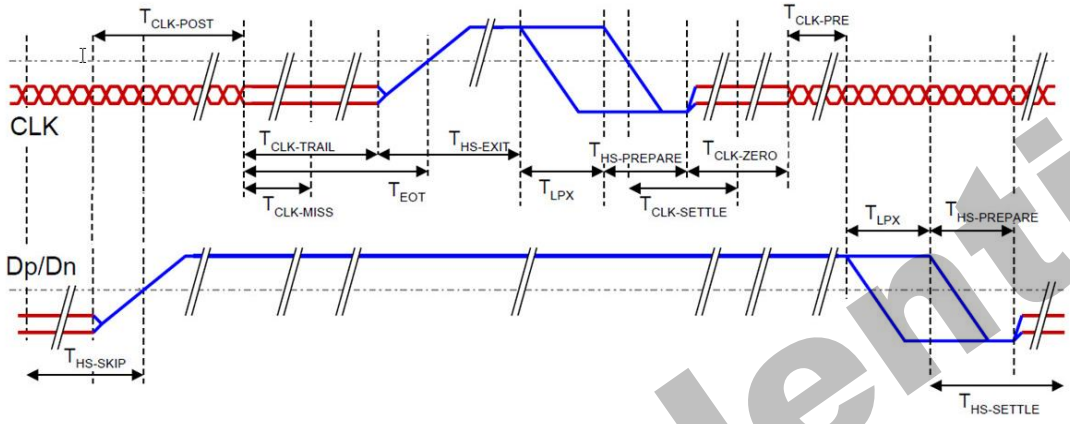
Hb –> HBlank or dummy pixel，Setting by register P0:0x05 and P0:0x06.

Sh_delay -> Setting by register P0:0x2c.

win_width -> Setting by register P0:0x0f and P0:0x10, win_width = final_output_width + 8.

QWPCLK ->1/4 WPCLK.

7.2 Clock lane low-power



Notice:

- Clock must be reliable during high speed transmission and mode-switching.
- Clock can go to LP only if data lanes are in LP (and nothing relies on it).
- In Low-Power data lanes are conceptually asynchronous (independent of the high speed clock).

$T_{CLK\_HS\_PREPARE}$: setting by Register P3: 0x22

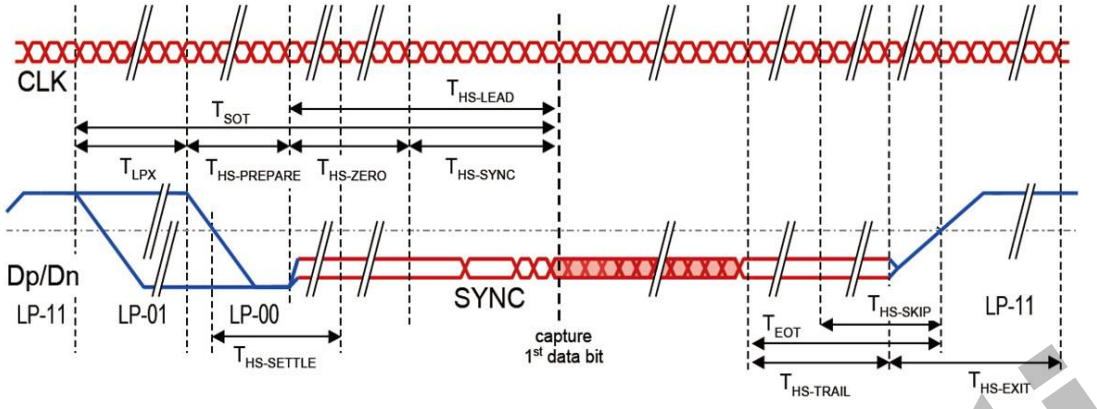
T_{CLK_ZERO}: setting by Register P3: 0x23

T_{CLK_PRE}: setting by Register P3: 0x24

T_{CLK_POST}: setting by Register P3: 0x25

T_{CLK_TRAIL}: setting by Register P3: 0x26

7.3 Data Burst



Notice:

- Clock keeps running and samples data lanes (except for lanes in LPS).
- Unambiguous leader and trailer sequences required to distill real bits.
- Trailer is removed inside PHY (a few bytes).
- Time-out to ignore line values during line state transition.

T_{LPX}: setting by Register P3:0x21

$T_{HS\_PREPARE}$: setting by Register P3: 0x29

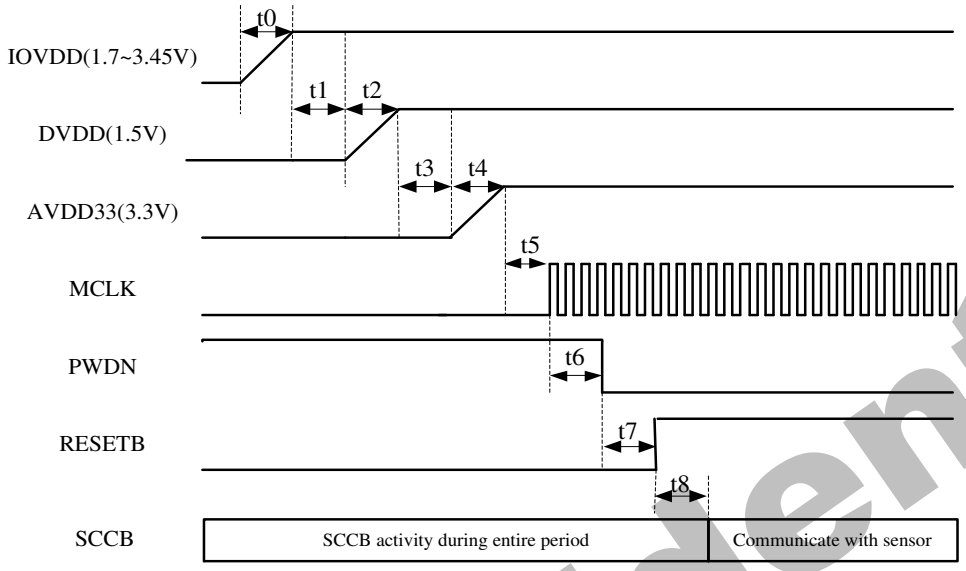
T_{HS_ZERO}: setting by Register P3: 0x2a

T_{HS_TRAIL}: setting by Register P3: 0x2b

T_{HS_EXIT}: setting by Register P3: 0x27

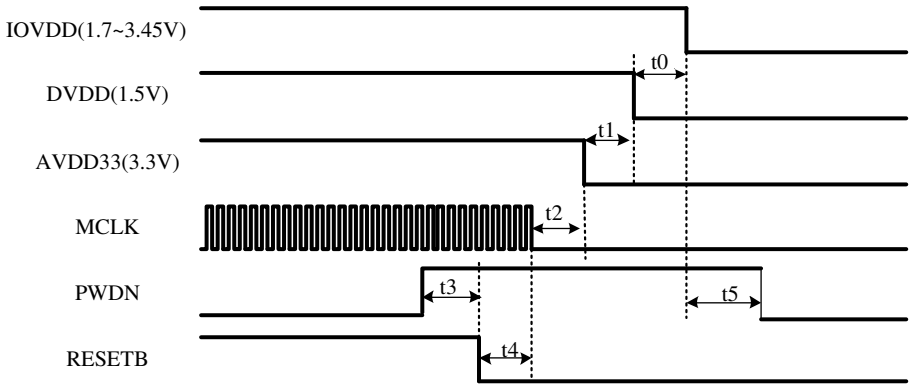
8. Power On/Off Sequence

8.1 Power on Sequence



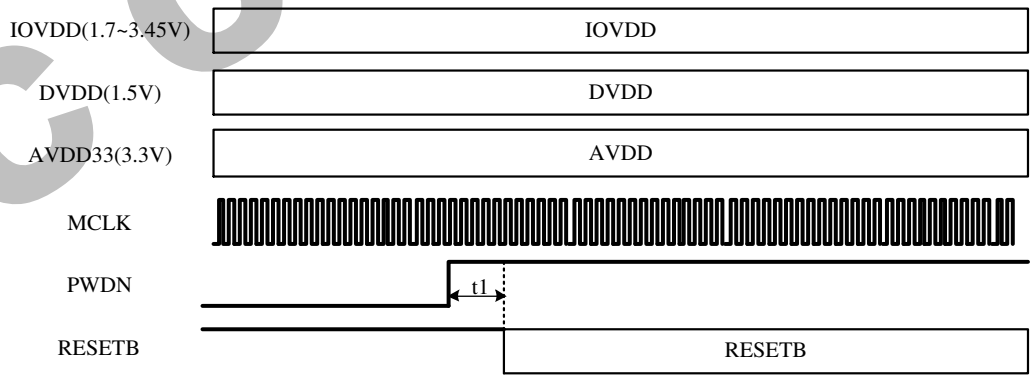
Parameter	Description	Min.	Max.	Unit
t0	IOVDD rising time	50		μs
t1	From IOVDD to DVDD	0		μs
t2	DVDD rising time	50		μs
t3	From DVDD to AVDD	50		μs
t4	AVDD rising time	50		μs
t5	From AVDD to MCLK applied	0		μs
t6	From MCLK applied to Sensor enable	0		μs
t7	From PWDN pull low to RESET pull high	0		μs
t8	From Power on to SCCB works	25		Mclk
MCLK	Frequency	6	27	MHz
MCLK	Duty cycle	45	55	%
SCCB	Frequency		400	KHz

8.2 Power off Sequence



Parameter	Description	Min.	Max.	Unit
t0	From IOVDD power down to PWDN pull low	0		μs
t1	From DVDD to IOVDD power down	0		μs
t2	From AVDD to DVDD power down	0		μs
t3	From MCLK disable to sensor AVDD power down	0		μs
t4	From sensor disable to RESET pull low	0		μs
t5	From sensor RESET pull low to MCLK disable	0		μs

8.3 Standby Sequence



Parameter	Description	Min.	Max.	Unit
t1	From sensor disable to RESETB pull low(if possible)	0		μs

9. Register List

System Register

Address	Name	Width	Default Value	R/W	Description
0xf0	Sensor_ID_high	8	0x10	RO	Sensor_ID
0xf1	Sensor_ID_low	8	0x54	RO	Sensor_ID
0xf2	pad_buf_mode pad_vb_hiz_mode I2C_open_ena pwd_dn data_pad_io, sync_pad_io	8	0x0f	RW	[7] pad_buf_mode [6] pad_vb_hiz_mode [5] I2C_open_ena [4] pwd_dn [3] data_pad_io [2:0] sync_pad_io
0xf4	clk_div_ratio[15:8]	8	0x07	RW	total read No.
0xf5	clk_div_ratio[7:0]	8	0xf0	RW	
0xf6	I2C_master_mode	8	0x0f	RW	[7] ignore if fail [6:4] master speed initial slow [3:0] try num
0xf7	PLL_mode1	8	0x00	RW	[7] FPD_mode [6] freq_div2_analog [4] buf_signal for hdr [3] FPD_clock_out_mode [2] cisctl regf regw sel [1] div2en [0] plldg_en
0xf8	PLL_mode2	8	0x00	RW	[6] close_2_frame_freq [5:0] digital pll div
0xf9	lvds_pll_en lvds_div7_en analog_pwc	6	0x21	RW	[5] lvds_pll_en [4] lvds_div7_en [3:2] lpldo_r [1]lpldo_en [0] apwd
0xfa	clk_div_mode	8	0x00	RW	[7] wclk div2 [6] txclk_sel [5] lvds pll mode2 en [4:0] LVDS_pll_div
0xfb	i2c_device_id	8	0x42	RO	[7:1] i2c_device_id [0] NA
0xfc	cm_mode	8	0x00	RW	[7] regf clk enable [6] mclk en [5] div2_mode [4] div2

					[3] isp all clock enable [2] serail_clk enable [1] re_lock_pll [0] not_use_pll
0xfd	mdclk_en updn REG_BUF_mode	8	0x00	RW	[7] mdclk_en [6:5] updn [4] CEN always enable [3] buf_en [1] sel_buf2 [0] sel_buf1
0xfe	Reset Page_select	8	0x00	RW	[7] soft_reset [6] cm_reset [5] mipi_reset [4] CISCTL_restart_n [3] spi_reset [2:0] page_select

Analog & CISCTL

Address	Name	Width	Default Value	R/W	Description
P0:0x01	CISCTL_buf_exp2[12:8]	5	0x00	RW	[4:0] Exposure2[12:8]
P0:0x02	CISCTL_buf_exp2[7:0]	8	0x04	RW	Exposure2[7:0]
P0:0x03	CISCTL_buf_exp[12:8]	5	0x00	RW	Exposure[12:8]
P0:0x04	CISCTL_buf_exp[7:0]	8	0x10	RW	Exposure[7:0]
P0:0x05	buf_CISCTL_hb[11:8]	4	0x01	RW	H Blanking(hb)
P0:0x06	buf_CISCTL_hb [7:0]	8	0xf4	RW	
P0:0x07	VB[12:8]	5	0x00	RW	Vertical blanking(vb)
P0:0x08	VB[7:0]	8	0x10	RW	
P0:0x09	row_start[9:8]	2	0x00	RW	Row Start
P0:0x0a	row_start[7:0]	8	0x00	RW	
P0:0x0b	Col_start[10:8]	3	0x00	RW	Col start
P0:0x0c	Col_start[7:0]	8	0x00	RW	
P0:0x0d	win_height[9:8]	3	0x02	RW	[7:3] NA [2:0] Window height[9:8]
P0:0x0e	win_height[7:0]	8	0xe0	RW	Window height[7:0]
P0:0x0f	win_width[10:8]	3	0x05	RW	[7:3] NA [2:0] Window width[10:8]
P0:0x10	win_width[7:0]	8	0x08	RW	window width[7:0]

P0:0x11	Reserved	8	0x32	RW	Reserved
P0:0x12	Reserved	8	0xc2	RW	Reserved
P0:0x13	CISCTL_vs_st	8	0x11	RW	Vs_st
P0:0x14	CISCTL_vs_et	8	0x01	RW	Vs_et
P0:0x15	Reserved	8	0x00	RW	Reserved
P0:0x16	Reserved	8	0x01	RW	Reserved
P0:0x17	CISCTL_mode1	8	0xc0	RW	[7:2] Reserved [1] updown [0] mirror
P0:0x22	ANALOG_ADC_r	8	0x48	RW	[7:4] Reserved [3:2] drv_sync [1:0] Reserved
P0:0x2c	CISCTL_sh_delay	8	0x18	RW	buf_CISCTL_sh_delay
P0:0x34	sync_with_colgain_mode sync_with_exp_mode vrefsw_reg ctsdsun_mode	8	0x00	RW	[5:4] Reserved [3:2] drv_data_low [1:0] Reserved
P0:0xcd	ANALOG_mode1	8	0x9a	RW	[7:2] Reserved [1:0] drv_pclk
P0:0xd2	Dac_ctl2	8	0xc5	RW	[7:6] Reserved [5:4] drv_data_high [3:0] Reserved

CSI/PHY1.0

Address	Name	Width	Default Value	R/W	Description
P3:0x01	DPHY_analog_mode1	8	0x00	RW	[7:5] NA [4] data0ctr [1] dphy_data0_en [0] dphy_clk_en
P3:0x02	DPHY_analog_mode2	8	0x00	RW	[6:4] data0diff [3] clkctr [2:0] clk_diff
P3:0x03	DPHY_analog_mode3	8	0x00	RW	[7] clklane_p2s_sel [6] NA [5] data0 delay1s [4] clk delay1s [1:0] disable_set
P3:0x04	FIFO_prog_full_level[7:0]	8	0x04	RW	FIFO_prog_full_level[7:0]

P3:0x05	FIFO_prog_full_level[11:8]	4	0x00	RW	[7:4] NA [3:0] FIFO_prog_full_level[11:8]
P3:0x06	FIFO_mode	8	0x00	RW	[6] manual CSI2_up mode [5] mipi write gate mode [4] fifo_rst_n_mode [3] bit10_switch_mode [1] write fifo gate [0] read fifo gate
P3:0x10	buf_CSI2_mode	8	0x00	RW	[7] CSI2_LE [5] ULP_mode [4] MIPI_ena [2] RAW8 [1] line_sync_mode [0] double_lane
P3:0x11	LDI_set	8	0x2b	RW	RAW10:2b / RAW8:2a
P3:0x12	LWC_set[7:0]	8	0x40	RW	1280x5/4 RAW10
P3:0x13	LWC_set[15:8]	8	0x06	RW	
P3:0x14	SYNC_set	8	0xb8	RW	SYNC_set
P3:0x15	DPHY_mode	8	0x10	RW	[6] mipi para invar when div2 [5] DATA lane gate [4] all_lane_open_mode [3:2] switch_msb_mode [1:0] clklane_mode
P3:0x16	LP_set	8	0x29	RW	[7:6] hi-z [5:4] lp_new [3:2] lp_one [1:0] lp_zero
P3:0x20	T_init_set	8	0x80	RW	Timing of initial setting, more than 100 us
P3:0x21	T_LPX_set	8	0x10	RW	Timing of LP setting, more than 50ns
P3:0x22	T_CLK_HS_PREPARE_set	8	0x05	RW	Timing of COCLK HS PREPARE setting, 38ns ~95ns LP00
P3:0x23	T_CLK_zero_set	8	0x30	RW	Timing of COCLK HS zero setting, more than 300ns
P3:0x24	T_CLK_PRE_set	8	0x02	RW	Timing of COCLK HS PRE of Data setting, more than 8UI
P3:0x25	T_CLK_POST_set	8	0x10	RW	Timing of COCLK HS Post of Data setting, 60ns +52UI
P3:0x26	T_CLK_TRAIL_set	8	0x08	RW	Timing of COCLK tail setting, 60ns
P3:0x27	T_HS_exit_set	8	0x10	RW	Timing of HS exit setting, more than 100ns
P3:0x28	T_wakeup_set	8	0xa0	RW	Timing of wakeup setting, 1ms

P3:0x29	T_HS_PREPARE_set	8	0x06	RW	Timing of data HS PREPARE setting, 45+4UI~85+5UI
P3:0x2a	T_HS_Zero_set	8	0x0a	RW	Timing of data HS zero setting, 140ns
P3:0x2b	T_HS_TRAIL_set	8	0x08	RW	Timing of data HS trail setting, 60ns
P3:0x30	MIPI_test	4	0x00	RW	[3] test clk hsvalid [2] test data hsvalid [1] mipi test clk mode [0] mipi test
P3:0x31	MIPI_test_data0	8	0x96	RW	MIPI_test_data0
P3:0x32	MIPI_test_data1	8	0x3a	RW	MIPI_test_data1
P3:0x33	MIPI_test_data2	8	0x87	RW	MIPI_test_data2
P3:0x34	MIPI_test_data3	8	0xb5	RW	MIPI_test_data3
P3:0x40	output_buf_mode1	8	0x00	RW	[2:1] delay_half_mode [0] output_buf_enable
P3:0x41	output_buf_mode2	8	0x00	RW	[2] pclk_buf_gate [1] buf_opclk_polarity [0] hsync polarity
P3:0x42	buf_win_width[7:0]	8	0x00	RW	buf_win_width[7:0]
P3:0x43	buf_win_width[11:8]	8	0x05	RW	buf_win_width[11:8]
P3:0x44	Win_end	4	0x00	RW	Win_end

ISP Related

Address	Name	Width	Default Value	R/W	Description
P1:0x00	Reserved	8	0x08	RW	Reserved
P1:0x01	Reserved	2	0x03	RW	Reserved
P1:0x17	CFA_sequence	4	0x00	RW	[3:2] CTL_CFA_sequence [1:0] CTL_dark_CFA_sequence
P1:0x80	block_enable1_buf	8	0x00	RW	[7] de_grid_en [6] BFF en [5] auto_dd_en [4] first_dd_en [3:2] Reserved
P1:0x88	debug_mode4	8	0xf3	RW	[7] Reserved [6] pclk_out_polarity [5] hsync_polarity [4] vsync_polarity [3:0] Reserved
P1:0x89	bypass_mode	8	0x03	RW	[7:6] Reserved

					[5] DNDD_out_mode [4] PREGAIN_out_mode [3:2] Reserved [1:0] bypass bits
P1:0x8c	debug_mode2	8	0x00	RW	[7] data delay half pclk [6] hsync delay half pclk [5:4] Reserved [3] test_image when in VGA or UXGA [2] input_test_image [1] LSC_test_image, [0] OUT test_image
P1:0x8f	Debug_mode5	8	0x09	RW	[4] gain_switch_A_mode2_delay [3] A_mode2_change_close_frame_en [2:0] A_mode2_change_num
P1:0x90	win_mode_buf	1	0x01	RW	[7:1] NA [0] crop out win mode
P1:0x91	out_win_y1[9:8]	2	0x00	RW	[7:3] NA [1:0] Crop _win_y1[9:8]
P1:0x92	out_win_y1[7:0]	8	0x00	RW	Crop _win_y1[7:0]
P1:0x93	out_win_x1[10:8]	3	0x00	RW	[7:3] NA [2:0] Crop _win_x1[11:8]
P1:0x94	out_win_x1[7:0]	8	0x00	RW	Crop _win_x1[7:0]
P1:0x95	out_win_height[9:8]	3	0x02	RW	[7:3] NA [1:0] Out window height[9:8]
P1:0x96	out_win_height[7:0]	8	0xd0	RW	Out window height[7:0]
P1:0x97	out_win_width[10:8]	3	0x05	RW	[7:3] NA [2:0] Out window width[11:8]
P1:0x98	out_win_width[7:0]	8	0x00	RW	Out window width[7:0]

BLK

Address	Name	Width	Default Value	R/W	Description
P1:0x40	Blk_mode1	8	0x23	RW	[7:2] Reserved [1] BLK_dark_current_en [0] BLK_offset_en
P1:0x45	manual_G1_odd_offset	8	0x00	RW	manual_G1_odd_offset
P1:0x46	manual_R1_odd_offset	8	0x00	RW	manual_R1_odd_offset
P1:0x47	manual_B2_odd_of	8	0x00	RW	manual_B2_odd_offset

	fset				
P1:0x48	manual_G2_odd_offset	8	0x00	RW	manual_G2_odd_offset
P1:0x60	offset_ratio_G1	8	0x60	RW	offset_ratio_G1,1.7
P1:0x61	dark_current_ratio_G1	8	0x20	RW	dark_current_ratio_G1, 1.7

GLOBAL/PRE/POSTGAIN

Address	Name	Width	Default Value	R/W	Description
P1:0xb0	buf_global_gain	8	0x40	RW	Global gain
P1:0xb1	buf_auto_pregain_sync[11:8]	4	0x01	RW	[7:4] NA [3:0] Auto_pregain_sync[11:8]
P1:0xb2	buf_auto_pregain[7:0]	8	0x00	RW	[7:0] Auto_pregain[7:0] [1:0] NA
P1:0xb4	Total_gain_manual [15:8]	8	0x01	RW	Total_gain_manual [15:8]
P1:0xb5	Total_gain_manual [7:0]	8	0x00	RW	Total_gain_manual [7:0]
P1:0xb6	buf_col_code	4	0x01	RW	[7:4] NA [3:0] Col_code
P1:0xb7	Reserved	1	0x00	RW	Reserved
P1:0xb8	channel_gain_G1_odd	8	0x80	RW	Channel_gain_G1_odd[10:3]
P1:0xb9	channel_gain_R1_odd	8	0x80	RW	Channel_gain_R1_odd[10:3]
P1:0xba	channel_gain_B2_odd	8	0x80	RW	Channel_gain_B2_odd[10:3]
P1:0xbb	channel_gain_G2_odd	8	0x80	RW	Channel_gain_G2_odd[10:3]
P1:0xbc	Channel_gain_G1_odd[2:0] Channel_gain_R1_odd[2:0]	8	0x00	RW	[5:3] channel_gain_G1_odd[2:0] [2:0] channel_gain_R1_odd[2:0]
P1:0xbd	Channel_gain_B2_odd[2:0] Channel_gain_G2_odd[2:0]	8	0x00	RW	[5:3] channel_gain_B2_odd[2:0] [2:0] channel_gain_G2_odd[2:0]

DD

Address	Name	Width	Default Value	R/W	Description
P4:0x42	de_grid_mode	8	0x00	RW	[5:2] Reserved [1:0] de_grid_mode
P4:0x81	DD_dark_bright_TH	8	0x05	RW	dark_bright_th
P4:0x83	DD_ratio	8	0xf2	RW	[7:2] Reserved [1:0] DD_ratio
P4:0x84	DD_is_bright_dark_th	8	0x33	RW	[7:4] bright_th [3:0] dark_th
P4:0x88	DD_luma_value_dd_th2	8	0x40	RW	DD_luma_value_dd_th2
P4:0x89	DD_luma_value_dd_th3	8	0x30	RW	DD_luma_value_dd_th3
P4:0x8a	DD_luma_value_dd_th4	8	0x20	RW	DD_luma_value_dd_th4
P4:0x8c	bright_no_dd2_th	8	0x40	RW	bright_no_dd2_th
P4:0x8d	bright_no_dd3_th	8	0x20	RW	bright_no_dd3_th
P4:0x8e	dark_no_dd2_th	8	0x40	RW	dark_no_dd2_th
P4:0x8f	dark_no_dd3_th	8	0x20	RW	dark_no_dd3_th
P4:0x90	luma_no_dd_th2	8	0x80	RW	luma_no_dd_th2
P4:0x91	luma_no_dd_th3	8	0x40	RW	luma_no_dd_th3

DARK OFFSET

Address	Name	Width	Default Value	R/W	Description
P4:0x40	WB_offset	8	0x00	RW	WB_offset