OmniVision

datasheet

PRELIMINARY SPECIFICATION

1/4" color CMOS 720p (1280 x 720) HD image sensor
with OmniPixel3-HS™ technology

OV9732

color CMOS 720p (1280 x 720) HD image sensor with OmniPixel3-HS™ technology

datasheet (CSP5)
PRELIMINARY SPECIFICATION

version 1.04
may 2015

To learn more about OmniVision Technologies, visit www.ovt.com.
OmniVision Technologies is publicly traded on NASDAQ under the symbol OVTI.

applications

- IP camera
- life style camera
- surveillance
- motion camera

ordering information

- **OV09732-H35A** (color, lead-free)
  35-pin CSP5

features

- support for image sizes: full size (1280x720), VGA (640x480), 2x2 RGB binning (640x360)
- support for output formats: 10-bit RAW output with 1-lane MIPI and DVP
- on-chip phase lock loop (PLL)
- programmable controls for frame rate, mirror and flip, gain/exposure, and windowing
- support for horizontal and vertical sub-sampling
- low power mode (LPM) function
- capable of maintaining register values at software power down
- standard SCCB interface
- GPIO tri-state configurability and programmable polarity
- FSIN
- image quality control: defect pixel correction (DPC) and automatic black level calibration (ABLC)

key specifications (typical)

- **active array size:** 1280 x 720
- **power supply:**
  analog: 3.1 ~ 3.45V (3.3V normal)
  core: 1.7 ~ 1.9V (1.8V normal)
  I/O: 1.7 ~ 1.9V (1.8V normal)
- **power requirements:**
  active: TBD
  standby: TBD
- **temperature range:**
  operating: -30°C to 70°C junction temperature (see **table 8-2**)
  stable image: 0°C to 50°C junction temperature (see **table 8-2**)
- **output formats:** 10-bit RAW RGB
- **lens size:** 1/4"
- **lens chief ray angle:** 9° (see **figure 10-2**)
- **input clock frequency:** 6 ~ 27 MHz (see **table 8-5**)
- **scan mode:** progressive
- **maximum image transfer rate:** 30 fps full resolution
- **sensitivity:** TBD
- **shutter:** rolling shutter
- **max S/N ratio:** TBD
- **dynamic range:** TBD
- **maximum exposure interval:** 798 x t_{ROW}
- **pixel size:** 3 µm x 3 µm
- **dark current:** TBD
- **image area:** 3888 µm x 2208 µm
- **package dimensions:** 4704 x 2994 µm

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1 signal descriptions

table 1-1 lists the signal descriptions and their corresponding pin numbers for the OV9732 image sensor. The package information is shown in **section 9**.

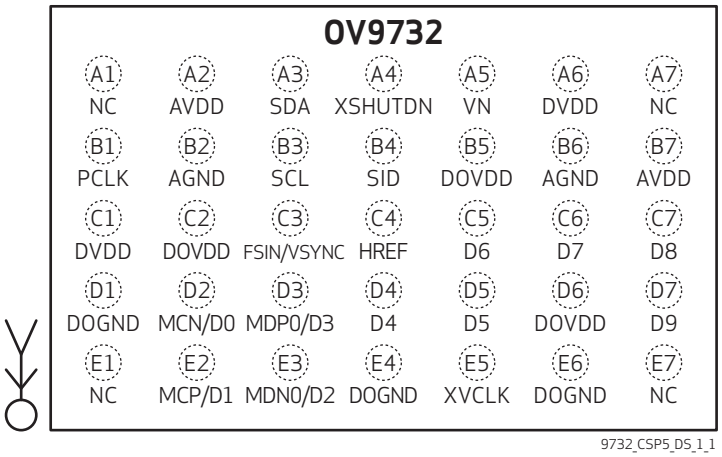
table 1-1 signal descriptions (sheet 1 of 2)

pin number	signal name	pin type	description
A1	NC	–	no connect
A2	AVDD	power	power for analog circuit
A3	SDA	I/O	SCCB data
A4	XSHUTDN	input	reset and power down (active low with internal pull down resistor)
A5	VN	reference	internal analog reference
A6	DVDD	power	power for digital circuit
A7	NC	–	no connect
B1	PCLK	I/O	DVP PCLK
B2	AGND	ground	ground for analog circuit
B3	SCL	input	SCCB input clock
B4	SID	input	SCCB address selection
B5	DOVDD	power	power for I/O circuit
B6	AGND	ground	ground for analog circuit
B7	AVDD	power	power for analog circuit
C1	DVDD	power	power for digital circuit
C2	DOVDD	power	power for I/O circuit
C3	FSIN/VSYNC	I/O	FSIN/VSYNC output
C4	HREF	I/O	DVP HREF output
C5	D6	I/O	DVP data bit 6 output
C6	D7	I/O	DVP data bit 7 output
C7	D8	I/O	DVP data bit 8 output
D1	DOGND	ground	ground for I/O circuit
D2	MCN/D0	I/O	MIPI TX clock lane negative output/DVP data bit 0 output
D3	MDP0/D3	I/O	MIPI TX data lane 0 positive output/DVP data bit 3 output
D4	D4	I/O	DVP data bit 4 output

table 1-1 signal descriptions (sheet 2 of 2)

pin number	signal name	pin type	description
D5	D5	I/O	DVP data bit 5 output
D6	DOVDD	power	power for I/O circuit
D7	D9	I/O	DVP data bit 9 output
E1	NC	–	no connect
E2	MCP/D1	I/O	MIPI TX clock lane positive output/DVP data bit 1 output
E3	MDN0/D2	I/O	MIPI TX data lane 0 negative output/DVP data bit 2 output
E4	DOGND	ground	ground for I/O circuit
E5	XVCLK	input	system input clock
E6	DOGND	ground	ground for I/O circuit
E7	NC	–	no connect

figure 1-1 pin diagram



9732_CSP5_DS_1_1

2 system level description

2.1 overview

The OV9732 color image sensor is a low voltage, high-performance 1/4-inch 720p CMOS image sensor that provides the full functionality of a single chip 720p (1280x720) and VGA (640x480) camera using OmniPixel3-HS™ technology. It provides full-frame, sub-sampled and cropped images in various formats via the control of the Serial Camera Control Bus (SCCB) interface.

The OV9732 has an image array capable of operating at up to 30 frames per second (fps) in 720p resolution and 45 fps in VGA resolution with complete user control over image quality, formatting and output data transfer. Some image processing functions, such as exposure control, defective pixel canceling are programmable through the SCCB interface. In addition, OmniVision image sensors use proprietary sensor technology to improve image quality by reducing or eliminating common lighting/electrical sources of image contamination, such as fixed pattern noise, smearing, etc., to produce a clean, fully stable, color image.

2.2 architecture

The OV9732 sensor core generates streaming pixel data at a constant frame rate. **figure 2-1** shows the functional block diagram of the OV9732 image sensor. **figure 2-2** shows an example application schematic using an OV9732 sensor.

The timing generator outputs clocks to access the rows of the imaging array, precharging and sampling the rows of the array sequentially. In the time between precharging and sampling a row, the charge in the pixels decreases with exposure to incident light. This is the exposure time in rolling shutter architecture.

The exposure time is controlled by adjusting the time interval between precharging and sampling. After the data of the pixels in the row has been sampled, it is processed through analog circuitry to correct the offset and multiply the data with corresponding gain. Following analog processing is the ADC which outputs 10-bit data for each pixel in the array.

figure 2-1 OV9732 block diagram

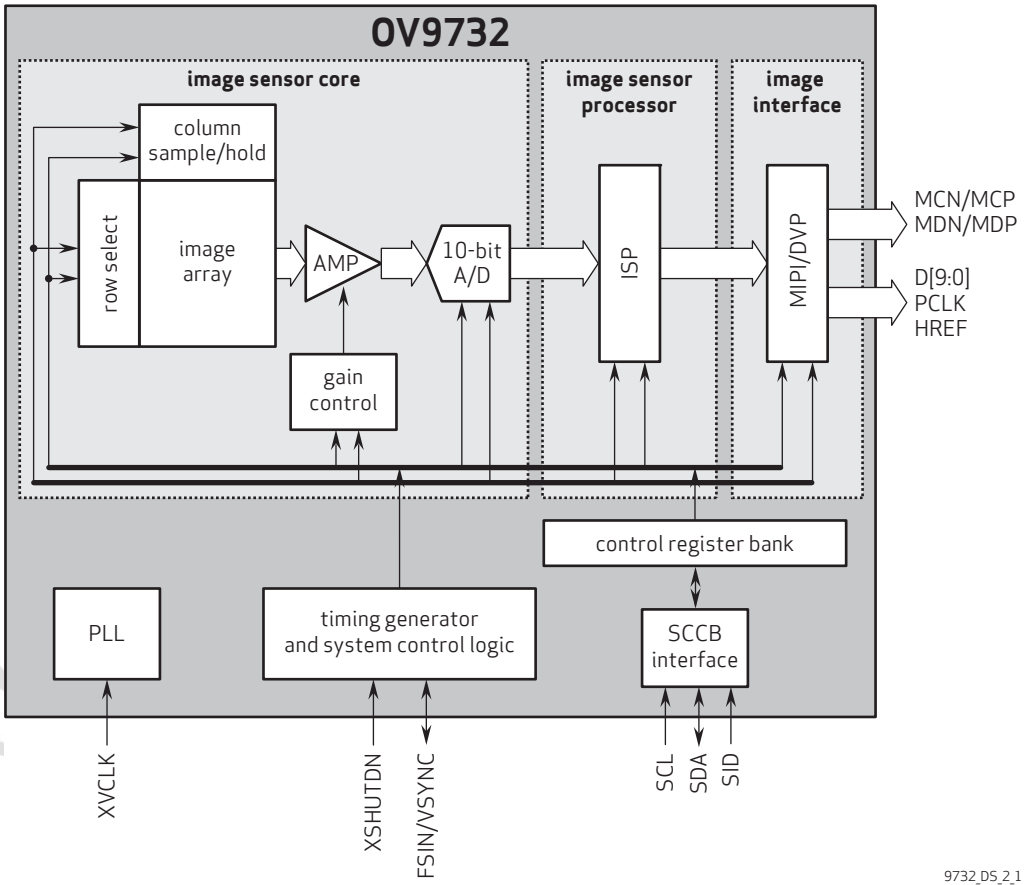
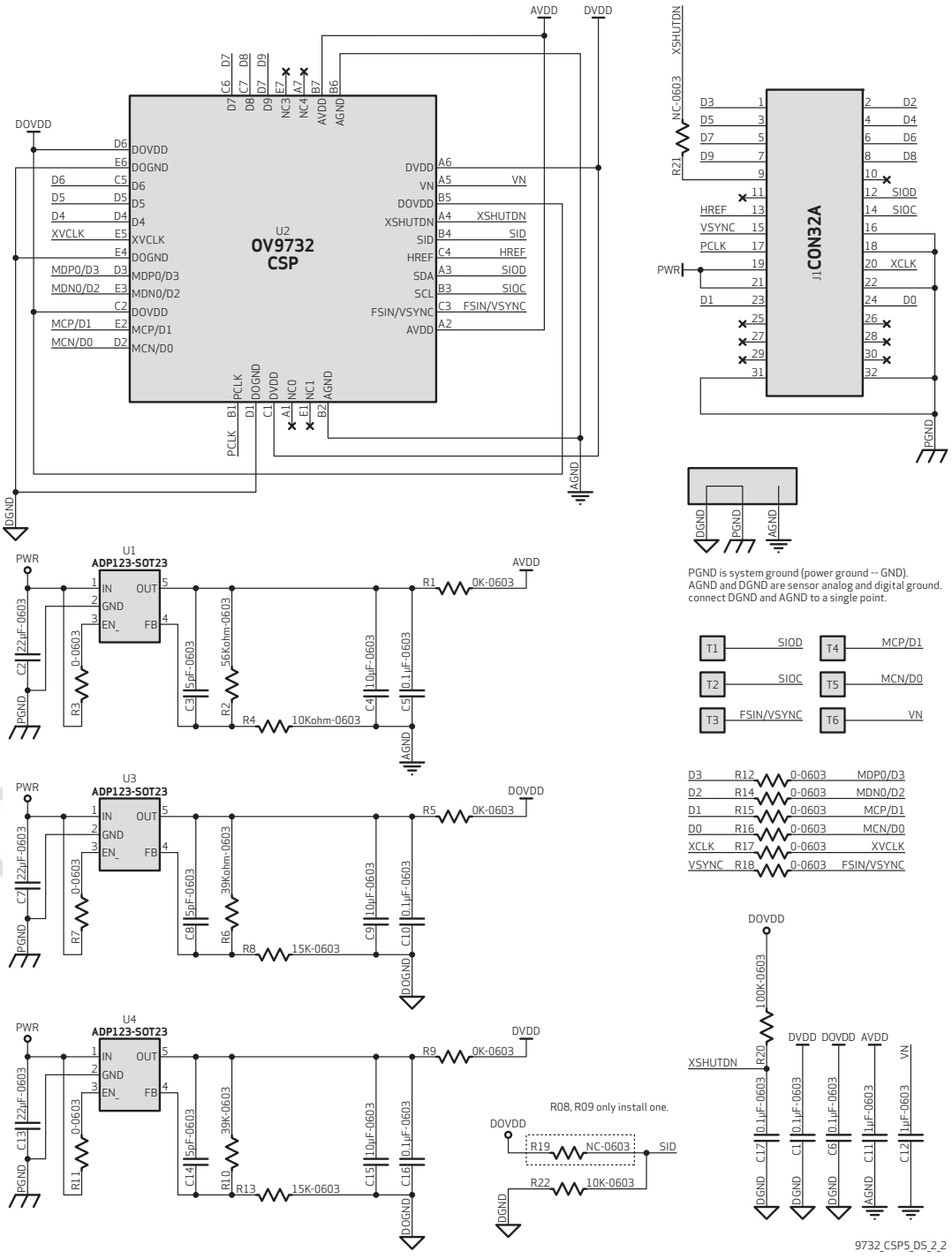


figure 2-2 reference design schematic (CSP5)



2.3 I/O control

The OV9732 I/O pad direction and driving capability can be easily adjusted. Driving capability and direction control for I/O pads lists the driving capability and direction control registers of the I/O pins.

table 2-1 driving capability and direction control for I/O pins

function	register	description
output drive capability control	0x3009	Bit[6:5]: output drive capability for MIPI/DVP 00: 1x 01: 2x 10: 3x 11: 4x
MIPI and DVP I/O control	0x3001	I/O control for MIPI may control any clock and data depending on the signal on certain output ports Bit[0]: MIPI output enable 0: Input 1: Output
MIPI I/O control	0x3002	I/O Control for MIPI Bit[3]: GPIO port 3 Bit[2]: GPIO port 2 Bit[1]: GPIO port 1 Bit[0]: GPIO port 0

2.4 format and frame rate

The OV9732 supports the following formats: RAW8, RAW10 through MIPI.

table 2-2 format and frame rate

format	resolution	frame rate	methodology	MIPI speed	pixel clock
full,10-bit	(1280+8)x(720+8)	30 fps	full resolution	360 Mbps	36 MHz
VGA, 10-bit	(640+8)x(480+8)	45 fps	crop from full	360 Mbps	36 MHz
2x2 binning RGB	(640+4)x(360+4)	60 fps	vertical/horizontal digital binning	180 Mbps	36 MHz
2x2 binning BW	(640+4)x(360+4)	60 fps	vertical neighbor pixels; horizontal neighbor pixels	180 Mbps	36 MHz

2.5 MIPI interface

The OV9732 supports a single lane MIPI interface with a data transfer rate of up to 480 Mbps. The MIPI interface provides a single uni-directional clock lane and uni-directional data lane to communicate to components in a mobile device. The data lane has full support for high speed (HS) and low power (LP) data transfer modes. Contact your local OmniVision FAE for more details. For MIPI control registers, please see **section 7-15**.

figure 2-3 MIPI timing

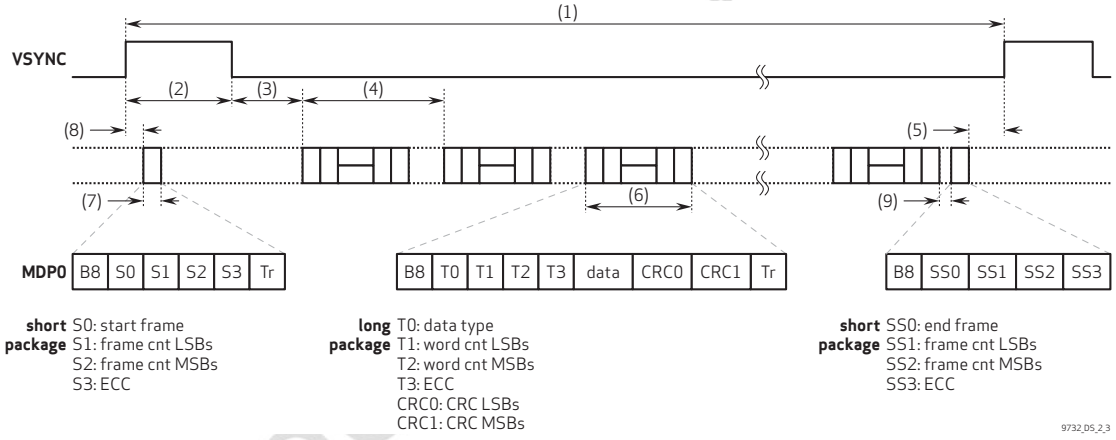


table 2-3 MIPI timing specification

mode	timing	
1280x720 (full size) 30 fps	(1)	1,185,356 tps
	(2)	512 tps
	(3)	30,771.54 tpp
	(4)	1847.89 tpp
	(5)	120,248.554 tpp
	(6)	1,622.91 tpp
	(7)	20.9 tpp
	(8)	88.5 tpp
	(9)	120,337.09 tpp
	where tps = 1 Tsclk, tpp = 1 Tpclk = 1 UI	

2.6 power management

OmniVision recommends cutting off all power supplies, including the external DVDD, when the sensor is not in use.

2.7 power up sequence

The digital and analog supply voltages can be powered up in any order (e.g., DOVDD then AVDD or AVDD then DOVDD). DVDD is supplied later.

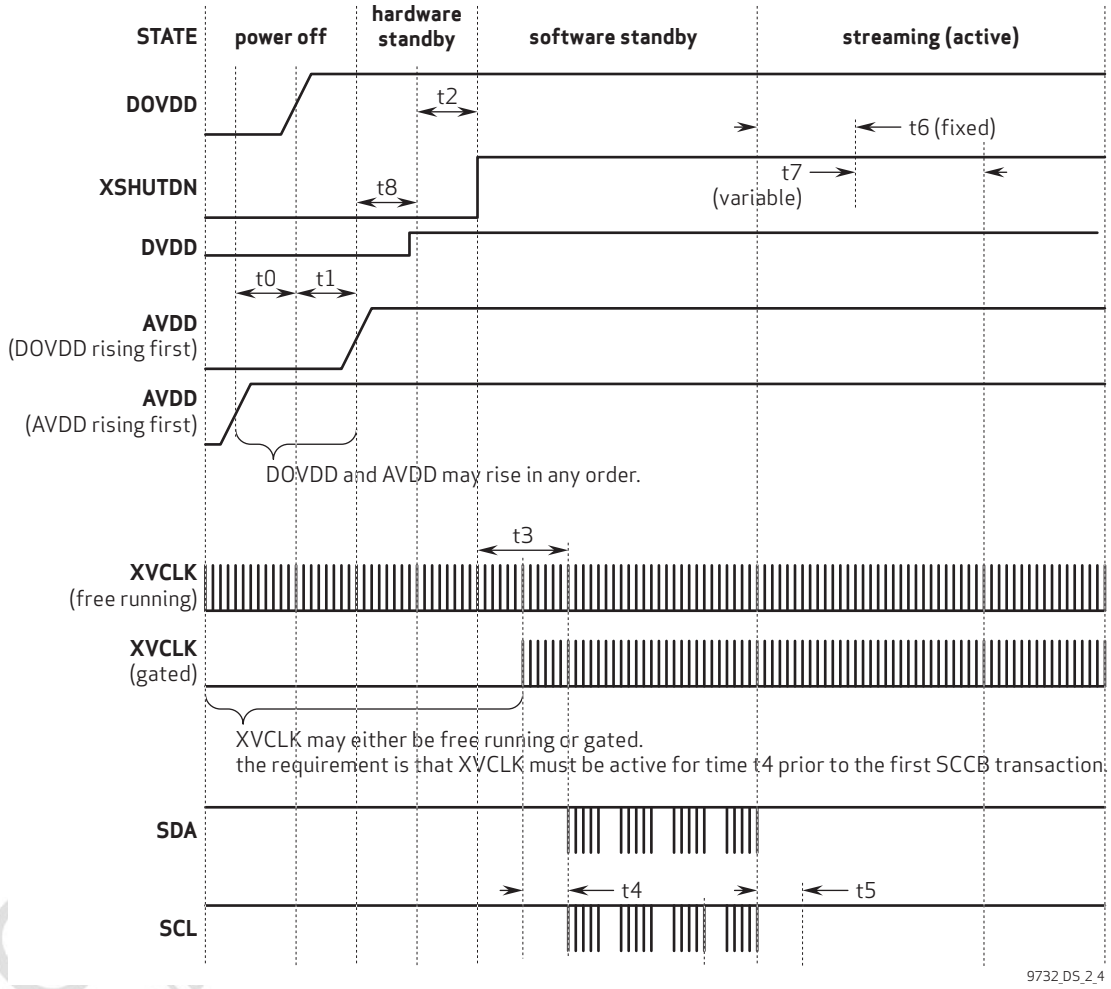
2.7.1 on-chip power up

The XVCLK clock can either be initially low and then enabled during software standby mode or XVCLK can be a free running clock.

table 2-4 power up sequence timing constraints

constraint	label	min	max	unit
AVDD rising - DOVDD rising	t0	AVDD and DOVDD may rise in any order		ns
DOVDD rising - AVDD rising	t1	rising separation can vary from 0 ns to infinity		ns
DVDD rising - XSHUTDN rising	t2	0.0	∞	
XSHUTDN rising - first SCCB transaction	t3	8192		XVCLK cycles
minimum number of XVCLK cycles prior to the first SCCB transaction	t4	8192		XVCLK cycles
PLL start up/lock time	t5		0.2	ms
entering streaming mode - first frame start sequence (fixed part)	t6		10	ms
entering streaming mode - first frame start sequence (variable part)	t7	delay is the integration time value		lines
AVDD or DVDD, whichever is last - DVDD rising	t8	0.0		

figure 2-4 power up sequence



2.8 power down sequence

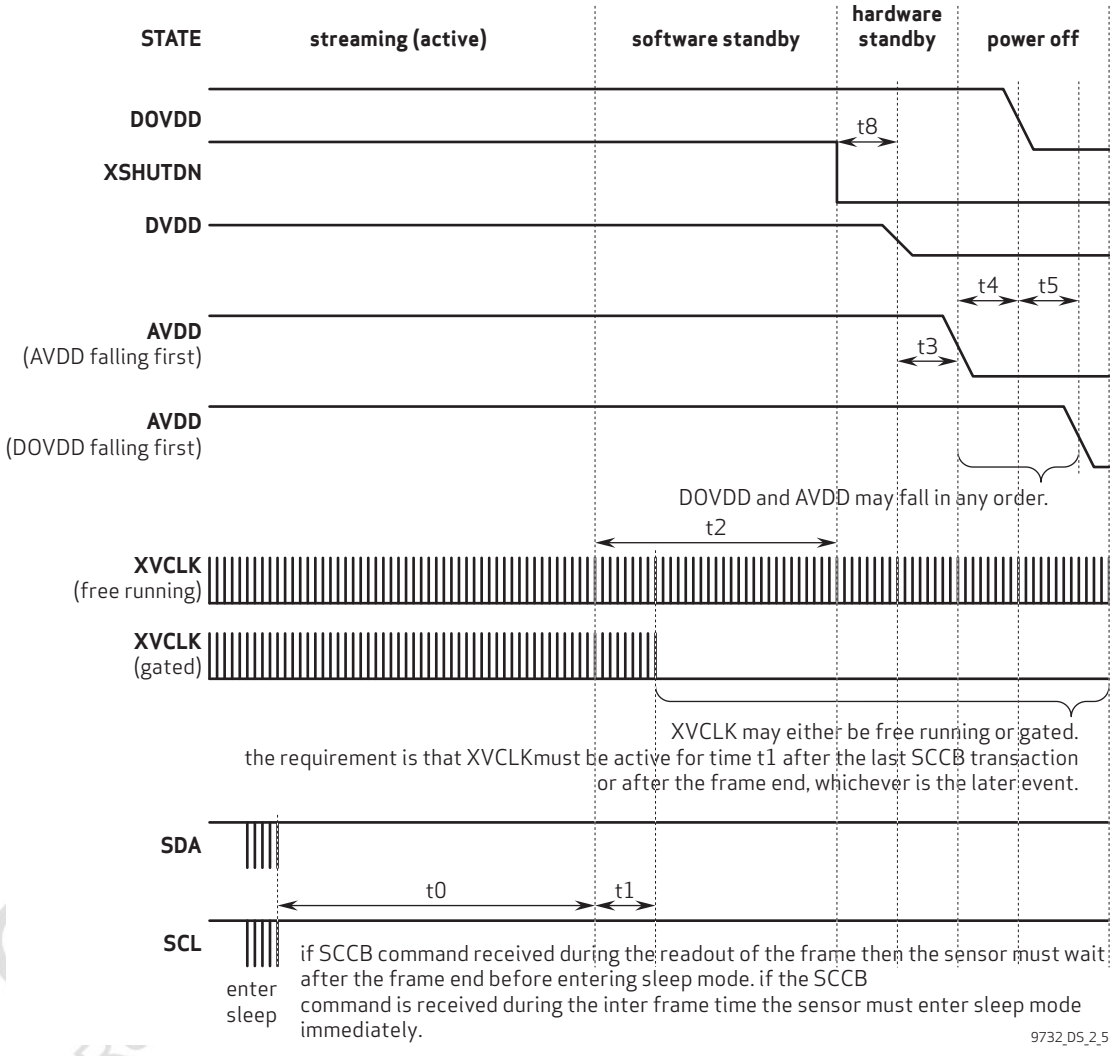
The digital and analog supply voltages can be powered down in any order (e.g., DOVDD, then AVDD or AVDD, then DOVDD). Similar to the power-up sequence, the XVCLK input clock may be either gated or continuous. If the SCCB command to exit streaming is received while a frame of data is being output, then the sensor must wait for the frame end before entering software standby mode.

If the SCCB command to exit streaming mode is received during the enter frame time, then the sensor must enter software standby mode immediately.

table 2-5 power down sequence timing constraints

constraint	label	min	max	unit
enter software standby SCCB command device in software standby mode	t0	when a frame of data is output, wait for the end before entering the software for standby; otherwise, enter the software standby mode immediately		
minimum of XVCLK cycles after the last SCCB transaction or MIPI frame end	t1	512		XVCLK cycles
last SCCB transaction or MIPI frame end, XSHUTDN falling	t2	512		XVCLK cycles
DVDD fall - AVDD or DOVDD, whichever is first	t3	0		
AVDD falling - DOVDD falling	t4	AVDD and DOVDD may fall in any order, the falling separation can vary from 0 ns to infinity		ns
DOVDD falling - AVDD falling	t5			ns
XSHUTDN fall - DVDD fall	t8	0		

figure 2-5 power down sequence



2.9 system clock control

The OV9732 has only one PLL and it generates a default 36 MHz system clock, 45 MHz pixel clock and 360 MHz MIPI serial clock from a 6~27 MHz input clock. The VCO range is from 500 MHz to 1200 MHz. A programmable clock is provided to generate different frequencies.

figure 2-6 clock scheme

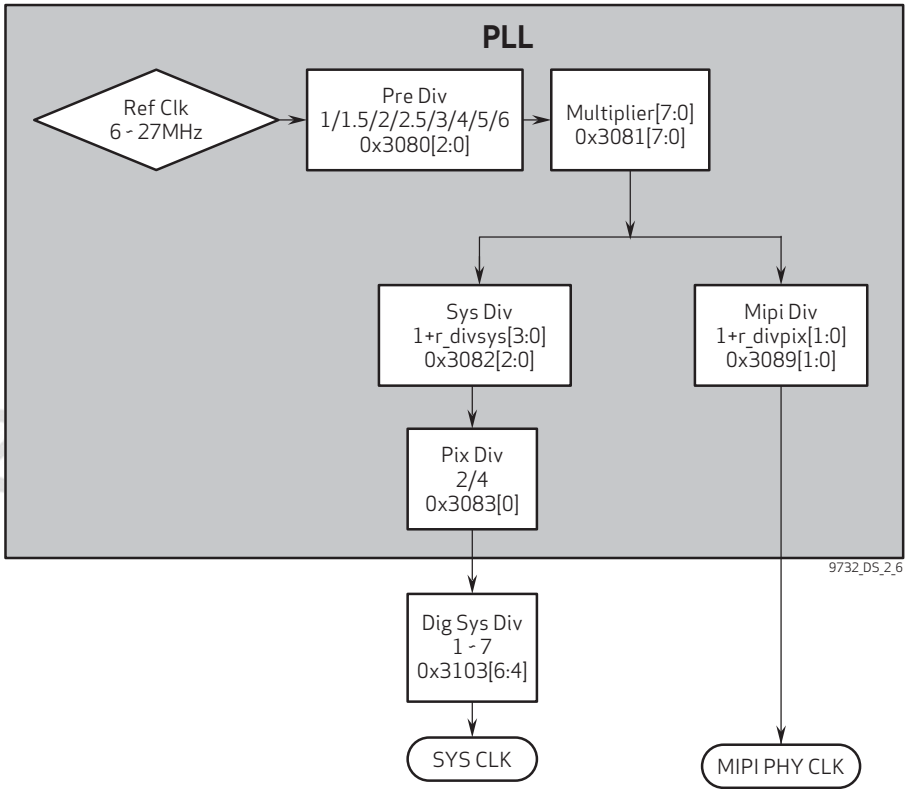


table 2-6 PLL registers

address	register name	default value	R/W	description
0x3080	PRE_PLL_CLK_DIV	0x02	RW	Bit[2:0]: Pre PLL clock divider value[2:0]
0x3081	PLL_MULTIPLIER	0x3C	RW	Bit[7:0]: PLL multiplier value[7:0]
0x3082	VT_SYS_CLK_DIV	0x04	RW	Bit[3:0]: Video timing system clock divider[3:0]
0x3083	VT_PIXEL_CLK_DIV	0x00	RW	Bit[0]: Video timing pixel clock divider[0]
0x3103	SYS_CLK_DIV	0x01	RW	Bit[6:4]: Output system clock divider 0x0~0x7: Div by 1 ~ 7

2.10 SCCB interface

The Serial Camera Control Bus (SCCB) interface controls the image sensor operation. Refer to the *OmniVision Technologies Serial Camera Control Bus (SCCB) Specification* for detailed usage of the serial control port.

In the OV9732, the SCCB identifies two IDs, SCCB_ID_1 and SCCB_ID_2. SCCB_ID_1 is controlled by SID pin. If SID is low, the SCCB_ID_1 is 0x6C; if SID is high, the SCCB_ID_1 is 0x20. The SCCB_ID_2 comes from register 0x302B, and the default value is 0x90. The SCCB slave can be connected by matching SCCB_ID_1 or SCCB_ID_2.

2.10.1 data transfer protocol

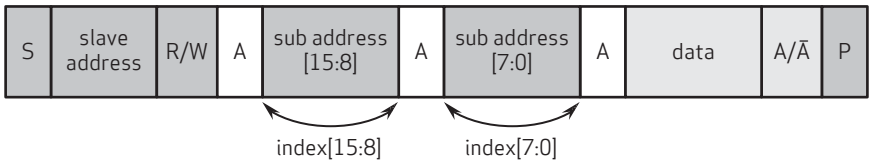
The data transfer of the OV9732 follows the SCCB protocol.

2.10.2 message format

The OV9732 supports the message format shown in **figure 2-7**. The 7-bit address of the OV9732 is 0x10. The repeated START (Sr) condition is not shown in **figure 2-8**, but is shown in **figure 2-9** and **figure 2-10**.

figure 2-7 message type

message type: 16-bit index, 8-bit data, and 7-bit slave address



from slave to master — S START condition — A acknowledge

from master to slave — P STOP condition — Ā negative acknowledge

direction depends on operation — Sr repeated START condition

9732_DS_2_7

2.10.3 read / write operation

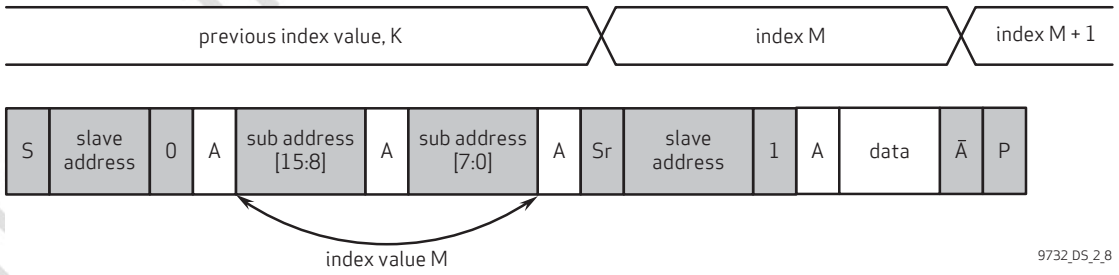
The OV9732 supports four different read operations and two different write operations:

- a single read from random locations
- a sequential read from random locations
- a single read from current location
- a sequential read from current location
- single write to random locations
- sequential write starting from random location

The index in the sensor automatically increases by one after each read/write operation.

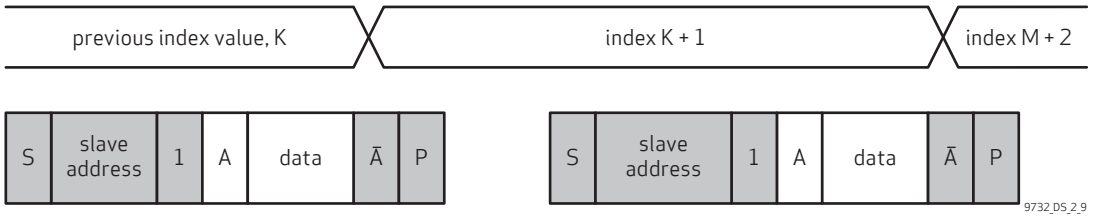
In a single read from random locations, the master does a dummy write operation to desired index, issues a repeated start condition and then addresses the camera again with a read operation. After acknowledging its slave address, the camera starts to output data onto the SDA line as shown in **figure 2-8**. The master terminates the read operation by setting a negative acknowledge and stop condition.

figure 2-8 SCCB single read from random location



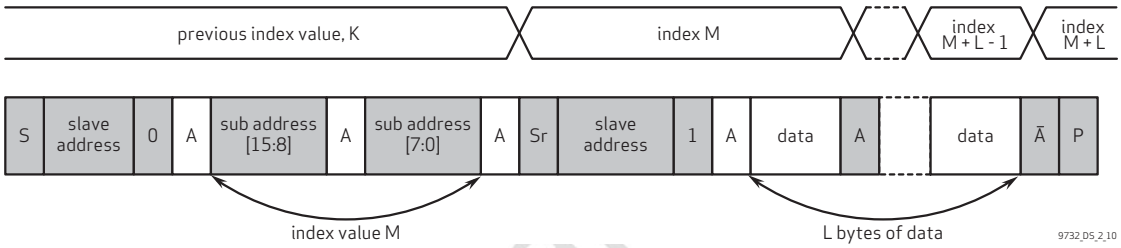
If the host addresses the camera with read operation directly without the dummy write operation, the camera responds by setting the data from last used index to the SDA line as shown in **figure 2-9**. The master terminates the read operation by setting a negative acknowledge and stop condition.

figure 2-9 SCCB single read from current location



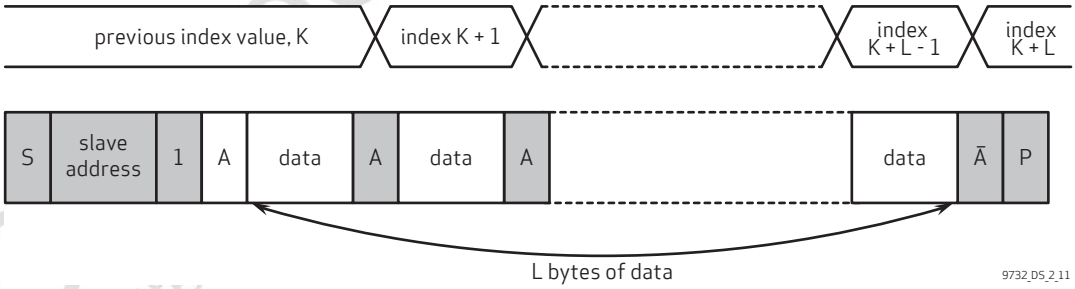
The sequential read from a random location is illustrated in **figure 2-10**. The master does a dummy write to the desired index, issues a repeated start condition after acknowledge from slave and addresses the slave again with read operation. If a master issues an acknowledge after receiving data, it acts as a signal to the slave that the read operation shall continue from the next index. When master has read the last data byte, it issues a negative acknowledge and stop condition.

figure 2-10 SCCB sequential read from random location



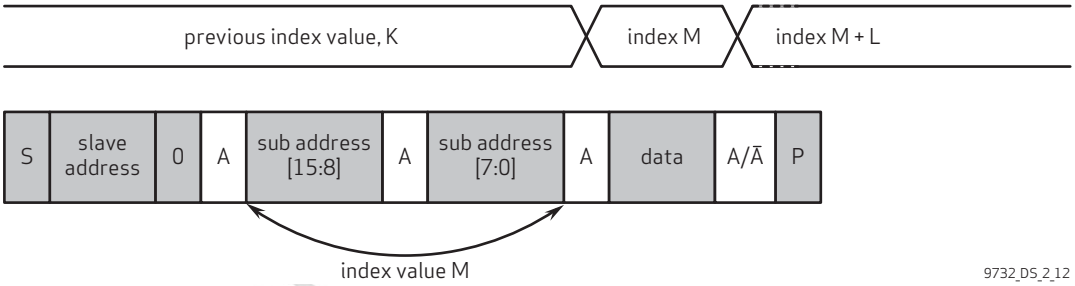
The sequential read from current location is similar to a sequential read from a random location. The only exception is that there is no dummy write operation. as shown in **figure 2-11**. The master terminates the read operation by setting a negative acknowledge and stop condition.

figure 2-11 SCCB sequential read from current location



The write operation to a random location is illustrated in **figure 2-12**. The master issues a write operation to the slave, sets the index and data correspondingly after the slave has acknowledged. The write operation is terminated with a stop condition from the master.

figure 2-12 SCCB single write to random location



The sequential write is illustrated in **figure 2-13**. The slave automatically increments the index after each data byte. The sequential write operation is terminated with stop condition from the master.

figure 2-13 SCCB sequential write to random location

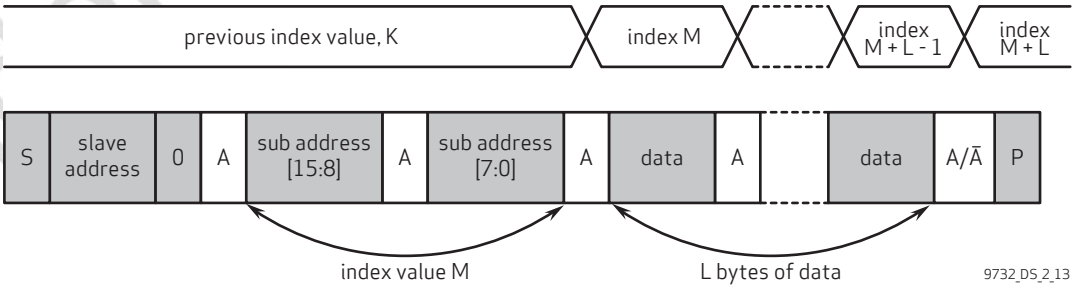


figure 2-14 SCCB interface timing

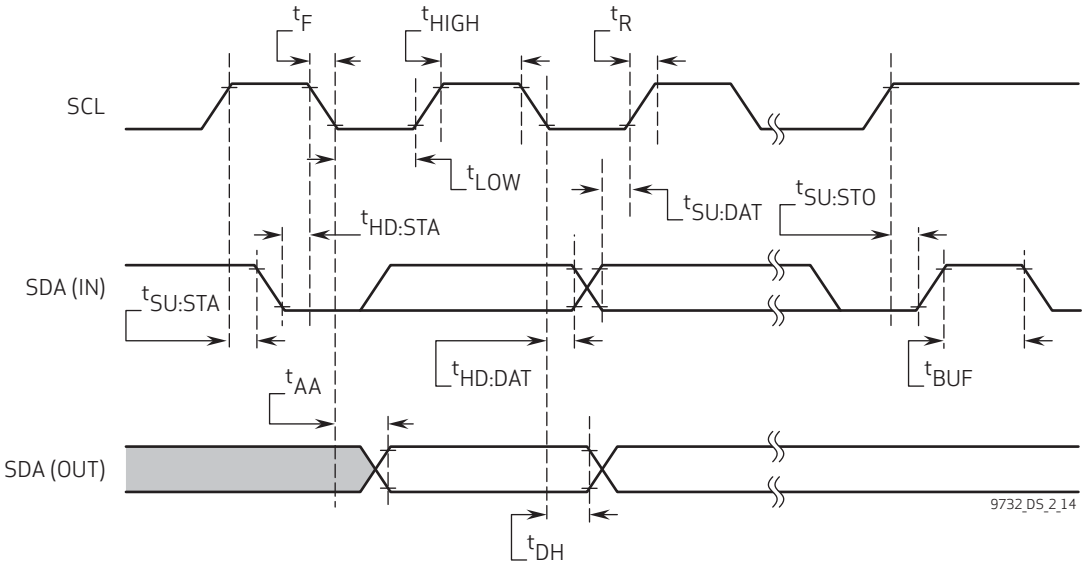


table 2-7 SCCB interface timing specifications[a]

symbol	parameter	min	typ	max	unit
f_{SCL}	clock frequency			400[b]	kHz
t_{LOW}	clock low period	1.3			µs
t_{HIGH}	clock high period	0.6			µs
t_{AA}	SCL low to data out valid	0.1		0.9	µs
t_{BUF}	bus free time before new start	1.3			µs
$t_{HD:STA}$	start condition hold time	0.6			µs
$t_{SU:STA}$	start condition setup time	0.6			µs
$t_{HD:DAT}$	data in hold time	0			µs
$t_{SU:DAT}$	data in setup time	0.1			µs
$t_{SU:STO}$	stop condition setup time	0.6			µs
t_R, t_F	SCCB rise/fall times			0.3	µs
t_{DH}	data out hold time	0.05			µs

a. SCCB timing is based on 400kHz mode

b. SCCB maximum speed is 400kHz when sensor master input clock (EXT_CLK) is greater than or equal to 13MHz. When EXT_CLK is less than 13MHz, the maximum SCCB speed is less than 400kHz (approximately EXT_CLK/32.5)

3 block level description

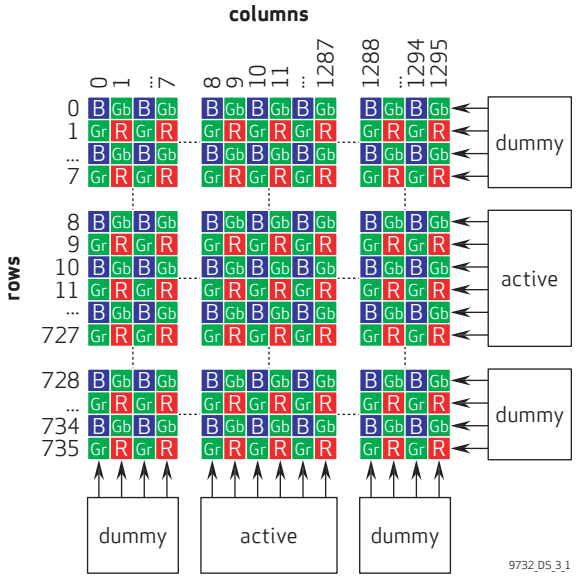
3.1 pixel array structure

The OV9732 sensor has an image array of 1296 columns by 736 rows (953,856 pixels). figure 3-1 shows a cross-section of the image sensor array.

The color filters are arranged in a Bayer pattern. The primary color BG/GR array is arranged in line-alternating fashion. Of the 953,856 pixels, 921,600 (1280x720) are active pixels and can be output. The other pixels are used for black level calibration and interpolation. The center 1288x728 pixels are suggested to be output from the whole active pixel array. The background processor can use the boundary pixels for additional processing.

The sensor array design is based on a field integration read-out system with line-by-line transfer and an electronic shutter with a synchronous pixel read-out scheme.

figure 3-1 sensor array region color filter layout



3.2 2x2 binning

The OV9732 supports a binning mode to provide a lower resolution output while maintaining the field of view. With binning mode ON, the voltage levels of adjacent pixels (of the same color) are averaged before being sent to the ADC. The OV9732 supports 2x2 binning, which is illustrated in figure 3-2, where the voltage levels of two horizontal (2x1) adjacent same-color pixels are averaged.

figure 3-2 example of 2x2 binning

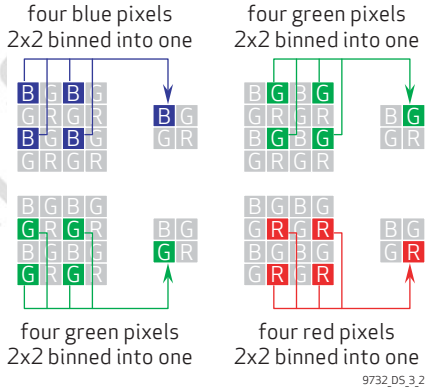


table 3-1 binning-related registers

address	register name	default value	R/W	description
0x3820	TIMING_FORMAT	0x08	RW	Bit[1]: Horizontal binning Bit[0]: Vertical binning

3.3 analog amplifier

When the column sample/hold circuit has sampled one row of pixels, the pixel data will shift out one-by-one into an analog amplifier.

3.4 10-bit A/D converters

The balanced signal is then digitized by the on-chip 10-bit ADC.

4 image sensor core digital functions

4.1 mirror and flip

The OV9732 provides mirror mode, which reverses the sensor data read-out order horizontally and flip mode, which reverses it vertically (see **figure 4-1**).

figure 4-1 mirror and flip samples

original image | mirrored image | flipped image | mirrored and flipped image

9732_DS_4_1

table 4-1 image orientation control registers

address	register name	default value	R/W	description
0x3820	ORIENTATION	0x10	RW	Bit[3]: Mirror ON/OFF select 0: Mirror OFF 1: Mirror ON Bit[2]: Flip ON/OFF select 0: Flip OFF 1: Flip ON

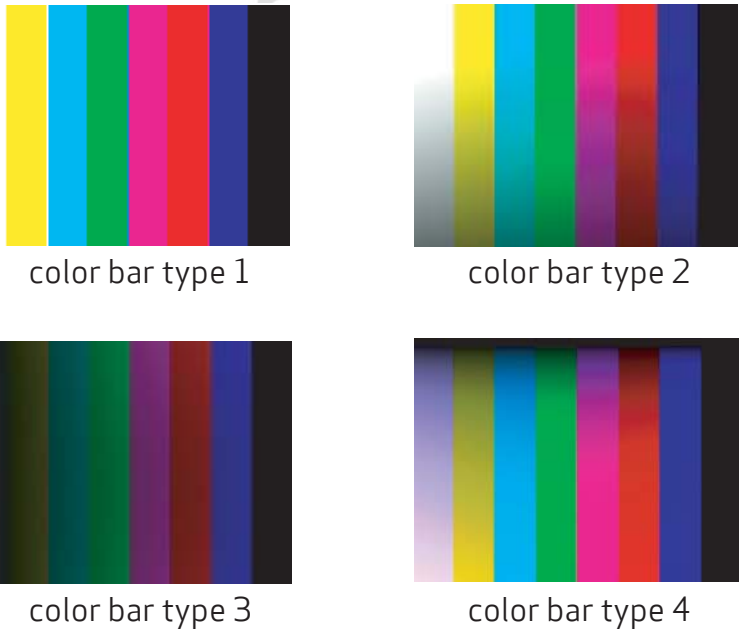
4.2 test pattern

For testing purposes, the OV9732 offers a color bar option.

4.2.1 color bar

There are four types of color bar which are switched by the bar-style register (0x5080[3:2]).

figure 4-2 color bar types



9732_DS_4_2

table 4-2 test pattern registers

address	register name	default value	R/W	description
0x5080	PRE CTRL00	0x00	RW	Bit[7]: Test pattern enable 0: Disable test function 1: Enable test function Bit[3:2]: color_bar_style 00: Standard color bar 01: Top-bottom darker color bar 10: Right-left darker color bar 11: Bottom-top darker color bar

4.3 exposure control/ gain control

The exposure control and gain control allow the image sensor to adjust the image brightness to a desired range by setting the proper exposure time and gain applied to the image. Exposure time and gain can be set manually from an external controller. The related registers are listed in **table 4-3**.

table 4-3 exposure/gain control functions

function	register	description
AEC enable	0x3503	Bit[0]: AEC enable 0: Reserved 1: Manual
AEC (exposure time)	0x3501~0x3502	0x3501[7:0] = AEC[15:8] 0x3502[7:0] = AEC[7:0]
AGC enable	0x3503	Bit[1]: AGC enable 0: Reserved 1: Manual
AGC (gain)	0x350A~0x350B	0x350A[1:0] = analog_gain_code_global[9:8] 0x350B[7:0] = analog_gain_code_global[7:0]

4.4 black level calibration (BLC)

The OV9732 black level calibration function compensates for dark current to ensure constant output black level regardless of change in exposure time, gain and temperature.

table 4-4 black level calibration controls

function	register	description
BLC enable	0x5000	Bit[0]: BLC enable 0: Disable 1: Enable
auto/manual mode	0x4001	Bit[4]: Offset manual mode 0: Auto mode 1: Manual mode
target	{0x4002[1:0], 0x4003}	Black Level to be Achieved

5 image sensor processor digital functions

5.1 ISP general control

table 5-1 ISP general control registers

address	register name	default value	R/W	description
0x5000	ISP CTRL00	0x2F	RW	ISP Control 00 (0: disable; 1: enable) Bit[6]: pre_isp_man_en Bit[5]: dgc_en Bit[4]: awb_gain_en Bit[3]: bc_en Bit[2]: wc_en Bit[1]: dcblc_en Bit[0]: blc_en
0x5001	ISP CTRL01	0x20	RW	Bit[6]: sof_sel Bit[5]: eof_sel1 Bit[4]: eof_sel0 Bit[3]: awb_out_sel Bit[2]: pre_out_sel Bit[1]: blc_out_sel Bit[0]: byp_isp_sel
0x5002	ISP CTRL02	0x10	RW	Bit[4]: bias_plus Bit[3]: bias_man_en Bit[2]: blkv_in Bit[1]: imgv_in Bit[0]: no_latch
0x5003	ISP CTRL03	0x10	RW	Bit[7:0]: bias_man[7:0]
0x5004	ISP CTRL4	0x01	RW	Bit[7]: size_man_en Bit[6:4]: win_y_offset_adjust
0x5006	ISP CTRL06	0x00	RW	Bit[7:0]: Manual horizontal size[15:8]
0x5007	ISP CTRL07	0x00	RW	Bit[7:0]: Manual horizontal size[7:0]
0x5008	ISP CTRL08	0x00	RW	Bit[7:0]: Manual vertical size[15:8]
0x5009	ISP CTRL09	0x00	RW	Bit[7:0]: Manual vertical size[7:0]
0x500B	DPC SRAM TEST	0x02	RW	Bit[5]: dpc_sram_test1 Bit[4]: dpc_sram_rme Bit[3:0]: dpc_sram_rm

6 image sensor output interface digital functions

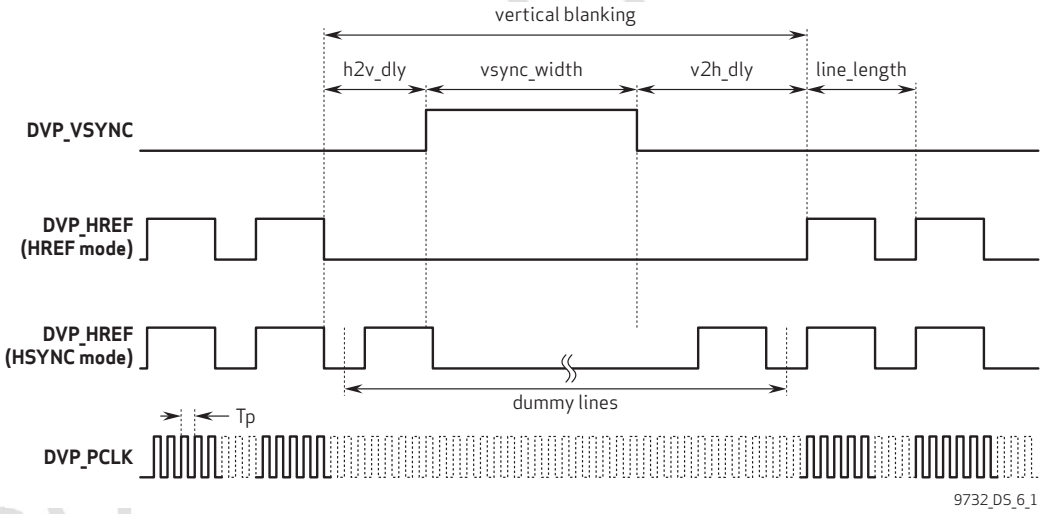
6.1 digital video port (DVP)

The digital video port (DVP) provides 10-bit parallel data output in all formats supported and extended features including HREF, CCIR656 format, HSYNC mode and test pattern output.

6.1.1 HREF mode

HREF mode is the default mode of the DVP (see **figure 6-1**). Each DVP_VSYNC indicates the starting of a new frame. DVP_VSYNC, DVP_HREF and DVP_PCLK can be reversed using the register settings.

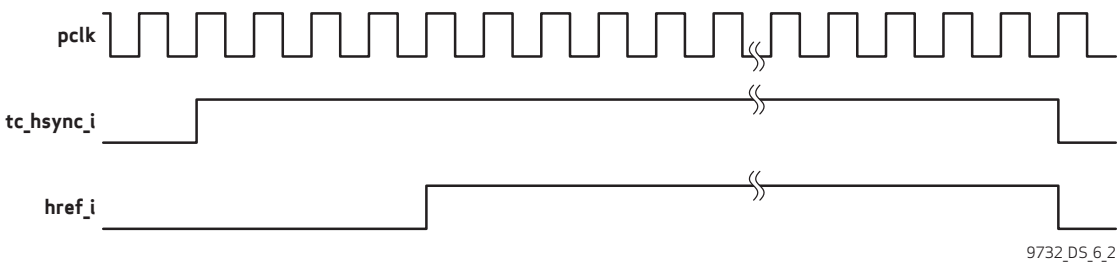
figure 6-1 DVP timing



6.1.2 input timing specifications

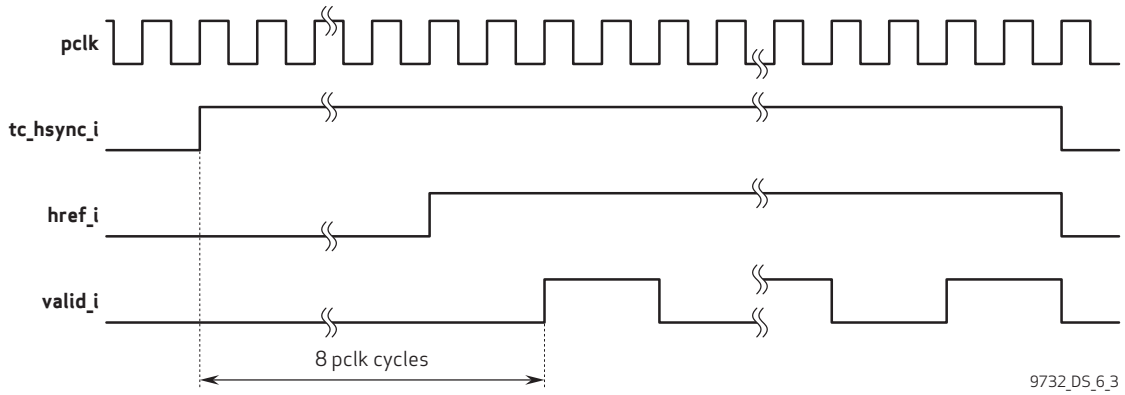
If CCIR656 is enabled, full size mode, tc_hsync_i should be ahead of href_i by 4 pclk cycles.

figure 6-2 full size, CCIR656 enable



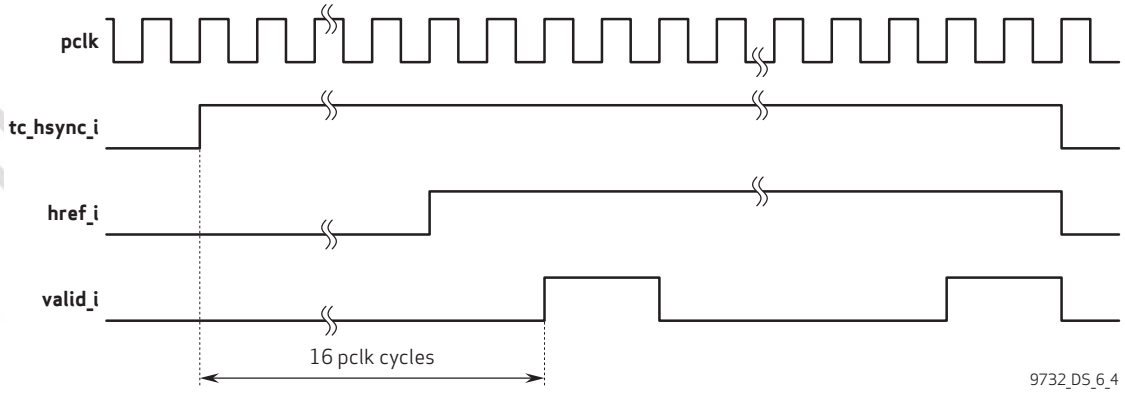
If CCIR656 is enabled, horizontal subsample 2 mode, tc_hsync_i should be ahead of href_i&valid_i by 8 pclk cycles.

figure 6-3 HSUBS 2, CCIR656 enable



If CCIR656 is enabled, horizontal subsample 4 mode, tc_hsync_i should be ahead of href_i&valid_i by 16 pclk cycles.

figure 6-4 HSUBS 4, CCIR656 enable

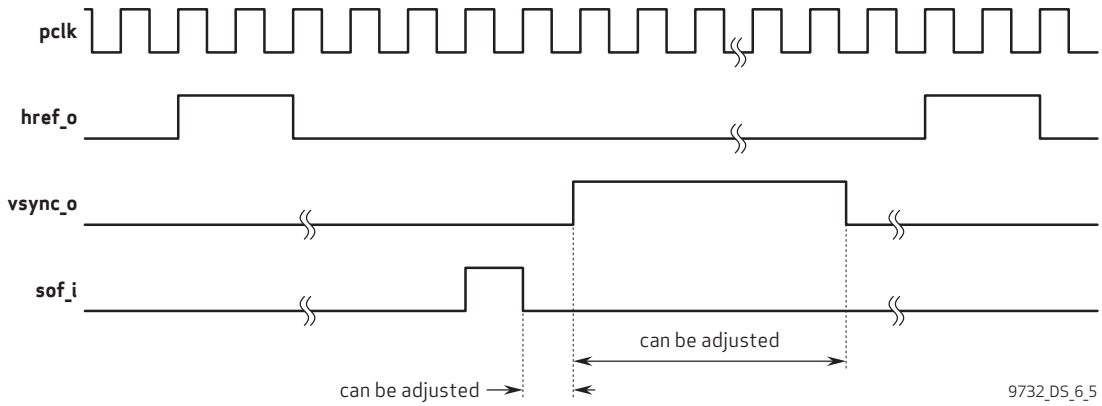


6.1.3 output timing specifications

The OV9732 DVP_VSYNC has three types: VSYNC_1, VSYNC_2 and VSYNC_3.

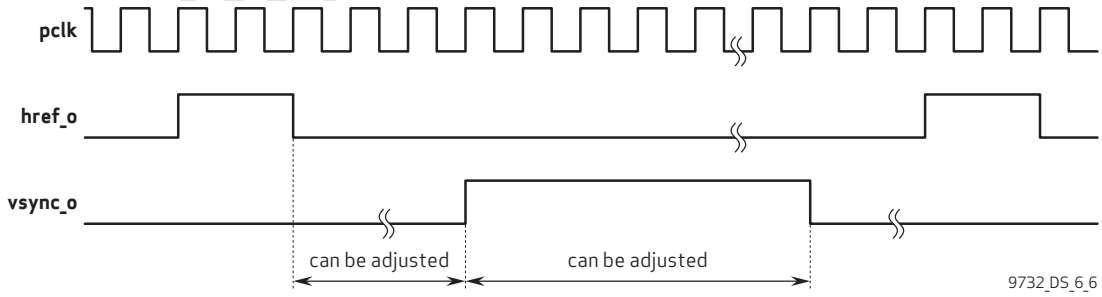
6.1.3.1 VSYNC mode 1 - generated by SOF, width controlled by register.

figure 6-5 VSYNC mode 1



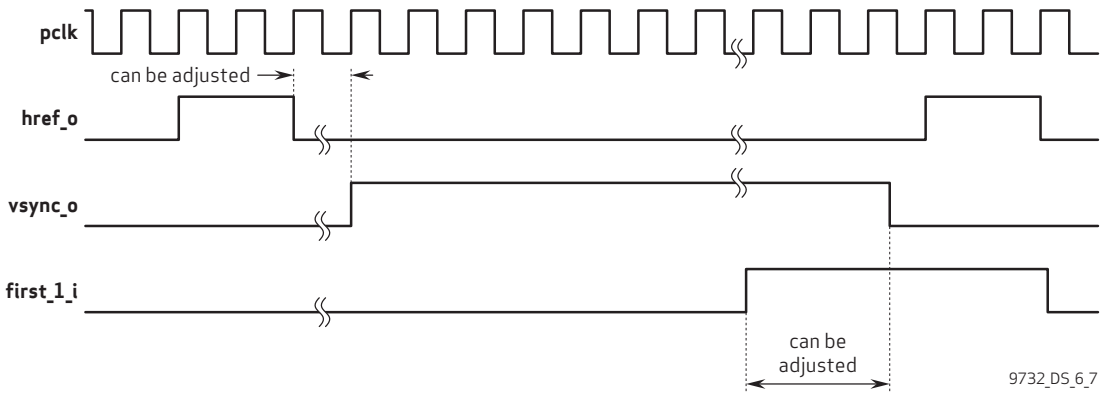
6.1.3.2 VSYNC mode 2 - generated by EOF, width controlled by register.

figure 6-6 VSYNC mode 2



6.1.3.3 VSYNC mode 3 - generated by EOF, unset by first_1_i, long VSYNC, turn to 1'b0 when first_1_i is set.

figure 6-7 VSYNC mode 3



The vsync_o rising edge delay is controlled by register vsync_delay({r5, r6, r7}) in all three VSYNC modes. VSYNC width is controlled by register vsync_width_pixel ({r2, r3}) for VSYNC mode 1 and 2. The steps of both registers vsync_delay and vsync_width_pixel are 1 pclk cycle.

Note that VSYNC mode 3 is a long VSYNC mode. The register vsync_width_pixel ({r2,r3}) controls VSYNC falling edge differently. It starts counting when both tc_hsync_i and first_1_i are high, and both signals are generated in the preceding VFIFO or timing_ctrl block.

7 register tables

The following tables provide descriptions of the device control registers contained in the OV9732. For all register enable/disable bits, ENABLE = 1 and DISABLE = 0. The device slave address is 0x6C for write and 0x6D for read (when SID=1, 0x20 for write and 0x21 for read).

7.1 general status [0x0100, 0x0103, 0x0106, 0x300A - 0x300B, 0x302A]

table 7-1 general status registers

address	byte	register name	default value	R/W	description
0x0100		MODE_SELECT	0x00	RW	Mode Select for Software Standby 0: Sleep 1: Streaming
0x0103		SOFTWARE_RESET	0x00	RW	Software Reset Setting this register to 1 resets sensor to its power up defaults. Value of this bit is also reset 0: Off 1: On
0x0106		FAST_STANDBY_CTRL	0x01	RW	Fast Standby Control 0: Frame completes before mode entry 1: Frame may be truncated before mode entry
0x300A	Hi	CHIP ID	0x97	R	Sensor Chip ID High Byte
0x300B	Lo	CHIP ID	0x32	R	Sensor Chip ID Low Byte
0x302A		CHIP REVISION	0xA0	R	Bit[7:0]: Chip revision number

7.2 SCCB control [0x0107, 0x3031]

table 7-2 SCCB control registers

address	register name	default value	R/W	description
0x0107	CCI_ADDRESS_PGM_ID	0x6C	RW	Expressed as 8-bit SCCB Programmable ID
0x3031	SCCB	0x02	RW	Expressed as 8-bit Bit[7:2]: Not used Bit[1]: SCCB programmable ID enable Bit[0]: sccb_id2_nack_en

7.3 IO control [0x3001 - 0x3002, 0x3009]

table 7-3 IO control registers

address	register name	default value	R/W	description
0x3001	PCLK/HREF/VSYNC OEN	0x00	RW	Bit[7:1]: Debug mode Bit[0]: Input/output control for GPIO port VSYNC
0x3002	GPIO OEN	0x00	RW	Bit[7:4]: Debug mode Bit[3]: GPIO port 3 Bit[2]: GPIO port 2 Bit[1]: GPIO port 1 Bit[0]: GPIO port 0
0x3009	OUTPUT DRIVE CAPABILITY CTRL	0x02	RW	Input/Output Control for SPI Bit[7]: Debug mode Bit[6:5]: Output drive capability for SPI IO 00: 1x 01: 2x 10: 3x 11: 4x Bit[4:0]: Debug mode

7.4 clock configuration [0x3080 - 0x3083, 0x3103]

table 7-4 clock configuration registers

address	register name	default value	R/W	description
0x3080	PRE_PLL_CLK_DIV	0x02	RW	Bit[2:0]: Pre PLL clock divider value[2:0]
0x3081	PLL_MULTIPLIER	0x3C	RW	Bit[7:0]: PLL multiplier value[7:0]
0x3082	VT_SYS_CLK_DIV	0x04	RW	Bit[3:0]: Video timing system clock divider[3:0]
0x3083	VT_PIXEL_CLK_DIV	0x00	RW	Bit[0]: Video timing pixel clock divider[0]
0x3103	SYS_CLK_DIV	0x01	RW	Bit[6:4]: Output system clock divider 0x0~0x7: Div by 1 ~ 7

7.5 analog control [0x3600 - 0x363F]

table 7-5 analog control registers

address	register name	default value	R/W	description
0x3600~ 0x363F	RSVD	–	–	Reserved

7.6 sensor control [0x3700 - 0x370C]

table 7-6 sensor control registers

address	register name	default value	R/W	description
0x3700~ 0x370C	RSVD	–	–	Reserved

7.7 PSRAM control [0x3780 - 0x3785]

table 7-7 PSRAM control registers

address	register name	default value	R/W	description
0x3780~ 0x3785	RSVD	–	–	Reserved

7.8 frame timing [0x3800 - 0x381D, 0x3820 - 0x3829]

table 7-8 frame timing registers (sheet 1 of 4)

address	register name	default value	R/W	description
0x3800	X ADDR START	0x00	RW	Bit[7:0]: x_addr_start[15:8] Array horizontal start point high byte
0x3801	X ADDR START	0x04	RW	Bit[7:0]: x_addr_start[7:0] Array horizontal start point low byte

table 7-8 frame timing registers (sheet 2 of 4)

address	register name	default value	R/W	description
0x3802	Y ADDR START	0x00	RW	Bit[7:0]: y_addr_start[15:8] Array vertical start point high byte
0x3803	Y ADDR START	0x04	RW	Bit[7:0]: y_addr_start[7:0] Array vertical start point low byte
0x3804	X ADDR END	0x05	RW	Bit[7:0]: x_addr_end[15:8] Array horizontal end point high byte
0x3805	X ADDR END	0x0B	RW	Bit[7:0]: x_addr_end[7:0] Array horizontal end point low byte
0x3806	Y ADDR END	0x02	RW	Bit[7:0]: y_addr_end[15:8] Array vertical end point high byte
0x3807	Y ADDR END	0xDB	RW	Bit[7:0]: y_addr_end[7:0] Array vertical end point low byte
0x3808	X OUTPUT SIZE	0x05	RW	Bit[7:0]: x_output_size[15:8] ISP horizontal output width high byte
0x3809	X OUTPUT SIZE	0x00	RW	Bit[7:0]: x_output_size[7:0] ISP horizontal output width low byte
0x380A	Y OUTPUT SIZE	0x02	RW	Bit[7:0]: y_output_size[15:8] ISP vertical output height high byte
0x380B	Y OUTPUT SIZE	0xD0	RW	Bit[7:0]: y_output_size[7:0] ISP vertical output height low byte
0x380C	HTS	0x05	RW	Bit[7:0]: HTS[15:8] Total pixels per line high byte
0x380D	HTS	0xC6	RW	Bit[7:0]: HTS[7:0] Total pixels per line low byte
0x380E	VTS	0x03	RW	Bit[7:0]: VTS[15:8] Total lines per frame high byte
0x380F	VTS	0x22	RW	Bit[7:0]: VTS[7:0] Total lines per frame low byte
0x3810	ISP X WIN	0x00	RW	Bit[7:0]: isp_x_win[15:8] ISP horizontal windowing offset high byte
0x3811	ISP X WIN	0x04	RW	Bit[7:0]: isp_x_win[7:0] ISP horizontal windowing offset low byte
0x3812	ISP Y WIN	0x00	RW	Bit[7:0]: isp_y_win[15:8] ISP vertical windowing offset high byte

table 7-8 frame timing registers (sheet 3 of 4)

address	register name	default value	R/W	description
0x3813	ISP Y WIN	0x04	RW	Bit[7:0]: isp_y_win[7:0] ISP vertical windowing offset low byte
0x3814	VSYNC CS POINT	0x00	RW	Bit[7:0]: vsync_cs_point[15:8]
0x3815	VSYNC CS POINT	0x01	RW	Bit[7:0]: vsync_cs_point[7:0]
0x3816	VSYNC START ROW	0x00	RW	Bit[7:0]: vsync_start_row[15:8]
0x3817	VSYNC START ROW	0x00	RW	Bit[7:0]: vsync_start_row[7:0]
0x3818	VSYNC END ROW	0x00	RW	Bit[7:0]: vsync_end_row[15:8]
0x3819	VSYNC END ROW	0x04	RW	Bit[7:0]: vsync_end_row[7:0]
0x381A	HSYNC FIRST	0x00	RW	Bit[7:0]: hsync_first[15:8] HSYNC first active row start position high byte
0x381B	HSYNC FIRST	0x00	RW	Bit[7:0]: hsync_first[7:0] HSYNC first active row start position low byte
0x381C	REG1C	0x01	RW	Bit[7:6]: Not used Bit[5]: init_man Bit[4]: vsync_polarity Bit[3]: ext_vs_re Bit[2]: ext_vs_en Bit[1:0]: grp_wr_start
0x381D	REG1D	0x20	RW	Bit[7:4]: Not used Bit[3:0]: fsin_mask Mask frame sync pulse 0: Input mode: sync sensor every one of {bit[3:0]+1} FSIN pulses 1: Output mode: output one VSYNC at each {bit[3:0]+1} frames
0x3820	FORMAT0	0x10	RW	Bit[7:4]: Not used Bit[3]: Mirror Bit[2]: vflip Bit[1]: hbin Bit[0]: vbin

table 7-8 frame timing registers (sheet 4 of 4)

address	register name	default value	R/W	description
0x3821	FORMAT1	0x00	RW	Bit[7:4]: Not used Bit[3:2]: hsub 00: Full 01: hsub2 10: hsub4 11: Not allowed Bit[1:0]: vsub 00: Full 01: vsub2 10: vsub4 11: Not allowed
0x3822	CS RST FSIN	0x00	RW	Bit[7:0]: cs_rst_fsin[15:8] CS reset value high byte at vs_ext
0x3823	CS RST FSIN	0x00	RW	Bit[7:0]: cs_rst_fsin[7:0] CS reset value low byte at vs_ext
0x3824	R RST FSIN	0x00	RW	Bit[7:0]: r_rst_fsin[15:8] R reset value high byte at vs_ext
0x3825	R RST FSIN	0x00	RW	Bit[7:0]: r_rst_fsin[7:0] R reset value low byte at vs_ext
0x3826	FVTS	0x00	RW	Bit[7:0]: FVTS[15:8] Fractional vertical timing size high byte
0x3827	FVTS	0x00	RW	Bit[7:0]: FVTS[7:0] Fractional vertical timing size low byte
0x3828	LN SYNC POINT	0x00	RW	Bit[7:0]: ln_sync_point[15:8] Unit is 16×sclk
0x3829	LN SYNC POINT	0x10	RW	Bit[7:0]: ln_sync_point[7:0] Unit is 16×sclk

7.9 AEC control [0x3500 - 0x3505, 0x3509 - 0x350B, 0x3510 - 0x3513]

table 7-9 AEC control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x3500	LONG EXPO	0x00	RW	Bit[7:4]: Debug mode Bit[3:0]: Long exposure[19:16]
0x3501	LONG EXPO	0x20	RW	Bit[7:0]: Long exposure[15:8]

table 7-9 AEC control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x3502	LONG EXPO	0x00	RW	Bit[7:0]: Long exposure[7:0] Low 4 bits are fraction bits
0x3503	AEC MANUAL	0x03	RW	Bit[7:6]: Not used Bit[5]: Gain change delay option 0: Not delay 1 frame 1: Delay 1 frame Bit[4]: Delay option 0: Disable 1: Enable Bit[3]: gain_change_delay Bit[2]: vts_manual Bit[1]: agc_manual Bit[0]: aec_manual
0x3504	MANUAL SNR GAIN	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Manual sensor gain[9:8]
0x3505	MANUAL SNR GAIN	0x00	RW	Bit[7:0]: Manual sensor gain[7:0]
0x3509	AEC CTRL 9	0x10	RW	Bit[7:5]: Not used Bit[4]: convert_en Bit[3]: gain_man_en Bit[2:0]: Not used
0x350A	LONG GAIN	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Long gain[9:8]
0x350B	LONG GAIN	0x10	RW	Bit[7:0]: Long gain[7:0]
0x3510	PK GAIN	–	R	Bit[7:2]: Not used Bit[1:0]: pk_gain_o[9:8]
0x3511	PK GAIN	–	R	Bit[7:0]: pk_gain_o[7:0]
0x3512	SNR GAIN	–	R	Bit[7:2]: Not used Bit[1:0]: snr_gain[9:8]
0x3513	SNR GAIN	–	R	Bit[7:0]: snr_gain[7:0]

7.10 BLC control [0x4000 - 0x4017, 0x4020 - 0x4041, 0x4050 - 0x405D]

table 7-10 BLC control registers (sheet 1 of 4)

address	register name	default value	R/W	description
0x4000	BLC CTRL 00	0xC1	RW	Bit[7:4]: Avg_weight Bit[3]: Target adjust disable Use offset to adjust target 0: Enable 1: Disable Bit[2]: Compensation enable Adjust on offset due to gain change 0: Enable 1: Disable Bit[1]: Dither_en 1 bit dithering 0: Enable 1: Disable Bit[0]: Median_en Median filter function enable
0x4001	BLC CTRL 01	0xE0	RW	Bit[7]: gain_trig_beh Bit[5]: format_trig_beh Bit[5]: Kocef manual enable Bit[4]: Offset manual enable Bit[3]: Zero line out enable Bit[2]: Black line out enable Bit[1:0]: Bypass mode
0x4002	BLC CTRL 02	0x00	RW	Bit[7:2]: Debug mode Bit[1:0]: Blacklevel target[9:8]
0x4003	BLC CTRL 03	0x10	RW	Bit[7:0]: Blacklevel target[7:0]
0x4004	BLC CTRL 04	0x00	RW	Bit[7:3]: Debug mode Bit[2:0]: Horizontal win start[10:8]
0x4005	BLC CTRL 05	0x02	RW	Bit[7:0]: Horizontal win start[7:0]
0x4006	BLC CTRL 06	0x00	RW	Bit[7:3]: Debug mode Bit[2:0]: Horizontal win pad[10:8]
0x4007	BLC CTRL 07	0x02	RW	Bit[7:0]: Horizontal win pad[7:0]
0x4008	BLC CTRL 08	0x00	RW	Bit[7:0]: Black line start line
0x4009	BLC CTRL 09	0x0B	RW	Bit[7:0]: Black line end line
0x400A	BLC CTRL 0A	0x02	RW	Bit[7:0]: Offset trigger threshold[15:8]
0x400B	BLC CTRL 0B	0x00	RW	Bit[7:0]: Offset trigger threshold[7:0]
0x400C	BLC CTRL 0C	0x00	RW	Bit[7:0]: CVDN black lines start
0x400D	BLC CTRL 0D	0x00	RW	Bit[7:0]: CVDN black lines end

table 7-10 BLC control registers (sheet 2 of 4)

address	register name	default value	R/W	description
0x400E	BLC CTRL 0E	0x00	RW	Bit[7:2]: Debug mode Bit[1:0]: Kcoef man value[9:8]
0x400F	BLC CTRL 0F	0x80	RW	Bit[7:0]: Kcoef man value[7:0]
0x4010	BLC CTRL 10	0xF0	RW	Bit[7]: Offset trigger enable Bit[6]: Gain change trigger enable Bit[5]: Format change trigger enable Bit[4]: Reset trigger enable Bit[3]: Manual average enable Bit[2]: Manual trigger Bit[1]: Freeze enable Bit[0]: Offset always updated
0x4011	BLC CTRL 11	0xFF	RW	Bit[7]: Debug mode Bit[6]: Offset trigger multiframe enable Bit[5]: Format trigger multiframe enable Bit[4]: Gain trigger multiframe enable Bit[3]: Reset trigger multiframe enable Bit[2]: Offset trigger multiframe mode Bit[1]: Format trigger multiframe mode Bit[0]: Gain trigger multiframe mode
0x4012	BLC CTRL 12	0x08	RW	Bit[7:6]: Debug mode Bit[5:0]: Reset trigger frame number
0x4013	BLC CTRL 13	0x02	RW	Bit[7:6]: Debug mode Bit[5:0]: Format trigger frame number
0x4014	BLC CTRL 14	0x02	RW	Bit[7:6]: Debug mode Bit[5:0]: Gain trigger frame number
0x4015	BLC CTRL 15	0x02	RW	Bit[7:6]: Debug mode Bit[5:0]: Offset trigger frame number
0x4016	BLC CTRL 16	0x00	RW	Bit[7:2]: Debug mode Bit[1:0]: Offset trigger threshold[9:8]
0x4017	BLC CTRL 17	0x10	RW	Bit[7:0]: Offset trigger threshold[7:0]
0x4020	BLC CTRL 20	0x00	RW	Bit[7:6]: Debug mode Bit[5:0]: Offset compensation th000
0x4021	BLC CTRL 21	0x00	RW	Bit[7:6]: Debug mode Bit[5:0]: Offset compensation k000
0x4022	BLC CTRL 22	0x00	RW	Bit[7:6]: Debug mode Bit[5:0]: Offset compensation th001
0x4023	BLC CTRL 23	0x00	RW	Bit[7:6]: Debug mode Bit[5:0]: Offset compensation k001
0x4024	BLC CTRL 24	0x00	RW	Bit[7:6]: Debug mode Bit[5:0]: Offset compensation th010

table 7-10 BLC control registers (sheet 3 of 4)

address	register name	default value	R/W	description
0x4025	BLC CTRL 25	0x00	RW	Bit[7:6]: Debug mode Bit[5:0]: Offset compensation k010
0x4026	BLC CTRL 26	0x00	RW	Bit[7:6]: Debug mode Bit[5:0]: Offset compensation th011
0x4027	BLC CTRL 27	0x00	RW	Bit[7:6]: Debug mode Bit[5:0]: Offset compensation k011
0x4028	BLC CTRL 28	0x00	RW	Bit[7:6]: Debug mode Bit[5:0]: Offset compensation th100
0x4029	BLC CTRL 29	0x00	RW	Bit[7:6]: Debug mode Bit[5:0]: Offset compensation k100
0x402A	BLC CTRL 2A	0x00	RW	Bit[7:6]: Debug mode Bit[5:0]: Offset compensation th101
0x402B	BLC CTRL 2B	0x00	RW	Bit[7:6]: Debug mode Bit[5:0]: Offset compensation k101
0x402C	BLC CTRL 2C	0x00	RW	Bit[7:6]: Debug mode Bit[5:0]: Offset compensation th110
0x402D	BLC CTRL 2D	0x00	RW	Bit[7:6]: Debug mode Bit[5:0]: Offset compensation k110
0x402E	BLC CTRL 2E	0x00	RW	Bit[7:6]: Debug mode Bit[5:0]: Offset compensation th111
0x402F	BLC CTRL 2F	0x00	RW	Bit[7:6]: Debug mode Bit[5:0]: Offset compensation k111
0x4030	BLC CTRL 30	0x00	RW	Bit[7:2]: Debug mode Bit[1:0]: Offset man 000[9:8]
0x4031	BLC CTRL 31	0x00	RW	Bit[7:0]: Offset man 000[7:0]
0x4032	BLC CTRL 32	0x00	RW	Bit[7:2]: Debug mode Bit[1:0]: Offset man 001[9:8]
0x4033	BLC CTRL 33	0x00	RW	Bit[7:0]: Offset man 001[7:0]
0x4034	BLC CTRL 34	0x00	RW	Bit[7:2]: Debug mode Bit[1:0]: Offset man 010[9:8]
0x4035	BLC CTRL 35	0x00	RW	Bit[7:0]: Offset man 010[7:0]
0x4036	BLC CTRL 36	0x00	RW	Bit[7:2]: Debug mode Bit[1:0]: Offset man 011[9:8]
0x4037	BLC CTRL 37	0x00	RW	Bit[7:0]: Offset man 011[7:0]
0x4038	BLC CTRL 38	0x00	RW	Bit[7:2]: Debug mode Bit[1:0]: Offset man 100[9:8]

table 7-10 BLC control registers (sheet 4 of 4)

address	register name	default value	R/W	description
0x4039	BLC CTRL 39	0x00	RW	Bit[7:0]: Offset man 100[7:0]
0x403A	BLC CTRL 3A	0x00	RW	Bit[7:2]: Debug mode Bit[1:0]: Offset man 101[9:8]
0x403B	BLC CTRL 3B	0x00	RW	Bit[7:0]: Offset man 101[7:0]
0x403C	BLC CTRL 3C	0x00	RW	Bit[7:2]: Debug mode Bit[1:0]: Offset man 110[9:8]
0x403D	BLC CTRL 3D	0x00	RW	Bit[7:0]: Offset man 110[7:0]
0x403E	BLC CTRL 3E	0x00	RW	Bit[7:2]: Debug mode Bit[1:0]: Offset man 111[9:8]
0x403F	BLC CTRL 3F	0x00	RW	Bit[7:0]: Offset man 111[7:0]
0x4040	BLC CTRL 40	0x00	RW	Bit[7:2]: Debug mode Bit[1:0]: r_rnd_gain_th[9:8]
0x4041	BLC CTRL 41	0x00	RW	Bit[7:0]: r_rnd_gain_th[7:0]
0x4050	BLC CTRL 50	–	R	Bit[7:2]: Debug mode Bit[1:0]: blc_offset000[9:8]
0x4051	BLC CTRL 51	–	R	Bit[7:0]: blc_offset000[7:0]
0x4052	BLC CTRL 52	–	R	Bit[7:2]: Debug mode Bit[1:0]: blc_offset001[9:8]
0x4053	BLC CTRL 53	–	R	Bit[7:0]: blc_offset001[7:0]
0x4054	BLC CTRL 54	–	R	Bit[7:2]: Debug mode Bit[1:0]: blc_offset010[9:8]
0x4055	BLC CTRL 55	–	R	Bit[7:0]: blc_offset010[7:0]
0x4056	BLC CTRL 56	–	R	Bit[7:2]: Debug mode Bit[1:0]: blc_offset011[9:8]
0x4057	BLC CTRL 57	–	R	Bit[7:0]: blc_offset011[7:0]
0x4058	BLC CTRL 58	–	R	Bit[7:2]: Debug mode Bit[1:0]: blc_offset100[9:8]
0x4059	BLC CTRL 59	–	R	Bit[7:0]: blc_offset100[7:0]
0x405A	BLC CTRL 5A	–	R	Bit[7:2]: Debug mode Bit[1:0]: blc_offset101[9:8]
0x405B	BLC CTRL 5B	–	R	Bit[7:0]: blc_offset101[7:0]
0x405C	BLC CTRL 5C	–	R	Bit[7:2]: Debug mode Bit[1:0]: blc_offset110[9:8]
0x405D	BLC CTRL 5D	–	R	Bit[7:0]: blc_offset110[7:0]

7.11 frame control [0x4201 - 0x4202]

table 7-11 frame control registers

address	register name	default value	R/W	description
0x4201	FC CTRL1	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Number of frames ON
0x4202	FC CTRL2	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Number of frames OFF

7.12 output data clipping [0x4300 - 0x4303]

table 7-12 output data clipping registers

address	register name	default value	R/W	description
0x4300	YMAX	0x03	RW	Bit[7:2]: Not used Bit[1:0]: Ymax[9:8] Ymax high byte
0x4301	YMAX	0xFF	RW	Bit[7:0]: Ymax[7:0] Ymax low byte
0x4302	YMIN	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Ymin[9:8] Ymin high byte
0x4303	YMIN	0x00	RW	Bit[7:0]: Ymin[7:0] Ymin low byte

7.13 output format control [0x4308]

table 7-13 output format control register

address	register name	default value	R/W	description
0x4308	FMT CTRL	0x02	RW	Output Format Control Bit[7:3]: Not used Bit[2]: Reserved Bit[1]: RAW8/RAW10 Bit[0]: Bypass format

7.14 DVP control [0x4700 - 0x470F]

table 7-14 DVP control register (sheet 1 of 2)

address	register name	default value	R/W	description
0x4700	MODE CTRL	0x04	RW	Mode Control Bit[7]: ccir656_fv_sel Bit[6]: ccir656_vblk generated from VSYNC Bit[5]: ccir656_blk_seq 0: 80,10 1: 10,80 Bit[4]: ccir656_blank_enable Bit[3]: ccir656_v_select 0: Vertical blanking sync code starts after end of last active line 1: Vertical blanking sync code starts at the end of last active line Bit[2]: ccir656_f value 0: Sync code fixed at field 0 1: Sync code fixed at field 1 Bit[1]: CCIR656 mode enable Bit[0]: HSYNC mode enable
0x4701	VSYNC WIDTH LINE	0x00	RW	Bit[7:0]: VSYNC width in terms of line count
0x4702	VSYNC WIDTH PIXEL H	0x02	RW	Bit[7:0]: VSYNC width in terms of pixel count[15:8]
0x4703	VSYNC WIDTH PIXEL L	0x00	RW	Bit[7:0]: VSYNC width in terms of pixel count[7:0]
0x4704	VSYNC CTRL	0x00	RW	Bit[7:4]: VSYNC mask Bit[3:2]: Reserved Bit[1:0]: VSYNC mode 00: SOF trigger 01: EOF trigger 10: Long VSYNC 11: Not allowed
0x4705	VSYNC DELAY H	0x00	RW	Bit[7:0]: VSYNC trigger to VSYNC positive edge delay[23:16]
0x4706	VSYNC DELAY M	0x00	RW	Bit[7:0]: VSYNC trigger to VSYNC positive edge delay[15:8]
0x4707	VSYNC DELAY L	0x00	RW	Bit[7:0]: VSYNC trigger to VSYNC positive edge delay[7:0]

table 7-14 DVP control register (sheet 2 of 2)

address	register name	default value	R/W	description
0x4708	POLARITY CTRL	0x01	RW	Bit[7:6]: Reserved Bit[5]: VSYNC gate clock enable Bit[4]: HREF gate clock enable Bit[3]: Reserved Bit[2]: HREF polarity Bit[1]: VSYNC polarity Bit[0]: PCLK polarity
0x4709	TEST PATTERN	0x00	RW	Bit[7:4]: Reserved Bit[3]: Bit test mode Bit[2]: Bit test 10-bit mode Bit[1]: Bit test 8-bit mode Bit[0]: Bit test enable
0x470A	DVP_CTRL	0x00	RW	Bit[5]: r_hsync_shift for HSYNC generation Bit[6]: r_first_1 for selection of r_first_i signal
0x470B	R_HSYNC_START	0xD0	RW	Bit[7:0]: r_hsync_start[7:0]
0x470C	R_HSYNC_START	0x02	RW	Bit[7:0]: r_hsync_start[15:8]
0x470D	R_FIRST_LINE	0x01	RW	Bit[7:0]: r_first_line[7:0]
0x470E	R_FIRST_LINE	0x00	RW	Bit[7:0]: r_first_line[15:8]
0x470F	HEADER_TRAILER	0x04	RW	Bit[7:0]: Additional length of HSYNC compared to HREF

7.15 MIPI control [0x4800 - 0x4808, 0x4810 - 0x483D, 0x484A - 0x484F]

table 7-15 MIPI control registers (sheet 1 of 8)

address	register name	default value	R/W	description
0x4800	MIPI_CTRL00	0x04	RW	Bit[7:6]: Reserved Bit[5]: gate_sc_en 0: Clock lane is free running 1: Gate clock lane when there is no packet to transmit Bit[4]: line_sync_en 0: Do not send line short packet for each line 1: Send line short packet for each line Bit[2]: pclk_inv_o 0: Using falling edge of mipi_pclk_o to generate MIPI bus to PHY 1: Using rising edge of mipi_pclk_o to generate MIPI bus to PHY Bit[1]: first_bit Change clk_lane first bit 0: Output 8'h55 1: Output 8'hAA Bit[0]: LPX_select for PCLK domain 0: Auto calculate t_lpx_p, unit pclk2x cycle 1: Use lpx_p_min[7:0]
0x4801	RSVD	–	–	Reserved

table 7-15 MIPI control registers (sheet 2 of 8)

address	register name	default value	R/W	description
0x4802	MIPI_CTRL02	0x00	RW	Bit[7]: hs_prepare_sel 0: Auto calculate T_hs_prepare, unit pclk2x 1: Use hs_prepare_min_o[7:0] Bit[6]: clk_prepare_sel 0: Auto calculate T_clk_prepare, unit pclk2x 1: Use clk_prepare_min_o[7:0] Bit[5]: clk_post_sel 0: Auto calculate T_clk_post, unit pclk2x 1: Use clk_post_min_o[7:0] Bit[4]: clk_trail_sel 0: Auto calculate T_clk_trail, unit pclk2x 1: Use clk_trail_min_o[7:0] Bit[3]: hs_exit_sel 0: Auto calculate T_hs_exit, unit pclk2x 1: Use hs_exit_min_o[7:0] Bit[2]: hs_zero_sel 0: Auto calculate T_hs_zero, unit pclk2x 1: Use hs_zero_min_o[7:0] Bit[1]: hs_trail_sel 0: Auto calculate T_hs_trail, unit pclk2x 1: Use hs_trail_min_o[7:0] Bit[0]: clk_zero_sel 0: Auto calculate T_clk_zero, unit pclk2x 1: Use clk_zero_min_o[7:0]
0x4803	MIPI_CTRL03	0x10	RW	Bit[7:5]: Debug mode Bit[4]: fifo_rd_spd_o Bit[3]: manu_ofset_o t_perio manual offset SMIA Bit[2]: r_manu_half2one t_period half to 1 SMIA Bit[1:0]: Reserved
0x4804	RSVD	–	–	Reserved
0x4805	MIPI_CTRL05	0x00	RW	Bit[7:4]: Debug mode Bit[3]: lpda_retim_manu_o Bit[2]: lpda_retim_sel_o 1: Manual Bit[1]: lpck_retim_manu_o Bit[0]: lpck_retim_sel_o 1: Manual

table 7-15 MIPI control registers (sheet 3 of 8)

address	register name	default value	R/W	description
0x4806	MIPI_CTRL06	0x00	RW	Bit[7:5]: Debug mode Bit[4]: pu_mark_en_o Power up mark1 enable Bit[3]: mipi_remot_rst Bit[2]: mipi_susp Bit[1]: smia_lane_ch_en Bit[0]: tx_lsb_first 0: High bit first 1: Low power transmit low bit first
0x4807	MIPI_CTRL07	0x03	RW	Bit[3:0]: sw_t_lpx ul_tx T_lpx
0x4808	MIPI_CTRL08	0x18	RW	Bit[7:0]: wkup_dly Mark1 wakeup delay/2^10
0x4810	FCNT_MAX	0xFF	RW	Bit[7:0]: fcnt_max[15:8] High byte of maximum frame counter of frame sync short packet
0x4811	FCNT_MAX	0xFF	RW	Bit[7:0]: fcnt_max[7:0] Low byte of maximum frame counter of frame sync short packet
0x4812~ 0x4813	RSVD	–	–	Reserved
0x4814	MIPI_CTRL14	0x2A	RW	Bit[7]: Debug mode Bit[6]: lpkt_dt_sel 0: Use mipi_dt 1: Use dt_man_o as long packet data Bit[5:0]: dt_man Manual data type
0x4815~ 0x4817	RSVD	–	–	Reserved
0x4818	HS_ZERO_MIN	0x00	RW	Bit[7]: Debug mode Bit[1:0]: hs_zero_min[9:8] High byte of minimum value of hs_zero, unit ns
0x4819	HS_ZERO_MIN	0x70	RW	Bit[7:0]: hs_zero_min[7:0] Low byte of minimum value of hs_zero Hs_zero_real = hs_zero_min_o + Tui*ui_hs_zero_min_o
0x481A	HS_TRAIL_MIN	0x0	RW	Bit[7:2]: Debug mode Bit[1:0]: hs_trail_min[9:8] High byte of minimum value of hs_trail, unit ns

table 7-15 MIPI control registers (sheet 4 of 8)

address	register name	default value	R/W	description
0x481B	HS_TRAIL_MIN	0x3C	RW	Bit[7:0]: hs_trail_min[7:0] Low byte of minimum value of hs_trail Hs_trail_real = hs_trail_min_o + Tui*ui_hs_trail_min_o
0x481C	CLK_ZERO_MIN	0x01	RW	Bit[7:2]: Debug mode Bit[1:0]: clk_zero_min[9:8] High byte of minimum value of clk_zero, unit ns
0x481D	CLK_ZERO_MIN	0x2C	RW	Bit[7:0]: clk_zero_min[7:0] Low byte of minimum value of clk_zero Clk_zero_real = clk_zero_min_o + Tui*ui_clk_zero_min_o
0x481E	CLK_PREPARE_MAX	0x5F	RW	Bit[7:0]: clk_prepare_max[7:0] Maximum value of clk_prepare, unit ns
0x481F	CLK_PREPARE_MIN	0x26	RW	Bit[7:0]: clk_prepare_min[7:0] Minimum value of clk_prepare Clk_prepare_real = clk_prepare_min_o + Tui*ui_clk_prepare_min_o
0x4820	CLK_POST_MIN	0x00	RW	Bit[7:2]: Debug mode Bit[1:0]: clk_post_min[9:8] High byte of minimum value of clk_post, unit ns
0x4821	CLK_POST_MIN	0x3C	RW	Bit[7:0]: clk_post_min[7:0] Low byte of minimum value of clk_post Clk_post_real = clk_post_min_o + Tui*ui_clk_post_min_o
0x4822	CLK_TRAIL_MIN	0x00	RW	Bit[7:2]: Debug mode Bit[1:0]: clk_trail_min[9:8] High byte of minimum value of clk_trail, unit ns
0x4823	CLK_TRAIL_MIN	0x3C	RW	Bit[7:0]: clk_trail_min[7:0] Low byte of minimum value of clk_trail clk_trail_real = clk_trail_min_o + Tui*ui_clk_trail_min_o
0x4824	LPX_P_MIN	0x00	RW	Bit[7:2]: Debug mode Bit[1:0]: lpx_p_min[9:8] High byte of minimum value of lpx_p, unit ns
0x4825	LPX_P_MIN	0x32	RW	Bit[7:0]: lpx_p_min[7:0] Low byte of minimum value of lpx_p Lpx_p_real = lpx_p_min_o + Tui*ui_lpx_p_min_o

table 7-15 MIPI control registers (sheet 5 of 8)

address	register name	default value	R/W	description
0x4826	HS_PREPARE_MIN	0x32	RW	Bit[7:0]: hs_prepare_min[7:0] Minimum value of hs_prepare, unit ns
0x4827	HS_PREPARE_MAX	0x55	RW	Bit[7:0]: hs_prepare_max[7:0] Maximum value of hs_prepare Hs_prepare_real = hs_prepare_max_o + Tui*ui_hs_prepare_max_o
0x4828	HS_EXIT_MIN	0x00	RW	Bit[7:2]: Debug mode Bit[1:0]: hs_exit_min[9:8] High byte of minimum value of hs_exit, unit ns
0x4829	HS_EXIT_MIN	0x64	RW	Bit[7:0]: hs_exit_min[7:0] Low byte of minimum value of hs_exit Hs_exit_real = hs_exit_min_o+ Tui*ui_hs_exit_min_o0]
0x482A	UI_HS_ZERO_MIN	0x06	RW	Bit[7:6]: Debug mode Bit[5:0]: Minimum UI value of hs_zero, unit UI
0x482B	UI_HS_TRAIL_MIN	0x04	RW	Bit[7:6]: Debug mode Bit[5:0]: Minimum UI value of hs_trail, unit UI
0x482C	UI_CLK_ZERO_MIN	0x00	RW	Bit[7:6]: Debug mode Bit[5:0]: Minimum UI value of clk_zero, unit UI
0x482D	UI_CLK_PREPARE	0x00	RW	Bit[7:4]: ui_clk_prepare_max Maximum UI value of clk_prepare, unit UI Bit[3:0]: ui_clk_prepare_min Minimum UI value of clk_prepare, unit UI
0x482E	UI_CLK_POST_MIN	0x34	RW	Bit[7:6]: Debug mode Bit[5:0]: ui_clk_post_min[5:0] Minimum UI value of clk_post, unit UI
0x482F	UI_CLK_TRAIL_MIN	0x00	RW	Bit[7:6]: Debug mode Bit[5:0]: ui_clk_trail_min[5:0] Minimum UI value of clk_trail, unit UI
0x4830	UI_LPX_P_MIN	0x00	RW	Bit[7:6]: Debug mode Bit[5:0]: ui_lpx_p_min[5:0] Minimum UI value of lpx_p (pclk2x domain), unit UI

table 7-15 MIPI control registers (sheet 6 of 8)

address	register name	default value	R/W	description
0x4831	UI_HS_PREPARE	0x64	RW	Bit[7:4]: ui_hs_prepare_max Maximum UI value of hs_prepare, unit UI Bit[3:0]: ui_hs_prepare_min Minimum UI value of hs_prepare, unit UI
0x4832	UI_HS_EXIT_MIN	0x00	RW	Bit[7:6]: Debug mode Bit[5:0]: ui_hs_exit_min[5:0] Minimum UI value of hs_exit, unit UI
0x4833	MIPI_PKT_STAR_SIZE	0x08	RW	Bit[7:6]: Debug mode Bit[5:0]: mipi_pkt_star_size[5:0]
0x4834~ 0x4836	RSVD	–	–	Reserved
0x4837	PCLK_PERIOD	0x2D	RW	Bit[7:0]: pclk_period[7:0] Period of pclk2x, pclk_div=1, and 1 bit decimal
0x4838	MIPI_LP_GPIO0	0x00	RW	Bit[7]: lp_sel0 0: Auto generate mipi_lp_dir0_o 1: Use lp_dir_man0 to be mipi_lp_dir0_o Bit[6]: lp_dir_man0 0: Input 1: Output Bit[5]: lp_p0_o Bit[4]: lp_n0_o Bit[3]: lp_sel1 0: Auto generate mipi_lp_dir1_o 1: Use lp_dir_man1 to be mipi_lp_dir1_o Bit[2]: lp_dir_man1 0: Input 1: Output Bit[1]: lp_p1_o Bit[0]: lp_n1_o

table 7-15 MIPI control registers (sheet 7 of 8)

address	register name	default value	R/W	description
0x4839	MIPI_LP_GPIO1	0x00	RW	Bit[7]: lp_sel2 0: Auto generate mipi_lp_dir2_o 1: Use lp_dir_man2 to be mipi_lp_dir2_o Bit[6]: lp_dir_man2 0: Input 1: Output Bit[5]: lp_p2_o Bit[4]: lp_n2_o Bit[3]: lp_sel3 0: Auto generate mipi_lp_dir3_o 1: Use lp_dir_man3 to be mipi_lp_dir3_o Bit[2]: lp_dir_man3 0: Input 1: Output Bit[1]: lp_p3_o Bit[0]: lp_n3_o
0x483A~ 0x483B	RSVD	–	–	Reserved
0x483C	MIPI_CTRL3C	0x02	RW	Bit[7:4]: Debug mode Bit[3:0]: t_clk_pre Unit: pclk2x cycle
0x483D	MIPI_LP_GPIO4	0x00	RW	Bit[7]: lp_ck_sel0 0: Auto generate mipi_ck_lp_dir0_o 1: Use lp_ck_dir_man0 to be mipi_ck_lp_dir0_o Bit[6]: lp_ck_dir_man0 0: Input 1: Output Bit[5]: lp_ck_p0_o Bit[4]: lp_ck_n0_o Bit[3]: lp_ck_sel1 0: Auto generate mipi_ck_lp_dir1_o 1: Use lp_ck_dir_man1 to be mipi_ck_lp_dir1_o Bit[2]: lp_ck_dir_man1 0: Input 1: Output Bit[1]: lp_ck_p1_o Bit[0]: lp_ck_n1_o

table 7-15 MIPI control registers (sheet 8 of 8)

address	register name	default value	R/W	description
0x484A	SEL_MIPI_CTRL4A	0x3F	RW	Bit[7:6]: Debug mode Bit[5]: slp_lp_pon_man_o Set for power up Bit[4]: slp_lp_pon_da Bit[3]: slp_lp_pon_ck Bit[2]: mipi_slp_man_st MIPI bus status manual control enabled in sleep mode Bit[1]: clk_lane_state Bit[0]: data_lane_state
0x484B	SMIA_OPTION	0x07	RW	Bit[7:2]: Debug mode Bit[1]: clk_start_sel_o 0: Clock starts after SOF 1: Clock starts after reset Bit[0]: sof_sel_o 0: Frame starts after HREF starts 1: Frame starts after SOF
0x484C	SEL_MIPI_CTRL4C	0x00	RW	Bit[7:4]: Debug mode Bit[3]: smia_fcnt_i select Bit[2]: prbs_enable Bit[1]: hs_test_only MIPI high speed only test mode enable Bit[0]: set_frame_cnt_0 Set frame count to inactive mode (keep 0)
0x484D	TEST_PATTEN_DATA	0xB6	RW	Bit[7:0]: test_patten_data[7:0] Data lane test pattern register
0x484E	FE_DLY	0x10	RW	Bit[7:0]: r_fe_dly_o Last packet to frame end delay / 2
0x484F	TEST_PATTEN_CK_DATA	0x55	RW	Bit[7:0]: clk_test_patten_reg

7.16 ISP control [0x5000 - 0x5004, 0x5006 - 0x5009, 0x500B - 0x5017]

table 7-16 ISP control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5000	ISP CTRL00	0x2F	RW	ISP Control 00 (0: disable; 1: enable) Bit[7]: Debug mode Bit[6]: pre_isp_man_en Bit[5]: dgc_en Bit[4]: awb_gain_en Bit[3]: bc_en Bit[2]: wc_en Bit[1]: Reserved Bit[0]: blc_en
0x5001	ISP CTRL01	0x20	RW	Bit[7]: Debug mode Bit[6]: sof_sel Bit[5]: eof_sel1 Bit[4]: eof_sel0 Bit[3]: awb_out_sel Bit[2]: pre_out_sel Bit[1]: blc_out_sel Bit[0]: byp_isp_sel
0x5002	ISP CTRL02	0x10	RW	Bit[7:5]: Not used Bit[4]: bias_plus Bit[3]: bias_man_en Bit[2]: blkv_in Bit[1]: imgv_in Bit[0]: no_latch
0x5003	ISP CTRL03	0x10	RW	Bit[7:0]: bias_man[7:0]
0x5004	ISP CTRL4	0x01	RW	Bit[7]: size_man_en Bit[6:4]: win_y_offset_adjust Bit[3:0]: Not used
0x5006	ISP CTRL06	0x00	RW	Bit[7:0]: Manual horizontal size[15:8]
0x5007	ISP CTRL07	0x00	RW	Bit[7:0]: Manual horizontal size[7:0]
0x5008	ISP CTRL08	0x00	RW	Bit[7:0]: Manual vertical size[15:8]
0x5009	ISP CTRL09	0x00	RW	Bit[7:0]: Manual vertical size[7:0]
0x500B	DPC SRAM TEST	0x02	RW	Bit[7:6]: Not used Bit[5]: dpc_sram_test1 Bit[4]: dpc_sram_rme Bit[3:0]: dpc_sram_rm
0x500C	MANUAL X_START	0x00	RW	Bit[7:4]: Not used Bit[3:0]: pre_isp manual x_start_address[11:8]
0x500D	MANUAL X_START	0x00	RW	Bit[7:0]: pre_isp manual x_start_address[7:0]

table 7-16 ISP control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x500E	MANUAL X_END	0x00	RW	Bit[7:4]: Not used Bit[3:0]: pre_isp manual x_end_address[11:8]
0x500F	MANUAL X_END	0x00	RW	Bit[7:0]: pre_isp manual x_end_address[7:0]
0x5010	MANUAL Y_START	0x00	RW	Bit[7:4]: Not used Bit[3:0]: pre_isp manual y_start_address[11:8]
0x5011	MANUAL Y_START	0x00	RW	Bit[7:0]: pre_isp manual y_start_address[7:0]
0x5012	MANUAL Y_END	0x00	RW	Bit[7:4]: Not used Bit[3:0]: pre_isp manual y_end_address[11:8]
0x5013	MANUAL Y_END	0x00	RW	Bit[7:0]: pre_isp manual y_end_address[7:0]
0x5014	MANUAL X_OUTPUT_SIZE	0x0	RW	Bit[7:4]: Not used Bit[3:0]: pre_isp manual x_output_size[11:8]
0x5015	MANUAL X_OUTPUT_SIZE	0x00	RW	Bit[7:0]: pre_isp manual x_output_size[7:0]
0x5016	MANUAL Y_OUTPUT_SIZE	0x00	RW	Bit[7:4]: Not used Bit[3:0]: pre_isp manual y_output_size[11:8]
0x5017	MANUAL Y_OUTPUT_SIZE	0x00	RW	Bit[7:0]: pre_isp manual y_output_size[7:0]

7.17 pre_ISP [0x5080]

table 7-17 pre_ISP register

address	register name	default value	R/W	description
0x5080	PRE_ISP CTRL0	0x00	R/W	Bit[7]: Test pattern enable 0: Disable test function 1: Enable test function Bit[6:4]: Not used Bit[3:2]: color_bar_style 00: Standard color bar 01: Top-bottom darker color bar 10: Right-left darker color bar 11: Bottom-top darker color bar Bit[1:0]: Not used

7.18 digital gain compensation [0x5100, 0x5102 - 0x5105]

table 7-18 digital gain compensation registers

address	register name	default value	R/W	description
0x5100	DGC CTRL0	0x05	RW	Bit[7:3]: Not used Bit[2]: dither_en Bit[1]: dgc_man_en Bit[0]: Not used
0x5102	DGC MAN	0x02	RW	Bit[1:0]: dgc_man[9:8]
0x5103	DGC MAN	0x00	RW	Bit[7:0]: dgc_man[7:0]
0x5104	DGC	–	R	Bit[1:0]: dgc[9:8]
0x5105	DGC	–	R	Bit[7:0]: dgc[7:0]

7.19 MWB control [0x5180 - 0x5185]

table 7-19 MWB control registers

address	register name	default value	R/W	description
0x5180	MWB R GAIN	0x04	RW	Bit[7:4]: Not used Bit[3:0]: mwb_r_gain[11:8]
0x5181	MWB R GAIN	0x00	RW	Bit[7:0]: mwb_r_gain[7:0]
0x5182	MWB G GAIN	0x04	RW	Bit[7:4]: Not used Bit[3:0]: mwb_g_gain[11:8]
0x5183	MWB G GAIN	0x00	RW	Bit[7:0]: mwb_g_gain[7:0]
0x5184	MWB B GAIN	0x04	RW	Bit[7:4]: Not used Bit[3:0]: mwb_b_gain[11:8]
0x5185	MWB B GAIN	0x00	RW	Bit[7:0]: mwb_b_gain[7:0]

7.20 WINC control [0x5700 - 0x570C]

table 7-20 WINC control registers

address	register name	default value	R/W	description
0x5700	WINC CTRL00	0x00	RW	Bit[7:5]: Not used Bit[4:0]: x_start_offset[12:8] Start address in horizontal high byte
0x5701	WINC CTRL01	0x00	RW	Bit[7:0]: x_start_offset[7:0] Start address in horizontal low byte
0x5702	WINC CTRL02	0x00	RW	Bit[7:5]: Not used Bit[4:0]: y_start_offset[12:8] Start address in vertical high byte
0x5703	WINC CTRL03	0x00	RW	Bit[7:0]: y_start_offset[7:0] Start address in vertical low byte
0x5704	WINC CTRL04	0x02	RW	Bit[7:5]: Not used Bit[4:0]: window_width[12:8] Select whole zone width high byte
0x5705	WINC CTRL05	0x80	RW	Bit[7:0]: window_width[7:0] Select whole zone width low byte
0x5706	WINC CTRL06	0x01	RW	Bit[7:4]: Not used Bit[3:0]: window_height[11:8] Select whole zone height high byte
0x5707	WINC CTRL07	0xE0	RW	Bit[7:0]: window_height[7:0] Select whole zone height low byte
0x5708	WINC CTRL08	0x00	RW	Bit[7:3]: Reserved Bit[2]: flip_offset_en Bit[1]: Window enable option Bit[0]: Manual window enable
0x5709	WINC RO09	–	R	Bit[7:4]: Not used Bit[3:0]: Pixel count[11:8] for debug
0x570A	WINC RO0A	–	R	Bit[7:0]: Pixel count[7:0] for debug
0x570B	WINC RO0B	–	R	Bit[7:4]: Not used Bit[3:0]: Line count[11:8] for debug
0x570C	WINC RO0C	–	R	Bit[7:0]: Line count[7:0] for debug

7.21 DPC control [0x5780 - 0x5785, 0x578E - 0x578F]

table 7-21 DPC control registers

address	register name	default value	R/W	description
0x5780	DPC CTRL00	0x03	RW	Bit[7:5]: Reserved Bit[4]: manual_mode_en Bit[3:2]: Reserved Bit[1:0]: edge_opt
0x5781	DPC CTRL01	0x0E	RW	Bit[7:4]: Reserved Bit[3]: sc_en Bit[2]: dc_en Bit[1]: cross_en Bit[0]: saturate_en
0x5782	DPC CTRL02	0x21	RW	Bit[7]: Reserved Bit[6:4]: wthre_list0 Bit[3]: Reserved Bit[2:0]: wthre_list1
0x5783	DPC CTRL03	0x04	RW	Bit[7:5]: Reserved Bit[4]: adpt_ptn Bit[3:0]: bthre_ratio
0x5784	DPC CTRL04	0x03	RW	Bit[7]: Reserved Bit[6:0]: gain_list[6:0]
0x5785	DPC CTRL05	0x46	RW	Bit[7:4]: Thre1 Bit[3:0]: Saturate
0x578E	DPC CTRL0E	–	R	Bit[7:5]: Reserved Bit[4]: ro_bthre3 Bit[3]: Reserved Bit[2:0]: ro_wthre[2:0]
0x578F	RO_BTHRE	–	R	Bit[7:5]: Not used Bit[4:0]: ro_bthre[4:0]

8 operating specifications

8.1 absolute maximum ratings

table 8-1 absolute maximum ratings

parameter		absolute maximum rating[a]
ambient storage temperature		-40°C to +125°C
supply voltage (with respect to ground)	V_{DD-IO}	4.5V
electro-static discharge (ESD)	human body model	2000V
	machine model	200V
all input/output voltages (with respect to ground)		-0.3V to V_{DD-IO} + 1V
I/O current on any input or output pin		± 200 mA
peak solder temperature (10 second dwell time)		245°C

a. exceeding the absolute maximum ratings shown above invalidates all AC and DC electrical specifications and may result in permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

8.2 functional temperature

table 8-2 functional temperature

parameter	range
operating temperature[a]	-30°C to +70°C junction temperature
stable image temperature[b]	0°C to 50°C junction temperature

a. sensor functions but image quality may be noticeably different at temperatures outside of stable image range

b. image quality remains stable throughout this temperature range

8.3 DC characteristics

table 8-3 DC characteristics (-30°C < T_J < 70°C)

symbol	parameter	min	typ	max	unit
supply					
V_{DD-IO}	supply voltage (digital I/O)	1.7	1.8	1.9	V
V_{DD-A}	supply voltage (analog)	3.1	3.3	3.45	V
V_{DD-D}	supply voltage (digital core)	1.7	1.8	1.9	V
I_{DD-A}	active (operating) current		TBD	TBD	mA
I_{DD-IO}			TBD	TBD	mA
I_{DD-D}			TBD	TBD	mA
$I_{DDS-SCCB}$	standby current		TBD	TBD	µA
$I_{DDS-XSHUTDN}$			TBD	TBD	µA
digital inputs (typical conditions: DOVDD = 1.8V)					
V_{IL}	input voltage LOW			0.81	V
V_{IH}	input voltage HIGH	1.89			V
C_{IN}	input capacitor			10	pF
digital outputs (standard loading 25 pF)					
V_{OH}	output voltage HIGH	1.62			V
V_{OL}	output voltage LOW			0.18	V
serial interface inputs					
V_{IL}[a]	SCL and SDA	-0.5	0	0.81	V
V_{IH}[a]	SCL and SDA	1.26	1.8	1.89	V

a. based on DOVDD = 1.8 V

8.4 AC characteristics

table 8-4 AC characteristics (T_A = 25°C, V_{DD-IO} = 2.8V)

symbol	parameter	min	typ	max	unit
ADC parameters					
B	analog bandwidth		12		MHz
DLE	DC differential linearity error		0.5		LSB
ILE	DC integral linearity error		1		LSB
	settling time for hardware reset			<1	ms
	settling time for software reset			<1	ms
	settling time for resolution mode change			<1	ms
	settling time for register setting			<300	ms

table 8-5 timing characteristics

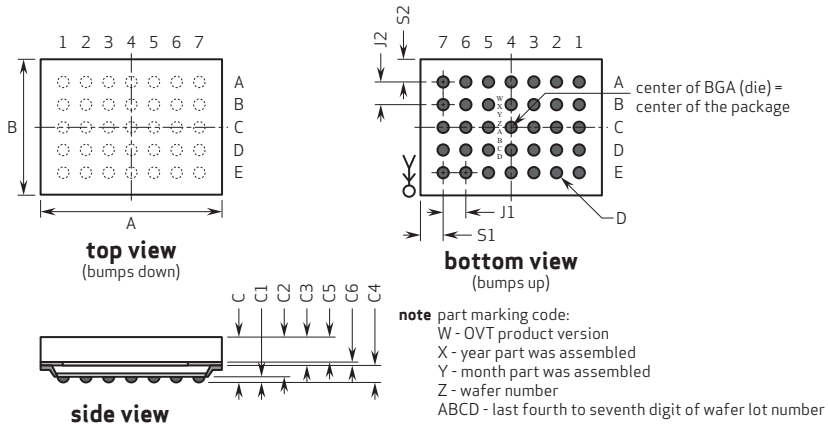
symbol	parameter	min	typ	max	unit
oscillator and clock input					
f_{OSC}	frequency (XVCLK)	6	24	27	MHz
t_r, t_f	clock input rise/fall time			5 (10[a])	ns
	clock input duty cycle	45	50	55	%

a. if using the internal PLL

9 mechanical specifications

9.1 physical specifications

figure 9-1 package specifications



note
Please use black material mask for the CSP PCB or add metal to the back of the PCB to avoid the CSP package pattern from showing through in the image under low color temperature lighting conditions.

table 9-1 package dimensions

parameter	symbol	min	typ	max	unit
package body dimension x	A	4679	4704	4729	µm
package body dimension y	B	2969	2994	3019	µm
package height	C	680	740	800	µm
ball height	C1	100	130	160	µm
package body thickness	C2	575	610	645	µm
thickness of glass surface to wafer	C3	425	445	465	µm
image plane height	C4	250	295	340	µm
glass thickness	C5	385	400	415	µm
air gap between sensor and glass	C6	41	45	49	µm
ball diameter	D	220	250	280	µm
total ball count	N		35 (4 NC)		
pins pitch x-axis	J1		660		µm
pins pitch y-axis	J2		510		µm
edge-to-pin center distance along x	S1	342	372	402	µm
edge-to-pin center distance along y	S2	447	477	507	µm

9.2 IR reflow specifications

note
The OV9732 uses a lead free package.

figure 9-2 IR reflow ramp rate requirements

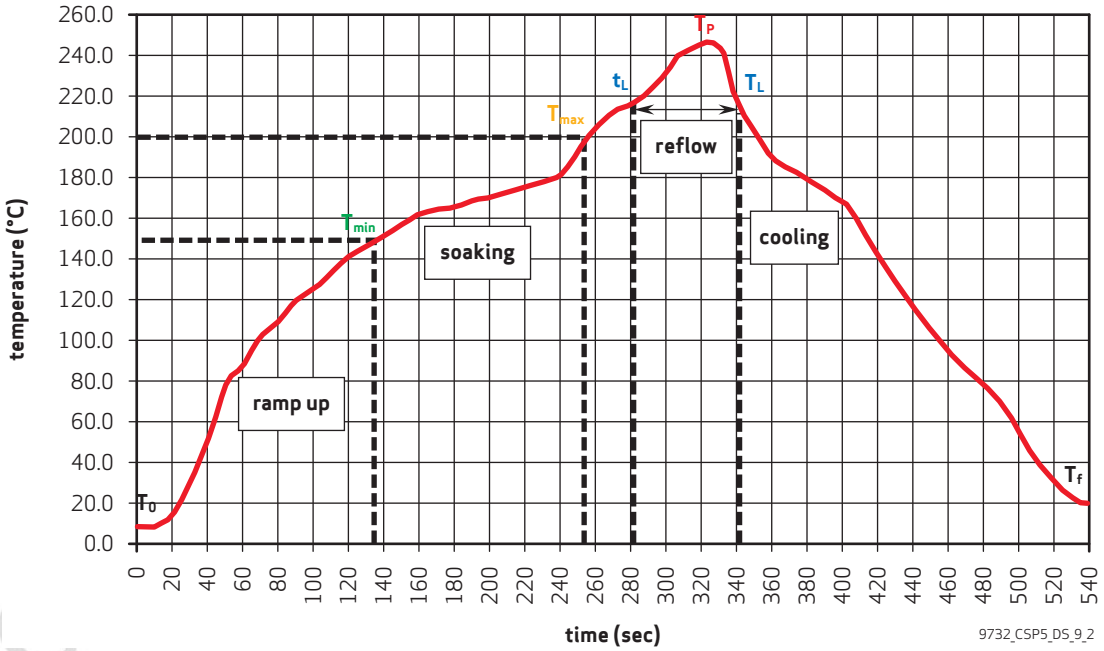


table 9-2 reflow conditions[ab]

zone	description	exposure
ramp up A (T_0 to T_{min})	heating from room temperature to 150°C	temperature slope ≤ 3°C per second
soaking	heating from 150°C to 200°C	90 ~ 150 seconds
ramp up B (t_L to T_P)	heating from 217°C to 245°C	temperature slope ≤ 3°C per second
peak temperature	maximum temperature in SMT	245°C +0/-5°C (duration max 30 sec)
reflow (t_L to T_L)	temperature higher than 217°C	30 ~ 120 seconds
ramp down A (T_P to T_L)	cooling down from 245°C to 217°C	temperature slope ≤ 3°C per second
ramp down B (T_L to T_f)	cooling down from 217°C to room temperature	temperature slope ≤ 2°C per second
T_0 to T_P	room temperature to peak temperature	≤ 8 minutes

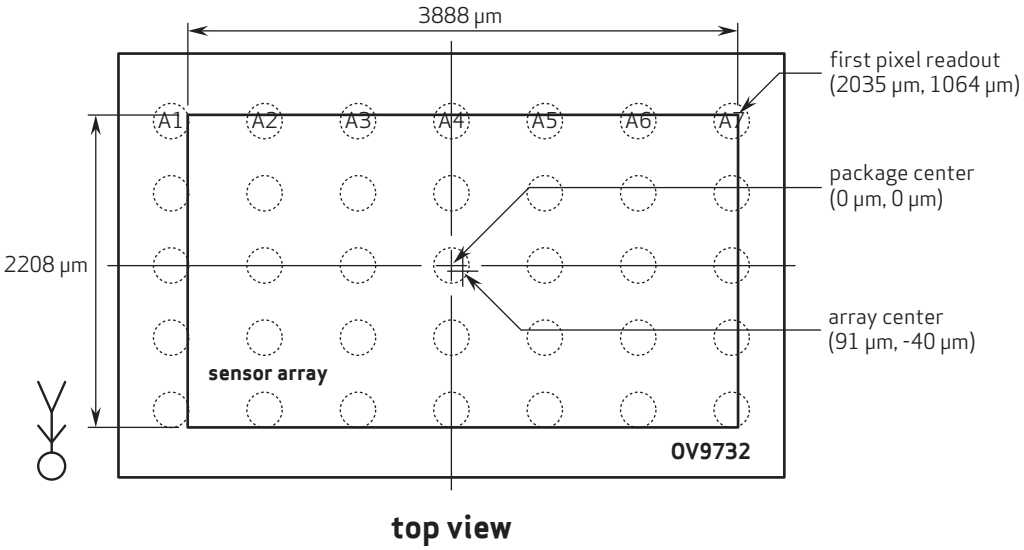
a. maximum number of reflow cycles = 3

b. N2 gas reflow or control O2 gas PPM <500 as recommendation

10 optical specifications

10.1 sensor array center

figure 10-1 sensor array center



top view

note 1 this drawing is not to scale and is for reference only.

note 2 as most optical assemblies invert and mirror the image, the chip is typically mounted with pins A1 to A7 oriented down on the PCB.

9732_CSP5_DS_10_1

10.2 lens chief ray angle (CRA)

figure 10-2 chief ray angle (CRA)

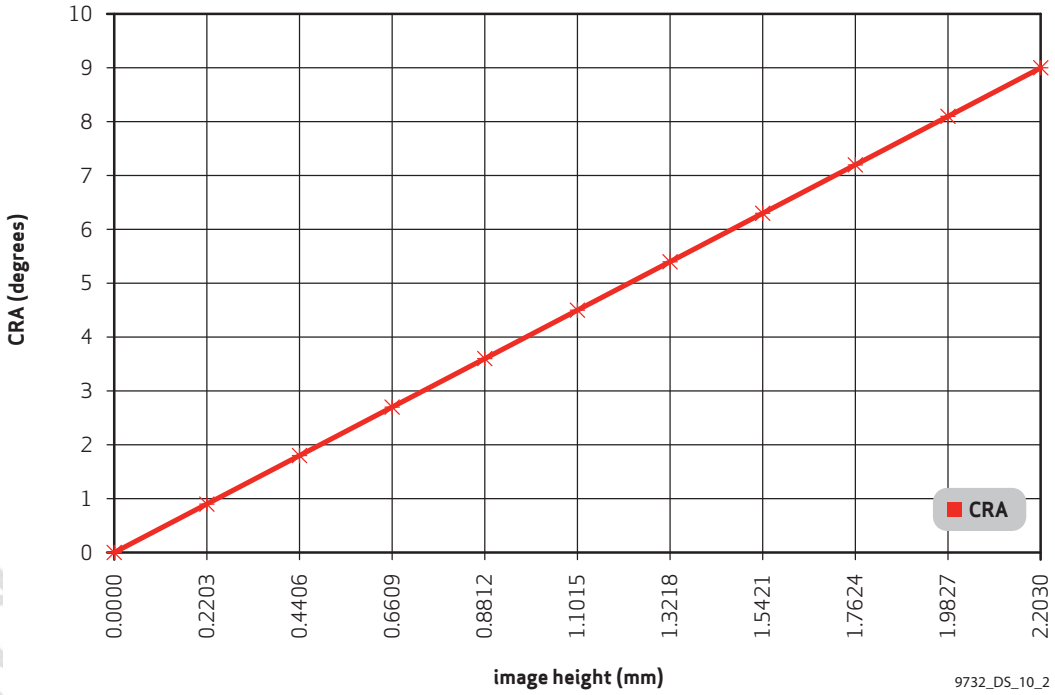


table 10-1 CRA versus image height plot

field (%)	image height (mm)	CRA (degrees)
0	0	0
0.1	0.2203	0.9
0.2	0.4406	1.8
0.3	0.6609	2.7
0.4	0.8812	3.6
0.5	1.1015	4.5
0.6	1.3218	5.4
0.7	1.5421	6.3
0.8	1.7624	7.2
0.9	1.9827	8.1
1	2.203	9

revision history

version 1.0 03.04.2015

- initial release

version 1.01 03.12.2015

- in key specifications, changed lens chief ray angle from 32.1° to 9°
- in section 10.2, updated figure 10-2 and table 10-1

version 1.02 03.20.2015

- in section 9.1, added sidebar note “Please use black material mask for the CSP PCB or add metal to the back of the PCB to avoid the CSP package pattern from showing through in the image under low color temperature lighting conditions.”

version 1.03 04.30.2015

- in section 7.21, changed title to DPC control [0x5780 ~ 0x5785, 0x578E ~ 0x578F]
- in table 7-21, updated all register default values and descriptions

version 1.04 05.11.2015

- in key specifications, updated operating temperature range to -30°C to 70°C junction temperature

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