General Description:

JX-H62 is an HD CMOS image sensor designed with a superior 3.0µm pixel with excellent low-light sensitivity and low dark current performance. It features a 30fps native high definition (HD) 720p video capability for camera applications in PC multimedia, security, and entertainment devices.

The JX-H62 consists of a 1296x732 active pixel sensor (APS) array with an on-chip 10-bit ADC, programmable gain control (PGA), and correlated double sampling (CDS) to significantly reduce fixed pattern noise (FPN). The sensor also has many standard programmable and automatic functions. It has both the industry compliant DVP parallel and MIPI CSI2 serial interfaces. The external host controller can access this device through a standard serial interface.

It is available in wafer-level packaged CSP.

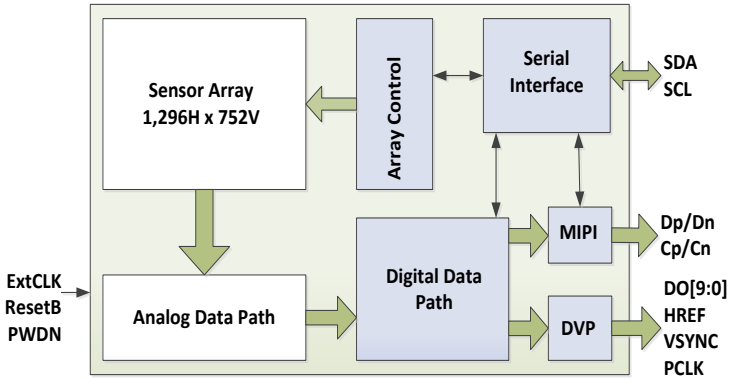
Features:

- Automatic functions:
  - AEC – Automatic Exposure Control
  - AGC – Automatic Gain Control
  - ABLC – Automatic Black Level Calibration
- Programmable controls:
  - Gain, exposure, frame rate and size
  - Image mirror and flip
  - Window panning and cropping
  - I2C slave ID
- Output formats:
  - DVP parallel interface
  - MIPI CSI2 1 Lane
- Data formats:
  - 10-bit RAW RGB
- Others
  - 50/60Hz flick noise cancellation
  - Register group write capability
  - Frame synchronization
  - Black sun spot cancellation

Key Specifications:

Optical format		1/4”
Active Pixels		1296H x 732V
Pixel size		3.0 x 3.0 µm
Color filter array		RGB Bayer pattern
Chief Ray Angle		17.5 degrees linear
Shutter type		Electronic rolling shutter
Maximum Frame Rate		30fps
Supply voltage	**Digital**	1.35 – 1.65V (1.5V nominal)
	Analog	2.6 – 3.0V (2.8V nominal)
	I/O	1.7 – 3.0V (1.8V nominal)
Power consumption	**Active**	45mA
	Standby	< 300 µA
Output Formats		10-bit RGB Raw Data
Sensitivity		TBD mV/lux-sec
Max SNR		TBD db
Dynamic Range		TBD db
Dark Current		<TBD mV/sec @ 45C
Operating junction temperature		-30 ˚C to 85 ˚C
Stable image junction temperature		TBD

Functional Block:



Component Order Information:

Part Number	Description
JX-H62-C1	CSP

Contents

Pin Diagram:

JX-H62's pin diagram is shown in Figure 1 and each pin's description is shown in Table 1:

Figure 1. H62's Top View CSP Pin Diagram

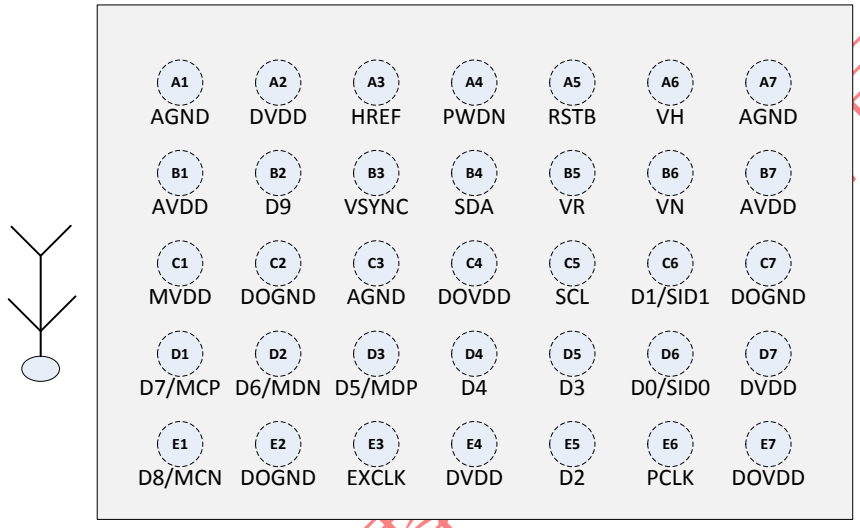


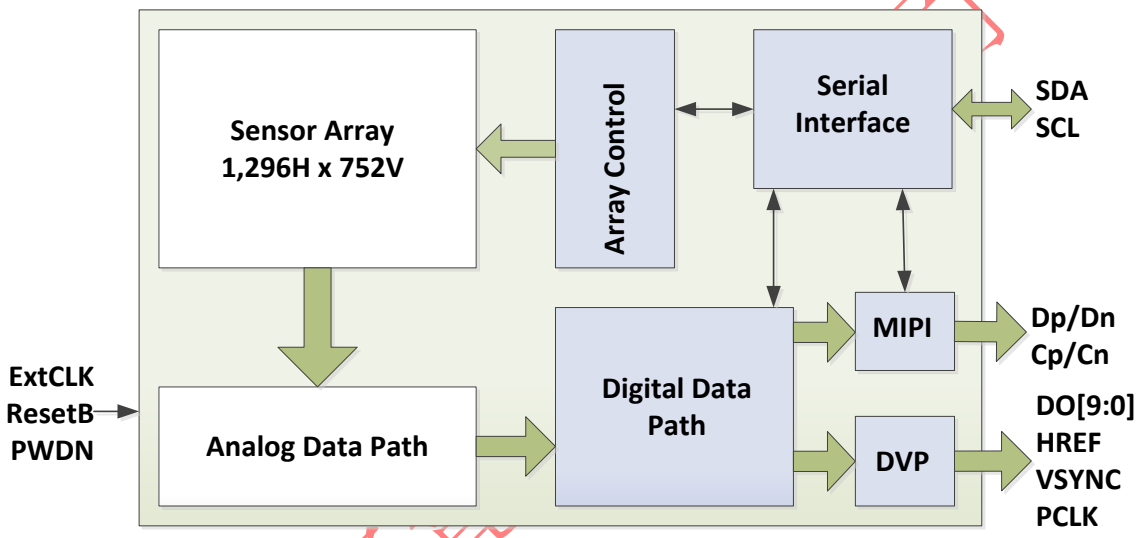
Table 1: Pin Description

Pin number	Pin name	Pin type	Description
A1	AGND	Supply	Analog ground
A2	DVDD	Supply	Digital core supply voltage. With embed regulator
A3	HREF	I/O	Line data valid signal output.
A4	PWDN	Input	Chip power down initiate pin. High active.
A5	RSTB	Input	System synchronize reset when driven low, it resumes normal operation with all configuration register set to factory default
A6	VH	Reference	Internal analog reference.
A7	AGND	Supply	Analog ground
B1	AVDD	Supply	Analog supply voltage.
B2	D9	I/O	DVP data output bit 9;
B3	VSYNC	I/O	Vertical synchronize signal, drive high when last frame end and drive low before next frame start. Also can be programmed as frame synchronize input
B4	SDA	I/O	Serial data, pull to DOVDD with a 4.3k Ω resistor
B5	VR	Reference	Analog Reference
B6	VN	Reference	Internal analog reference.
B7	AVDD	Supply	Analog supply voltage.
C1	MVDD	Supply	MIPI block supply voltage, connect to DVDD pin.
C2	DOGND	Supply	Digital I/O ground
C3	AGND	Supply	Analog ground
C4	DOVDD	Supply	Digital I/O supply voltage.
C5	SCL	Input	Serial interface clock input.
C6	D1/SID1	I/O	DVP data output bit 1; I2C Slave ID programming bit<1>, default pull down internally. I2C slave ID can be programmed as “60/61”, “64/65”, “68/69” or ”6C/6D” for write and read.
C7	DOGND	Supply	Digital I/O ground
D1	D7/MCP	I/O	DVP data output bit 7 or MIPI clock lane positive output.
D2	D6/MDN	I/O	DVP data output bit 6 or MIPI data lane negative output.
D3	D5/MDP	I/O	DVP data output bit 5 or MIPI data lane positive output.
D4	D4	I/O	DVP data output bit 4.
D5	D3	I/O	DVP data output bit 3.
D6	D0/SID0	I/O	DVP data output bit 0; I2C Slave ID programming bit<0>, default pull down internally.
D7	DVDD	Supply	Digital core supply voltage. With embed regulator
E1	D8/MCN	I/O	DVP data output bit 8 or MIPI clock lane negative output.
E2	DOGND	Supply	Digital I/O ground
E3	EXCLK	Input	System clock input.
E4	DVDD	Supply	Digital core supply voltage. With embed regulator
E5	D2	I/O	DVP data output bit 2.
E6	PCLK	I/O	Pixel clock.
E7	DOVDD	Supply	Digital I/O supply voltage.

Functional Overview:

The JX-H62 is a progressive-scan CMOS image sensor. It has an on-chip, phase-locked loop (PLL) to generate internal clocks from a single master input clock running between 6 and 27MHz. Its analog data process and digital data process can handle up to 70Mp/s at corresponding pixel clock 70MHz. Figure 2 illustrates a block diagram of the sensor.

Figure 2. Functional Block Diagram



User can access and program JX-H62 sensor internal registers through the two-wire serial bus. The core of the sensor is a 1296x732 active-pixel array. The timing and control circuitry sequences through the rows of the array, resetting and then reading each row in turn. In the time interval between resetting and reading that row, the pixels in the row integrate the incident light. The exposure is controlled by varying the time interval between reset and readout. Once a row has been read, the data from the columns is sequenced through an analog signal path to apply gain and analog signal to digital signal converter (ADC). The ADC output passes through a digital processing path for black level calibration. Then the data will output though a DVP port or MIPI CSI-2 standard interface.

Pixel Array Format:

The JX-H62 pixel array consists of a 1296-column by 752-row matrix of pixels addressed by column and row. The address (column 0, row 0) represents the upper-right corner of the entire array (please refer to Figure 3 for Pixel array structure). The first 8 rows are optical black row for black level calibration, and outside of the 1280x732 active pixels are several boundary pixels: 6 rows on top, 6 rows below, 8 columns on the right and 8 columns on the left. The detailed pixel array arrangement and default read out direction is noted in the Figure 4.

Figure 3: Pixel array structure

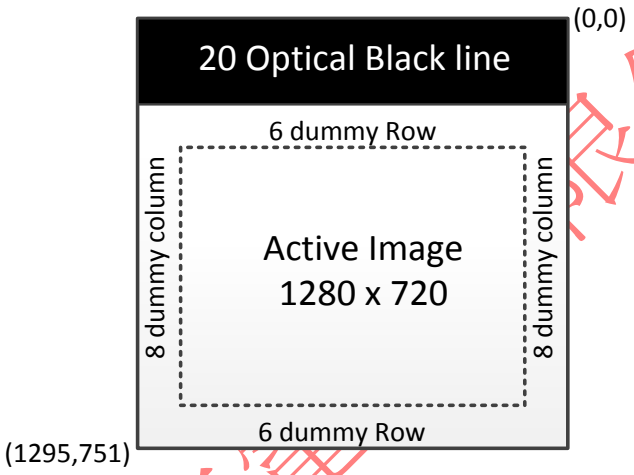
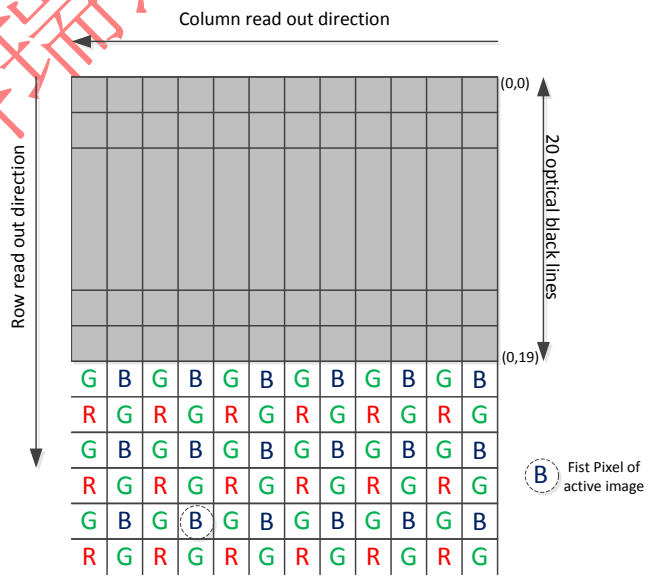


Figure 4: Pixel array detail with default read out direction.



Data Output Format:

The output images are divided into frames, which are further divided into lines. By default, the sensor produces 720 lines (rows) of 1280 columns each. The VSYNC and HREF signals indicate the boundaries between frames and lines, respectively. PCLK can be used as a clock to latch the data. For each PCLK cycle, one 10-bit pixel data outputs on the D[9:0] pins (Figure 5). The pixel data is valid when HREF signal is asserted. The VSYNC signal indicates frame end and new frame start. JX-H62 default frame timing is illustrated as figure 6.

Figure 5: row data output timing

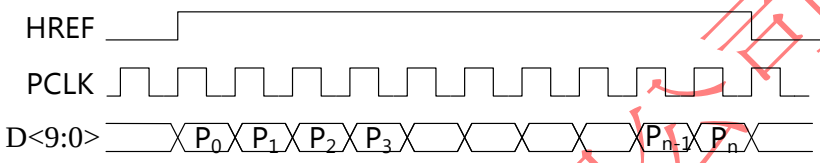
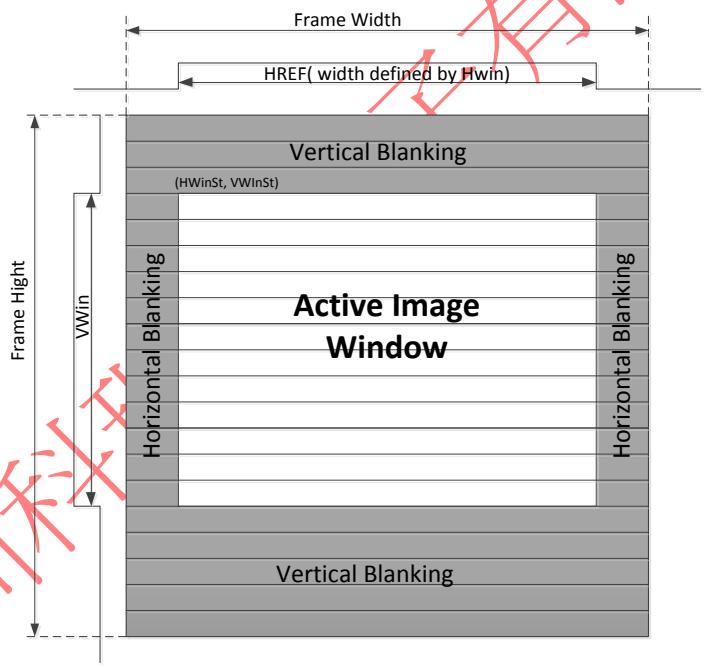


Figure 6: Default frame timing



As shown above in figure 5, a line (row) period can be calculated as Trow = Frame_width * Tpclk, and frame rate can be calculated as fps=1/(Frame_hight * Trow).

As default configuration, VSYNC, PCLK and Data are all valid at PCLK rising edge. For user convenience, JX-H62 provides register bits to control HREF, VSYNC and PCLK polarity. In addition, PCLK also have adjustable delay control.

For pixel Bayer pattern data output, several settings can have effect on pixel output sequences. These registers include HWIn_St, VWin_St, HAddr_St, Mirror, V_Flip. Please consult your SOI AE for further information.

Sensor Luminance Control:

JX-H62 has built-in automatic luminance control capability. The main purpose for luminance control is to get proper image level through exposure and gain adjustment. There are 2 configurations described below:

1) 50/60Hz flick noise cancelling (also known as banding filter). When this feature is turned on, user needs to set the line equivalents of 1/100s or 1/120s, exposure will attempt to stay within n/100s or n/120s boundaries (where "n" is an integer number). The gap between each step will be filled with gain. If the light is too strong, exposure will continuously adjust to under 1/100s or 1/120 boundary conditions. Under this condition, the moving or fixed light bands may still be observed by user.

2) Auto frame rate adjustment. For some extreme low light condition, JX-H62 provides the option to automatically slow down the frame rate to adjust exposure to a proper image level. The lowest frame rate is 1/8.

Test Pattern Output:

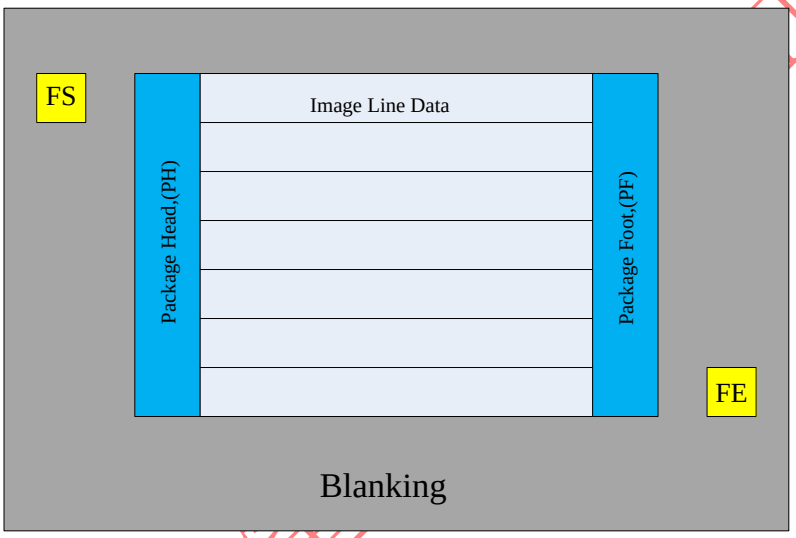
JX-H62 can output test patterns as described below:

1) Walking "1" test pattern: for most sensor module connectivity test, JX-H62 provides walking "1" test pattern.

MIPI interface:

JX-H62 support MIPI CSI-2 compliant interface. It has one pair of differential clock lane and one pair of differential data lane. JX-H62 can output raw8 or raw10 mode through MIPI interface. In raw8 mode, only 8 MSBs of 10-bit data will output and user needs to set MIPI clock speed at 8x parallel port pixel clock. In raw10 mode, user needs to set MIPI PHY clock as 10x parallel port pixel clock.

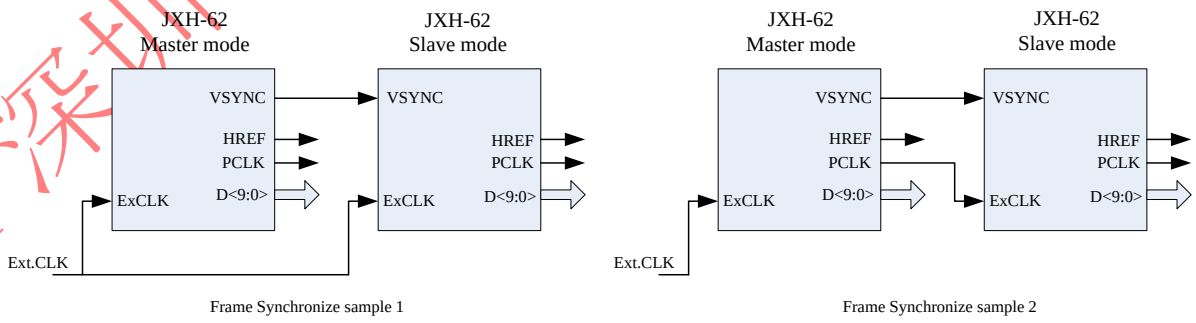
Figure 7: MIPI interface frame timing



Frame Synchronization:

JX-H62 provides the capability of frame synchronization. By setting VSYNC pin as input and enable frame-sync option, JX-H62 will work as slave device and synchronized with an external VSYNC. If all master devices and slave devices use same timing setting, all devices frame timing mismatch will be less than few pixel clocks. Figure 8 shows 2 ways to realize frame synchronization.

Figure 8: Frame Synchronization illustration



In the above 2 frame synchronize configurations, sample 2 will have more accurate synchronization than sample 1 because the slave device will have exactly same pixel clock as the master.

Serial Interface:

The serial interface is a two-wire bi-directional bus. Both wires (Serial Clock -SCL and Serial Data - SDA) are connected to DOVDD via a pull-up resistor, and when the bus is free both lines are high. The two-wire serial interface defines several different transmission stages as follows:

- A start bit
- The slave device 7-bit address
- An (No) acknowledge bit coming from slave
- An 8-bit or 16-bit message (address and/or data)
- A stop bit (or another 8bit or 16bit message in multiple Read/Write access)

Figure 9: I2C Timing chart

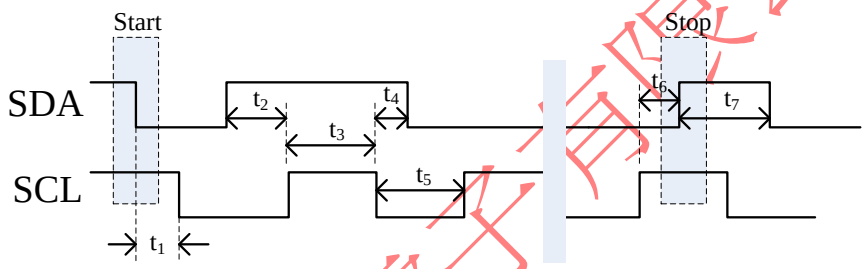
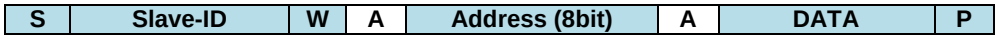


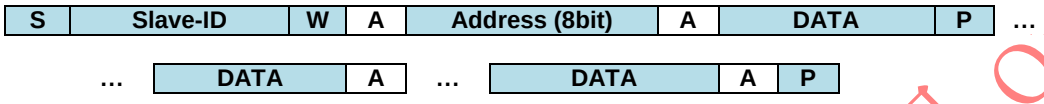
Table 2: I2C timing characteristic

Symbol	Description	Min	Max	Units
	SCL clock frequency	0	400k	Hz
t1	Hold time for START condition	0.6	-	µs
t2	Data setup time	160	-	ns
t3	High period of the SCL clock	0.6	-	µs
t4	Data hold time	0	0.9	µs
t5	Low period of the SCL clock	1.3	-	µs
t6	Setup time for STOP condition	0.6	-	µs
t7	Bus free time between STOP and START condition	1.3	-	µs
	Rise time for both SDA and SCL signals		300	ns
	Fall time for both SDA and SCL signals		300	ns
Cb	Capacitive load for each bus line		400	pF

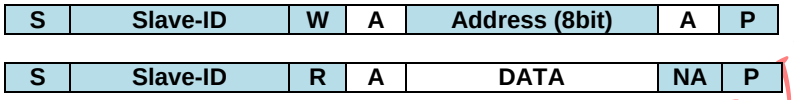
Single Write Mode operation



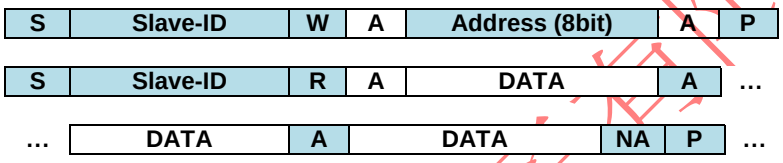
Multiple Write Mode (Register address is increased automatically) operation



Single Read Mode operation



Multiple Read Mode (Register address is increased automatically) operation



S: start conditions, A: acknowledge bit, NA: no acknowledge, DATA: 8 bit data, P: stop condition
JX-H62 slave ID is programmable, default is 0x60/61 for write and read. User can program DVP data bit<1:0> for other configuration. The slave ID program table is list below:

D[1]	D[0]	Read/Write
X	X	60/61
X	Pull high	64/65
Pull high	X	68/69
Pull high	Pull high	6C/6D

.

Register Group Write Function:

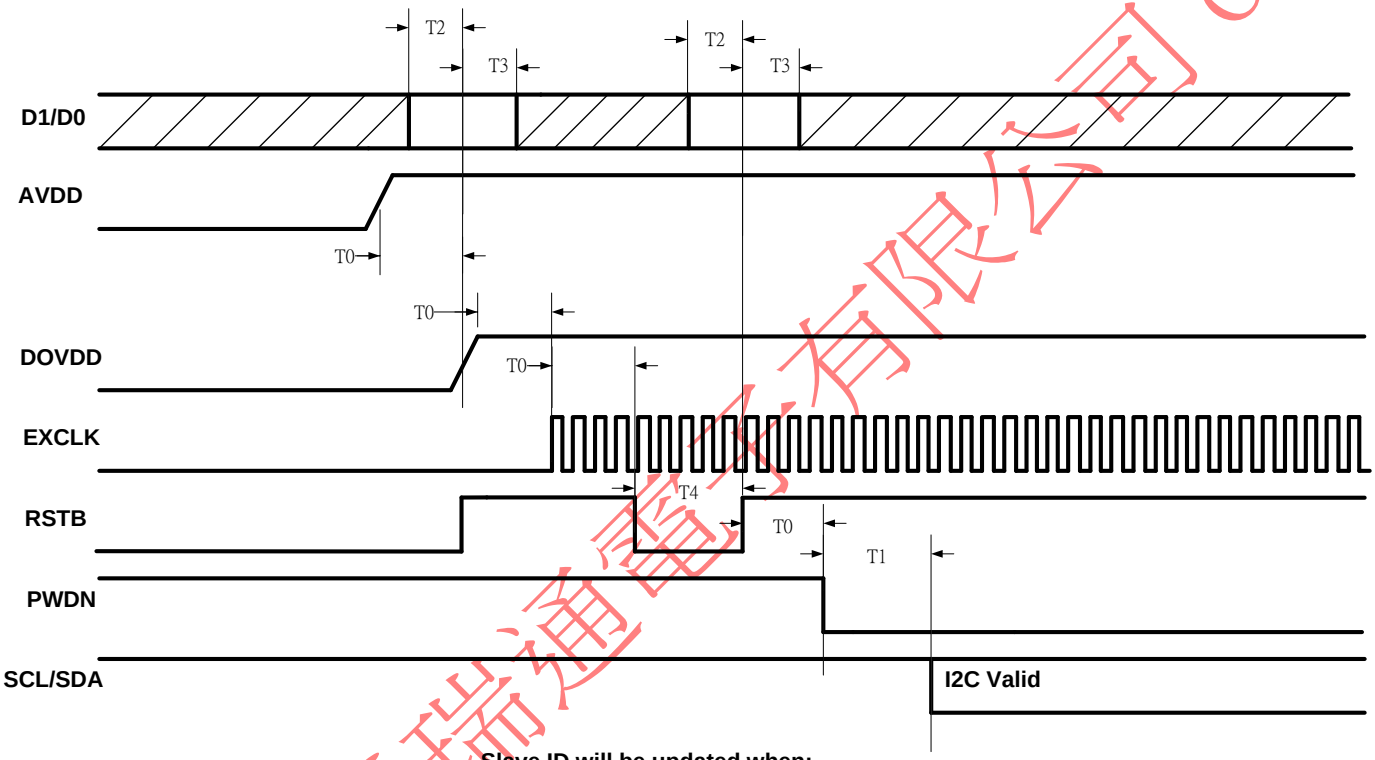
JX-H62 provides register group write function, user can pre-load address and data from register 0xC0 to 0xFF, then trigger this function by setting Reg0x1F[7], normally JX-H62 will auto write back group register content at next vertical blanking period and reset Reg0x1F[7]. JX-H62 can update up to 32bytes of registers.

User can always monitor Reg0x1F[7] to make sure group write procedure is finished or not.

Power on/off sequence:

Figure 10 shows a reference power up sequence of JX-H62.

Figure 10. Power up sequence for JX-H62



Note:
1. T0 >= 0 us
2. T1 >= 8192 EXCLK cycles
3. T2>= 1ms
4. T3>= 1ms
5. T4>= 10ms

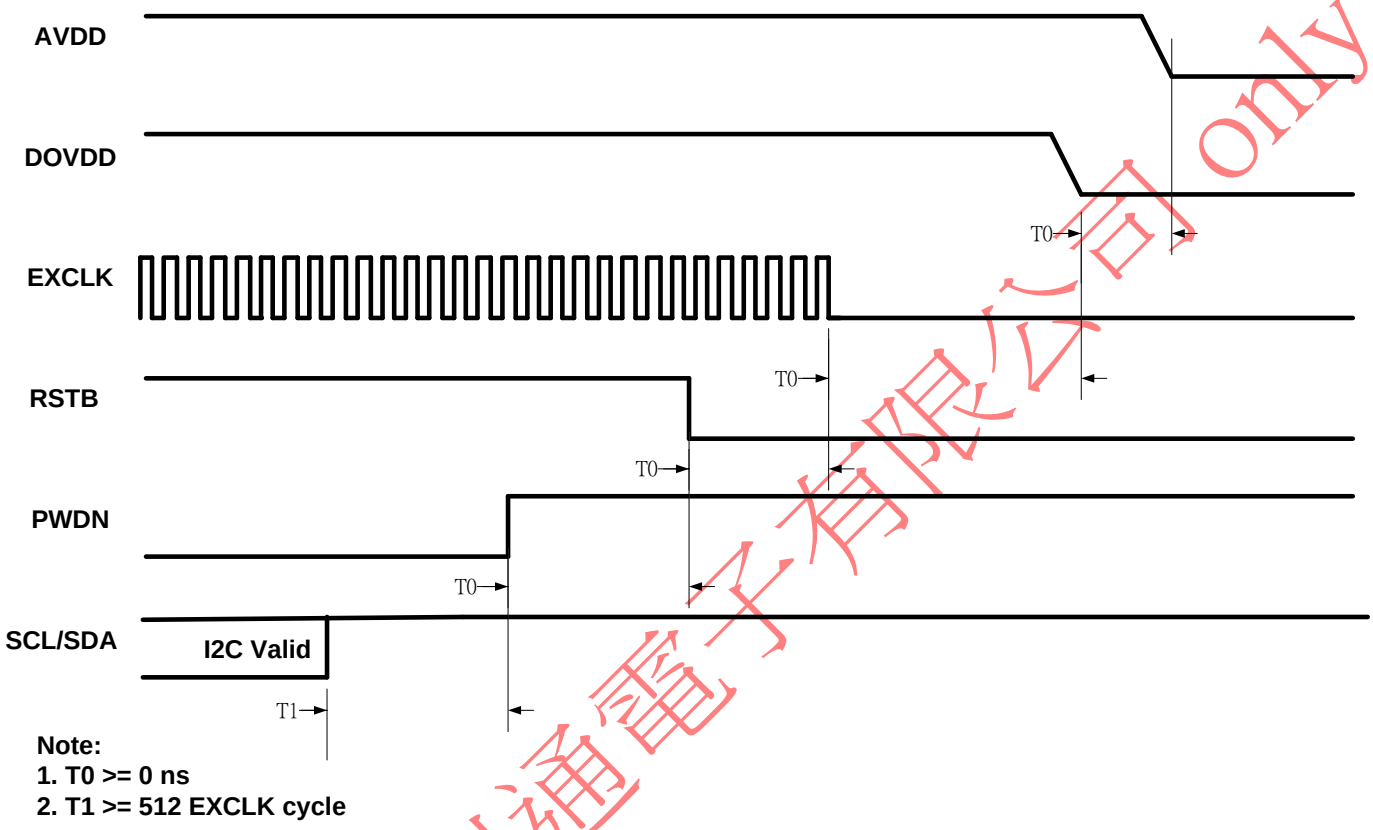
Slave ID will be updated when:
1. Power up (DOVDD)
2. Hardware reset pin: Low -> High
3. Software reset : Reg0x12[7]=" 1"

Please stable D1/D0 when issue above commands.

D[1]	D[0]	Read/Write
X	X	60/61
X	Pull high	64/65
Pull high	X	68/69
Pull high	Pull high	6C/6D

Figure 11 shows a reference power down sequence of JX-H62.

Figure 11. Power down sequence for JX-H62



Electrical Characteristics:

Table 3. Absolute maximum ratings

Symbol	Descriptions	Absolute maximum rating	Units
V_{DD-IO}	I/O Digital Power	4.5	V
V_{DD-A}	Analog Power	4.5	V
V_{DD-D}	Core Digital Power	4.5	V
V_I	Input voltages	-0.3v to V_{DD-IO} + 1V	V
T_A	Ambient Temperature	TBD	ºC
T_S	Storage Temperature	TBD	ºC

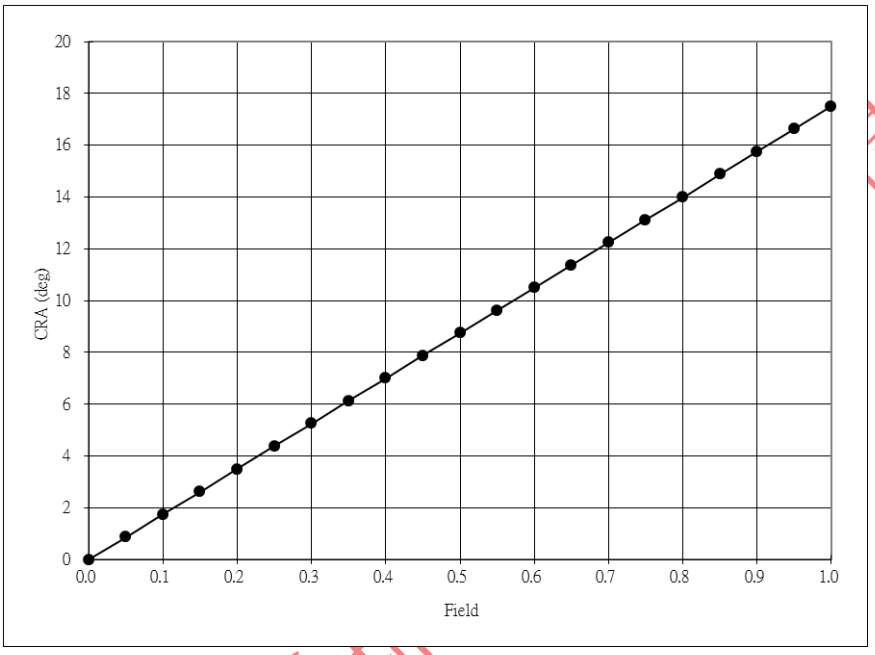
Table 4. DC Characteristics (0°C ≤ TA ≤ 85°C, Voltages referenced to GND)

Symbol	Descriptions	Max	Typ	Min	Units
supply					
V_{DD-IO}	Supply voltage (DOVDD)	3.0	1.8	1.7	V
V_{DD-A}	Supply voltage (AVDD)	3.0	2.8	2.6	V
V_{DD-D}	Supply voltage (DVDD) With embed regulator	1.65	1.5	1.35	V
Digital Inputs					
V_{IL}	Input voltage LOW	0.2* V_{DD-IO}	-	-	V
V_{IH}	Input voltage HIGH			0.7*V_{DD-IO}	V
C_{IN}	Input capacitor	10			pF
Digital Outputs (loading 20pF)					
V_{OH}	Output voltage HIGH			V_{DD-IO} – 0.2	V
V_{OL}	Output voltage LOW	0.2			V
Power consumption (Internal DVDD, EVDD short to DVDD;DVP output mode; AVDD=2.8V, DOVDD=1.8V)					
I_{DD-IO}	Supply current (V_{DD-IO}=1.8V@30fps FHD without digital I/O loading)		15		mA
I_{DD-A}	Supply current (V_{DD-A}=2.8V@30fps FHD)		20		mA
Power consumption (Internal DVDD, EVDD short to DVDD;MIPI output mode; AVDD=2.8V, DOVDD=1.8V)					
I_{DD-IO}	Supply current (V_{DD-IO}=1.8V@30fps FHD without digital I/O loading)		25		mA
I_{DD-A}	Supply current (V_{DD-A}=2.8V@30fps FHD)		20		mA
Ipwrdn	HW PWDN Pin active		300		uA

CRA Specifications:

JX-H62 is designed with a linear chief ray angle curve as shown in Figure 10. The shifting of the color filter and microlenses on the sensor is critical to accommodate the ever shorter height of the camera module as well as minimizing shading at the corner of the image.

Figure 10. CRA Curve for JX-H62

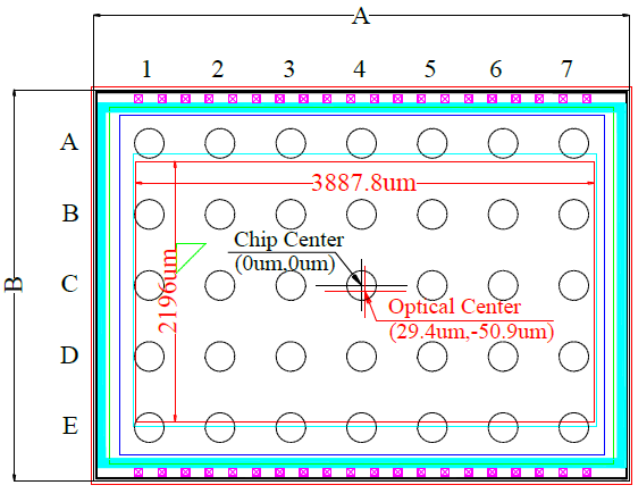


Field	CRA
0.00	0.000
0.05	0.875
0.10	1.750
0.15	2.625
0.20	3.500
0.25	4.375
0.30	5.250
0.35	6.125
0.40	7.000
0.45	7.875
0.50	8.750
0.55	9.625
0.60	10.500
0.65	11.375
0.70	12.250
0.75	13.125
0.80	14.000
0.85	14.875
0.90	15.750
0.95	16.625
1.00	17.500

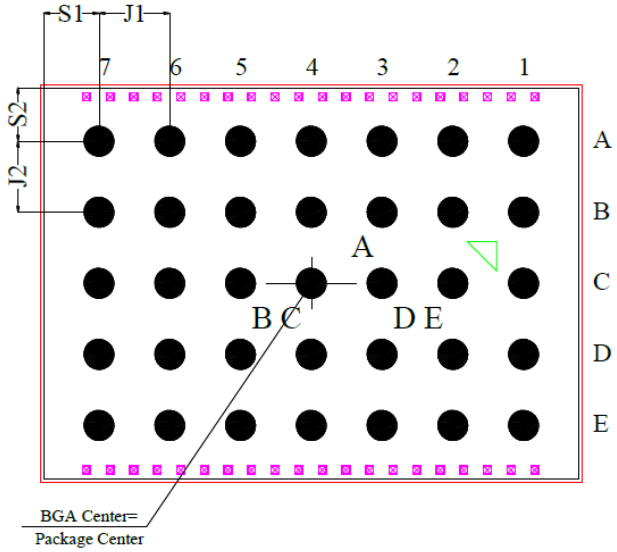
Mechanical Specifications:

JX-H62 is available in CSP packaged component. Figure 11 shows top view and bottom view of the CSP component. Table 5 shows the nominal dimensions for the packaged chip.

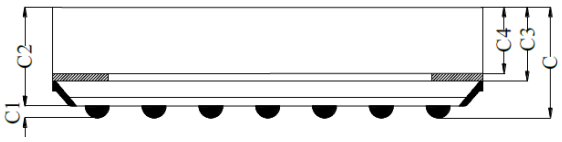
Figure 11. CSP Top, Bottom, Side View



Top View



Bottom View



Side View

Table 5. Dimensions for JX-H62 CSP package (in mm)

	Symbol	Nominal	Min	Max
		Millimeters		
Package Body Dimension X	A	4.539	4.514	4.564
Package Body Dimension Y	B	3.304	3.279	3.329
Package Height	C	0.740	0.680	0.800
Ball Height	C1	0.130	0.100	0.160
Package Body Thickness	C2	0.610	0.575	0.645
Thickness from top glass surface to wafer	C3	0.445	0.425	0.465
Glass Thickness	C4	0.400	0.385	0.415
Ball Diameter	D	0.250	0.220	0.280
Total Ball Count	N	35		
Pins pitch X axis	J1	0.6		
Pins pitch Y axis	J2	0.6		
Edge to Pin Center Distance along X	S1	0.4695	0.4395	0.4995
Edge to Pin Center Distance along Y	S2	0.4520	0.4220	0.4820

CSP Module Schematic (Reference):

Figure 13,14 show reference schematics for CSP DVP/MIPI module.

Figure 13. Reference schematic for H62 CSP DVP module

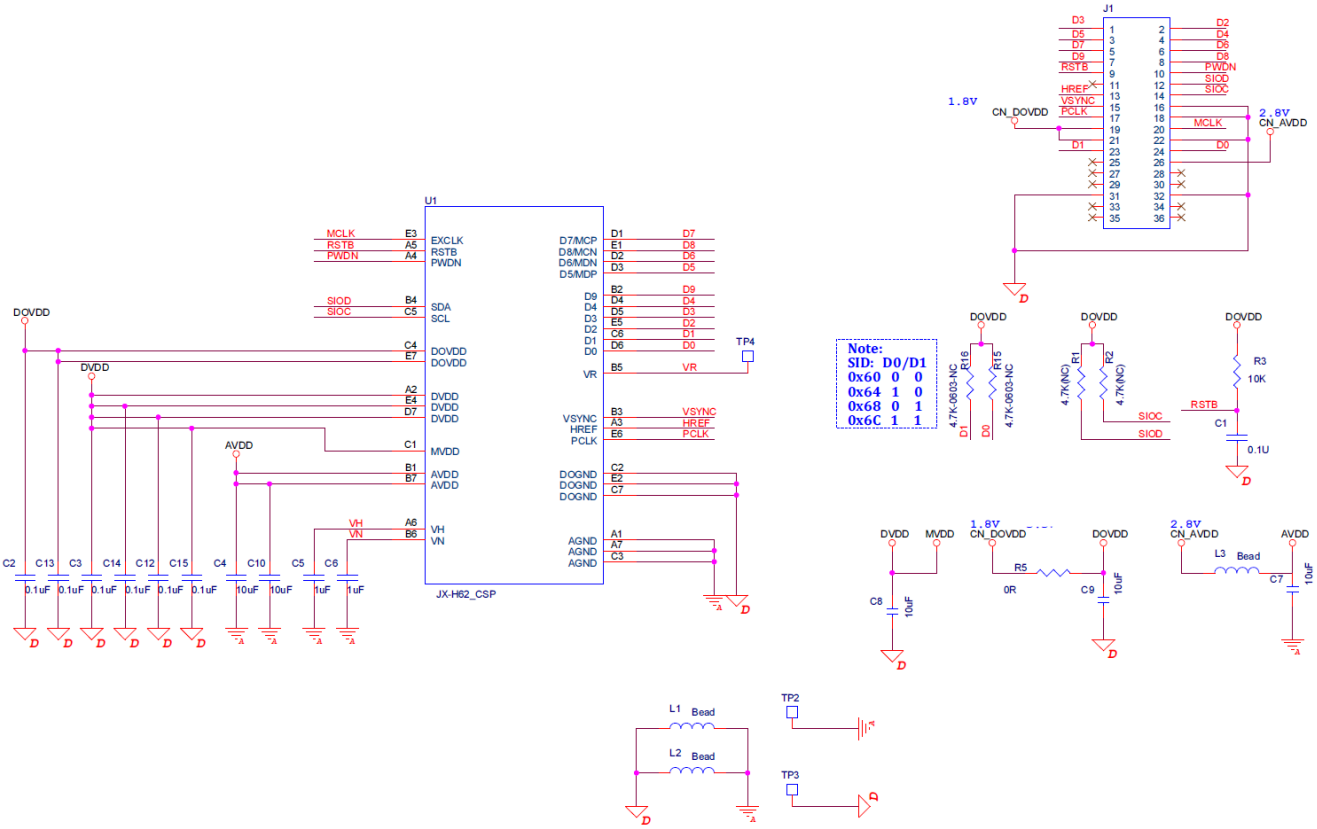
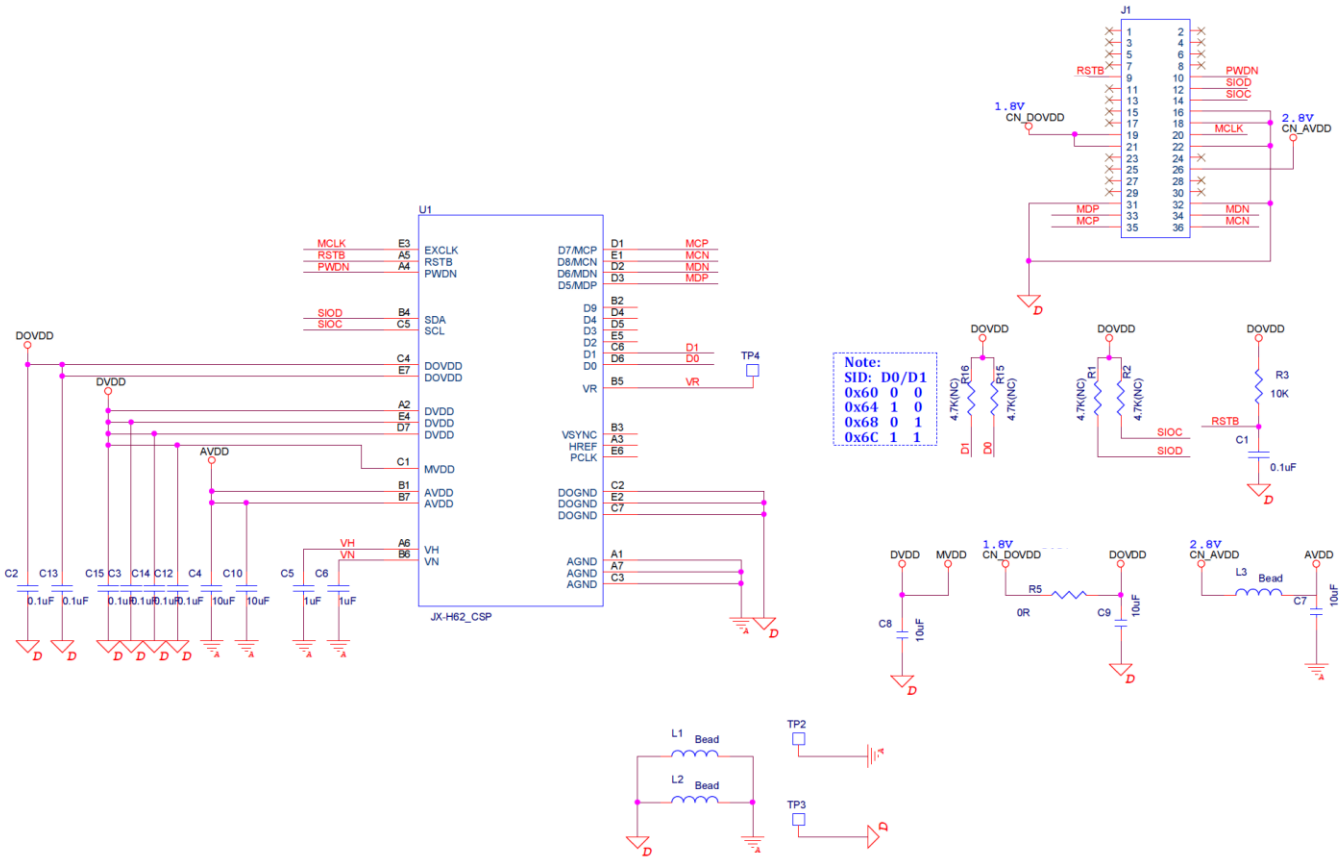


Figure 14. Reference schematic for H62 CSP MIPI module



Register Descriptions:

Address (Hex)	Register Name	Default (Hex)	R/W	Description
00	PGA	00	RW	Programmable gain, valid 0 to 4F,PGA[7] reserved Total gain = 2^PGA[6:4]*(1+PGA[3:0]/16)
01	EXP	FF	RW	Exposure line LSBs, EXP[7:0]
02	EXP	00	RW	Exposure line MSBs, EXP[15:8]. Exposure time is defined by EXP[15:0] at line period base. T_{EXP}=EXP[15:0]*T_{row}
03-08	PLEXP	FF	RW	Reserved
09	VER	00	R	Version ID
0A	PIDH	A0	R	Product ID MSBs.
0B	PIDL	62	R	Product ID LSBs.
0C	DVP1	40	RW	DVP control 1. DVP1[7]: RSVD DVP1[6]: Sensor sun spot elimination control, “1”: disable sun spot elimination, “0”: enable sun spot elimination. DVP1[5:2]: RSVD DVP1[1:0]: DVP test mode output option. “00”: DVP output normal image data. “01”: DVP[9:0] = Output 10-bit walk “1” test pattern.“10”,“11”: RSVD
0D	DVP2	50	RW	DVP control 2. DVP2[7:4]: RSVD DVP2[3:2]: PAD drive capability. “00”: min, “11”: max. DVP2[1:0]: Digital gain. “00”:1x, “01” and “10”: 2x, “11”:4x
0E	PLL1	10	RW	PLL control 1. PLL1[7]: PLL bypass selection. “1”: PLLclk = Input clock/PLL_Pre_Ratio. “0”: see PLL2[3:0]. PLL1[6:2]: reserved PLL1[1:0]: PLL pre-divider ratio. PLL_Pre_Ratio = 1 + PLL[1:0] Default : “00”
0F	PLL2	04	RW	PLL control 2. PLL2[7]: Reserved. PLL2[6]: Clock divider, “1”: VCO clock divided by 2 to generate system and mipi clock. DAC clock no change. “0”: normal; PLL2[5:3]: DAC Clock divider: DAC Clock = VCO/(1+PLL2[5:3]) PLL2[2:1]: System clock divider:Mipi_pclk/(1+PLL2[2:1]) PLL2[0]: Mipi Pclk divider: 0: 1/8 for Mipi raw 8 data mode; 1: 1/10 for Mipi raw 10 data mode.
10	PLL3	26	RW	PLL control 3. PLL VCO multiplier. VCO = Input clock*PLL3[7:0]/PLL_Pre_Ratio
11	CLK	80	RW	Digital system clock control CLK[7]: System clock option. “1”: system clock use PLLclk directly. “0”: system clock use PLLclk after digital divide clock CLK[6]: system clock digital doubler on/off selection. “1”: on, “0”: off CLK[5:0]: system clock divide ratio. default : “000000”

				Equation: When CLK[5:0] > 0: System clock = PLLclk *(1+CLK[6])/(2*CLK[5:0]) When CLK[5:0] = 0: System clock = PLLclk*(1+CLK[6])/2
12	SYS	00	RW	System status set up SYS[7]: Soft reset initialize, "1": initial system reset, it will reset whole sensor to factory default status, and this bit will clear after reset. default : "0": normal mode SYS[6]: Sleep mode on/off selection, "1": sensor into sleep mode. No data output and all internal operation stops. External controller can stop sensor clock, while I2C interface still can work. default : "0": normal mode SYS[5]: mirror image on/off, "1": mirrored image output, "0": normal image output SYS[4]: flip image on/off, "1": flipped image output, "0": normal image output. SYS[3:0]:RSVD.
13	LCCtrl1	81	RW	Luminance control registers 1. LCCtrl1[7:6]: Gain ceiling at auto mode. "00": maximum 4X analog gain. "01": 8X, "10": 16X, "11": 32X LCCtrl1[5:3]: Auto Frame rate ceiling control. "000": disable auto frame rate adjust. "001": max frame rate down to 1/2, "010": down to 1/3; "011": down to 1/4; "100": down to 1/5; "101": down to 1/6; "110": down to 1/7; "111": down to 1/8; LCCtrl1[2]: Banding filter on/off selection. "1": on. "0": off LCCtrl1[1]: RSVD LCCtrl1[0]: automatic luminance control on/off selection, "0": auto, "1": manual
14	LCCtrl2	80	RW	Luminance Control register 2. LCCtrl2[7:0]: Image luminance expect target.
15	LCCtrl3	44	RW	Luminance Control register 3 LCCtrl3[7:4]: auto Luminance control adjustment trigger range. LCCtrl3[3:0]: auto luminance control stable range
16	LCCtrl4	C0	RW	Luminance control register 4 LCCtrl[7:0]: Luminance control large step adjustment high threshold
17	LCCtrl5	40	RW	Luminance control register 5 LCCtrl[7:0]: Luminance control large step adjustment low threshold
18	LCCtrl6	99	RW	Luminance control register 6 LCCtrl6[7:0]: Banding filter minimum exposure line LSBs;Band[7:0]
19	LCCtrl17	28	RW	Luminance control register 7 LCCtrl7[7:6]: PCLK delay option. LCCtrl7[5]: AGC delay 1 frame valid option. Manually gain apply option, "0": manual gain will apply at next VSYNC, "1": manual gain will delay 1 frame to apply. LCCtrl7[4:2]: RSVD LLCCtrl7[1:0]: Banding filter minimum exposure line MSBs. Band[9:8]
1A	LCCtrl8	80	RW	Reserved
1B	LCCtrl9	49	RW	Luminance control register 9 LCCtrl9[7:3]:RSVD LCCtrl9[2:1]: pre-precharge line selection, "00": 1 line, "01:2lines, "10": 3 lines, "11": 4 lines. LCCtrl9[0]: pre-precharge option on/off selection, "0": off, "1": on.
1C	LCCtrl10	00	R	Luminance control register 10 LCCtrl10[7:0]: image luminance average value.
1D	DVP3	00	RW	DVP control 3 DVP3[7:0]: GPIO direction control for data output port D[7:0]. "1": enable output. "0": tri-state output.
1E	DVP4	1C	RW	DVP control 4 DVP4[7]: PCLK polarity control. "0": data output at rising edge of PCLK, "1":data output at falling edge of PCLK DVP4[6]: HREF polarity control. 0: positive ; 1: negative

				DVP4[5]: VSYNC polarity control. 0: positive ; 1: negative DVP4[4:0]: GPIO direction control for output port: PCLK, HREF, VSYNC and D[9:8] "1": enable output. "0": tri-state output.
1F	GLat	00	RW	Group latch control GLat[7]: Group write trigger. "1": system will write reg0xC0 to 0xFF content to proper register. This bit will clear after group write. "0": inactive group write function.. GLat[6]: Group latch trigger time option, "0": trigger at vertical blanking period. "1": group latch trigger immediately. GLat[5:0] : RSVD
20	FrameW	AE	RW	Sensor frame time width LSBs; FrameW[7:0]
21	FrameW	08	RW	Sensor frame time width MSBs; FrameW[15:8] FrameW[15:0]: sensor frame width.
22	FrameH	EE	RW	Sensor frame time high LSBs ;FrameH[7:0]
23	FrameH	02	RW	Sensor frame time high MSBs. FrameH[15:8] FrameH[15:0]: sensor frame high. Sensor frame rate is defined as Fpclk / (FrameW*FrameH). Fpclk: frequency of pixel clock
24	HWin	00	RW	Image horizontal output window width LSBs: HWin[7:0]
25	VWin	D0	RW	Image vertical output window high LSBs: VWin[7:0]
26	HVWin	25	RW	Image output window horizontal and vertical MSBs. { VWin[11:8],HWin[11:8]}
27	HWinSt	F8	RW	Image horizontal output window start position LSBs. HWinSt[7:0]
28	VWinSt	0F	RW	Image vertical output window start position LSBs. VWinSt[7:0]
29	HVWinSt	03	RW	Image output window horizontal and vertical start position MSBs. {VWinSt[11:8],HWinSt[11:8]}
2A	CShift1	FC	RW	Column shift control 1 Cshift1[7:6]: Column SRAM data shift start position LSBs.
2B	Cshift2	21	RW	Column shift control 2 Cshift2[7:6]: SRAM read out start address, MSBs, SenHASt[9:8] default :"00" CShift2[5:2]: RSVD CShift2[1:0]: column shift timing MSBs
2C	SenHASt	00	RW	Sensor physical column shift start address LSBs, SenHASt[7:0]; each bit represent 8 pixels
2D	SenVSt	00	RW	Sensor physical vertical start address, LSBs. SenVSt[7:0]; each bit represent 4 lines
2E	SenVEnd	BC	RW	Sensor physical vertical end address, LSBs. SenVEnd[7:0] ;each bit represent 4 lines
2F	SenVadd	00	RW	Sensor vertical address settings. SenVadd[7:4]: RSVD SenVadd[3:2]: SenVEnd[9:8] SenVadd[1:0]: SenVSt[9:8]
30 – 42	SenT1	98	RW	RSVD
43	VS_POS1	00	RW	VSYNC position LSBs: VS_POS[7:0];
44	VS_POS2	40	RW	VS_POS2[7:4]: VSYNC width selection. VS_POS2[3:0]: VSYNC position MSBs ,VS_POS[11:8];
45	SenT14	09	RW	SenT14[7]: SRAM read out start address, MSBs, SenHASt[10]; SenT14[6:0]: Reserved.
46	BLCCtrl1	CB	RW	BLCCtrl1[7:3]: RSVD

				BLCCtrl1[2]: BLC dithering algorithm on/off. BLCCtrl1[1]: BLC rounding algorithm on/off. BLCCtrl1[0]: RSVD
47	BLCCtrl2	47	RW	BLCCttrl[7]: BLC limitation control, “0”: BLC max value is 0x200, “1”: BLC max value is 0x400. BLCCtrl2[6:0]: Reserved.
48	BLCOpt1	02	RW	RSVD
49	BLC_TGT	04	RW	Black level calibration target level. BLC_TGT[7]: sign bit. . “0”: BLC target offset is positive. “1”: negative. BLC_TGT[6:0]: target level.
4A	BLCCtrl2	03	RW	BLC control BLCCtrl[7]: BLC_B bit 10 BLCCtrl[6]: BLC_Gb bit 10 BLCCtrl[5]: BLC_Gr bit 10 BLCCtrl[4]: BLC_R bit 10 BLCCtrl[3:2]: ABLC do continue frames after AE stable, 00: reserved, 01:4frames, 10:2frames, 11:1frames.. BLCCtrl[1]: BLC action option. “0”: Sensor do BLC only when triggered. “1”: always do BLC. BLCCtrl[0]: auto BLC function on/off selection. “0”: sensor stop calculate black value. “1”: sensor calculates black value automatically.
4B	BLC_B	00	RW	B channel black value LSBs. BLC_B[7:0]
4C	BLC_Gb	00	RW	Gb channel black value LSBs. BLC_Gb[7:0]
4D	BLC_Gr	00	RW	Gr channel black value LSBs. BLC_Gr[7:0]
4E	BLC_R	00	RW	R channel black value LSBs. BLC_R[7:0]
4F	BLC_H	00	RW	Black value MSBs. {BLC_R[9:8],BLC_Gr[9:8],BLC_Gb[9:8],BLC_B[9:8]}
50 - 58				RSVD
59	VSun2	80	RW	Second stage black sun control VSun2[7:5]: reserved VSun2[4]: Second stage black sun switch on/off enable, “0”: always off. “1”: Black sun will switch to second stage when analog gain greater than 2x. VSun2[3:0]: Second stage black sun reference control. Strength : (Strong) 1,0,F,E,D,C,B,A,9,8,7,6,5,4,3,2. (Weak);
5A - 69	SRAM	00	RW	RSVD
6A	PWC4	3A	RW	Power control 4 PWC4[7:4]: RSVD PWC4[3:0]: first stage black sun control Strength : (Strong) 1,0,F,E,D,C,B,A,9,8,7,6,5,4,3,2. (Weak);
6B - 6F				RSVD
70	Mipi1	49	RW	Mipi timing control 1 Mipi1[7:5]: Tlpx Mipi1[4:2]: RSVD Mipi1[1]: Mipi 8/10 bit mode switch, “0”: 10-bit, “1”: 8-bit mode Mipi1[0]: reserved
71	Mipi2	8A	RW	Mipi timing control 2 Mipi2[7:5]: Ths-zero Mipi2[4:0]: RSVD
72	Mipi3	68	RW	Mipi timing control 3 Mipi3[7:5]: Ths-prepare

				Mipi3[4:0]: RSVD
73	Mipi4	33	RW	Mipi timing control 4 Mipi4[7]: Mipi pixel clock option Mipi4[6:4]: Ths-trail Mipi4[3:0]: RSVD
74	Mipi5	53	RW	Mipi timing control 5 Mipi5[7]: Mipi_sleep on/off Mipi5[6]: Mipi continues mode or strobe mode selection Mipi5[5:0]: reserved
75	Mipi6	2B	RW	Mipi data type ID
76	Mipi7	40	RW	Mipi word count LSBs
77	Mipi8	06	RW	Mipi word count MSBs
78	Mipi9	18	RW	Mipi timing control 9 Mipi9[7]: CK-pre timing option Mipi9[6:0]: RSVD
79	DPHY1	00	RW	Mipi PHY control 1
7A	DPHY2	00	RW	DPHY2[7]: Mipi interface power down. DPHY2[6:0]: RSVD
7B	DPHY3	02	RW	DPHY3[7:2]:RSVD DPHY3[1:0]: RSVD
7C - 85	DPHY4	0C	RW	RSVD
C0	Group0	0A	RW	Group write 1st data address
C1	Group1	0A	RW	Group write 1st data value.
C2	Group2	0A	RW	Group write 2nd data address
C3	Group3	0A	RW	Group write 2nd data value.
…	…	…	…	…
FE	Group62	0A	RW	Group write 32nd data address
FF	Group63	0A	RW	Group write 32nd data value.

Document Revision Control

Version Number #	Date Released	Comments
R0.0	Mar/8/2016	Initial release of JX-H62 datasheet
R01		NA
R0.2	Apr/2016	C3 pad mistype(D3);; Max gain modify to 0x4f (From 0x7F);; Modify: Reg0x74[7:0] : MIPI sleep, MIPI continuous mode….