General Description:

JX-F22 is a high performance 2.0MP CMOS image sensor designed and fabricated with SOI's 3.0um pixel technology. It can deliver images at 60fps (MIPI) in full HD mode and 30fps in HDR mode.

The JX-F22 consists of a 1932 x 1088 active pixel sensor (APS) array with on-chip 10-bit ADC, programmable gain control (PGA), and correlated double sampling (CDS) to significantly reduce fixed pattern noise (FPN). The sensor also has many standard programmable and automatic functions. It has both the industry compliant DVP parallel and MIPI CSI2 dual-data lane serial interfaces. The external host controller can access this device through a standard serial interface.

It is available in wafer-level packaged CSP.

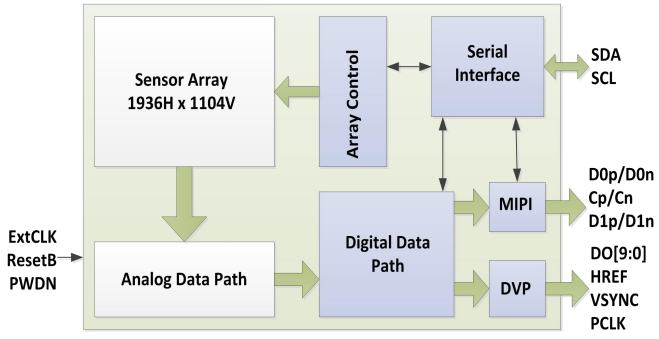
Features:

- Automatic functions:
  - ABLC – Automatic Black Level Calibration
- Programmable controls:
  - Gain, exposure, frame rate and size
  - Image mirror and flip
  - Window panning and cropping
  - I2C slave ID
- Output formats:
  - DVP parallel interface
  - MIPI CSI2 (dual lane)
- Data formats:
  - 10-bit RAW RGB
- HDR mode support
- Others
  - 50/60Hz flick noise cancellation
  - Frame sync
  - Register group write capability
  - Black sun spot cancellation

Key Specifications:

Optical format		1/2.7"
Active Pixels		1932H x 1088V
Pixel size		3.0 x 3.0 μm
Color filter array		RGB Bayer pattern
Chief Ray Angle		17.5 degrees linear
Shutter type		Electronic rolling shutter
Maximum Frame Rate		FHD: 1920x1080 @60fps(MIPI) 1920x1080 @30fps(DVP) HDR: 1920x1080@30fps(MIPI), 2 frame staggered output
Supply voltage	**Digital**	1.35 – 1.65V (1.5V nominal; With embedded 1.5V regulator)
	Analog	2.6 – 3.0V (2.8V nominal)
	I/O	1.7 – 3.45V (1.8V nominal)
Power consumption	**Active**	88 mA@FHD 30fps(MIPI)
	Standby	Typ.: 30 uA
Output Formats		10-bit RGB Raw Data
Sensitivity		3900 mV/lux-sec
Max SNR		38 db
Dynamic range		73 db
Dark Current		12 mV/sec @ 45 ˚C
Operating junction temperature		-30 ˚C to 85 ˚C
Stable image junction temperature		60 ˚C

Functional Block:



Component Order Information:

Part Number	Description
JX-F22-C1	CSP,DVP interface
JX- F22-C1-D3	CSP,DVP interface
JX- F22-C1-M6	CSP,MIPI interface

Contents

Pin Diagram:

JX-F22's pin diagram is shown in Figure 1 and each pin's description is shown in Table 1:

Figure 1: JX-F22 CSP top view

Table 1: Pin Description

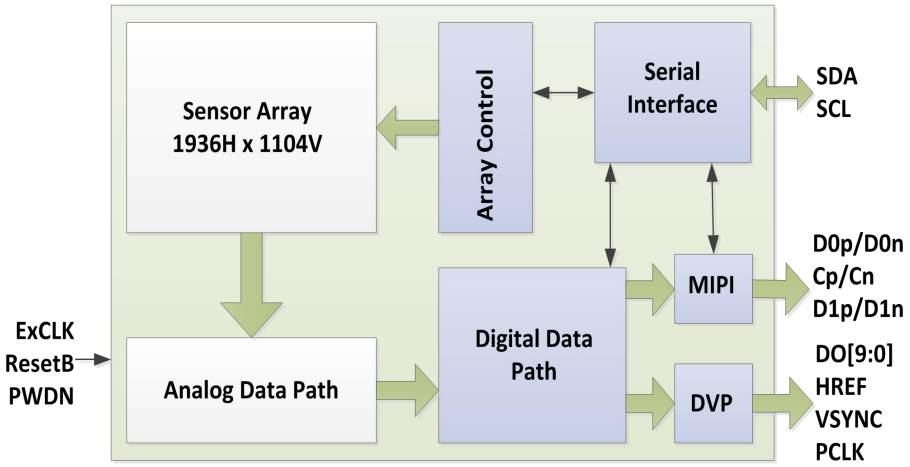
Pin number	Pin name	Pin type	Description
A1	AGND	Supply	Analog ground
A2	DOGND	Supply	Digital I/O ground
A3	DOVDD	Supply	Digital I/O supply voltage.
A4	PWDN	Input	System power down control. High active.
A5	DVDD	Supply	Digital core supply voltage. With embedded 1.5V regulator
A6	DOGND	Supply	Digital I/O ground
A7	NC		
A8	DOGND	Supply	Digital I/O ground
A9	DVDD	Supply	Digital core supply voltage. With embedded 1.5V regulator
A10	AGND	Supply	Analog ground
B1	AVDD	Supply	Analog supply voltage.
B2	DVDD	Supply	Digital core supply voltage. With embedded 1.5V regulator
B3	SCL	Input	Serial interface clock input.
B4	SDA	I/O	Serial data, pull to DOVDD with a 4.3k Ω resistor
B5	RSTB	Input	System synchronize reset when driven low, it resumes normal operation with all configuration register set to factory default
B6 – B8	NC		
B9	VH	Reference	Internal analog reference.
B10	AVDD	Supply	Analog supply voltage.
C1	VR	Reference	Analog Reference
C2	HREF	I/O	Line data valid signal output.
C3	VSYNC	I/O	Vertical synchronize signal, drive high when last frame end and drive low before next frame start. Also can be programmed as frame synchronize input
C4			
C5 – C9	NC		
C10	VN	Reference	Internal analog reference.
D1	D8	I/O	DVP data output bit 8.
D2	D5	I/O	DVP data output bit 5.
D3			
D4	D3	I/O	DVP data output bit 3
D5	D0/SID0	I/O	Pixel data output bit 0. I2C Slave ID programming bit<0>, default pull down internally.
D6	EXCLK	Input	System clock input.
D7	MDN1	I/O	MIPI data lane 1 negative output.
D8	MDP1	I/O	MIPI data lane 1 positive output.
D9	NC		
D10	DOVDD	Supply	Digital I/O supply voltage.
E1	PCLK	I/O	DVP Pixel clock output.
E2	D7	I/O	Pixel data output bit 7.
E3	DVDD	Supply	Digital core supply voltage. With embedded 1.5V regulator
E4	DOGND	Supply	Digital I/O ground
E5	D2	I/O	DVP data output bit 2
E6	AGND	Supply	Analog ground
E7	DOGND	Supply	Digital I/O ground

E8	MCP	I/O	MIPI clock lane positive output.
E9	MDN0	I/O	MIPI data lane 0 negative output.
E10	DOGND	Supply	Digital I/O ground
F1	D9	I/O	DVP data output bit 9
F2	D6	I/O	DVP data output bit 6
F3	DOVDD	Supply	Digital I/O supply voltage.
F4	D4	I/O	DVP data output bit 4
F5	D1/SID1	I/O	DVP data output bit 1. I2C Slave ID programming bit<1>, default pull down internally. I2C slave ID can be programmed as “80/81”, “84/85”, “88/89” or ”8C/8D” for write and read.
F6	AVDD	Supply	Analog supply voltage.
F7	EVDD	Supply	PLL block supply voltage. Connect to DVDD.
F8	MCN	I/O	MIPI clock lane negative output.
F9	MDP0	I/O	MIPI data lane 0 positive output.
F10	DVDD	Supply	Digital core supply voltage. With embedded 1.5V regulator

Functional Overview:

The JX-F22 is a progressive-scan CMOS image sensor. It has an on-chip, phase-locked loop (PLL) to generate internal clocks from a single master input clock running between 6 and 27MHz. Its analog data process and digital data process can handle up to 163.2Mp/s at corresponding pixel clock 163.2MHz. Figure 2 illustrates the sensor's block diagram.

Figure 2. Functional Block Diagram



User can access and program JX-F22 sensor internal registers through the two-wire serial bus. The core of the sensor is a 1936x1088 pixel array. The timing and control circuitry sequences through the rows of the array, resetting and then reading each row in turn. In the time interval between resetting and reading that row, the pixels in the row integrate the incident light. The exposure is controlled by varying the time interval between reset and readout. Once a row has been read, the data from the columns is sequenced through an analog signal path to apply gain and analog signal to digital signal converter (ADC). The ADC output passes through a digital processing path for black level calibration. Then the data will output though a DVP port or MIPI CSI-2 standard interface.

Pixel Array Format:

The JX-F22 pixel array consists of a 1936-column by 1112-row matrix of pixels addressed by column and row. The address (column 0, row 0) represents the upper-right corner of the entire array (please refer to Figure 3 for JX-F22's Pixel array structure). The first 24 rows are optical black row for black level calibration. Outside of the 1920x1080 active pixels, there are several boundary pixels: 4 rows on top, 4 rows at the bottom, 8 columns on the right, and 8 columns on the left. The detailed pixel array arrangement and default read out direction is noted in the following two figures:

Figure 3: Pixel array structure

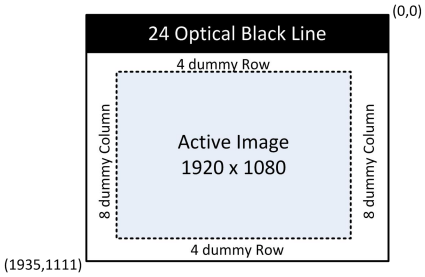
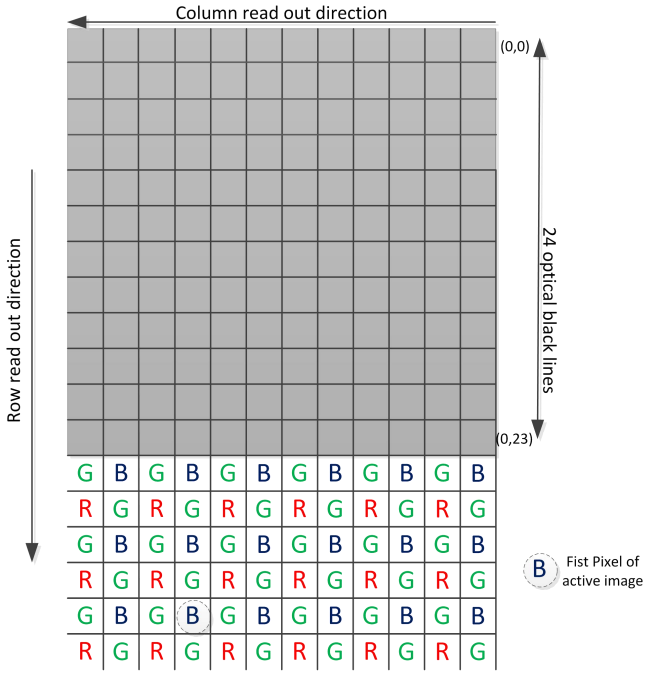


Figure 4: Pixel array detail with default read out direction.



Data Output Format:

The output images are divided into frames, which are further divided into lines. By default, the sensor produces 1088 lines (rows) of 1936 columns each. The VSYNC and HREF signals indicate the boundaries between frames and lines, respectively. PCLK can be used as a clock to latch the data. For each PCLK cycle, one 10-bit pixel data outputs on the D[9:0] pins (Figure 5). The pixel data is valid when HREF signal is asserted. The VSYNC signal indicates frame end and new frame start. JX-F22 default frame timing is illustrated as figure 6.

Figure 5: Row data output timing

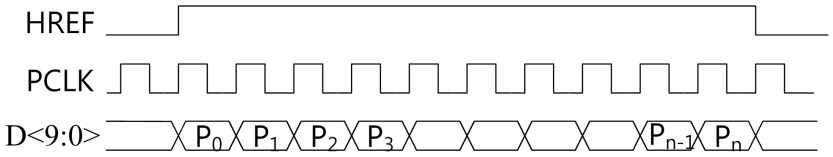
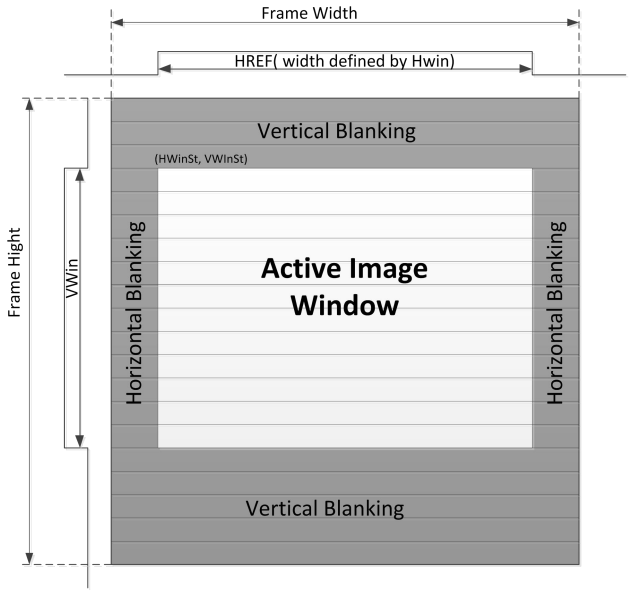


Figure 6: Default frame timing



As shown above in Figure 6, a line (row) period can be calculated as Trow = Frame_width * Thclk, and frame rate can be calculated as fps=1/(Frame_hight * Trow).

As default configuration, VSYNC, PCLK and Data are all valid at PCLK rising edge. For user convenience, JX-F22 provides register bits to control HREF, VSYNC and PCLK polarity. In addition, PCLK also have adjustable delay control.

For pixel Bayer pattern data output, several settings can have effect on pixel output sequences. These registers include HWIn_St, VWin_St, Haddr_St, Mirror, V_Flip. Please consult your SOI AE for further information.

HDR mode

JX-F22 support HDR mode, user can set 2 different exposure times and output 2 frame data (long and short exposure) in staggered output mode. Below is a diagram to illustrate frame output timing under this mode.

Figure 7: HDR frame timing in DVP output

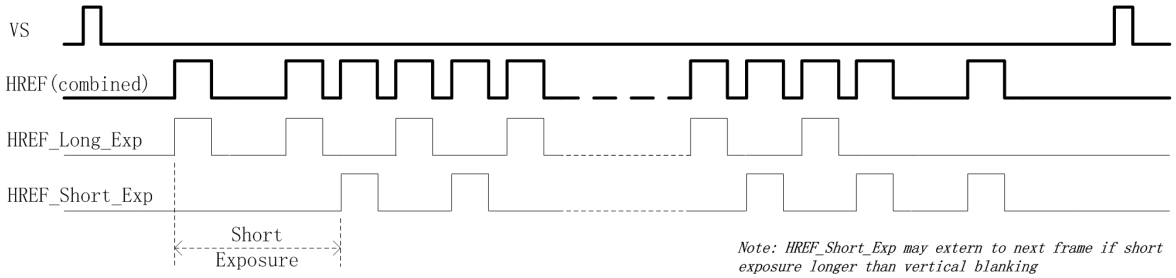
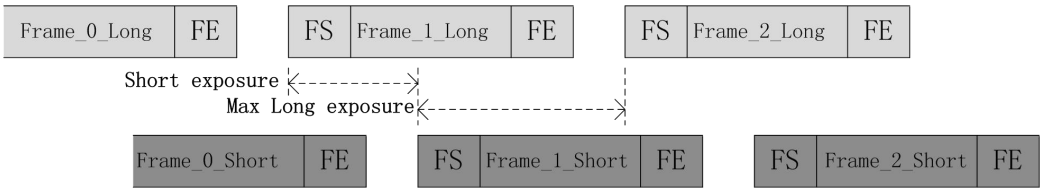


Figure 8: HDR frame timing in MIPI output



Notes: 1) Long_exposure + short_exposure <= Frame_high

Test Pattern Output:

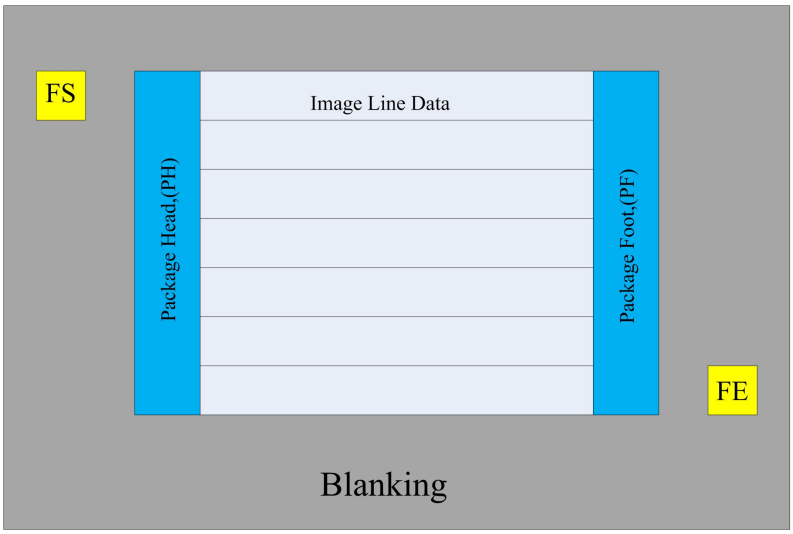
JX-F22 can output following test patterns as described below:

1) Walking “1” test pattern: for most sensor module connectivity test, JX-F22 provides walking “1” test pattern.

MIPI interface:

JX-F22 supports MIPI CSI-2 compliant interface. It has one pair of differential clock lane and two pairs of differential data lane. JX-F22 can output raw8 or raw10 mode through the MIPI interface. In raw8 mode, only 8 MSBs of 10-bit data will output and user needs to set MIPI clock speed at 8x parallel port pixel clock. In raw10 mode, user needs to set MIPI PHY clock as 10x parallel port pixel clock.

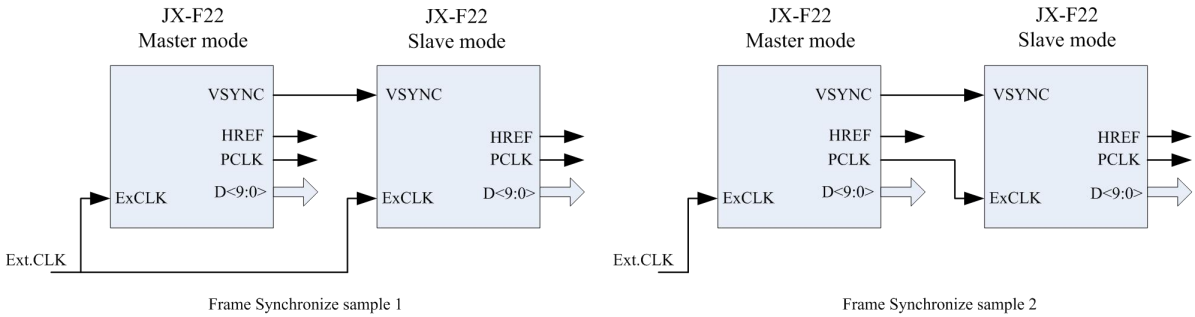
Figure 9: MIPI interface frame timing



Frame Synchronization:

JX-F22 provides the capability of frame synchronization. By setting VSYNC pin as input and enable frame-sync option, JX-F22 will work as slave device and synchronized with an external VSYNC. If all master devices and slave devices use same timing setting, all devices frame timing mismatch will be less than few pixel clocks. Figure 8 shows 2 ways to realize frame synchronization.

Figure 8: Frame Synchronization illustration



In the above 2 frame synchronize configurations, sample 2 will have more accurate synchronization than sample 1 because the slave device will have exactly same pixel clock as the master.

Serial Interface:

The serial interface is a two-wire bi-directional bus. Both wires (Serial Clock –SCL and Serial Data – SDA) are connected to DOVDD via a pull-up resistor, and when the bus is free both lines are high. The two-wire serial interface defines several different transmission stages as follows:

- A start bit
- The slave device 7-bit address
- An (No) acknowledge bit coming from slave
- An 8-bit or 16-bit message (address and/or data)
- A stop bit (or another 8bit or 16bit message in multiple Read/Write access)

Figure 10: I2C Timing chart

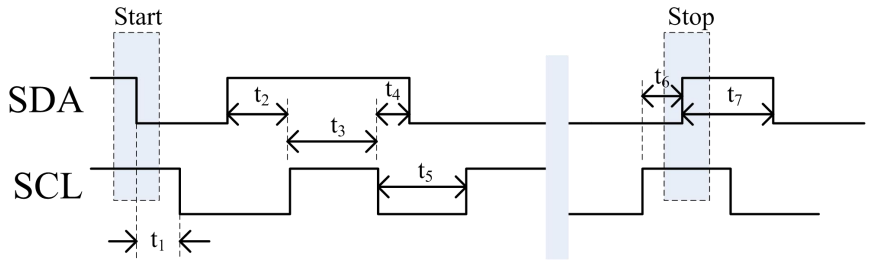
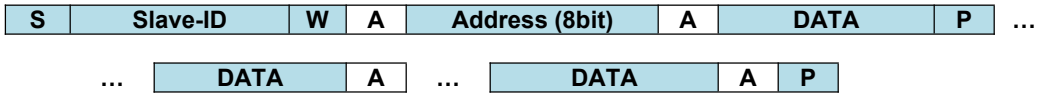


Table 2: I2C timing characteristic

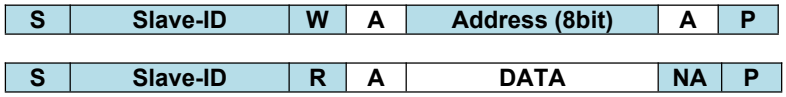
Symbol	Description	Min	Max	Units
	SCL clock frequency	0	400k	Hz
t1	Hold time for START condition	0.6	-	µs
t2	Data setup time	160	-	ns
t3	High period of the SCL clock	0.6	-	µs
t4	Data hold time	0	0.9	µs
t5	Low period of the SCL clock	1.3	-	µs
t6	Setup time for STOP condition	0.6	-	µs
t7	Bus free time between STOP and START condition	1.3	-	µs
	Rise time for both SDA and SCL signals		300	ns
	Fall time for both SDA and SCL signals		300	ns
Cb	Capacitive load for each bus line		400	pF

Single Write Mode operation

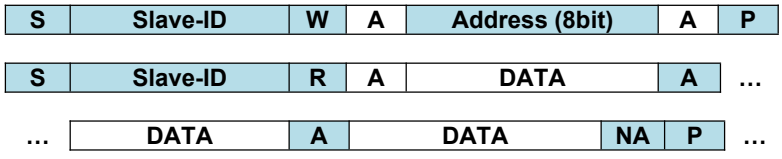
Multiple Write Mode (Register address is increased automatically) operation



Single Read Mode operation



Multiple Read Mode (Register address is increased automatically) operation



S: start conditions, A: acknowledge bit, NA: no acknowledge, DATA: 8 bit data, P: stop condition.
JX-F22 slave ID is programmable, default is 0x80/81 for write and read. User can program DVP data bit<1:0> for other configuration. The slave ID program table is list below:

D[1]	D[0]	Read/Write
X	X	81/80
X	Pull high	85/84
Pull high	X	89/88
Pull high	Pull high	8D/8C

Register Group Write Function:

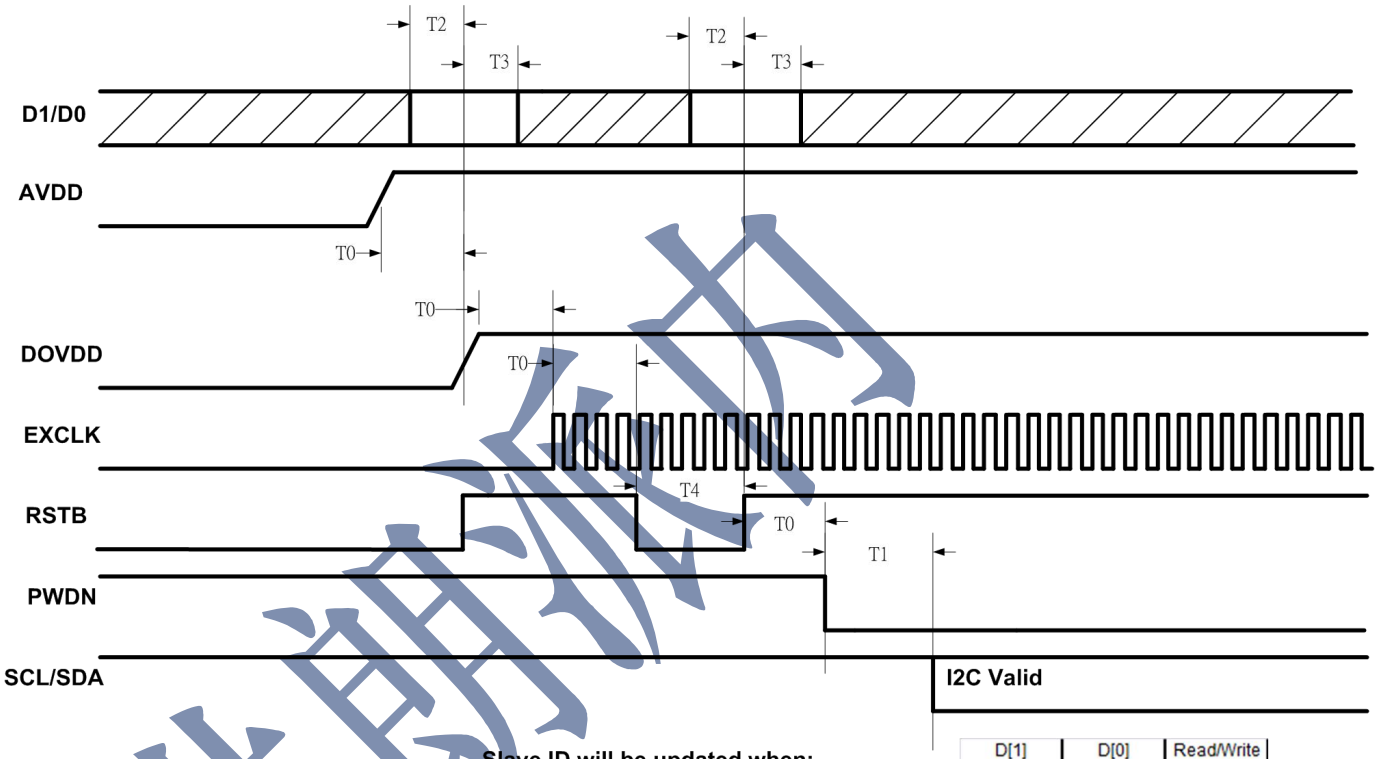
JX-F22 provides register group write function, user can pre-load address and data from register 0xC0 to 0xFF, then trigger this function by setting Reg0x1F[7], normally JX-F22 will auto write back group register content at next vertical blanking period and reset Reg0x1F[7] JX-F22 can update up to 32bytes of registers.

User can always monitor Reg0x1F[7] to make sure group write procedure is finished or not.

Power on/off sequence:

Figure 10 shows a reference power up sequence of JX-F22.

Figure 10. Power up sequence for JX-F22



Note:
1. T0 >= 0 us
2. T1 >= 8192 EXCLK cycles
3. T2>= 1ms
4. T3>= 1ms
5. T4>= 10ms

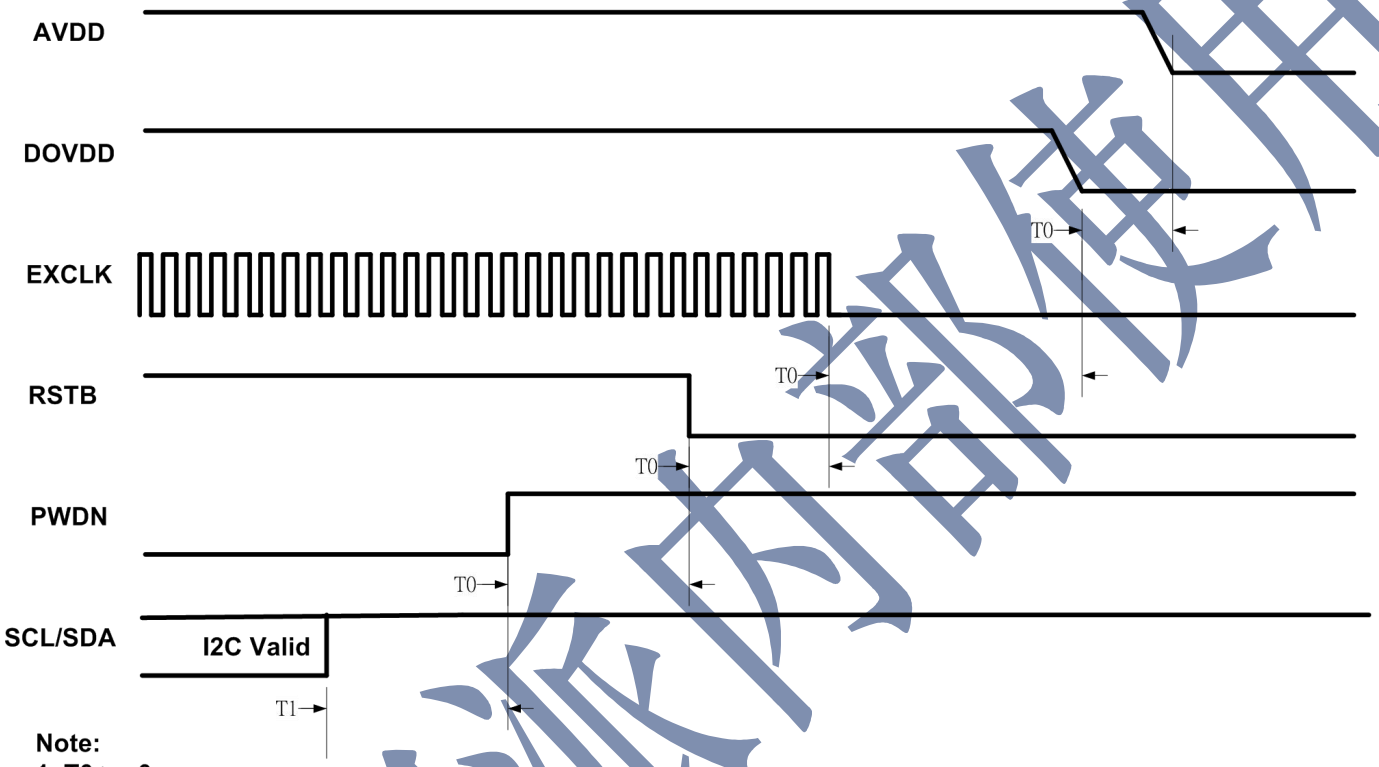
Slave ID will be updated when:
1. Power up (DVDD/DOVDD)
2. Hardware reset pin: Low -> High
3. Software reset : Reg0x12[7]=" 1"

Please stable D1/D0 when issue above commands.

D[1]	D[0]	Read/Write
X	X	81/80
X	Pull high	85/84
Pull high	X	89/88
Pull high	Pull high	8D/8C

Figure 11 shows a reference power down sequence of JX-F22.

Figure 11. Power down sequence for JX-F22



Electrical Characteristics:

Table 3. Absolute maximum ratings

Symbol	Descriptions	Absolute maximum rating	Units
V_{DD-IO}	I/O Digital Power	4.5	V
V_{DD-A}	Analog Power	4.5	V
V_{DD-D}	Core Digital Power	4.5	V
V_{I}	Input voltages	-0.3v to V_{DD-IO} + 1V	V
T_{AS}	Ambient Storage Temperature	-40 ~ 125	ºC

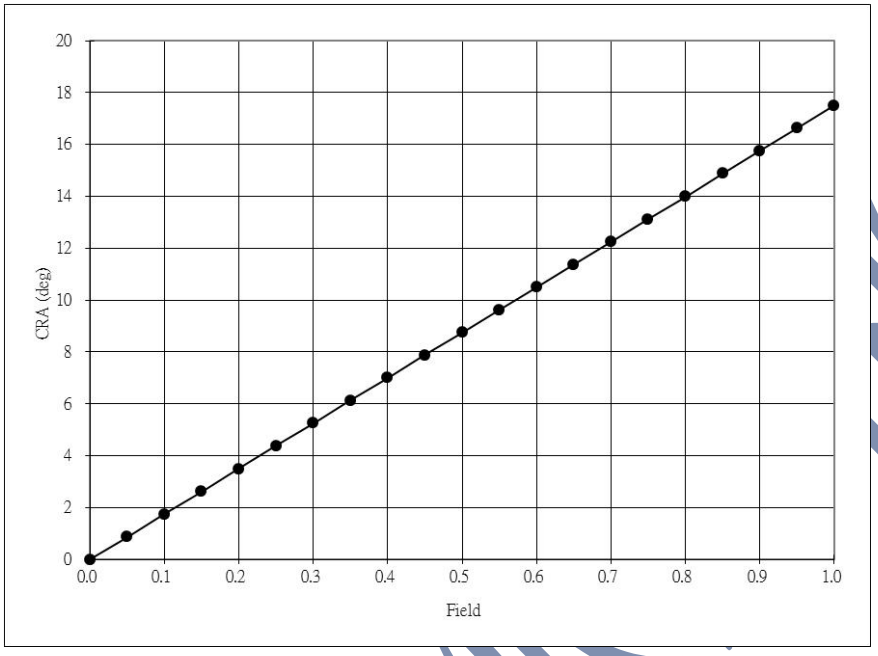
Table 4. DC Characteristics (0°C ≤ TA ≤ 85°C, Voltages referenced to GND)

Symbol	Descriptions	Max	Typ	Min	Units
supply					
V_{DD-IO}	Supply voltage (DOVDD)	3.45	1.8	1.7	V
V_{DD-A}	Supply voltage (AVDD)	3.0	2.8	2.6	V
V_{DD-D}	Supply voltage (DVDD) With embed regulator	1.65	1.5	1.35	V
Digital Inputs					
V_{IL}	Input voltage LOW	0.2* V_{DD-IO}	-	-	V
V_{IH}	Input voltage HIGH			0.7*V_{DD-IO}	V
C_{IN}	Input capacitor	10			pF
Digital Outputs (loading 20pF)					
V_{OH}	Output voltage HIGH			V_{DD-IO} – 0.2	V
V_{OL}	Output voltage LOW	0.2			V
Power consumption (Internal DVDD, EVDD short to DVDD;DVP output mode; AVDD=2.8V, DOVDD=2.8V)					
I_{DD-IO}	Supply current (V_{DD-IO}=2.8V@30fps FHD without digital I/O loading)		35		mA
I_{DD-A}	Supply current (V_{DD-A}=2.8V@30fps FHD)		55		mA
Power consumption (Internal DVDD, EVDD short to DVDD;MIPI output mode; AVDD=2.8V, DOVDD=2.8V)					
I_{DD-IO}	Supply current (V_{DD-IO}=2.8V@30fps MIPI2L FHD)		33		mA
I_{DD-A}	Supply current (V_{DD-A}=2.8V@30fps MIPI2L FHD)		55		mA
Power consumption (Internal DVDD, EVDD short to DVDD;MIPI output mode; AVDD=2.8V, DOVDD=2.8V)					
I_{DD-IO}	Supply current (V_{DD-IO}=2.8V@60fps MIPI2L FHD)		43		mA
I_{DD-A}	Supply current (V_{DD-A}=2.8V@60fps MIPI2L FHD)		55		mA
Ipwrdn	HW PWDN Pin active		30		uA

CRA Specifications:

JX-F22 is designed with a linear chief ray angle curve as shown in Figure 11. The shifting of the color filter and microlenses on the sensor is critical to accommodate the ever shorter height of the camera module as well as minimizing shading at the corner of the image.

Figure 11. CRA Curve for JX-F22

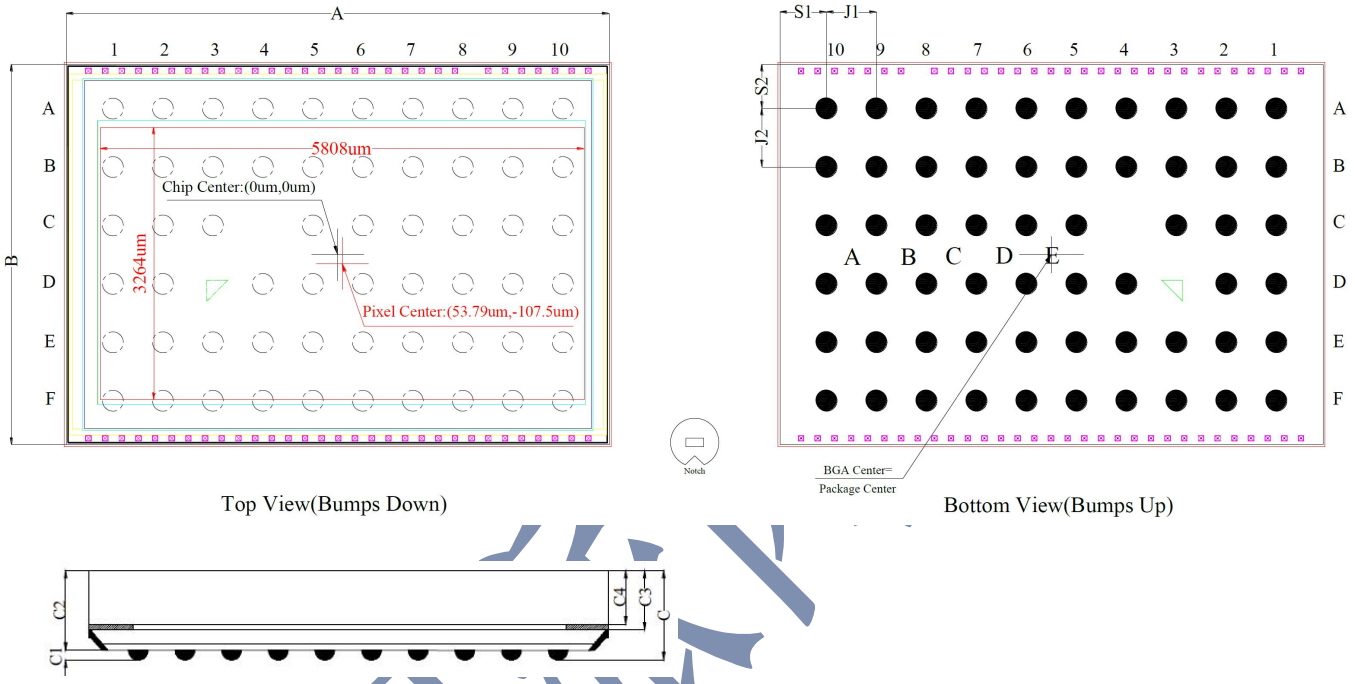


Field	CRA
0.00	0.000
0.05	0.875
0.10	1.750
0.15	2.625
0.20	3.500
0.25	4.375
0.30	5.250
0.35	6.125
0.40	7.000
0.45	7.875
0.50	8.750
0.55	9.625
0.60	10.500
0.65	11.375
0.70	12.250
0.75	13.125
0.80	14.000
0.85	14.875
0.90	15.750
0.95	16.625
1.00	17.500

Mechanical Specifications:

JX-F22 is available in CSP packaged component. Figure 12 shows top view and bottom view of the CSP component. Table 5 shows the nominal dimensions for the packaged chip.

Figure 12. CSP Top, Bottom, Side View



Top View(Bumps Down)

Bottom View(Bumps Up)

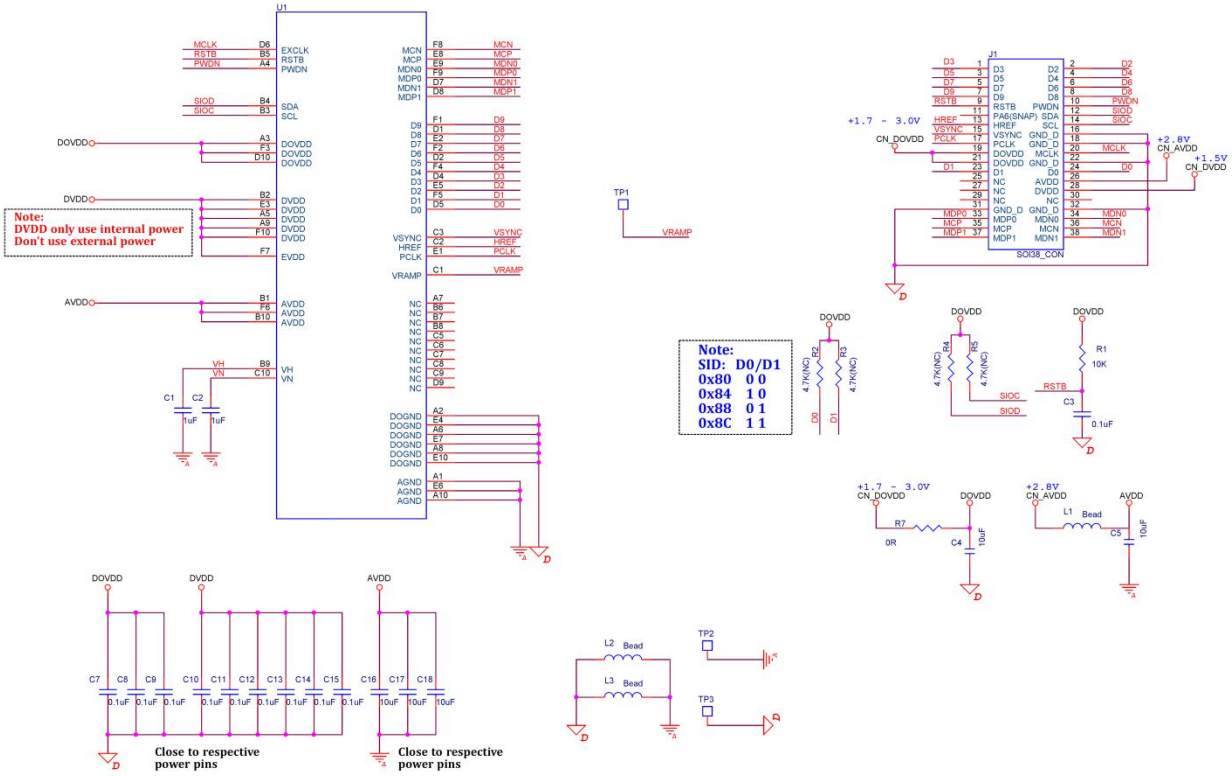
Table 5. Dimensions for JX-F22 CSP package (in mm)

	Symbo	Nominal	Min	Max	Nominal	Min	Max
		Millimeters			Inches		
Package Body Dimension X	A	6.517	6.492	6.542	0.25657	0.25559	0.25756
Package Body Dimension Y	B	4.554	4.529	4.579	0.17929	0.17831	0.18028
Package Height	C	0.770	0.710	0.830	0.03031	0.02795	0.03268
Ball Height	C1	0.130	0.100	0.160	0.00512	0.00394	0.00630
Package Body Thickness	C2	0.640	0.605	0.675	0.02520	0.02382	0.02657
Thickness from top glass surface to wafer	C3	0.445	0.425	0.465	0.01752	0.01673	0.01831
Glass Thickness	C4	0.400	0.385	0.415	0.01575	0.01516	0.01634
Ball Diameter	D	0.250	0.220	0.280	0.00984	0.00866	0.01102
Total Ball Count	N	58(10NC)					
Pins pitch X axis	J1	0.6					
Pins pitch Y axis	J2	0.7					
Edge to Pin Center Distance along X	S1	0.5585	0.5285	0.5885	0.02199	0.02081	0.02317
Edge to Pin Center Distance along Y	S2	0.5270	0.4970	0.5570	0.02075	0.01957	0.02193

CSP Module Schematic (Reference):

Figure 13 shows a reference schematic for CSP module.

Figure 13. Reference schematic for CSP module



Register Descriptions:

Write Slave ID:0x80/84/88/8C Read Slave ID:0x81/85/89/8D

Address (Hex)	Register Name	Default (Hex)	R/W	Description
00	PGA	00	RW	Programmable gain, valid 00 to 4F,PGA[7] reserved ; Total gain = 2^PGA[6:4]*(1+PGA[3:0]/16)
01	EXP	FF	RW	Exposure line LSBs, EXP[7:0]
02	EXP	00	RW	Exposure line MSBs, EXP[15:8].;AEC[15:8] Exposure time is defined by EXP[15:0] at line period base. T_{EXP}=EXP[15:0]*T_{Line}
03 – 04				RSVD
05	EXP_S	00	RW	Short exposure lines in HDR mode, EXP_S[7:0]: each bit equals to 2 lines, short_exposure_time = (EXP_S[7:0] *2 + 1) * T_{Line}
06-08				Reserved
09	VER	02	R	Ver[7:0] ;;Version ID.
0A	PIDH	0F	R	PIDH[7:0]:Product ID MSBs. “0x0F”
0B	PIDL	22	R	PIDL[7:0]: Product ID LSBs. “0x22”
0C	DVP1	44	RW	DVP control 1. DVP1[7]: RSVD DVP1[6]: Sensor sun spot elimination control, “1”: disable sun spot elimination, “0”: enable sun spot elimination. DVP1[5:2]: RSVD. DVP1[1:0]: DVP test mode output option. “00”: DVP output normal image data. “01”: DVP[9:0] = Output 10-bit walk “1” test pattern.; others: RSVD
0D	DVP2	50	RW	DVP control 2. DVP2[7:4]: RSVD DVP2[3:2]: PAD drive capability. “00”: min, “11”: max. DVP2[1:0]: Digital gain. “00”:1x, “01” and “10”: 2x, “11”:4x
0E	PLL1	10	RW	PLL control 1. PLL1[7]: PLL bypass selection. “1”: PLLclk = Input clock/PLL_Pre_Ratio. “0”: see PLL2[1:0]. PLL1[6:4]: reserved PLL1[3]: reserved PLL1[2]: external clock input pad circuit option, “0”: internal no Schmitt trigger; “1”: internal has Schmitt trigger. PLL1[1:0]: PLL pre-divider ratio. PLL_Pre_Ratio = 1 + PLL[1:0]
0F	PLL2	04	RW	PLL control 2. PLL2[7:4]: RSVD PLL2[3]: R_MIPI; “1” : MIPIPCLK=1/2VCO; “0” MIPIPCLK=VCO; PLL2[2]: RSVD PLL2[1:0]: PLL clock divider. PLLclk = VCO/(1+PLL2[1:0])
10	PLL3	26	RW	PLL control 3. PLL VCO multiplier. VCO = Input clock*PLL3[7:0]/PLL_Pre_Ratio
11	CLK	80	RW	Reserved

12	SYS	00	RW	System status set up SYS[7]: Soft reset initialize, "1": initial system reset, it will reset whole sensor to factory default status, and this bit will clear after reset. Default : "0": normal mode SYS[6]: Sleep mode on/off selection, "1": sensor into sleep mode. No data output and all internal operation stops. External controller can stop sensor clock, while I2C interface still can work. Default : "0" : normal mode SYS[5]: mirror image on/off, "1": mirrored image output, "0": normal image output SYS[4]: flip image on/off, "1": flipped image output, "0": normal image output. SYS[3]: HDR mode on/off selection. "0": normal mode, "1": HDR mode. SYS[2]: horizontal skip or binning mode select default : "0" : binning mode SYS[1]: vertical skip or full mode selection. Default : "0" : full mode SYS[0]: RSVD
13	LCCtrl1	81	RW	Luminance control register 1. LCCtrl1[7:6]: Gain ceiling at auto mode. "00": maximum 4X analog gain. "01": 8X, "10": 16X, "11": 32X LCCtrl1[5:3]: Auto Frame rate ceiling control. "000": disable auto frame rate adjust. "001": max frame rate down 1/2, "011": max frame rate down 1/4; "111": max frame rate down 1/8; LCCtrl1[2]: Banding filter on/off selection. "1": on. "0": off LCCtrl1[1]: RSVD. LCCtrl1[0]: automatic luminance control on/off selection, "0": auto, "1": manual
14	LCCtrl2	80	RW	Luminance Control register 2. LCCtrl2[7:0]: Image luminance expect target.
15	LCCtrl3	44	RW	Luminance Control register 3 LCCtrl3[7:4]: auto Luminance control adjustment trigger range. LCCtrl3[3:0]: auto luminance control stable range
16	LCCtrl4	C0	RW	Luminance control register 4 LCCtrl[7:0]: Luminance control large step adjustment high threshold
17	LCCtrl5	40	RW	Luminance control register 5 LCCtrl[7:0]: Luminance control large step adjustment low threshold
18	LCCtrl6	99	RW	Luminance control register 6 LCCtrl6[7:0]: Banding filter minimum exposure line LSBs;Band[7:0]
19	LCCtrl17	28-mipi/44-DVP	RW	Luminance control register 7 LCCtrl7[7:6]: PCLK delay option. LCCtrl7[5]: AGC delay 1 frame valid option. "0": manual gain will apply at next VSYNC;"1": manual gain will delay 1 frame to apply. LCCtrl7[4]:RSVD LCCtrl7[3:2]: System clock selection, "00": use 1/4 clock as hclk, and 1/2 clock as ADC clock, known as half clock option. "01": use 1/2 clock as hclk and 1/2 clock as ADC clock. "1x": use full PLL clock as hclk and ADC clock. So no 2x clock for DVP output. Can use in MIPI mode. LLCCtrl7[1:0]: Banding filter minimum exposure line MSBs. Band[9:8]
1A	LCCtrl8	80	RW	Luminance control register 8 LCCtrl8[7:0]: RSVD
1B	LCCtrl9	49/4F	RW	Luminance control register 9 LCCtrl9[7:3]: RSVD LCCtrl9[2:1]: pre-precharge line selection, "00": 1 line, "01:2lines, "10": 3 lines, "11": 4 lines. LCCtrl9[0]: pre-precharge option on/off selection, "0": off, "1": on.
1C	LCCtrl10	00	R	Luminance control register 10 LCCtrl10[7:0]: image luminance average value.
1D	DVP3	00	RW	DVP control 3 DVP3[7:0]: GPIO direction control for data output port D[7:0]. "1": enable output. "0": tri-state output.
1E	DVP4	1C	RW	DVP control 4

				DVP4[7]: PCLK polarity control. "0": data output at rising edge of PCLK, "1":data output at falling edge of PCLK DVP4[6]: HREF polarity control. "0": positive, "1":negative DVP4[5]: VSYNC polarity control. . "0": positive, "1":negative DVP4[4:0]: GPIO direction control for output port: PCLK, HREF, VSYNC and D[9:8] . "1": enable output. "0": tri-state output.
1F	Glat	00	RW	Group latch control Glat[7]: Group write trigger. "1": system will write reg0xC0 to 0xFF content to proper register. This bit will clear after group write. "0": inactive group write function.. Glat[6]: Group latch trigger time option, "0": trigger at vertical blanking period. "1": group latch trigger immediately. Glat[5:1]: reserved Glat[0]: Scan_Trig: When write 1 ,Trig scan once then reset to 0
20	FrameW	B0	RW	Sensor frame time width LSBs; FrameW[7:0]
21	FrameW	04	RW	Sensor frame time width MSBs; FrameW[15:8] FrameW[15:0]: sensor frame width
22	FrameH	56	RW	Sensor frame time high LSBs ;FrameH[7:0]
23	FrameH	04	RW	Sensor frame time high MSBs. FrameH[15:8] FrameH[15:0]: sensor frame high. Sensor frame rate is defined as Fpclk / (FrameW*FrameH). Fpclk: frequency of pixel clock.
24	Hwin	C0	RW	Image horizontal output window width LSBs: Hwin[7:0]
25	Vwin	38	RW	Image vertical output window high LSBs: Vwin[7:0]
26	HVWin	43	RW	Image output window horizontal and vertical MSBs. { Vwin[11:8],Hwin[11:8]}
27	HwinSt	D0	RW	Image horizontal output window start position LSBs. HwinSt[7:0]
28	VwinSt	14	RW	Image vertical output window start position LSBs. VwinSt[7:0]
29	HVWinSt	01	RW	Image output window horizontal and vertical start position MSBs. {VwinSt[11:8],HwinSt[11:8]}
2A – 2B				RSVD
2A	Cshift1	C0	RW	Column shift control 1 Cshift1[7:6]: Column SRAM data shift start position LSBs. Cshift[7:6]
2B	Cshift2	21	RW	Column shift control 2 Cshift2[7:2]: RSVD Cshift2[1:0]: Column SRAM data shift start position MSBs, Cshift[9:8]
2C	SenHASt	00	RW	Sensor physical column shift start address LSBs, SenHASt[7:0]; each bit represent **2** pixels
2D	SenVSt	00	RW	Sensor physical vertical start address, LSBs. SenVSt[7:0]; each bit represent 4 lines
2E	SenVEnd	14	RW	Sensor physical vertical end address, LSBs. SenVEnd[7:0] ;each bit represent 4 lines
2F	SenVadd	44	RW	Sensor vertical address settings. SenVadd[7:4]: RSVD SenVadd[3:2]: SenVEnd[9:8] SenVadd[1:0]: SenVSt[9:8]
30 -38			RW	RSVD
39	SenT10	80	RW	Sensor timing control 10 SenT10[7:5]:RSVD SenT10[4]: delay HREF output by one PCLK. Can be used as output color sequence change.

				SenT10[3:0]: RSVD.
3A-42			RW	RSVD
41	SenT12	C8	RW	Sensor timing control 12 SenT12[7:0]: Array SRAM shift out pixel number LSBs, in 2 pixels step.
42	SenT13	O3	RW	Sensor timing control 13 SenT13[7:2]: RSVD SenT13[1:0]: Array SRAM shift out pixel number MSBs.
43	VS_POS1	00	RW	VSYNC position LSBs: VS_POS[7:0];
44	VS_POS2	40	RW	VS_POS2[7:4]: VSYNC width selection. VS_POS2[3:0]: VS_POS[11:8];
45 – 46		C9	RW	RSVD
47	LBLC	54/12	RW	Line BLC control LBLC[7]: BLC limitation control, “0”: BLC max value is 0x200, “1”: BLC max value is 0x400 LBLC[6:0]: reserved
48	BLCOpt1	00	RW	BLC control option 1 BLCopt1[7]: “0”: normal, “1”:BLC adjust only when the difference bigger than a threshold BLCopt1[6:4]: RSVD BLCopt1[3:0]: BLC adjustment threshold.
49	BLC_TGT	04	RW	Black level calibration target level. BLC_TGT[7]: sign bit.“0” positive; “1” negative BLC_TGT[6:0]: target level.
4A	BLCCtrl	03	RW	BLC control BLCCtrl[7]: BLC_B bit 10 BLCCtrl[6]: BLC_Gb bit 10 BLCCtrl[5]: BLC_Gr bit 10 BLCCtrl[4]: BLC_R bit 10 BLCCtrl[3:2]: reserved BLCCtrl[1]: BLC action option. “0”: Sensor do BLC only when triggered. “1”: always do BLC. BLCCtrl[0]: auto BLC function on/off selection. “0”: sensor stop calculate black value. “1”: sensor calculates black value automatically.
4B	BLC_B	00	RW	B channel black value LSBs. BLC_B[7:0]
4C	BLC_Gb	00	RW	Gb channel black value LSBs. BLC_Gb[7:0]
4D	BLC_Gr	00	RW	Gr channel black value LSBs. BLC_Gr[7:0]
4E	BLC_R	00	RW	R channel black value LSBs. BLC_R[7:0]
4F	BLC_H	00	RW	Black value MSBs. {BLC_R[9:8],BLC_Gr[9:8],BLC_Gb[9:8],BLC_B[9:8]}
50	SBLCCtrl	03	RW	Short exposure BLC control in HDR mode SBLCCtrl[7]: SBLC_B bit 10 SBLCCtrl[6]: SBLC_Gb bit 10 SBLCCtrl[5]: SBLC_Gr bit 10 SBLCCtrl[4]: SBLC_R bit 10 SBLCCtrl[3:1]: reserved SBLCCtrl[0]: BLC target option when digital gain apply, “1”: BLC target level not effect when apply digital gain, “0”: BLC target level will change when apply digital gain.
51	SBLC_B	00	RW	Short exposure B channel black value LSBs. SBLC_B[7:0]
52	SBLC_Gb	00	RW	Short exposure Gb channel black value LSBs. SBLC_Gb[7:0]

53	SBLC_Gr	00	RW	Short exposure Gr channel black value LSBs. SBLC_Gr[7:0]
54	SBLC_R	00	RW	Short exposure R channel black value LSBs. SBLC_R[7:0]
55	SBLC_H	00	RW	Short exposure black value MSBs. {SBLC_R[9:8],SBLC_Gr[9:8],SBLC_Gb[9:8],SBLC_B[9:8]}
56-58				RSVD
59	Vsun2	80	RW	Second stage black sun control Vsun2[7:5]: reserved. Vsun2[4]: Second stage black sun switch on/off enable, “0”: always off. “1”: Black sun will switch to second stage when analog gain greater than 2x. Vsun2[3:0]: Second stage black sun reference control. Strength : (Strong) 1,0,F,E,D,C,B,A,9,8,7,6,5,4,3,2. (Weak)
5A-5E			RW	RSVD
5F	DAC_Pll0	01	RW	DAC PLL control 0 DACPLL0[7]: DAC PLL bypass on/off selection ; 1: Bypass on, 0: By pass off DACPLL0[6:4]: RSVD DACPLL0[3:2]: DAC PLL post divider bypass on/off selection ; 1: Bypass on, 0: By pass off DACPLL0[1:0]: DAC PLL pre- divider DAC_CLK=input clock/(DAC PLL pre-divider + 1) * DAC PLL VCO multiplier / (DAC PLL post divider + 1)
60	DAC_Pll1	1C	RW	DAC PLL control 1 DACPLL1[7:6]: RSVD DACPLL1[5:0]:DAC PLL VCO multiplier
51 – 65			RW	RSVD
66	PWC0	08	RW	PWC5[7:6]: RSVD PWC5[5:4]: D-phy Lp high voltage reference voltage control ; 00- min, 11- max. PWC5[3:0]: RSVD;
67-69	RSVD		RW	RSVD
6A	PWC4	3A	RW	Power control 4 PWC4[7:4]: reserved PWC4[3:0]: first stage black sun control. Strength : (Strong) 1,0,F,E,D,C,B,A,9,8,7,6,5,4,3,2. (Weak)
6B	DPHY1	00	RW	Mipi PHY control 1 DPHY1[7:6]: MPCKSkew[1:0] DPHY1[5:4]:HSCKSkew[1:0] DPHY1[3:2]CKSkew[1:0] Clock Lane Skew Control : 00:Min, .. 11:max. DPHY1[1:0]:D0Skew[1:0]
6C	DPHY2	00	RW	DPHY2[7]: Mipi interface power down. “0”: enable ;”1” normal mode DPHY2[6:5]:RSVD DPHY2[4]: Second data lane disable on/off selection “0”: enable “; 1” :disable; DPHY2[3:2]Pg_Vcm[1:0] D-phy Hs Tx output voltage control 01:min, 00,11,10 : max DPHY2[1:0]:D1Skew[1:0]
6D	DPHY3	02	RW	DPHY3[7:3]:RSVD DPHY3[2]: Mipi data lane 1 disable on/off selection;; 1” :disable; “0”: enable DPHY3[1:0]: RSVD
6E -6F	DPHY4	0C	RW	RSVD
70	Mipi1	49	RW	Mipi timing control 1 Mipi1[7:5]: Tlpx Mipi1[4:2]: Tck-pre Mipi1[1]: Mipi 8/10 bit mode switch, “0”: 10-bit, “1”: 8-bit mode

				Mipi1[0]: reserved
71	Mipi2	8A	RW	Mipi timing control 2 Mipi2[7:5]: Ths-zero Mipi2[4:0]: Tck-zero
72	Mipi3	68	RW	Mipi timing control 3 Mipi3[7:5]: Ths-prepare Mipi3[4:0]: Tck-post
73	Mipi4	33	RW	Mipi timing control 4 Mipi4[7]: Mipi pixel clock option Mipi4[6:4]: Ths-trail Mipi4[3:0]: Tck-trail
74	Mipi5	53	RW	Mipi timing control 5 Mipi5[7:4]: reserved Mipi5[3]: Mipi virtual channel ID revise Mipi5[2]: Mipi byte clock revise Mipi5[1]: Mipi continues mode or strobe mode selection "1" free run; "0" Normal ; Mipi5[0]: Mipi interface sleep on/off Mipi should wait a complete frame than enter sleep mode. "1" Sleep mode enable; "0" Normal ;
75	Mipi6	2B	RW	Mipi data type ID;
76	Mipi7	60	RW	Mipi word count LSBs
77	Mipi8	09	RW	Mipi word count MSBs
78	Mipi9	14	RW	Mipi timing control 9 Mipi9[7]: CK-pre timing option 0: Auto; 1 Manual Mipi9[6:0]: Mipi TX start point adjust related to DVP HREF and internal FIFO
79-BF				RSVD
C0	Group0	0A	RW	Group write 1st data address
C1	Group1	0A	RW	Group write 1st data value.
C2	Group2	0A	RW	Group write 2nd data address
C3	Group3	0A	RW	Group write 2nd data value.
…	…	…	…	…
FE	Group62	0A	RW	Group write 32nd data address
FF	Group63	0A	RW	Group write 32nd data value.

Document Revision Control

Version Number #	Date Released	Comments
R0.0	2/8/2016	Initial release of JX-F22 datasheet
R0.1	5/4/2016	modify CSP package mechanical info Modify max gain : 0x4F Modify pixel array structure- optical black 24 lines, Active pixel sensor array 1932x1088 Delete binning mode.
R0.2	7/8/2016	Modify for AB version
R0.3	8/25/2016	Modify stable image junction temperature
R0.4	9/20/2016	Modify Reg0x11 : Reserved Supply Voltage : DVDD : With embedded 1.5V regulator
R1.0	10/10/2016	Key Spec info. Supply voltage (DOVDD): 1.7 ~ 3.45V
R1.1	11/02/2016	Modify Component Order Information