T10

Smart Video Processor

Data Sheet

Release Date: Jun. 14, 2016

北京君正集成电路股份有限公司
Ingenic Semiconductor Co.,Ltd.

T10 Smart Video Processor

Data Sheet

Disclaimer

Ingenic Semiconductor Co., Ltd.

Ingenic Headquarters, Zhongguancun Software Park,
Dongbeiwang West Road, Haidian District, Beijing, China,
Tel: 86-10-56345000
Fax: 86-10-56345001
Http: //www.ingenic.com

CONTENTS

1 Overview

T10 is a smart video application processor targeting for video devices like mobile camera, security survey, video talking, video analysis and so on. This SOC introduces a kind of innovative architecture to fulfill both high performance computing and high quality image and video encoding requirements addressed by video devices. T10 provides high-speed CPU computing power, excellent image signal process, fluent 1280x1024 resolution video recording.

The CPU (Central Processing Unit) core, equipped with 32kB instruction and 32kB data level 1 cache, and 128kB level 2 cache, operating at 1GHz, and full feature MMU function performs OS related tasks. At the heart of the CPU core is XBurst® processor engine. XBurst® is an industry leading microprocessor core which delivers superior high performance and best-in-class low power consumption. A hardware floating-point unit which compatible with IEEE754 is also included. The MXU2.0(SIMD128) instruction set has been implemented by XBurst® engine, and is one part of the CPU.

With the powerful CPU, T10 supports various computer vision applications, such as face detection, human detection, gesture recognition, and etc. Also people can develop new computer vision application using the MXU2.0 to accelerate it.

The VPU (Video Processing Unit) core is powered with another XBurst® processor engine. Together with the on chip video accelerating engine and post processing unit, T10 delivers high video performance. The maximum resolution of 1280x1024 in the format of H.264 are supported in encoding. And 720P@30fps, with VGA@30fps are supported at the same time with maximum performance.

The ISP (Image signal processor) core supports excellent image process with the image coming from raw sensors. It supports DVP interface. With the functions, such as 3A, 2D denoise, 3D denoise, WDR, HDR, lens shading, it can supply maximum resolution 1280x1024 resolution image for view or encoding to store or transfer.

For more quickly and easily to use T10, one 512Mbit DDR2 is integrated.

On-chip modules such as audio CODEC, multi-channel SAR-ADC controller and camera interface offer designers a economical suite of peripherals for video application. WLAN, Bluetooth and expansion options are supported through high-speed SPI and MMC/SD/SDIO host controllers. Other peripherals such as USB OTG, UART and SPI as well as general system resources provide enough computing and connectivity capability for many applications..

1.1 Block Diagram

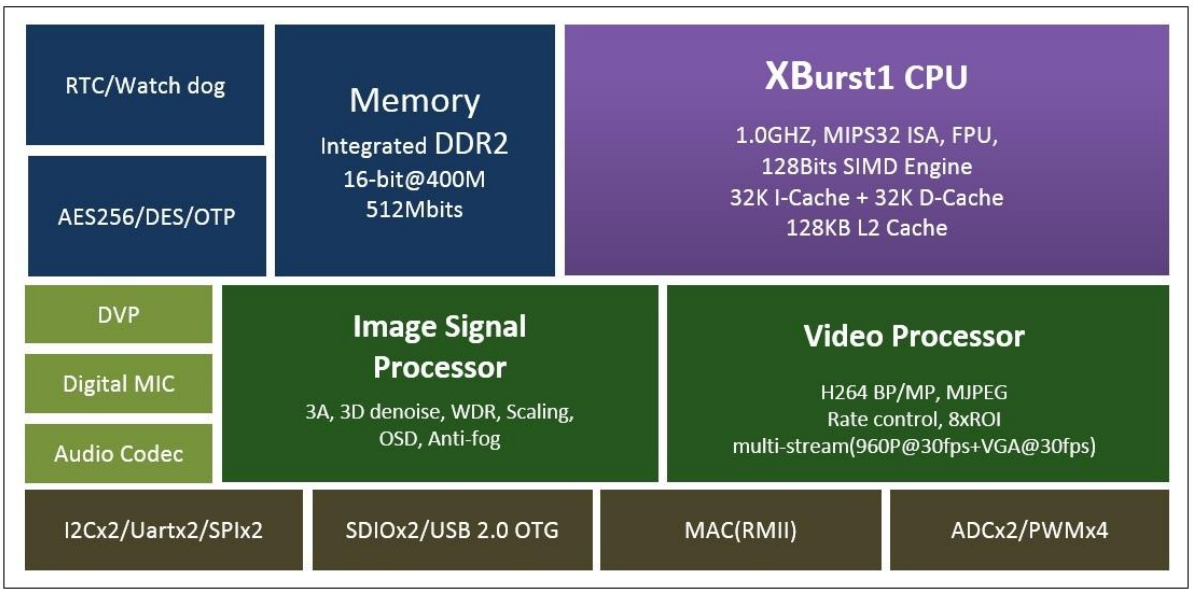


Figure 1-1 T10 Diagram

1.2 Features

1.2.1 CPU

- XBurst®-1 core
  - XBurst® RISC instruction set
  - XBurst® SIMD128 instruction set
  - XBurst® FPU instruction set supporting both single and double floating point format which are IEEE754 compatible
  - XBurst® 9-stage pipeline micro-architecture, the operating frequency is 1G.
  - MMU
- 32-entry joint-TLB
- 8 entry Instruction TLB
- 8 entry data TLB
  - L1 Cache
- 32kB instruction cache
- 32kB data cache
  - Hardware debug support
  - 16kB tight coupled memory
- L2 Cache
  - 128kB unify cache

1.2.2 VPU

Include Video Codec and JEPG Codec,

- H.264 encoding up to 960P(1280x960)@40fps
- JPEG compressing up to 100Mega-pixels per second (baseline)

1.2.3 ISP

- Max input resolution 1280x1024 image
- 100 MHZ maximum pixel rate
- Input image up to 12bit RAW or Up to 24bit RGB. Both RGB and YCbCr are supported from SoC sensors.
- Up to 2 output channel. Image crop and downscaler.
- 2-D and 3-D noise reduction filter lead to high levels of noise reduction with minimal effect on edges and textures.
- Single frame and multi-frame WDR/HDR provide high dynamic range in both still and video capture modes.
- Advanced demosaic, colour processing, lens shading, defog, glare, static/dynamic defect pixel and other modules provide high image quality.
- 3A supported.
- Flash timer

1.2.4 Image post processor(IPU)

- Input format
  - Separate frame: YUV /YCbCr (4:2:0, 4:2:2, 4:4:4, 4:1:1, NV12/21), RGB888
  - Packaged data: YUV422, RGB888, RGB565, RGB555, YUV444
  - Separate frame in block format: YUV/YCbCr 420
- Output data format
  - RGB (565, 555, 888, AAA)
  - Packaged data YUV422
  - NV12/21
- Color convention coefficient: configurable (CSC enable)
- Minimum input image size (pixel): 4x4
- Maximum input image size (pixel): 8096x8096
- Maximum output image size (pixel)
  - Width: up to 4095
  - Height: up to 4095
- OSD function:
  - Support 5 layers OSD
  - Support all output data format listed above.
  - Support 12 port-duff OSD modes

1.2.5 Video input

- Video input
  - DVP Input data format: YUV422, RGB565, RGB555, RAW8, RAW10, RAW12.

1.2.6 Audio

- Integrated Audio codec.
  - 24 bits DAC with 93dB SNR
  - 24 bits ADC with 92dB SNR
  - Support signal-ended and differential microphone input and line input
  - Automatic Level Control (ALC) for smooth audio recording
  - Pure logic process: no need for mixed signal layers and less mask cost
  - Programmable input and output analog gains
  - Digital interpolation and decimation filter integrated
  - Sampling rate 8K/12K/16K/24K/32/44.1K/48K/96K

1.2.7 Memory Interface

- Integrated 512Mbits DDR2
- Static memory interface
  - Support 6 external chip selection CS6~1#. Each bank can be configured separately
  - The size and base address of static memory banks are programmable
  - Direct interface to 8-bit bus width external memory interface devices or external static memory to each bank. Read/Write strobe setup time and hold time periods can be programmed and inserted in an access cycle to enable connection to low-speed memory
  - Wait insertion by WAIT pin
  - Automatic wait cycle insertion to prevent data bus collisions in case of consecutive memory accesses to different banks, or a read access followed by a write access to the same bank

1.2.8 System Functions

- Clock generation and power management
  - On-chip 12/24/48MHZ oscillator circuit
  - External 32.768KHZ input
  - One four-chip phase-locked loops (PLL) with programmable multiplier
  - CCLK, HHCLK, H2CLK, PCLK, H0CLK, DDR_CLK, VPU_CLK frequency can be changed separately for software by setting registers
  - SSI clock supports 50M clock
  - MSC clock supports 100M clock
  - Functional-unit clock gating
  - Shut down power supply for P0, VPU, GPU, GPS, P1
- Timer and counter unit with PWM output and/or input edge counter

  - Provide eight separate channels, six of them have input signal transition edge counter
  - 16-bit A counter and 16-bit B counter with auto-reload function every channel
  - Support interrupt generation when the A counter underflows
  - Three clock sources: RTCLK (real time clock), EXCLK (external clock input), PCLK (APB Bus clock) selected with 1, 4, 16, 64, 256 and 1024 clock dividing selected
  - Every channel has PWM output
- OS timer
  - 64-bit counter and 32-bit compare register
  - Support interrupt generation when the counter matches the compare register
  - Two clock sources: RTCLK (real time clock), HCLK (system bus clock) selected with 1, 4, 16, 64, 256 and 1024 clock dividing selected
- Interrupt controller
  - Total 64 interrupt sources
  - Each interrupt source can be independently enabled
  - Priority mechanism to indicate highest priority interrupt
  - All the registers are accessed by CPU
  - Unmasked interrupts can wake up the chip in sleep mode
  - Another set of source, mask and pending registers to serve for PDMA
- Watchdog timer
  - Generates WDT reset
  - A 16-bit Data register and a 16-bit counter
  - Counter clock uses the input clock selected by software
- PCLK, EXTAL and RTCCLK can be used as the clock for counter
- The division ratio of the clock can be set to 1, 4, 16, 64, 256 and 1024 by software
- Direct memory access controllers
  - Support up to 32 independent DMA channels
  - Descriptor or No-Descriptor Transfer mode compatible with previous JZ SOC
  - Transfer data units: 1-byte, 2-byte, 4-byte, 16-byte, 32-byte, 64-byte, 128-byte
  - Transfer number of data unit: $1 \sim 2^{24} - 1$
  - Independent source and destination port width: 8-bit, 16-bit, 32-bit
  - Fixed three priorities of channel groups: 0~3, highest; 4~11: mid; 12~31: lowest
  - An extra INTC IRQ can be bound to one programmable DMA channel
- SAR A/D Controller
  - 2 Channels
  - Resolution: 10-bit
  - Integral nonlinearity: ±1 LSB
  - Differential nonlinearity: ±0.5 LSB
  - Resolution/speed: up to 2MSPS
  - Max Frequency: 24MHz
  - Low power dissipation: 1.5mW(worst)
  - Support multi-touch detect
  - Support write control command by software
  - Single-end and Differential Conversion Mode

- Support external touch screen controller
- Pin Description

- RTC (Real Time Clock)
  - Need external 32768Hz oscillator for 32k clock generation
  - 32-bits second counter
  - Programmable and adjustable counter to generate accurate 1 Hz clock
  - Alarm interrupt, 1Hz interrupt
  - Stand alone power supply, work in hibernating mode
  - Power down controller
  - Alarm wakeup
  - External pin wakeup with up to 2s glitch filter
- OTP Slave Interface
  - Total 512 bits. Lower 192bits are read only, other higher bits are read-able and write-able

1.2.9 Peripherals

- General-Purpose I/O ports
  - Each port can be configured as an input, an output or an alternate function port
  - Each port can be configured as an interrupt source of low/high level or rising/falling edge triggering. Every interrupt source can be masked independently
  - Each port has an internal pull-up or pull-down resistor connected. The pull-up/down resistor can be disabled
  - GPIO output 6 interrupts, 1 for every group, to INTC
- SMB Controller
  - Two-wire SMB serial interface – consists of a serial data line (SDA) and a serial clock (SCL)
  - Two speeds
    - Standard mode (100 Kb/s)
    - Fast mode (400 Kb/s)
  - Device clock is identical with pclk
  - Programmable SCL generator
  - Master or slave SMB operation
  - 7-bit addressing/10-bit addressing
  - 16-level transmit and receive FIFOs
  - Interrupt operation
  - The number of devices that you can connect to the same SMB-bus is limited only by the maximum bus capacitance of 400pF
  - APB interface
  - 2 independent SMB channels (SMB0, SMB1)
- One Normal Speed Synchronous serial interfaces (SFC0)
  - 3 protocols support: National's Microwire, TI's SSP, and Motorola's SPI
  - transmit-only or receive-only operation
  - MSB first for command and data transfer, and LSB first for address transfer

- 64 entries x 32 bits wide data FIFO
- one device select
- Configurable sampling point for reception
- Configurable timing parameters: tSLCH, tCHSH and tSHSL
- Configurable flash address wide are supported
- 7 transfer formats: Standard SPI, Dual-Output/Dual-Input SPI, Quad-Output/Quad-Input SPI, Dual-I/O SPI, Quad-I/O SPI, Full Dual-I/O SPI, Full Quad-I/O SPI
- two data transfer mode: slave mode and DMA mode
- Configurable 6 phases for software flow

- One Normal Speed Synchronous serial interfaces (SSI0)
  - 3 protocols support: National's Microwire, TI's SSP, and Motorola's SPI
  - Full-duplex or transmit-only or receive-only operation
  - Programmable transfer order: MSB first or LSB first
  - 128 entries deep x 32 bits wide transmit and receive data FIFOs
  - Configurable normal transfer mode or Interval transfer mode
  - Programmable clock phase and polarity for Motorola's SSI format
  - Two slave select signal (SSI_CE_ / SSI_CE2_) supporting up to 2 slave devices
  - Back-to-back character transmission/reception mode
  - Loop back mode for testing
- Two UARTs (UART0, UART1)
  - Full-duplex operation
  - 5-, 6-, 7- or 8-bit characters with optional no parity or even or odd parity and with 1, 1½, or 2 stop bits
  - 64x8 bit transmit FIFO and 64x11bit receive FIFO
  - Independently controlled transmit, receive (data ready or timeout), line status interrupts
  - Internal diagnostic capability Loopback control and break, parity, overrun and framing-error is provided
  - Separate DMA requests for transmit and receive data services in FIFO mode
  - Supports modem flow control by software or hardware
  - Slow infrared asynchronous interface that conforms to IrDA specification
- Two MMC/SD/SDIO controllers (MSC0, MSC1)
  - Fully compatible with the MMC System Specification version 4.2
  - Support SD Specification 3.0
  - Support SD I/O Specification 1.0 with 1 command channel and 4 data channels
  - Consumer Electronics Advanced Transport Architecture (CE-ATA – version 1.1)
  - Maximum data rate is 50MBps
  - Support MMC data width 1bit ,4bit and 8bit
  - Built-in programmable frequency divider for MMC/SD bus
  - Built-in Special Descriptor DMA
  - Maskable hardware interrupt for SDIO interrupt, internal status and FIFO status
  - 128 x 32 built-in data FIFO
  - Multi-SD function support including multiple I/O and combined I/O and memory
  - IRQ supported enable card to interrupt MMC/SD controller

- Single or multi block access to the card including erase operation
- Stream access to the MMC card
- Supports SDIO read wait, interrupt detection during 1-bit or 4-bit access
- Supports CE-ATA digital protocol commands
- Support Command Completion Signal and interrupt to CPU
- Command Completion Signal disable feature
- The maximum block length is 4096bytes

- USB 2.0 OTG interface
  - Complies with the USB 2.0 standard for high-speed (480 Mbps) functions and with the On-The-Go supplement to the USB 2.0 specification
  - Operates either as the function controller of a high- /full-speed USB peripheral or as the host/peripheral in point-to-point or multi-point communications with other USB functions
  - Supports Session Request Protocol (SRP) and Host Negotiation Protocol (HNP)
  - UTMI+ Level 3 Transceiver Interface
  - Soft connect/disconnect
  - 16 Endpoints:
  - Dedicate FIFO
  - Supports control, interrupt, ISO and bulk transfer

1.2.10 Bootrom

16kB Boot ROM memory

1.3 Characteristic

Item	Characteristic
Process Technology	40nm CMOS low power
Power supply voltage	General purpose I/O: 1.6~3.6V DDR I/O for DDR2: 1.8V± 0.1V RTC I/O: 1.8V~3.6V EFUSE programming: 2.5V± 10% Analog power supply 1: 2.5V± 10% Analog power supply 2: 3.3V± 10% Core: 1.1 -0.1/+0.2 V
Package	BGA181 10mm x 10mm x 1.22mm, 0.65mm pitch
Operating frequency	1GHz

2 Packaging and Pinout Information

2.1 Overview

T10 processor is offered in 188-pin LFBGA package, which is 10mm x 10mm x 1.22mm outline, 15 x 15 matrix ball grid array and 0.65mm ball pitch, show in Figure 2-1. The T10 pin to ball assignment is show in Figure 2-2.

The detailed pin description is listed in Table 2-1~ Table 2-18.

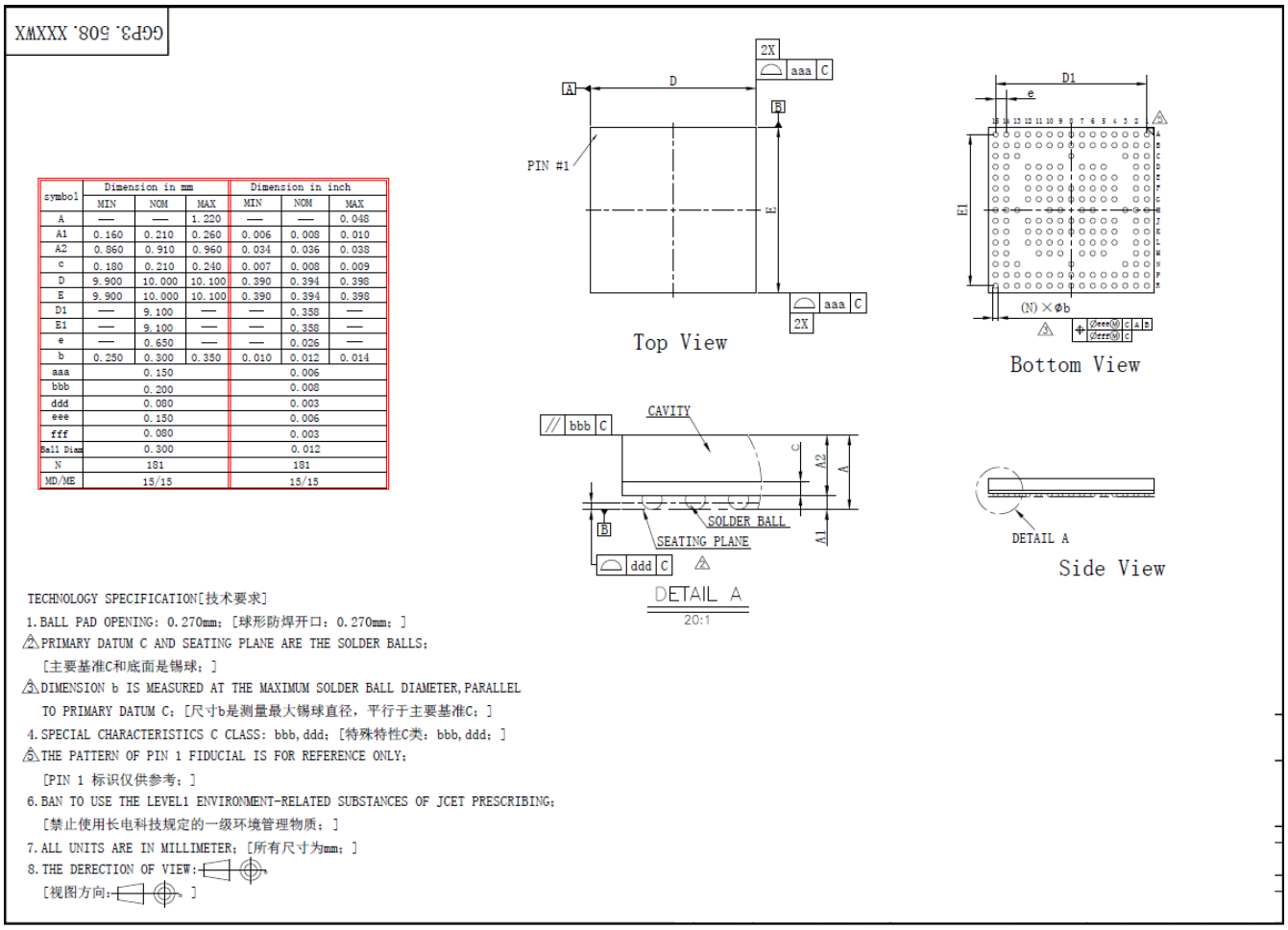
2.2 Solder Process

T10 package is lead-free. It's reflow profile follows the IPC/JEDEC lead-free reflow profile as contained in J-STD-020C.

2.3 Moisture Sensitivity Level

T10 package moisture sensitivity is level 3.

2.4 T10 Package



symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	—	—	1.220	—	—	0.048
A1	0.160	0.210	0.260	0.006	0.008	0.010
A2	0.860	0.910	0.960	0.034	0.036	0.038
c	0.180	0.210	0.240	0.007	0.008	0.009
D	9.900	10.000	10.100	0.390	0.394	0.398
E	9.900	10.000	10.100	0.390	0.394	0.398
D1	—	9.100	—	—	0.358	—
E1	—	9.100	—	—	0.358	—
e	—	0.650	—	—	0.026	—
b	0.250	0.300	0.350	0.010	0.012	0.014
aaa	0.150			0.006		
bbb	0.200			0.008		
ddd	0.080			0.003		
eee	0.150			0.006		
fff	0.080			0.003		
Ball Diam	0.300			0.012		
N	181			181		
MD/ME	15/15			15/15		

TECHNOLOGY SPECIFICATION[技术要求]

1. BALL PAD OPENING: 0.270mm; [球形防焊开口: 0.270mm;]
2. PRIMARY DATUM C AND SEATING PLANE ARE THE SOLDER BALLS;
   [主要基准C和底面是锡球;]
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C; [尺寸b是测量最大锡球直径, 平行于主要基准C;]
4. SPECIAL CHARACTERISTICS C CLASS: bbb, ddd; [特殊特性C类: bbb, ddd;]
5. THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY;
   [PIN 1 标识仅供参考;]
6. BAN TO USE THE LEVEL1 ENVIRONMENT-RELATED SUBSTANCES OF JCET PRESCRIBING;
   [禁止使用长电科技规定的一级环境管理物质;]
7. ALL UNITS ARE IN MILLIMETER; [所有尺寸为mm;]
8. THE DERECTION OF VIEW: [视图方向:]

Figure 2-1 T10 package outline drawing

T10 Ball Assignment Ver1.0

BGA181, 10mm X 10mm X 1.22mm, 0.65pitch, top view

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	0
A		SMB1_SDA_PB25	GPIO_PC17	MSC1_D3_PC07	MSC1_CLK_PC02	MSC1_D1_PC05	SSI0_GPC_DRV_VBUS_PC13	SSI0_CLK_DMIC_CLK_PC15	SSI0_DT_DMIC_DAT1_PC12	CS2_SMB0_SDA_PA12	GPIO_PA20	GPIO_PA18	SA2_DVP_D10_PA10	SD7_DVP_D7_PA07	SD6_DVP_D6_PA06	SD1_DVP_D1_PA01	A
B		PWM1_CLK32K_OUT_PB18	SMB1_SCK_PB26	MSC1_D2_PC06	MSC1_CMD_PC03	MSC1_D0_PC04	SSI0_CE0_PC16	SSI0_DR_DMIC_DAT0_PC11	SSI0_CE1_PC14	RD_SMB0_SCK_PA13	GPIO_PA21	GPIO_PA19	CS1_DVP_D11_PA11	SA0_DVP_D8_PA08	SD5_DVP_D5_PA05	SD0_DVP_D0_PA00	B
C		BOOT_SEL1_PC01	PWM0_PB17	GPIO_PC18					ZQ					SA1_DVP_D9_PA09	SD4_DVP_D4_PA04	DVP_VSYNC_PA17	C
D		EFUSE_AVDD	BOOT_SEL0_PC00			VDDMEM	VDDMEM	VDDMEM		VDDMEM	VDDMEM	VDDMEM	VREF		SD3_DVP_D3_PA03	DVP_PCLK_PA14	D
E		PLL_AVDDHV	PLL_AVSS		VDDMEM	DDRVDD	DDRVDD	VDDMEM		VDDMEM	DDRVDD	DDRVDD	DDRVDD		SD2_DVP_D2_PA02	DVP_HSYNC_PA16	E
F		EXCLK_O	PLL_AVDD		VSSMEM	VSSMEM	DDRVDD	DDRVDD	DDRVSS	DDRVDD	DDRVDD	VSSMEM	VDDIO_D		DVP_MCLK_PA15	GPIO_PA22	F
G		RST_OUT	EXCLK_I		VSSMEM	VSSMEM	VSSMEM	DDRVSS	DDRVSS	DDRVSS	VSSMEM	VSSMEM	VDDIO_D		SFC_GPC_PA25	SFC_CLK_PA27	G
H		ADC_AVDD	ADC_VREF	ADC_AVSS			DDRVSS	DDRVSS		DDRVSS	VSSMEM			SFC_DR_PA24	SFC_DT_PA23	SFC_CE1_PA26	H
J		ADC_AUX0	ADC_AUX1		AVSOTG	VSS	VSS	VSS	DDRVSS	DDRVSS	VSS	VSS	VSS		GPIO_PB30	SFC_CE0_PA28	J
K		OTG_ID0	OTG_VBUS0		CODEC_AGND	VDD	VDD	VSS	VSS	VSS	VSS	VSS	VSS		MSC0_D2_PB02	GPIO_PB29	K
L		AVDOTG	OTG_DP0		VDD	VDD	VDD	VDD		VDD	VDD	VDD	VDDIO		MSC0_CMD_PB05	MSC0_D3_PB03	L
M		OTG_DM0	OTG_TXRTUNE			VDD	VDD	VDD		VDDIO	VDDIO	VDDIO			MSC0_D0_PB00	MSC0_CLK_PB04	M
N		osc32_I	osc32_O	WKUP					GMAC_MDIO_PB11					PWM3_FLASH_OUT_PC09	SPK_ENABLE_PB31	MSC0_D1_PB01	N
P		RTC_VDDIO	PWRON	TEST_TE	CODEC_HPOUT	CODEC_MICP	CODEC_AVDD	GMAC_TXD0_PB13	GMAC_TXCLK_PB06	GMAC_RXD0_PB15	GMAC_PHY_CLK_PB07	UART0_TXD_TDO_PB22	UART0_RTS_PB21	UART1_RXD_TMS_PB24	GPIO_PB28	PWM2_FLASH_STORBE_IN_PC08	P
R		PPRST_	RTC_VDD	CODEC_VCM	CODEC_MICBIAS	CODEC_MICN	GMAC_TXD1_PB14	GMAC_TXEN_PB08	GMAC_MDCK_PB10	GMAC_RXDV_PB09	GMAC_RXD1_PB16	UART0_RXD_TDI_PB19	UART0_CTS_PB20	UART1_TXD_TCK_PB23	TRST	GPIO_PB27	R
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	

Figure 2-2 T10 pin to ball assignment

2.5 Pin Description [1][2]

2.5.1 DDR

Table 2-1 DDR2 Pins (2)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
VREF	AI	D12		VREF0: DDR2 input reference voltage	VDD_{MEM}/2
ZQ	AIO	C8		ZQ: DDR2 External reference which is connected to a 240ohm resister to VSSIOm	

2.5.2 DVP/Static Memory

Table 2-2 DVP/Static memory/ Pins

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
SD0 DVP_D0 PA00	IO I IO	B15	4mA pullup-pe	SD0: Static memory data bus bit 0 DVP_D0:DVP data bit0 PA00: GPIO group A bit 0	VDDIO_D
SD1 DVP_D1 PA01	IO I IO	A15	4mA pullup-pe	SD1: Static memory data bus bit 1 DVP_D0:DVP data bit 1 PA01: GPIO group A bit 1	VDDIO_D
SD2 DVP_D2 PA02	IO I IO	E14	4mA pullup-pe	SD2: Static memory data bus bit 2 DVP_D2:DVP data bit 2 PA02: GPIO group A bit 2	VDDIO_D
SD3 DVP_D3 PA03	IO I IO	D14	4mA pullup-pe	SD3: Static memory data bus bit 3 DVP_D3:DVP data bit3 PA03: GPIO group A bit 3	VDDIO_D
SD4 DVP_D4 PA04	IO I IO	C14	4mA pullup-pe	SD4: Static memory data bus bit 4 DVP_D4:DVP data bit 4 PA04: GPIO group A bit 4	VDDIO_D
SD5 DVP_D5 PA05	IO I IO	B14	4mA pullup-pe	SD5: Static memory data bus bit 5 DVP_D5:DVP data bit 5 PA05: GPIO group A bit 5	VDDIO_D
SD6 DVP_D6 PA06	IO I IO	A14	4mA pullup-pe	SD6: Static memory data bus bit 6 DVP_D6:DVP data bit 6 PA06: GPIO group A bit 6	VDDIO_D
SD7 DVP_D7 PA07	IO I IO	A13	4mA pullup-pe	SD7: Static memory data bus bit 7 DVP_D7:DVP data bit 7 PA07: GPIO group A bit 7	VDDIO_D
SA0 DVP_D8 PA08	O I IO	B13	4mA pullup-pe	SA0: Static memory address bus bit 0 DVP_D8:DVP data bit 8 PA08: GPIO group A bit 8	VDDIO_D
SA1 DVP_D9 PA09	O I IO	C13	4mA pullup-pe	SA1: Static memory address bus bit 1 DVP_D9:DVP data bit 9 PA09: GPIO group A bit 9	VDDIO_D

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
SA2 DVP_D10 PA10	IO I IO	A12	4mA pullup-pe	SA2: Static memory data bus bit 10 DVP_D10:DVP data bit 10 PA10: GPIO group A bit 10	VDDIO_D
CS1 DVP_D11 PA11	O I IO	B12	4mA pullup-pe	CS1: Static memory chip 1 select DVP_D11:DVP data bit 11 PA11: GPIO group A bit 11	VDDIO_D
CS2 I2C0_SDA PA12	O IO IO	A9	4mA pullup-pe rst-pe	CS2: Static memory chip 2 select I2C0_SDA: I2C 0 serial data PA12: GPIO group A bit 12	VDDIO_D
RD I2C0_SCL PA13	O IO IO	B9	4mA pullup-pe rst-pe	RD: Static memory read I2C0_SCL: I2C 0 serial clock PA13: GPIO group A bit 13	VDDIO_D
DVP_PCLK PA14	I IO	D15	4mA pullup-pe rst-pe	DVP_PCLK: camera sensor clock input PA14: GPIO group A bit 14	VDDIO_D
DVP_MCLK PA15	IO IO	F14	8mA pullup-pe rst-pe	DVP_MCLK: DVP clock output PA15: GPIO group A bit 15	VDDIO_D
DVP_HSYNC PA16	O IO	E15	4mA pullup-pe rst-pe	DVP_HSYNC: DVP horizontal sync PA16: GPIO group A bit 16	VDDIO_D
DVP_VSYNC PA17	O IO	C15	4mA pullup-pe rst-pe	DVP_VSYNC: DVP vertical sync PA17: GPIO group A bit 17	VDDIO_D
PA22	IO	F15	4mA pullup-pe rst-pe Schmitt	PA22: GPIO group A bit 22	VDDIO_D

2.5.3 GPIO

Table 2-3 GPIO Pins (11)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
PA18	IO	A11	4mA pullup-pe rst-pe	PA18: GPIO group A bit 18	VDDIO_D
PA19	IO	B11	4mA pulldown-pe rst-pe	PA19: GPIO group A bit 19	VDDIO_D
PA20	IO	A10	4mA	PA20: GPIO group A bit 20	VDDIO_

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
			pullup-pe rst-pe		D
PA21	IO	B10	4mA pullup-pe rst-pe	PA19: GPIO group A bit 19	VDDIO_D
PB27	IO	R15	8mA pullup-pe rst-pe	PB27: GPIO group B bit 27	VDDIO
PB28	IO	P14	4mA pulldown-pe rst-pe	PA28: GPIO group B bit 28	VDDIO
PB29	IO	K15	4mA pullup-pe rst-pe Schmitt	PB29: GPIO group B bit 29	VDDIO
PB30	IO	J14	4mA pullup-pe rst-pe Schmitt	PB30: GPIO group B bit 30	VDDIO
SPK_ENABLE_PB31	IO	N14	4mA pulldown-pe rst-pe Schmitt	PB31: GPIO group B bit 31, used as speaker enable in GPIO	VDDIO
PC17	IO	A2	8mA pullup-pe	PC17: GPIO group C bit 17	VDDIO
PC18	IO	C3	8mA pullup-pe	PC18: GPIO group C bit 18	VDDIO

2.5.4 MSCx

Table 2-4 MSC0/MSC1, Pins (12)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
MSC0_D0 PB00	IO IO	M14	4mA pullup-pe rst-pe	MSC0_D0: MSC (MMC/SD) 0 data bit 0 PB00: GPIO group B bit 00	VDDIO
MSC0_D1 PB01	IO IO	N15	4mA pullup-pe rst-pe	MSC0_D1: MSC (MMC/SD) 0 data bit 1 PB01: GPIO group B bit 01	VDDIO
MSC0_D2 PB02	IO IO	K14	4mA pullup-pe rst-pe	MSC0_D2: MSC (MMC/SD) 0 data bit 2 PB02: GPIO group B bit 02	VDDIO
MSC0_D3 PB03	IO IO	L15	4mA pullup-pe rst-pe	MSC0_D3: MSC (MMC/SD) 0 data bit 3 PB03: GPIO group B bit 03	VDDIO
MSC0_CLK PB04	O IO	M15	8mA pulldown-pe	MSC0_CLK: MSC (MMC/SD) 0 clock output PB04: GPIO group B bit 04	VDDIO

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
			rst-pe		
MSC0_CMD PB05	IO IO	L14	4mA pullup-pe rst-pe	MSC0_CMD: MSC (MMC/SD) 0 command PB05: GPIO group B bit 05	VDDIO
MSC1_D0 PC04	IO IO	B5	4mA pullup-pe	MSC1_D0: MSC (MMC/SD) 0 data bit 0 PC04: GPIO group B bit 04	VDDIO
MSC1_D1 PC05	IO IO	A5	4mA pullup-pe	MSC1_D1: MSC (MMC/SD) 0 data bit 1 PC05: GPIO group B bit 05	VDDIO
MSC1_D2 PC06	IO IO	B3	4mA pullup-pe	MSC1_D2: MSC (MMC/SD) 0 data bit 2 PC06: GPIO group B bit 06	VDDIO
MSC1_D3 PC07	IO IO	A3	4mA, pullup-pe	MSC1_D3: MSC (MMC/SD) 0 data bit 3 PC07: GPIO group B bit 07	VDDIO
MSC1_CLK PC02	O IO	A4	8mA pullup-pe	MSC1_CLK: MSC (MMC/SD) 0 clock output PC02: GPIO group B bit 02	VDDIO
MSC1_CMD PC03	IO IO	B4	4mA pullup-pe	MSC1_CMD: MSC (MMC/SD) 0 command PC03: GPIO group B bit 03	VDDIO

2.5.5 I2C

Table 2-5 I2C0/I2C1 Pins (4; all GPIO shared: PA12~13, PB25~26)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
CS2 I2C0_SDA PA12	O IO IO	A9	4mA pullup-pe rst-pe	CS2: Static memory chip 2 select I2C0_SDA: I2C 0 serial data PA12: GPIO group A bit 12	VDDIO_D
RD_ I2C0_SCL PA13	O IO IO	B9	4mA pullup-pe rst-pe	RD_: Static memory read I2C0_SCL: I2C 0 serial clock PA13: GPIO group A bit 13	VDDIO_D
I2C1_SDA PB25	IO IO	A1	4mA pullup-pe rst-pe	I2C1_SDA: I2C 1 serial data PB25: GPIO group B bit 25	VDDIO
I2C1_SCL PB26	IO IO	B2	4mA pullup-pe rst-pe	I2C1_SCL: I2C 1 serial clock PB26: GPIO group B bit 26	VDDIO

2.5.6 PWM

Table 2-6 PWM Pins (4)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
PWM0 PB17	IO IO	C2	4mA pulldown-pe rst_pe	PWM0: PWM output or pulse input 0 PB17: GPIO group B bit 17.	VDDIO
PWM1 CLK32K_out PB18	IO O IO	B1	4mA pulldown-pe rst_pe	PWM1: PWM output or pulse input 1 CLK32K_OUT: 32.768K clock out PB18: GPIO group B bit 18.	VDDIO

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
PWM2 FLASH_STORE_IN PC08	IO I IO	P15	4mA pullup-pe	PWM2: PWM output or pulse input 2 FLASH_STORE_IN: camera flash store input PC08: GPIO group C bit 08.	VDDIO
PWM3 FLASH_OUT PC09	IO O IO	N13	4mA pullup-pe	PWM3: PWM output or pulse input 3 FLASH_OUT: camera flash out PC09: GPIO group C bit 09.	VDDIO

2.5.7 MAC(RMII)

Table 2-7 GMAC Pins (10)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
GMAC_TXCLK PB06	I IO	P8	4mA pullup-pe	GMAC_TXCLK: gmac transmitting clock PB06: GPIO group B bit 06	VDDIO
GMAC_TXEN PB08	O IO	R7	4mA pullup-pe	GMAC_TXEN: gmac transmitting enable PB08: GPIO group B bit 08	VDDIO
GMAC_PHY_CLK PB07	O IO	P10	8mA pullup-pe	GMAC_PHY_CLK: gmac phy clock PB07: GPIO group B bit 07	VDDIO
GMAC_RXDV PB09	I IO	R9	4mA pullup-pe	GMAC_RXDV: gmac receive data valid PB09: GPIO group B bit 09	VDDIO
GMAC_MDCK PB10	O IO	R8	4mA pulldown-pe rst-pe	GMAC_MDCK: gmac manage data clock PB10: GPIO group B bit 10	VDDIO
GMAC_MDIO PB11	IO IO	N8	4mA pullup-pe	GMAC_MDIO: gmac MDIO which is clocked by MDC PB11: GPIO group B bit 11	VDDIO
GMAC_TXD0 PB13	O IO	P7	4mA pullup-pe	GMAC_TXD0: gmac transmit data bit 0 PB13: GPIO group B bit 13	VDDIO
GMAC_TXD1 PB14	O IO	R6	4mA pullup-pe	GMAC_TXD1: gmac transmit data bit 1 PB14: GPIO group B bit 14	VDDIO
GMAC_RXD0 PB15	I IO	P9	4mA pullup-pe	GMAC_RXD0: gmac receive data bit 0 PB15: GPIO group B bit 15	VDDIO
GMAC_RXD1 PB16	I IO	R10	4mA pullup-pe	GMAC_RXD1: gmac receive data bit 1 PB16: GPIO group B bit 16	VDDIO

2.5.8 UART/JTAG

Table 2-8 UART Pins (6)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
UART0_RXD TDO PB19	I O IO	R11	4mA pull-up	UART0_RXD: uart0 receive data TDO: JTAG data ouput PB19: GPIO group B bit 19	VDDIO
UART0_CTS PB20	I IO	R12	4mA pull-up	UART0_CTS: UART0 CTS input PB20: GPIO group B bit 20	VDDIO
UART0_RTS PB21	I IO	P12	4mA pull-up	UART0_RTS: UART0 RTS output PB21: GPIO group B bit 21	VDDIO
UART0_TXD TDI PB22	O I IO	P11	4mA pull-up	UART0_TXD: UART0 transmit data TDI: JTAG data input PB22: GPIO group B bit 22	VDDIO
UART1_TXDTCK PB23	O I IO	R13	4mA pull-up	UART1_TXD: UART1 transmit data TCK: JTAG clock PB23: GPIO group B bit 23	VDDIO
UART1_RXD TMS PB24	I I IO	P13	4mA pull-up rst-pe	UART1_RXD: UART1 receive data TMS: JTAG mode select PB24: GPIO group B bit 24	VDDIO

2.5.9 SFC/SSI/OTG

Table 2-9 SFC/SSI/OTG Pins (12)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
SFC_DT PA23	IO IO	H14	4mA pull-up rst_pe	SFC_DT: high speed ssi transmit data PA23: GPIO group A bit 23	VDDIO
SFC_DR PA24	IO IO	H13	4mA pull-up rst_pe	SFC_DR: high speed ssi receive data PA24: GPIO group A bit 24	VDDIO
SFC_GPC PA25	IO IO	G14	4mA pull-up rst-pe	SFC_GPC: high speed ssi general-purpose control PA25: GPIO group A bit 25	VDDIO
SFC_CE1 PA26	IO IO	H15	4mA pull-down rst-pe	SFC_CE1: high speed ssi chip 1 select PA26: GPIO group A bit 26	VDDIO
SFC_CLK PA27	IO IO	G15	8mA pull-up rst-pe	SFC_CLK: high speed ssi clock PA27: GPIO group A bit 27	VDDIO
SFC_CE0 PA28	IO IO	J15	4mA pull-up rst-pe	SFC_CE0: high speed ssi chip 0 select PA28: GPIO group A bit 28	VDDIO
SSI0_DR DMIC_DAT0 PC11	I IO	B7	4mA pull-up	SSI0_DR: high speed ssi receive data DMIC_DAT0: dmic sensor data1 PC11: GPIO group C bit 11	VDDIO
SSI0_DT DMIC_DAT1 PC12	I O IO	A8	4mA pull-up	SSI0_DT: high speed ssi transmit data DMIC_DAT1:dmic sensor data1 PC12: GPIO group C bit 12	VDDIO
SSI0_GPC DRV_VBUS PC13	I O IO	A6	4mA pull-up rst-pe	SSI0_GPC: high speed ssi general-purpose control DRV_VBUS: USB OTG VBUS driver control signal PC13: GPIO group C bit 13	VDDIO
SSI0_CE1 PC14	IO IO	B8	4mA pull-up	SSI0_CE1: high speed ssi chip 1 select PC14: GPIO group C bit 14	VDDIO
SSI0_CLK PC15	IO IO	A7	4mA pull-up	SSI0_CLK: high speed ssi clock PC15: GPIO group C bit 15	VDDIO
SSI0_CE0 PC16	IO IO	B6	4mA pull-down rst-pe	SSI0_CE0: high speed ssi chip 0 select PC16: GPIO group C bit 16	VDDIO

2.5.10 System

Table 2-10 JTAG/Watch reset out Pins(2)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
TRST_	I	R14	Schmitt pull-down	TRST_: JTAG reset	
RST_OUT_	O	G1	pull-up	RST_OUT_: system reset output	

Table 2-11 System Pins(2)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
PC00 (BOOT_SEL0)	IO I	D2	4mA pullup-pe	PC00: GPIO group C bit 00 It is taken as BOOT select bit 0 by Boot ROM code	VDDIO
PC01 (BOOT_SEL1)	IO I	C1	4mA pullup-pe	PC01: GPIO group C bit 01 It is taken as BOOT select bit 1 by Boot ROM code	VDDIO

2.5.11 Digital power/ground

Table 2-12 IO/Core power supplies for FBGAs (48)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
VDDMEM	P	D5,D6,D7, D9,D10,D1 1,E4,E7,E9		VDDMEM: IO digital power for DRAM, 1.8V ± 0.1V	-
VSSMEM	P	F4,F5,F11, G4,G5,G6, G10,G11,H 10		VSSMEM: IO digital ground for DRAM, 0V	-
VDDIO_D	P	F12,G12		VDDIO_D: IO digital power for DVP power domain, 1.8V~3.3V	-
VDDIO	P	L12,M9,M1 0,M11		VDDIO: IO digital power for none DRAM/NAND, 3.3V	-
VSS	P	J5,J6,J7,J1 0,J11,J12, K7,K8,K9, K10,K11,K 12		VSS: IO digital gound for none DRAM and CORE digital ground, 0V	-
VDD	P	K5,K6,L4,L 5,L6,L7,L9, L10,L11,M 5,M6,M7		VDD: CORE digital power, 1.1V	-

2.5.12 Analog - OTG

Table 2-13 USB 2.0 OTG (7)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
OTG_DP0	AIO	L2		OTG_DP0: OTG OTG data plus	AVDOTG
OTG_DM0	AIO	M1		OTG_DM0: OTG data minus	AVDOTG
OTG_VBUS0	AIO	K2		OTG_VBUS0: OTG 5-V power supply pin for OTG. An external charge pump must provide power to this pin	AVDOTG
OTG_ID0	AI	K1		OTG_ID0: OTG mini-receptacle identifier. It differentiates a mini-A from a mini-B plug. If this signal is not used, internal resistance pulls the signal's voltage level to AVDOTG33.	AVDOTG
OTG_TXRTUNE	AIO	M2		OTG_TXRTUNE: Transmitter resister tune. It connects to an external resistor of 300Ω with 1% tolerance to analog ground AVSOTG, that adjusts the OTG 2.0 high-speed source impedance	AVDOTG
AVDOTG	P	L1		AVDOTG: OTG 2.0 host & OTG analog power, 3.3V	-
AVSOTG	P	J4		AVSOTG: OTG analog ground	-

2.5.13 Analog - SAR ADC

Table 2-14 SAR ADC Pins (5)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
ADC_AUX0	AI	J1		ADC_AUX0: ADC general purpose input	AVD_{AD}
ADC_AUX1	AI	J2		ADC_AUX1: ADC general purpose input	AVD_{AD}
ADC_AVDD	P	H1		AVDADC: ADC analog power, 3.3 V	-
ADC_AVSS	P	H3		AVSADC: ADC analog ground	-
ADC_VREF	AI	H2		Voltage reference, 0.5* ADC_AVDD ~0.99* ADC_AVDD	-

2.5.14 Analog - CODEC

Table 2-15 CODEC Pins (6)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
CODEC_MICP	AI	P5		CODEC_MICP: differential microphone input	CODEC_AVDD
CODEC_MICN	AI	R5		CODEC_MICN: differential microphone input	CODEC_AVDD
CODEC_VCM	AO	R3		CODEC_VCM: Reference voltage output	CODEC_AVDD

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
CODEC_MICBIAS	AO	R4		CODEC_MICBIAS: Microphone bias output	CODEC_AVDD
CODEC_HPOUT	AO	P4		CODEC_HPOUT: headphone output	CODEC_AVDD
CODEC_AVDD	P	P6		CODEC_AVDD:3.3v analog supply	CODEC_AVDD
CODEC_AGND	P	K4		CODEC_AVSS: Analog ground	CODEC_AGND

2.5.15 Analog - EFUSE

Table 2-16 EFUSE Pins for Two EFUSE (1)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
EFUSE_AVDD	P	D1		AVDEFUSE: EFUSE programming power, 0V/2.5V	AVD_{AD}

2.5.16 Analog - CPM

Table 2-17 CPM Pins (5)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
EXCLK_I	AI	G2	2~30 MHz Oscillator, OSC on/off	EXCLK_XIN: OSC input or 24MHz clock input	VDD33
EXCLK_O	AO	F1		EXCLK_XOUT: OSC output	VDD33
PLL_AVDDHV	P	E1		PLL_AVDDHV: PLL analog power, 3.3V	-
PLL_AVDD	P	F2		PLL_AVDD: PLL analog power, 1.1V	-
PLL_AVSS	P	E2		AVSPLL: PLL0~3 analog ground	-

2.5.17 Analog - RTC

Table 2-18 RTC Pins (8)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
OSC32_I	AI	N1	32768Hz Oscillator	OSC32_IN:32768Hz clock input	VDDRTC
OSC32_O	AO	N2		OSC32_OUT: Reserved	VDDRTC
PWRON	O	P2	8mA	PWRON: Power on/off control of main power	VDDRTC
WKUP*	I	N3	Schmitt	WKUP: Wakeup signal after main power down	VDDRTC
PPRST_	I	R1	Schmitt	PPRST_: RTC power on reset and RESET-KEY reset input	VDDRTC
TEST_TE	I	P3	Schmitt, pull-down	TEST_TE: Manufacture test enable, program readable	VDDRTC
RTC_VDD	P	R2		RTC_VDD: 1.1V power for RTC	-
RTC_VDDIO	P	P1		RTC_VDDIO: 3.3V power for RTC	-

NOTES:

1 The meaning of phases in IO cell characteristics are:

- Bi-dir, Single-end: bi-direction and single-ended DDR IO are used.
- Output, Single-end: output and single-ended DDR IO are used.
- Output, Differential: output and differential signal DDR IO are used.
- Bi-dir, Differential: bi-direction and differential signal DDR IO are used.
- 8/16mA out: The IO cell's output driving strength is about 8/16mA.
- Pull-up: The IO cell contains a pull-up resistor.
- Pull-down: The IO cell contains a pull-down resistor.
- Pullup-pe: The IO cell contains a pull-up resistor and the pull-up resistor can be enabled or disabled by setting corresponding register.
- Pulldown-pe: The IO cell contains a pull-down resistor and the pull-down resistor can be enabled or disabled by setting corresponding register.
- rst-pe: these pins are initialed (during reset and after reset) to IO internal pull (up or down) enabled. Otherwise, the pins are initialed to pull disabled
- Schmitt: The IO cell is Schmitt triger input.

2 All GPIO shared pins are reset to GPIO input.

3 *: This pin has GPIO function as group A bit 30, but only input/interrupt function.

3 Electrical Specifications

3.1 Absolute Maximum Ratings

The absolute maximum ratings for the processors are listed in Table 3-1. Do not exceed these parameters or the part may be damaged permanently. Operation at absolute maximum ratings is not guaranteed.

Table 3-1 Absolute Maximum Ratings

Parameter	Min	Max	Unit
Storage Temperature	-65	150	°C
Operation Temperature	-40	125	°C
VDDMEM power supplies voltage	-0.5	1.98	V
VDDIO power supplies voltage	-0.5	3.6	V
VDDIOD power supplies voltage	-0.5	3.6	V
VDD power supplies voltage	-0.2	1.21	V
PLL_AVDD power supplies voltage	-0.2	1.21	V
PLL_AVDDHV power supplied voltage	-0.5	3.6	V
EFUSE_AVDD power supplies voltage	-0.5	2.75	V
RTC_VDD(11) power supplies voltage	-0.5	1.3	V
RTC_VDD_IO power supplies voltage	-0.5	3.63	V
AVDOTG power supplies voltage	-0.5	3.63	V
ADC_AVDD power supplies	-0.5	3.63	V
CODEC_AVDD power supplies voltage	-0.5	3.63	V
Maximum ESD stress voltage, Human Body Model; Any pin to any supply pin, either polarity, or Any pin to all non-supply pins together, either polarity. Three stresses maximum.	-	2000	V

3.2 Recommended operating conditions

Table 3-2 Recommended operating conditions for power supplies

Symbol	Description	Min	Typical	Max	Unit
VMEM	VDDMEM voltage for SSTL18 (DDR2)	1.7	1.8	1.9	V
VDDIO	VDDIO voltage	3	3.3	3.6	V
VDDIO_D	VDDIOD voltage	1.62	1.8	3.6	V
VDD	VDDcore voltage	0.99	1.1	1.21	V
PLL_AVDD	AVDPLL analog voltage	1.08	1.1	1.21	V
PLL_AVDDHV	AVDPLL analog IO voltage	1.62	1.8/2.5	3.63	V

EFUSE_AVDD	AVDEFUSE voltage	2.25	2.5	2.75	V
RTC_VDD	VDDRTC11 voltage	0.99	1.1	1.21	V
RTC_VDDIO	VDDRTC voltage	1.8	3.3	3.6	V
AVDOTG	AVDUSB33 voltage	3.0	3.3	3.6	V
ADC_AVDD	AVDAD voltage	3.0	3.3	3.6	V
CODEC_AVDD	CODEC_AVDD voltage	2.97	3.3	3.63	V

Table 3-3 Recommended operating conditions for VDDIO/VDDIOn/VDDRTC supplied pins

Symbol	Parameter	Min	Typical	Max	Unit
V_{IH18}	Input high voltage for 1.8V I/O application	1.17		3.6	V
V_{IL18}	Input low voltage for 1.8V I/O application	–0.3		0.63	V
V_{IH25}	Input high voltage for 2.5V I/O application	1.7		3.6	V
V_{IL25}	Input low voltage for 2.5V I/O application	–0.3		0.7	V
V_{IH33}	Input high voltage for 3.3V I/O application	2		3.6	V
V_{IL33}	Input low voltage for 3.3V I/O application	–0.3		0.8	V

Table 3-4 Recommended operating conditions for others

Symbol	Description	Min	Typical	Max	Unit
T_A	Ambient temperature	–20		85	°C

Table 3-5 Recommended operating conditions for ADC pins

Symbol	Description	Min	Typical	Max	Unit
V_{IADC}	ADC_XP/ADC_XM/ADC_YP/ADC_YM/ADC_AUX1/ADC_AUX2 input voltage range	0		AVD_{AD}	V

3.3 DC Specifications

The DC characteristics for each pin include input-sense levels and output-drive levels and currents. These parameters can be used to determine maximum DC loading, and also to determine maximum transition times for a given load. All DC specification values are valid for the entire temperature range of the device.

Table 3-6 DC characteristics for V_{REFMEM} and V_{TT}

Symbol	Parameter	Min	Typical	Max	Unit
VREFM	Reference voltage supply	0.49	0.9	0.51	VMEM
VTT	Terminal Voltage	VREFM – 0.4	VREFM	VREFM + 0.4	V

Table 3-7 DC characteristics for VDDIO/VDDIOn/VDDRTC supplied pins for 1.8V application

Symbol	Parameter		Min	Typical	Max	Unit
V_T	Threshold point		0.77	0.84	0.92	V
V_{T+}	Schmitt trig low to high threshold point		0.99	1.1	1.19	V
V_{T-}	Schmitt trig high to low threshold point		0.62	0.73	0.82	V
V_{TPU}	Threshold point with pull-up resistor enabled		0.77	0.84	0.91	V
V_{TPD}	Threshold point with pull-down resistor enabled		0.77	0.85	0.92	V
V_{TPU+}	Schmitt trig low to high threshold point with pull-up resistor enabled		0.99	1.1	1.19	V
V_{TPU-}	Schmitt trig high to low threshold point with pull-down resistor enabled		0.62	0.73	0.81	V
V_{TPD+}	Schmitt trig low to high threshold point with pull-down resistor enabled		0.99	1.1	1.2	V
V_{TPD-}	Schmitt trig high to low threshold point with pull-up resistor enabled		0.62	0.73	0.82	V
I_L	Input Leakage Current @ V_I=1.8V or 0V				±10	μA
I_{OZ}	Tri-State output leakage current @ V_I=1.8V or 0V				±10	μA
R_{PU}	Pull-up Resistor		79	129	218	kΩ
R_{PD}	Pull-down Resistor		73	127	233	kΩ
V_{OL}	Output low voltage				0.45	V
V_{OH}	Output high voltage		1.35			V
I_{OL}	Low level output current @ V_{OL}(max)	8mA	6.9	12.5	20.1	mA
		16mA	11.5	20.8	33.5	mA
I_{OH}	High level output current @ V_{OH}(min)	8mA	4.9	11.6	22.6	mA
		16mA	8.4	19.9	38.8	mA

Table 3-8 DC characteristics for VDDIO/VDDIOn/VDDRTC supplied pins for 2.5V application

Symbol	Parameter	Min	Typical	Max	Unit
V_T	Threshold point	1.03	1.13	1.23	V
V_{T+}	Schmitt trig low to high threshold point	1.32	1.45	1.56	V
V_{T-}	Schmitt trig high to low threshold point	0.92	1.01	1.12	V
V_{TPU}	Threshold point with pull-up resistor enabled	1.03	1.13	1.23	V
V_{TPD}	Threshold point with pull-down resistor enabled	1.05	1.14	1.23	V
V_{TPU+}	Schmitt trig low to high threshold point with pull-up resistor enabled	1.32	1.45	1.55	V
V_{TPU-}	Schmitt trig high to low threshold point with pull-down resistor enabled	0.91	1	1.12	V
V_{TPD+}	Schmitt trig low to high threshold point with pull-down resistor enabled	1.33	1.46	1.56	V

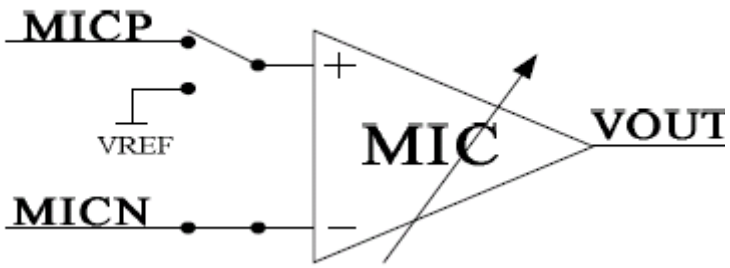
V_{TPD-}	Schmitt trig high to low threshold point with pull-up resistor enabled		0.92	1.01	1.13	V
I_L	Input Leakage Current @ V_I=1.8V or 0V				±10	μA
I_{OZ}	Tri-State output leakage current @ V_I=1.8V or 0V				±10	μA
R_{PU}	Pull-up Resistor		53	82	132	kΩ
R_{PD}	Pull-down Resistor		51	82	143	kΩ
V_{OL}	Output low voltage				0.7	V
V_{OH}	Output high voltage		1.7			V
I_{OL}	Low level output current @ V_{OL}(max)	8mA	15.1	25.3	37.3	mA
		16mA	25.1	42.2	62.2	mA
I_{OH}	High level output current @ V_{OH}(min)	8mA	13.3	26.6	46.4	mA
		16mA	22.8	45.7	79.6	mA

Table 3-9 DC characteristics for VDDIO/VDDIOn/VDDRTC supplied pins for 3.3V application

Symbol	Parameter		Min	Typical	Max	Unit
V_T	Threshold point		1.34	1.46	1.6	V
V_{T+}	Schmitt trig low to high threshold point		1.69	1.83	1.96	V
V_{T-}	Schmitt trig high to low threshold point		1.21	1.32	1.46	V
V_{TPU}	Threshold point with pull-up resistor enabled		1.33	1.44	1.59	V
V_{TPD}	Threshold point with pull-down resistor enabled		1.36	1.47	1.6	V
V_{TPU+}	Schmitt trig low to high threshold point with pull-up resistor enabled		1.69	1.82	1.94	V
V_{TPU-}	Schmitt trig high to low threshold point with pull-down resistor enabled		1.2	1.31	1.45	V
V_{TPD+}	Schmitt trig low to high threshold point with pull-down resistor enabled		1.71	1.84	1.97	V
V_{TPD-}	Schmitt trig high to low threshold point with pull-up resistor enabled		1.23	1.33	1.46	V
I_L	Input Leakage Current @ V_I=1.8V or 0V				±10	μA
I_{OZ}	Tri-State output leakage current @ V_I=1.8V or 0V				±10	μA
R_{PU}	Pull-up Resistor		41	60	92	kΩ
R_{PD}	Pull-down Resistor		43	64	104	kΩ
V_{OL}	Output low voltage				0.4	V
V_{OH}	Output high voltage		2.4			V
I_{OL}	Low level output current @ V_{OL}(max)	8mA	13.1	20.2	27.4	mA
		16mA	21.9	33.8	45.7	mA
I_{OH}	High level output current @ V_{OH}(min)	8mA	19.3	38.2	64.5	mA
		16mA	33.1	65.4	110.5	mA

3.4 Audio codec

3.4.1 Microphone input



There are two microphone input channels, MICR and MICN. They can be configured as either single-ended input or differential inputs by the microphone PGA(MIC).

In single-ended mode., MICN is input to MIC, respectively. In differential mode, MICP is also input to MIC to form a differential input pair with MICN.

Microphone PGA has two gains to amplify the input signal, that is, 0dB and +20dB.

3.4.2 ALC

Automatic Level Control (ALC) function is included to adjust the signal level, which is input into ADC. ALC will measure the signal magnitude and compare it to defined threshold. Then it will adjust the ALC controlled PAG (ALC) gain according to the comparison result.

The programmable gain range of ALC controlled PAG is from -18dB to +28.5dB. The tuning step is 1.5dB.

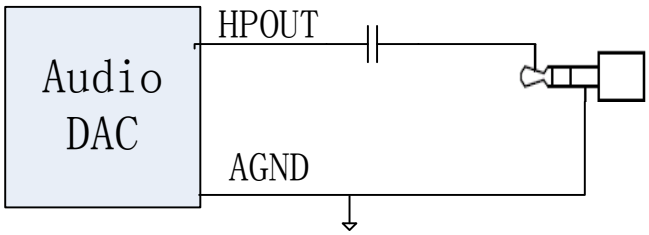
3.4.3 Headphone output

DAC output can drive 16Ohm or 32 Ohm headphone load through DC-blocking capacitor.

In the configuration using DC-blocking capacitor, shown in following figure, the headphone ground is connected to the real ground. The capacitance and the load resistance determine the lower cut-off frequency. For instance, if 16 Ohm headphone and 100uF DC-blocking capacitor are used, the lower cut-off frequency is

$$f = \frac{1}{2\pi RC} = \frac{1}{2\pi \times 16 \times 100 \times 10^{-6}} = 99.5Hz$$

The DC-blocking capacitor can be increased to lower the cut-off frequency for better bass response.



The headphone driver chooses DAC output as input. It has a gain rang from -39dB to +6dB with a tuning step of 1.5dB.

3.4.4 Microphone bias

Microphone bias output is used to bias external microphones. The bias voltage can varies from 0.5*CODEC_AVDD to 0.85* CODEC_AVDD with a step of 0.05* CODEC_AVDD.

3.5 Power On, Reset and BOOT

3.5.1 Power-On Timing

The external voltage regulator and other power-on devices must provide the T10 processor with a specific sequence of power and resets to ensure proper operation. Figure 3-1 shows this sequence and Table 3-10 gives the timing parameters. Following are the name of the power.

- VDDRTC: RTC_VDD_IO, RTC_VDD
- AVDAUD: CODEC_AVDD
- VDD11: all 1.1V power supplies, include VDDCORE, PLL_AVDD
- VDD: all other digital IO, include DDR power supplies: VDDMEM, VDDIO, VDDIOD
- AVD: all other analog power supplies: ADC_AVDD, AVDOTG,PLL_AVDDHV
- AVDEFUSE

Table 3-10 Power-On Timing Parameters

Symbol	Parameter	Min	Max	Unit
t_{R_VDDRTC}	VDDRTC rise time[1]	0	5	ms
t_{R_VDD}	VDD rise time[1]	0	5	ms
t_{D_VDD}	Delay between VDDRTC arriving 50% (or 90%) to VDD33 arriving 50% (or 90%)	0	–	ms
t_{R_VDD11}	VDD11 rise time[1]	0	5	ms
t_{D_VDD11}	Delay between VDD arriving 50% (or 90%) to VDD11 arriving 50% (or 90%)	–1	1	ms
t_{R_AVDAUD}	AVDAUD rise time[1]	0	5	ms
t_{D_AVDAUD}	Delay between VDD11 arriving 50% (or 90%) to AVDAUD arriving 50% (or 90%)	0.01	1	ms
t_{R_AVD}	AVD rise time[1]	0	5	ms
t_{D_AVDA}	Delay between VDD arriving 50% to AVD arriving 50%	-1	1	ms
$t_{D\_PPRST\_}$	Delay between VDDAUD stable and PPRST_ deasserted	TBD[3]	–	ms[2]
$t_{D\_VPEFUSE}$	Delay between PPRST_ finished and E-fuse programming power apply	0	–	ms

NOTES:

- The power rise time is defined as 10% to 90%.
- The PPRST_ must be kept at least 100us. After PPRST_ is deasserted, the corresponding chip reset will be extended at least 40ms.
- It must make sure the EXCLK is stable and all power(except AVDEFUSE) is stable.

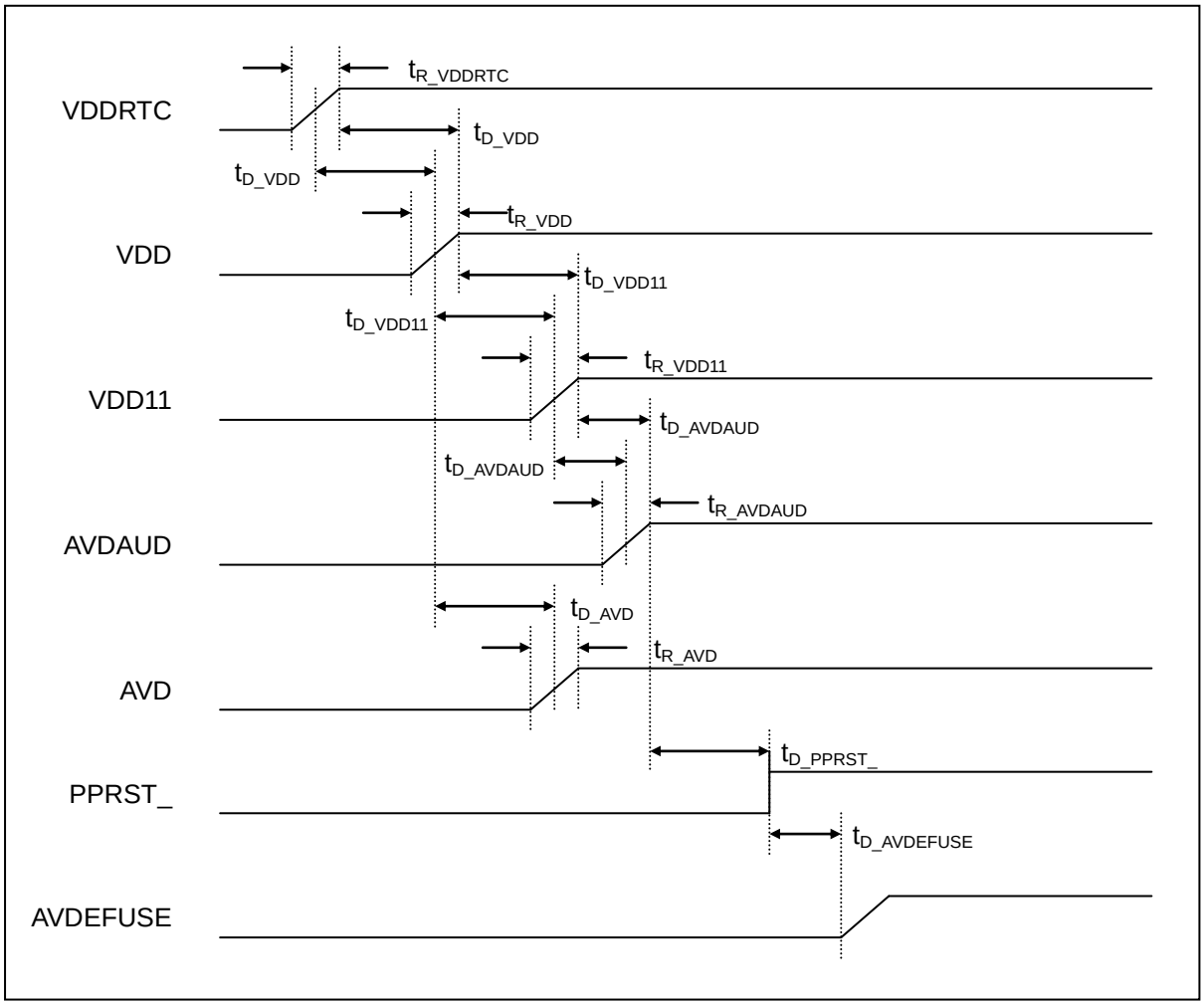


Figure 3-1 Power-On Timing Diagram

3.5.2 Reset procedure

There 3 reset sources: 1 PPRST_ pin reset; 2 WDT timeout reset; and 3 hibernating reset when exiting hibernating mode. After reset, program start from boot.

- PPRST_ pin reset.
  This reset is trigged when PPRST_ pin is put to logic 0. It happens in power on RTC power and RESET-KEY pressed to reset the chip from unknown dead state. The reset end time is about 1M EXCLK cycles after rising edge of PPRST_.
- WDT reset.
  This reset happens in case of WDT timeout. The reset keeps for about a few RTCLK cycles.
- Hibernating reset.
  This reset happens in case of wakeup the main power from power down. The reset keeps for about 1ms ~ 125ms programable, plus 1M EXCLK cycles, start after WKUP_ signal is

recognized.

After reset, all GPIO shared pins are put to GPIO input function and most of their internal pull-up/down resistor are set to on, see “2.5Pin Description [1][2]” for details. The PWRON is output 1. The oscillators are on. The USB 2.0 OTG PHY and USB 1.1 PHY, the audio CODEC DAC/ADC, the SAR-ADCs is put in suspend mode.

3.5.3 BOOT

The boot sequence of the T10 is controlled by boot_sel[1:0]. The configuration is shown as follow:

Table 3-11 Boot Configuration of T10

boot_sel[1:0]	Boot method
00	MMC/SD boot @ MSC0 (MMC/SD use GPIO Port B. MSC1 use GPIO Port C)
01	SFC boot @ CS4 (SPI boot @ SSI0)
10	NOR boot @ CS2 (just for FPGA testing)
11	USB boot @ USB 2.0 device, EXTCLK=24MHz

The boot procedure is showed in the following flow chart:
As shown in boot sequence Block Diagram，After reset, the boot program on the internal boot ROM executes as follows:

1 Disable all interrupts and read boot_sel[1:0] to determine the boot method.
2 There 26KB backup reading failed, the 26KB backup at 128th, 256 th , …, and finally 1024th page will be tried in consecutive order.
3 If it is boot from MMC/SD card at MSC0, its function pins MSC0_D0, MSC0_CLK, MSC0_CMD are initialized, the boot program loads the 26KB code from MMC/SD card to cache and jump to it. Only one data bus which is MSC0_D0 is used.
4 If it is boot from USB, a block of code will be received through USB cable connected with host PC and be stored in cache. Then branch to this area in cache.
5 If it is boot from SPI nor/nand at SFC, its function pins SFC_CLK,SFC_CE, SFC_DR,SFC_DT, SFC_WP,SFC_HOLD are initialized,the boot program loads the 12kB code from SPI NAND/NOR flash to cache and jump to it.
6 If it is boot from NOR Flash, the boot program jump to nor and run directory.

When SFC boot start failure, the program in bootrom will go into SPI boot, AT first the program in bootrom fetch a 16 bytes flag information table(The first 16 bytes in SPL signature) from the SPI device. the program in bootrom check the flag table to decide the SPI address length , SPI device type(SPI_NOR flash or SPI_NAND flash), clk rate, receive code length and the check data. SPI_boot detailed process shown "SPI Boot Procedure". Any irregularity in boot steps, SPI boot will disable SSI controller and jump to MSC0 boot.

When MSC0 boot start failure, the program in bootrom will go into MSC1 boot，If it is boot from MMC/SD card at MSC1, its function pins MSC1_D0, MSC1_CLK, MSC1_CMD are initialized, the boot program loads the 26KB code from MMC/SD card to cache and jump to it. Only one data bus which is MSC1_D0 is used. If MSC1 boot start failure, jump to USB boot.

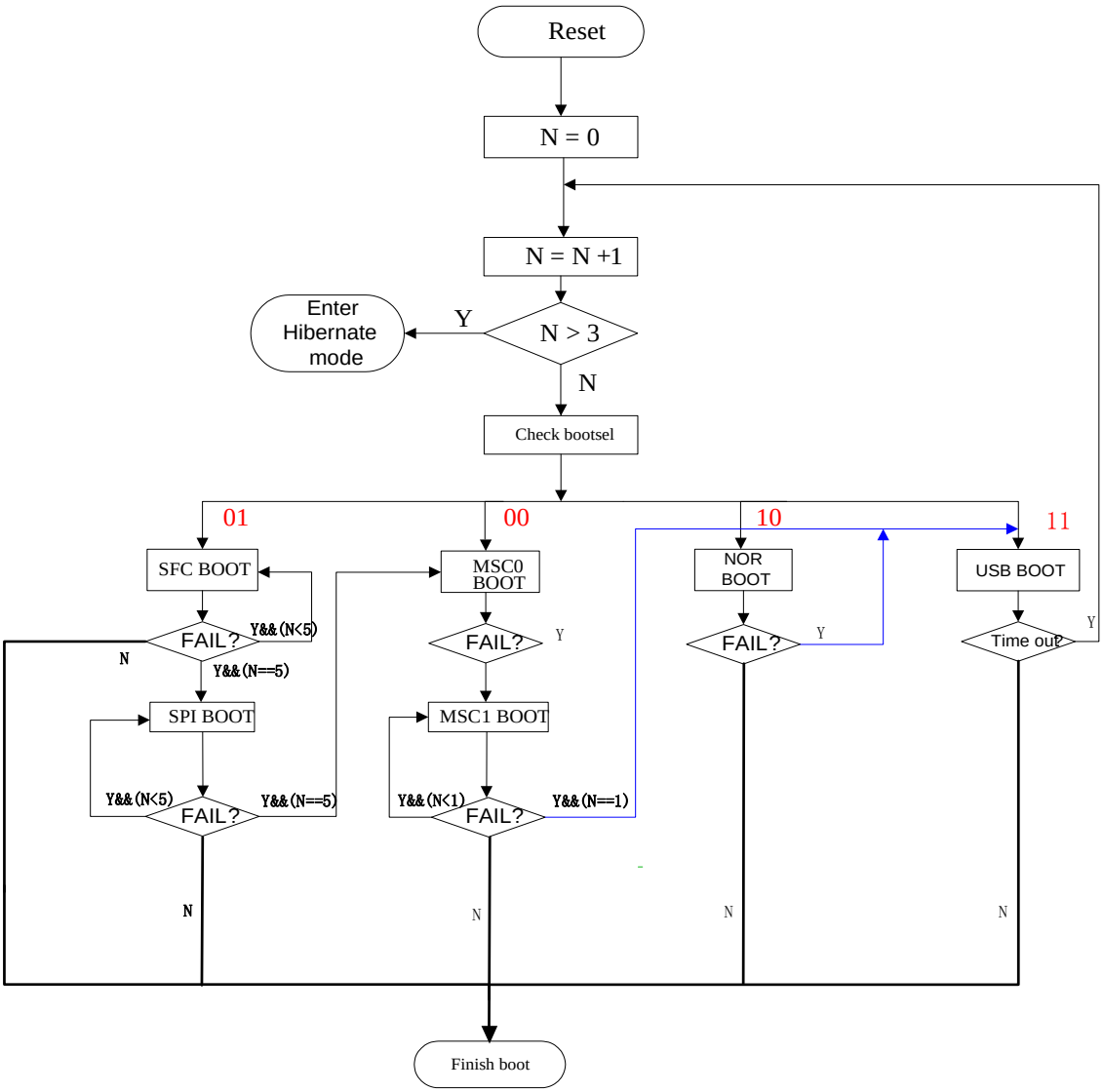


Figure 3-2 Boot sequence diagram of T10