GC4653

1/3” 4Mega CMOS Image Sensor

Datasheet

Beta 1.0

2019-07-12

GENERATION REVISION HISTORY

REV.	*EFFECTIVE DATE*	*DESCRIPTION OF CHANGES*	*AUTHOR*
Beta1.0	*2019-07-12*	*Beta Document Release*	*DSC-AE Dept.*

Galaxycore Incorporation

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Content

1. Sensor Overview

1.1 General Description

GC4653 is a high quality 4Mega CMOS image sensor, for security camera products, digital camera products and mobile phone camera applications. The full-scale integration of high-performance makes the GC4653 fit the design and reduce the implementation process.

GC4653 incorporates a 2560H x 1440V pixel array, on-chip 12/10-bit ADC, and image signal processor. It provides RAW12 and RAW10 data format with MIPI interface. It has a commonly used two-wire serial interface for host to control the operation of the whole sensor.

1.2 Features

- Standard optical format of 1/3 inch
- 2.0μm × 2.0μm BSI pixel
- Output formats: Raw Bayer 12bit/10bit
- Power supply requirement: AVDD28: 2.7~2.9V(Typ2.8V)
  DVDD: 1.15~1.25V(Typ1.2V)
  IOVDD: 1.7~1.9V (Typ1.8V)
- PLL support
- Support for frame sync
- MIPI(2_lane) interface support
- Horizontal/Vertical mirror
- Image processing module
- OTP support (2Kbits total)
- Package: CSP

1.3 Application

- Surveillance Cameras
- Smart Home Systems
- IoT Cameras
- Car Driving Recordes
- Video telephony and conferencing equipment

1.4 Technical Specifications

Parameter	Typical value
Optical Format	1/3 inch
Pixel Size	2.0μm x 2.0μm(BSI)
Active pixel array	2560 x 1440
Shutter type	Electronic rolling shutter
ADC resolution	12/10-bit ADC
Max Frame rate	30fps@full size
Power Supply	AVDD28: 2.8 V DVDD: 1.2V IOVDD: 1.8V
Power Consumption	120mW@30fps
Max Optical lens chief ray angle(CRA)	10 ℃(linear)
Sensitivity	2.4V/Lux.s
Dynamic range	81dB
SNR	38dB
Operating temperature:	-20 ~ 80℃
Stable Image temperature	0~60℃
Package type	41PIN-CSP

2. DC Characteristics

2.1 Power Down Current

Item	Symbol	Min	Typ	Max	Unit
Analog	I_{AVDD}	—	TBD	—	uA
Digital	I_{DVDD}	—	TBD	—	uA
I/O	I_{IOVDD}	—	TBD	—	uA

RST: L, PWND: L
Typ. Analog: 2.8V, Digital: 1.2V, I/O:1.8V, T_j=25℃

2.2 Standby Current

Item	Symbol	Min	Typ	Max	Unit
Analog	I_{AVDD}	—	TBD	—	uA
Digital	I_{DVDD}	—	TBD	—	uA
I/O	I_{IOVDD}	—	TBD	—	uA

Power off, T_j=25℃

2.3 Operation Current

- **Full size (MIPI 2 lane)**

Item	Symbol	Min	Typ	Max	Unit
Analog	I_{AVDD}	—	25	—	mA
Digital	I_{DVDD}	—	33	—	mA
I/O	I_{IOVDD}	—	4	—	mA

INCLK: 27MHz, Frame rate: 30fps, Raw 10

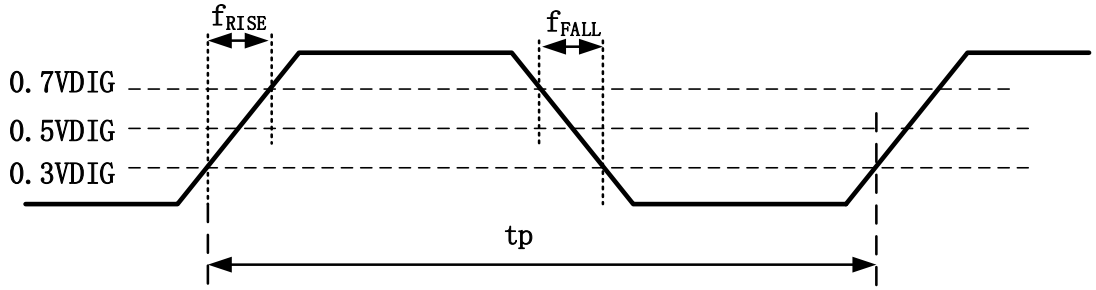
Typ. Analog: 2.8V, Digital: 1.2V, I/O:1.8V, T_j=25

2.4 DC Characteristics

Item	Symbol	Min	Typ	Max	Unit
Power supply	V_{AVDD}	2.7	2.8	3.3	V
	V_{DVDD}	1.15	1.2	1.3	V
	V_{IOVDD}	1.7	1.8	3.3	V
Digital Input(Conditions: AVDD = 2.8V, DVDD = 1.2V, IOVDD = 1.8V)					
Input voltage HIGH	$\mathbf{V_{IH}}$	0.7*VIF			V
Input voltage LOW	$\mathbf{V_{IL}}$			0.3*VIF	V
Digital Output(Conditions: AVDD = 2.8V, IOVDD = 1.8V, standard Loading 25PF)					
Output voltage HIGH	$\mathbf{V_{OH}}$	0.8*VIF			V
Output voltage LOW	$\mathbf{V_{OL}}$			0.2*VIF	V

3. AC Characteristics

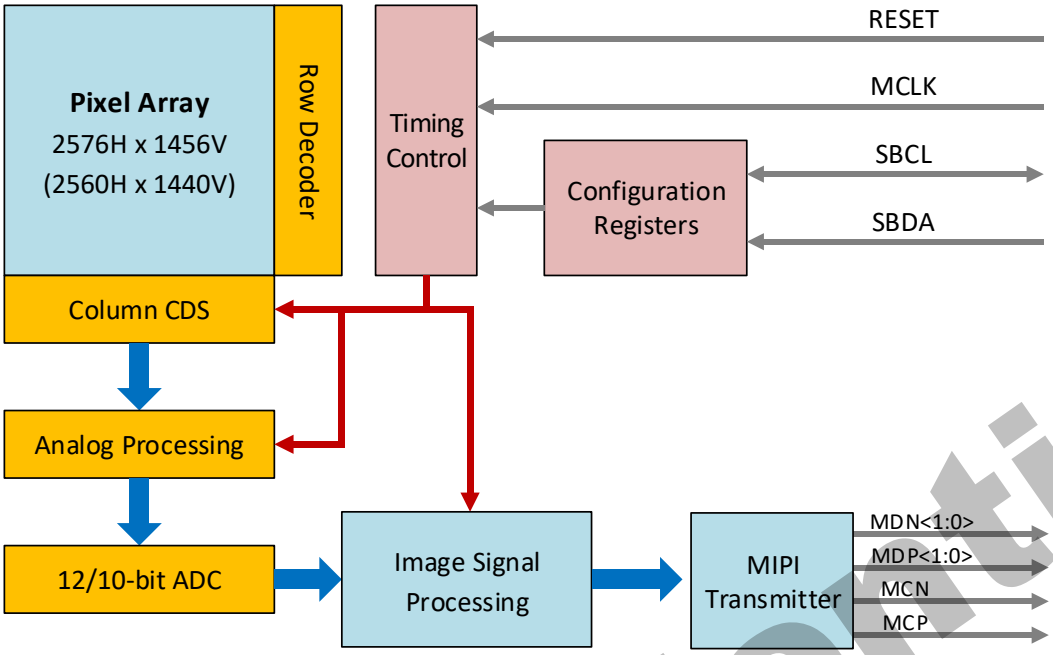
master clock wave diagram



Input clock square waveform specifications：

Item	Symbol	Min.	Typ.	max	unit
Frequency	f_{SCK}	6	27	36	MHz
jitter (period, peak-to-peak)	T_{jitter}			600	ps
Rise Time	f_{RISE}	1		15	ns
Fall Time	f_{FALL}	1		15	ns
Duty Cycle	f_{DUTY}	40		60	%
Input Leakage	f_{ILEAK}	-10		10	μA

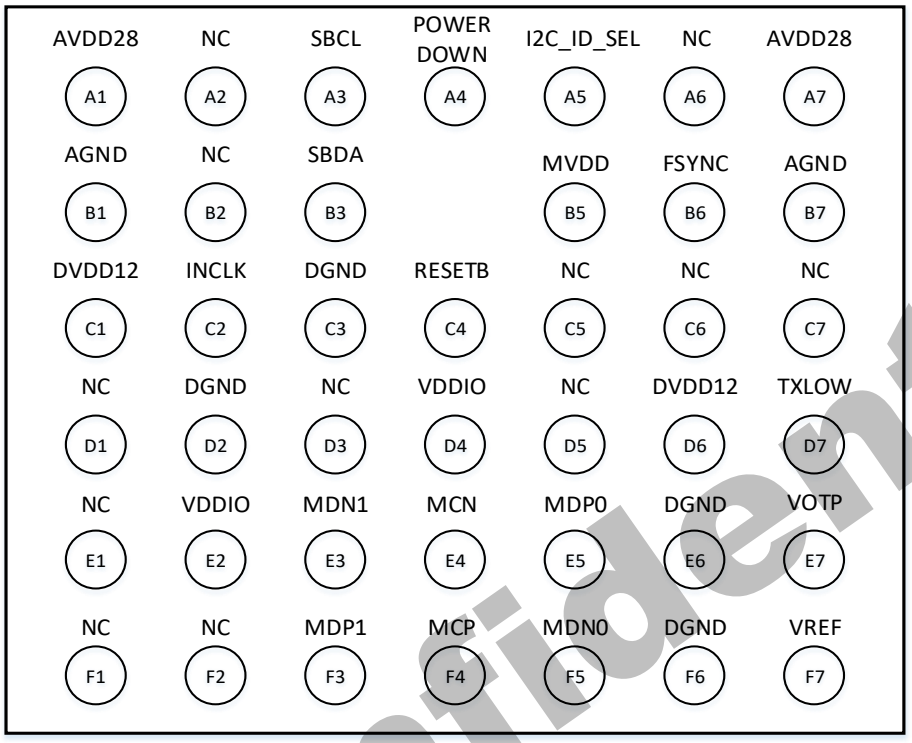
4. Block Diagram



GC4653 has an active image array of 2560x1440 pixels. The active pixels are read-out progressively through column/row driver circuits. In order to reduce fixed pattern noise, CDS circuits are adopted. The analog signal is transferred to digital signal by 12 bit A/D converter. The digital signals are processed in the ISP Block. Users can easily control these functions via two-wire serial interface bus.

5. Chip Information

5.1 Pin Diagram (CSP)



Top View

5.2 Pin Coordinates and Description

Pin	Name	Pin Type	Description
A1	AVDD28	AVDD28	ANALOG POWER
A2	NC	NC	NC
A3	SBCL	Input	Two-wire serial bus, clock
A4	POWERDOWN	Input	Sensor power down control:（floating forbidden） 0: standby 1: normal work
A5	I2C_ID_SEL	Input	ID_SEL（floating forbidden） 0: 0x52/0x53 (default) 1: 0x20/0x21
A6	NC	NC	NC
A7	AVDD28	AVDD28	ANALOG POWER
B1	AGND	Ground	Ground for analog
B2	NC	NC	NC

B3	SBDA	I/O	Two-wire serial bus, data
B4	\	\	\
B5	MVDD	Power	DIGITAL POWER
B6	FSYNC	I/O	Frame sync control
B7	AGND	Ground	Ground for analog
C1	DVDD12	POWER	DIGITAL POWER
C2	INCLK	Input	Sensor input clock
C3	DGND	Ground	Ground for digital
C4	RESETB	Input	Chip reset control:（floating forbidden） 0: chip reset 1: normal work
C5	NC	NC	NC
C6	NC	NC	NC
C7	NC	NC	NC
D1	NC	NC	NC
D2	DGND	Ground	Ground for digital
D3	NC	NC	NC
D4	VDDIO	POWER	I/O POWER.
D5	NC	NC	NC
D6	DVDD12	POWER	DIGITAL POWER
D7	TXLOW	POWER	Internal power supply, please connect 2.2μF capacitor to analog ground..
E1	NC	NC	NC
E2	VDDIO	POWER	I/O POWER.
E3	MDN1	Output	MIPI data <1> (-)
E4	MCN	Output	MIPI clock (-)
E5	MDP0	Output	MIPI data <0> (+)
E6	DGND	Ground	Ground for digital
E7	VOTP	POWER	For OTP power supply
F1	NC		
F2	NC		
F3	MDP1	Output	MIPI data <1> (+)
F4	MCP	Output	MIPI clock (+)
F5	MDN0	Output	MIPI data <0> (-)
F6	DGND	Ground	Ground for digital
F7	VREF	POWER	Internal power supply, please connect 2.2μF capacitor to analog ground.

5.3 Package Specification (unit: mm)

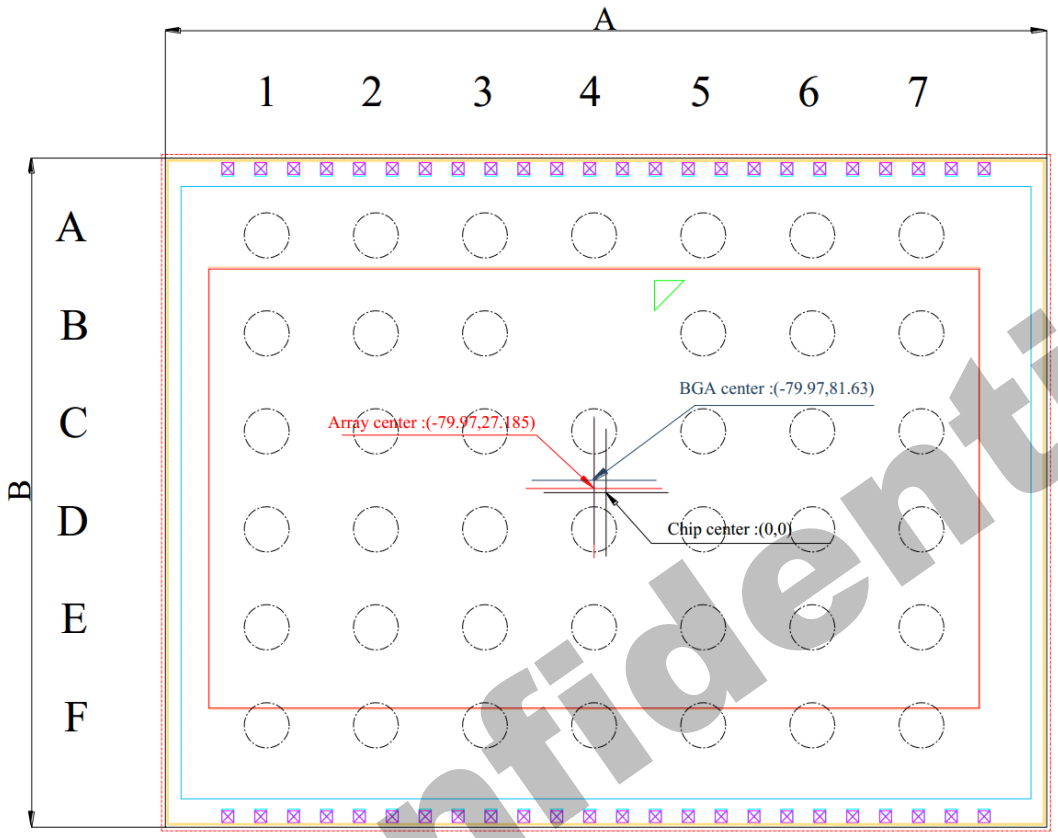


图 3-2 GC4653 封装示意图（Top View Image Side 单位 μm）

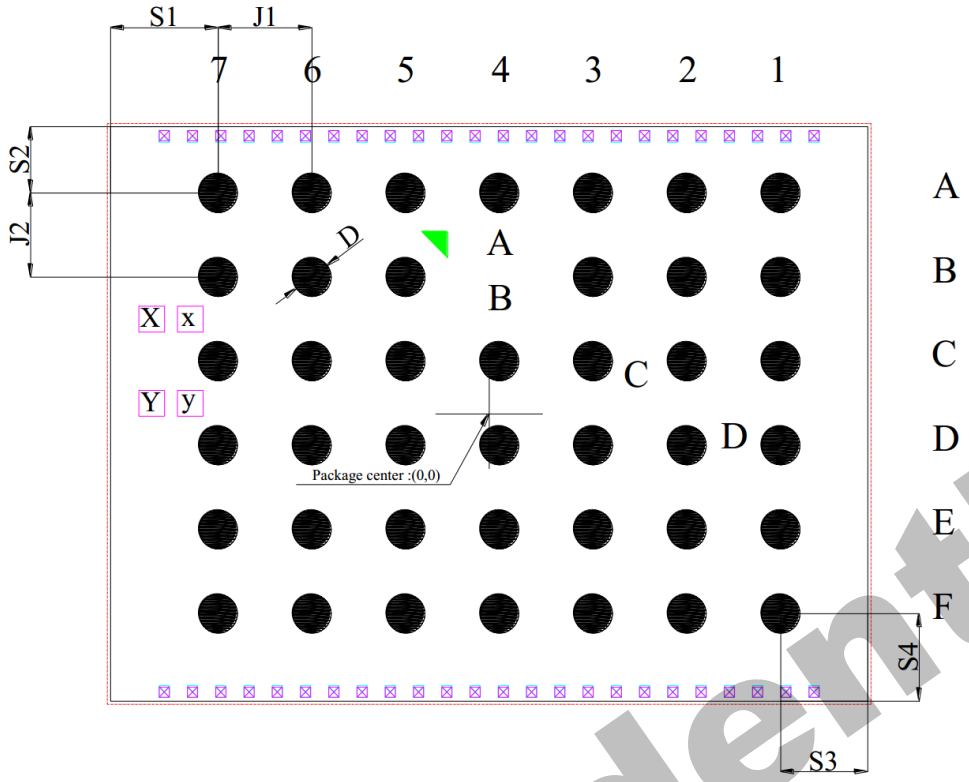


图 3-3 GC4653 封装示意图（Bottom View BGA Side 单位 μm）

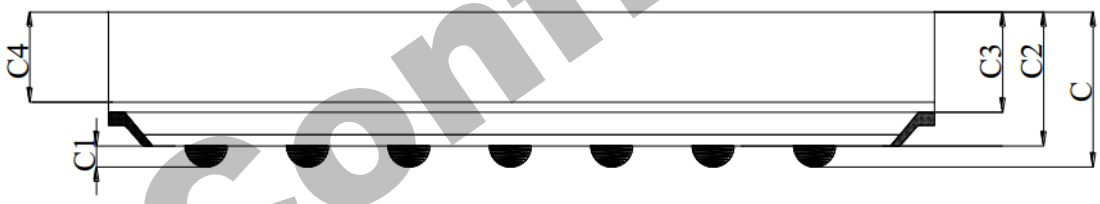


图 3-4 GC4653 封装示意图（Side View）

表 3-2 封装尺寸表

Description	Symbol	Nominal	Min.	Max.
		Millimeters		
Package Body Dimension X	A	5.896	5.871	5.921
Package Body Dimension Y	B	4.438	4.413	4.463
Package Height	C	0.780	0.725	0.835
Ball Height	C1	0.150	0.120	0.180
Package Body Thickness	C2	0.630	0.595	0.665
Thickness from top glass surface to wafer	C3	0.445	0.425	0.465
Glass Thickness	C4	0.400	0.390	0.405
Ball Diameter	D	0.300	0.270	0.310
Total Ball Count	N	41(13NC)		

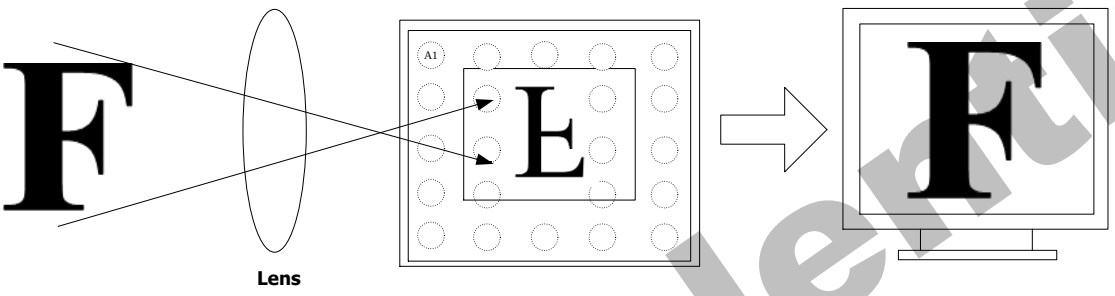
Ball Count X axis	N1	7		
Ball Count Y axis	N2	6		
Pins pitch X axis	J1	0.730		
Pins pitch Y axis	J2	0.650		
BGA ball center to package center offset in X-direction	X	0.07997	0.055	0.105
BGA ball center to package center offset in Y-direction	Y	0.08163	0.057	0.107
BGA ball center to chip center offset in X-direction	X1	0.07997	0.055	0.105
BGA ball center to chip center offset in Y-direction	Y1	0.08163	0.057	0.107
Edge to Pin Center Distance along X	S1	0.83797	0.808	0.868
Edge to Pin Center Distance along Y	S2	0.51237	0.482	0.542
Edge to Pin Center Distance along X’	S3	0.67803	0.648	0.708
Edge to Pin Center Distance along Y’	S4	0.67563	0.646	0.706

注：芯片的封装中心、光学中心及 BGA 中心不是重合的，在 Top View 视角下以封装中心为原点（0, 0），BGA 中心坐标为（-79.97, 81.63），光学中心坐标为（-79.97, 27.185），单位 μm。

6. Optical Specifications

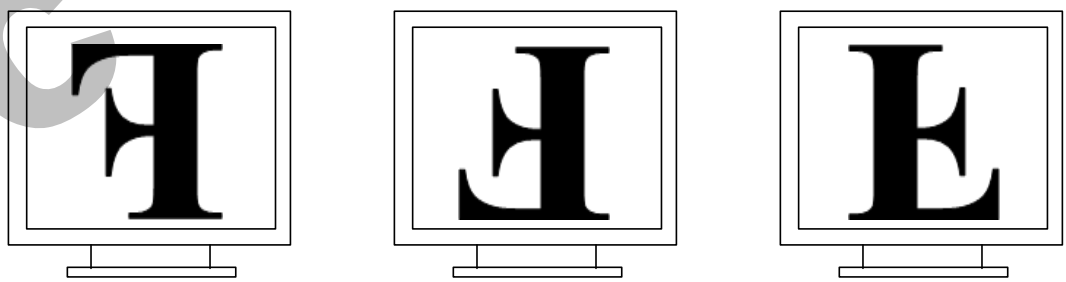
6.1 Readout Position

The GC4653 default status is readout from the lower left corner with pin A1 located in the upper left corner. The image is inverted vertically and horizontally by the lens, so proper image output results when Pin A1 is located in the upper left corner.



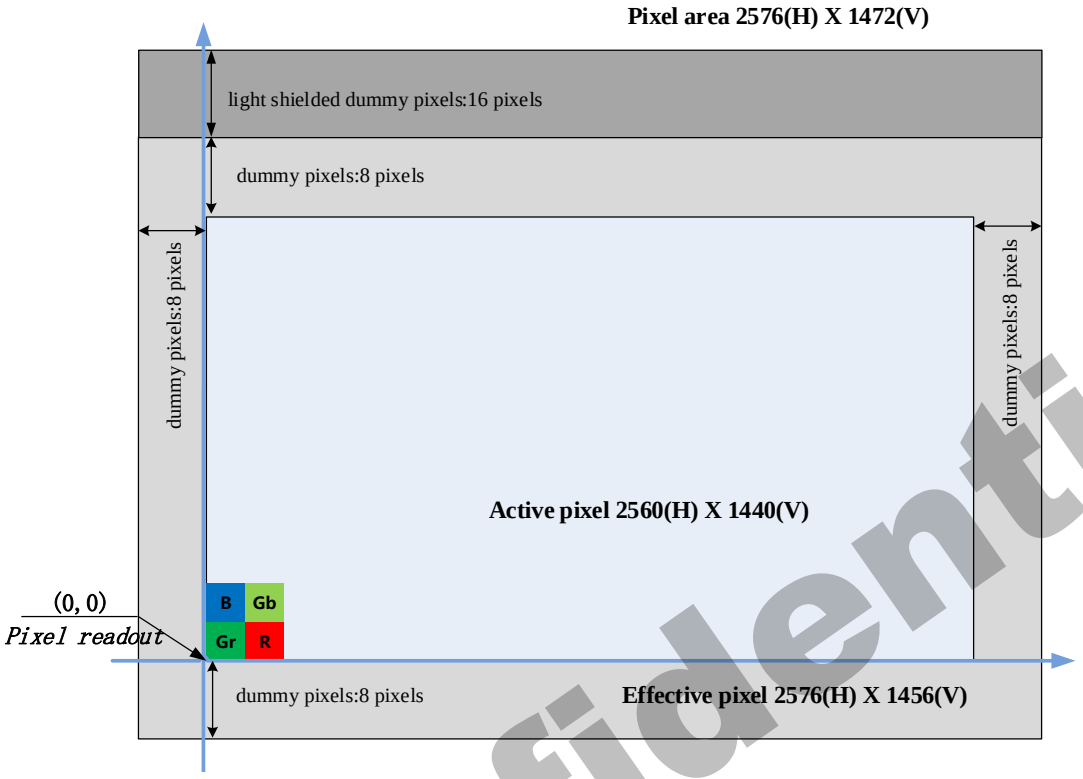
Readout direction can be set by the registers.

Function	Register Address	Register Value	First Pixel
Normal	0x0101[1:0]	00	Gr
Horizontal mirror	0x0101[1:0]	01	R
Vertical Flip	0x0101[1:0]	10	B
Horizontal Mirror and Vertical Flip	0x0101[1:0]	11	Gb



Horizontal Mirror Horizontal Mirror and Vertical Flip Vertical Flip

6.2 Pixel Array



Pixel array is covered by Bayer pattern color filters. The primary color GR/BG array is arranged in line-alternating way.

If no flip in column, column is read out from 0 to 2559. If flip in column, column is read out from 2559 to 0.

If no flip in row, row is read out from 0 to 1439. If flip in row, row is read out from 1439 to 0.

6.3 Lens Chief Ray Angle (CRA)

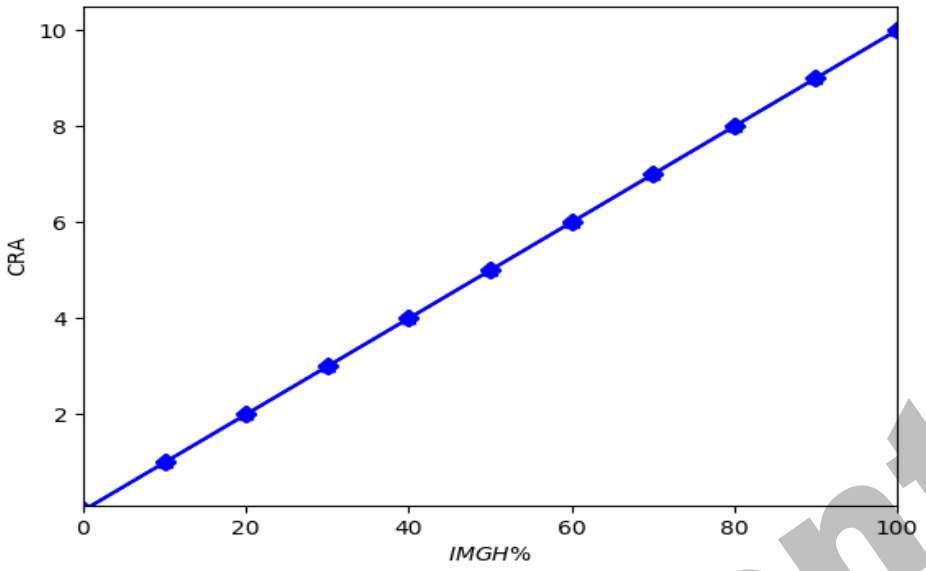


Image Height (%)	Image Height (mm)	CRA (degree)
00	0.000	0.00
10	0.294	1
20	0.587	2
30	0.881	3
40	1.175	4
50	1.469	5
60	1.762	6
70	2.056	7
80	2.350	8
90	2.643	9
100	2.937	10

7. Two-wire Serial Bus Communication

GC4653 Device Address:

ID_SEL	Slave address write mode	Slave address read mode
0(default)	**0x52**	**0x53**
1	**0x20**	**0x21**

7.1 Protocol

The host must perform the role of a communications master and GC4653 acts as either a slave receiver or transmitter. The master must do

- Generate the **Start(S)/Stop(P)** condition
- Provide the serial clock on **SBCL.**

Single Register Writing:

S	52H	A	Register Address [15:8]	A	Register Address [7:0]	A	Data	A	P

Incremental Register Writing:

S	52H	A	Register Address [15:8]	A	Register Address [7:0]	A	Data (1)	A	… …	Data (N)	A	P

Single Register Reading:

S	52H	A	Register Address [15:8]	A	Register Address [7:0]	A	S	53H	A	Data	NA	P

Notes:

From master to slave From slave to master

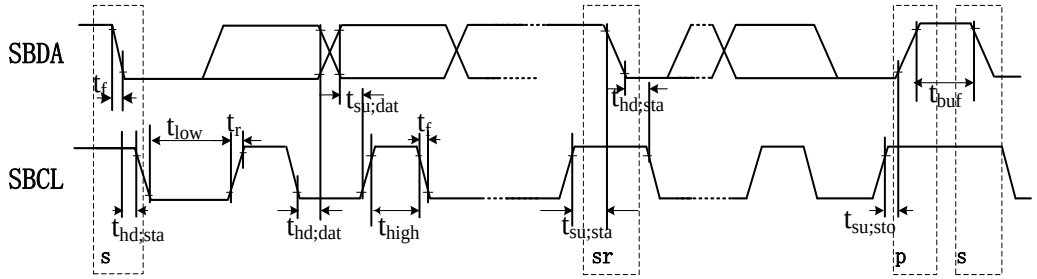
S: Start condition **P:** Stop condition

A: Acknowledge bit **NA:** No acknowledge

Register Address: Sensor register address

Data: Sensor register value

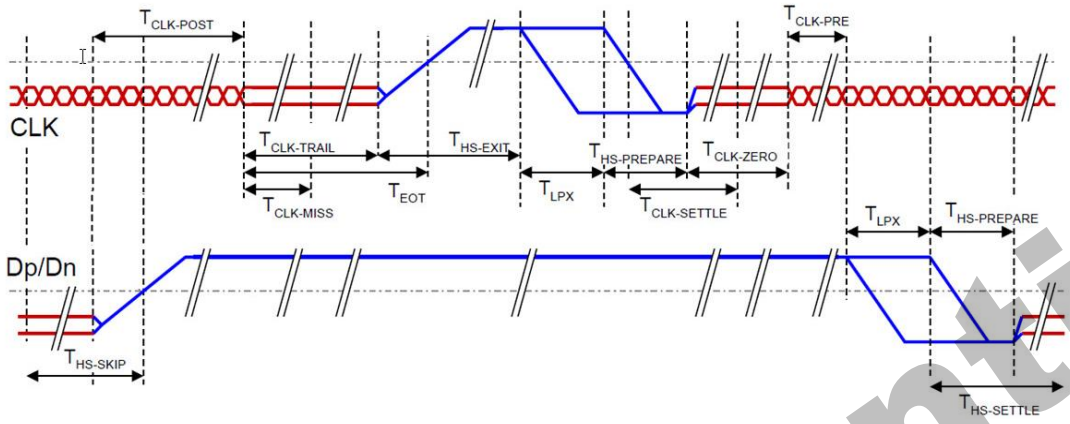
7.2 Serial Bus Timing



Parameter	Symbol	Min.	Typ.	Max.	Unit
SBCL clock frequency	F_{scl}	0	--	400	KHz
Bus free time between a stop and a start	t_{buf}	1.3	--	--	μs
Hold time for a repeated start	$t_{hd;sta}$	0.6	--	--	μs
LOW period of SBCL	t_{low}	1.3	--	--	μs
HIGH period of SBCL	t_{high}	0.6	--	--	μs
Set-up time for a repeated start	$t_{su;sta}$	600	--	--	ns
Data hold time	$t_{hd;dat}$	0	--	900	ns
Data Set-up time	$t_{su;dat}$	100	--	--	ns
Rise time of SBCL, SBDA	t_r	--	--	300	ns
Fall time of SBCL, SBDA	t_f	--	--	300	ns
Set-up time for a stop	$t_{su;sto}$	0.6	--	--	μs
Capacitive load of bus line (SBCL, SBDA)	C_b	--	--	--	pf

8. Applications

8.1 Clock lane low-power



Notice:

- Clock must be reliable during high speed transmission and mode-switching.
- Clock can go to LP only if data lanes are in LP (and nothing relies on it).
- In Low-Power data lanes are conceptually asynchronous (independent of the high speed clock).

$T_{CLK\_HS\_PREPARE}$: setting by Register 0x0122

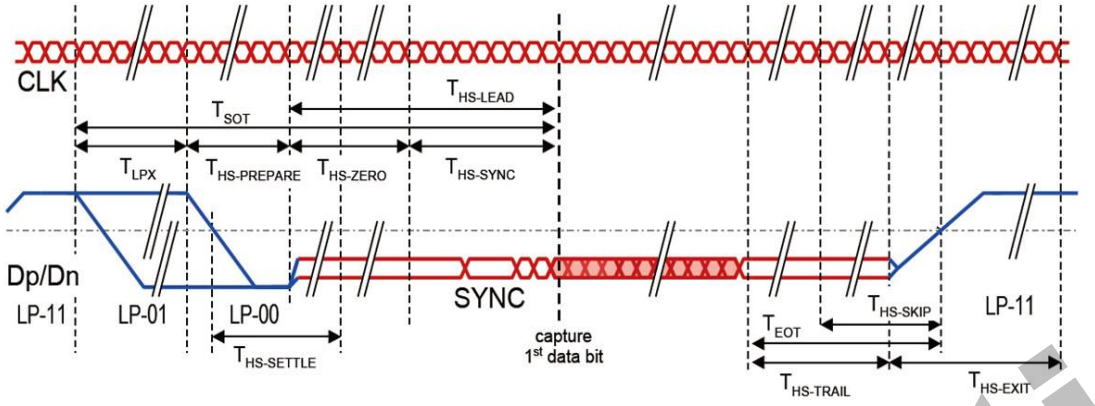
T_{CLK_ZERO}: setting by Register 0x0123

T_{CLK_PRE}: setting by Register 0x0124

T_{CLK_POST}: setting by Register 0x0125

T_{CLK_TRAIL}: setting by Register 0x0126

8.2 Data Burst



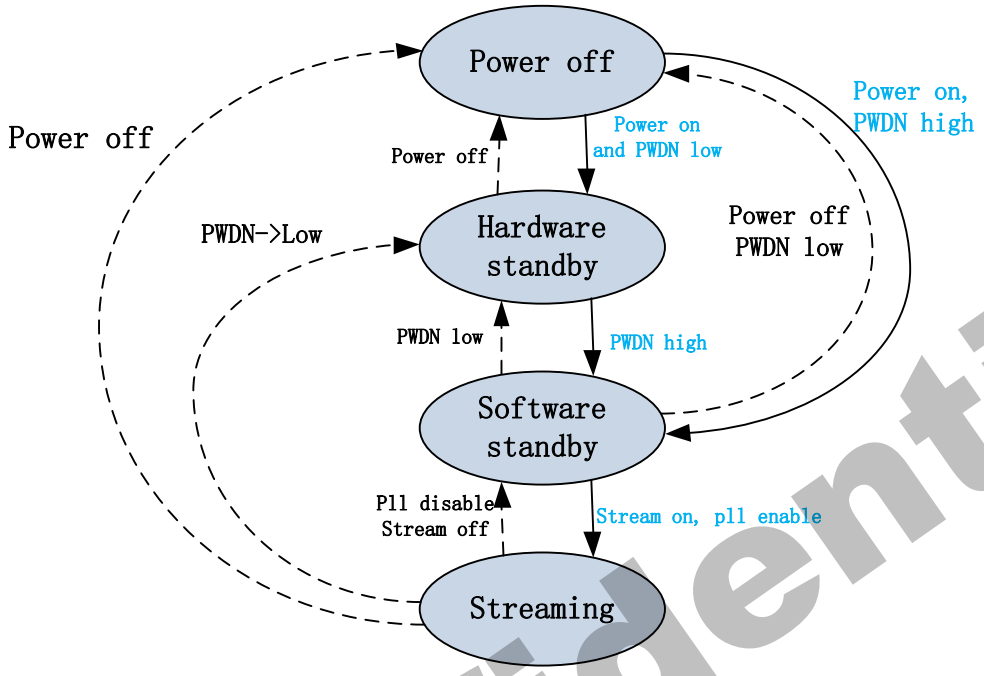
Notice:

- Clock keeps running and samples data lanes (except for lanes in LPS).
- Unambiguous leader and trailer sequences required to distill real bits.
- Trailer is removed inside PHY (a few bytes).
- Time-out to ignore line values during line state transition.

T_{LPX}:	setting by Register	0x0121
$T_{HS\_PREPARE}$:	setting by Register	0x0129
T_{HS_ZERO}:	setting by Register	0x012a
T_{HS_TRAIL}:	setting by Register	0x012b
T_{HS_EXIT}:	setting by Register	0x0127

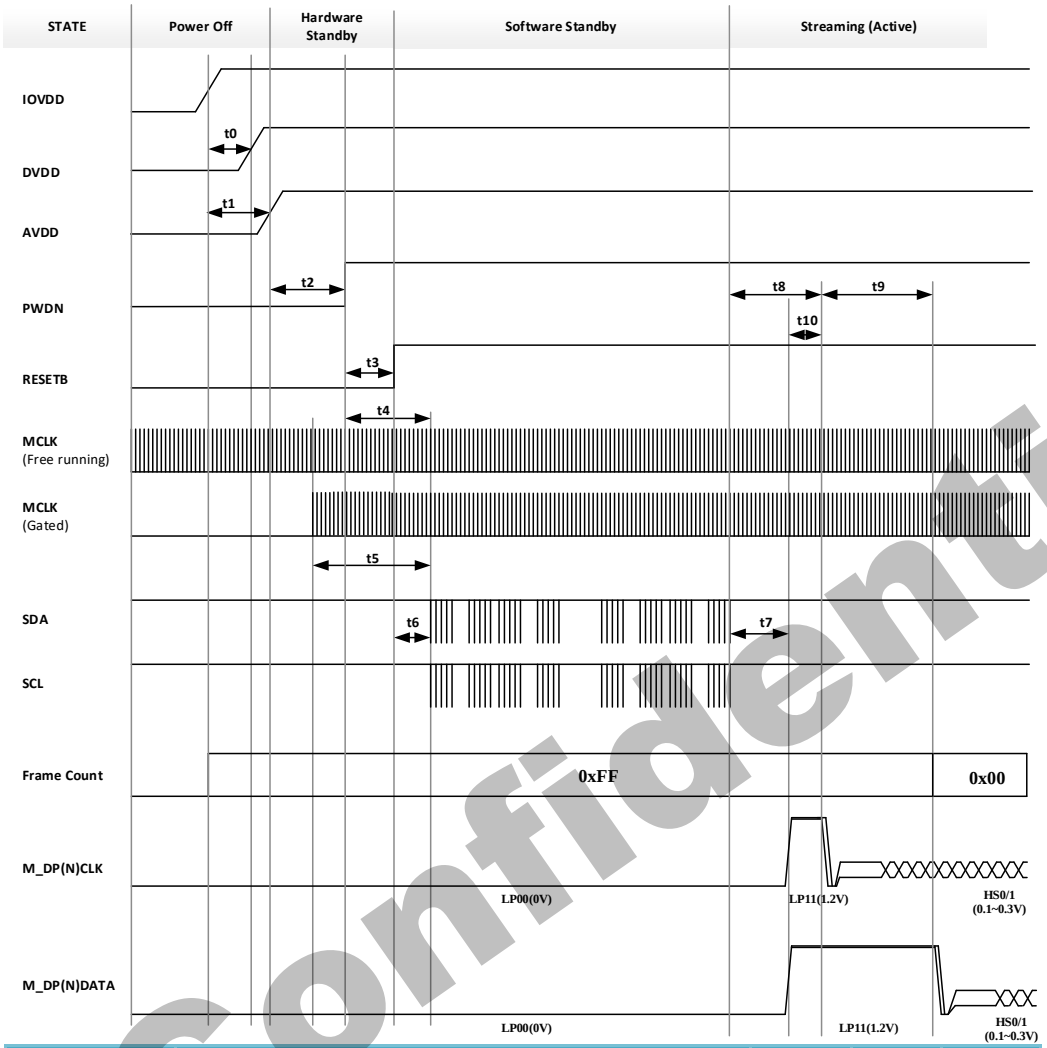
9. Function description

9.1 Operation mode



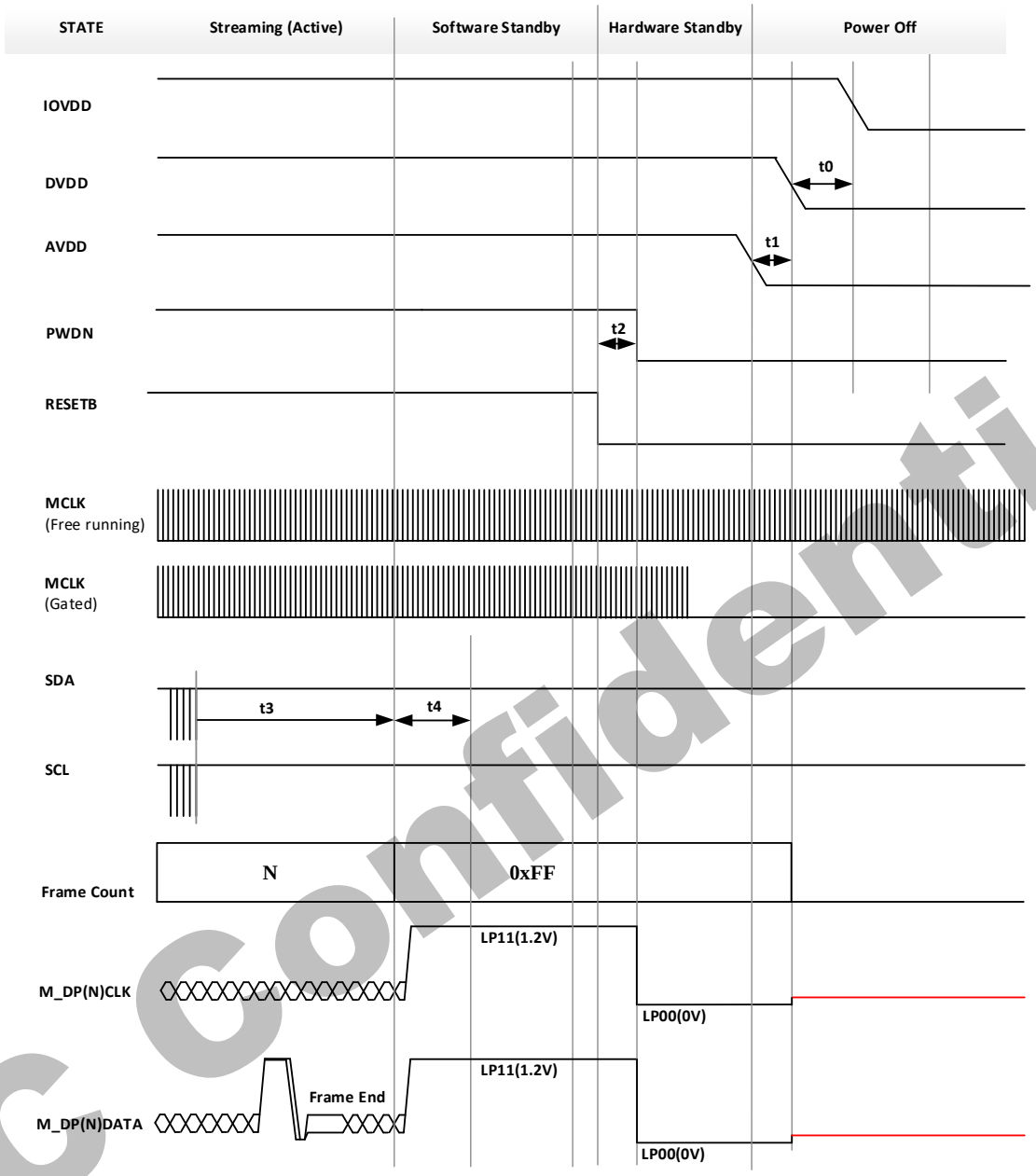
Power state	Description	Activate
Power off	Power supplies are turned off	None
Hardware standby	No communication with sensor, low level on PWDN and RESETB, and stop MCLK	PWDN low
Software standby	Two- wire serial communication with sensor, pll is ready for fast return to streaming mode	Stream mode off PLL disable RESETB high PWDN high
Streaming	Sensor is fully powered and is streaming image data on the MIPI CSI-2 bus	All

9.2 Power on Sequence



Parameter	Description	Min.	Max.	Unit
t0	From IOVDD to DVDD12	50	-	µs
t1	From IOVDD to AVDD28	50	-	µs
t2	From AVDD28 to PWDN pull high	0	-	µs
t3	From PWDN pull high to RESETB pull high	0	-	µs
t4	PWDN rising to first I2C transaction	50	-	µs
t5	Minimum No. of MCLK cycles prior to the first I2C transaction	1200	-	MCLK
t6	From RESETB rising to first I2C transaction	50	-	µs
t7	PLL start up/lock time	-	1	ms
t8	Entering streaming mode – First frame start sequence (fixed part)		10	ms
t9	Entering streaming mode – First frame start sequence (variable part)	-		lines
t10	DPHY initialization period (TINIT)	0.1	-	ms

9.3 Power off Sequence



Parameter	Description	Min.	Max.	Unit
t0	From DVDD12 pull down to IOVDD pull down	0	-	μs
t1	From AVDD28 pull down to DVDD12 pull down	0	-	μs
t2	From RESETB pull low to PWDN pull low	0	-	μs
t3	Enter Software Standby CCI command – Device in Software Standby mode	0	-	μs
t4	Minimum number of MCLK cycles after the last CCI transaction or MIPI frame end code.	2000		MCLK

➢ Recommended power on/off sequence is above.

- If the sensor's power cannot be cut off, please keep power supply, then set PWDN pin low. It will make sensor standby
- Register should be reloaded before works.
- If the standby sequence needs to be modified, please contact FAE of *Galaxycore Inc.*

9.4 Black level calibration

Black level is caused by pixel characteristics and analog channel offset, which makes poor image quality in dark condition and color balance, to reduce these, sensor automatically calibrates the black level every frame with light shield pixel array.

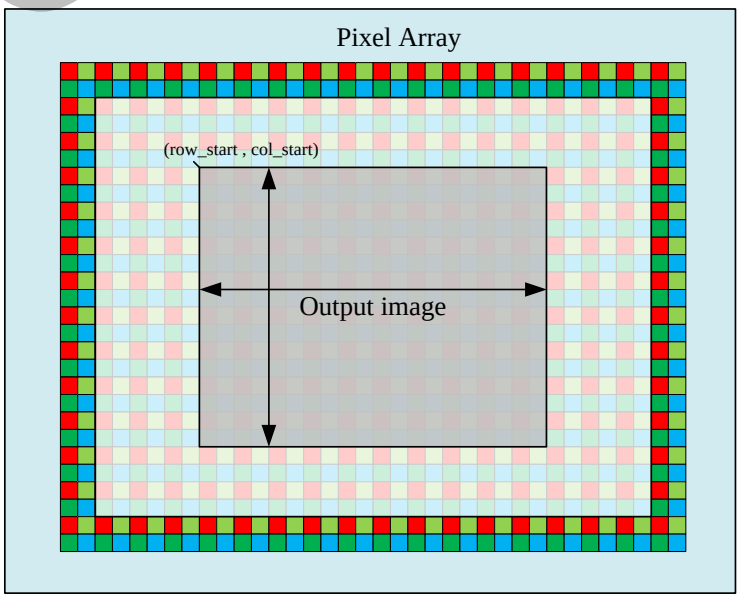
9.5 Integration time

The integration time is controlled by the integration time registers

Addr.	Register name	Description
0x0202	Shutter time	[5:0] shutter time[13:8]
0x0203		[7:0] shutter time[7:0]
0x0340	Frame length	[5:0] frame length[13:8]
0x0341		[7:0] frame length[7:0]

9.6 Windowing

GC4653 has a rectangular pixel array 2560 x 1440, it can be windowed by output size control, the output image windowing can be used to adjust output size, and it will affect field angle.

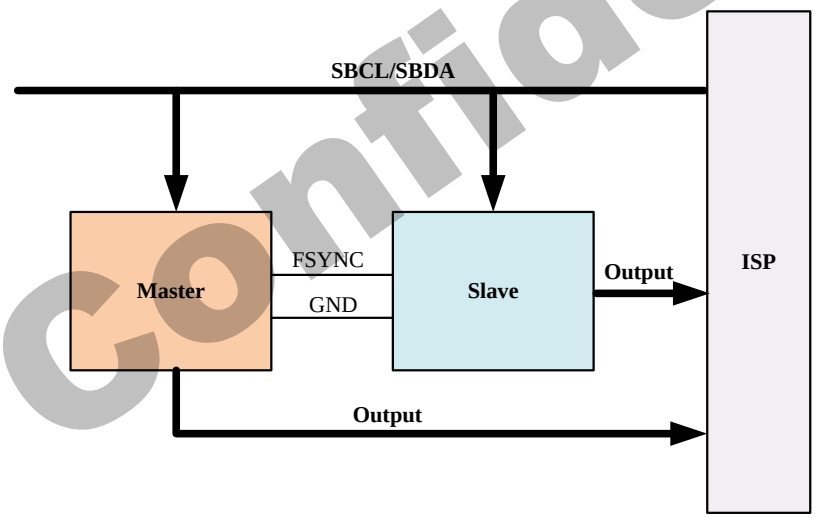


Output window array control

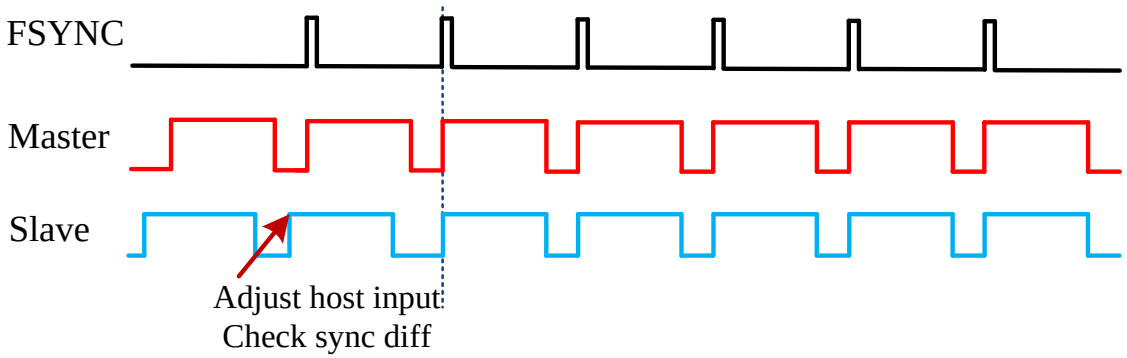
Addr.	Register name	Description
0x0351	Row start	[2:0] Out_window_y1[10:8]
0x0352		[7:0] Out_window_y1[7:0]
0x0353	Col start	[3:0] Out_window_x1[11:8]
0x0354		[7:0] Out_window_x1[7:0]
0x034e	window height	[3:0] Out window height[11:8]
0x034f		[7:0] Out window height[7:0]
0x034c	window width	[3:0] Out window width[11:8]
0x034d		[7:0] Out window width[7:0]

9.7 Frame sync mode

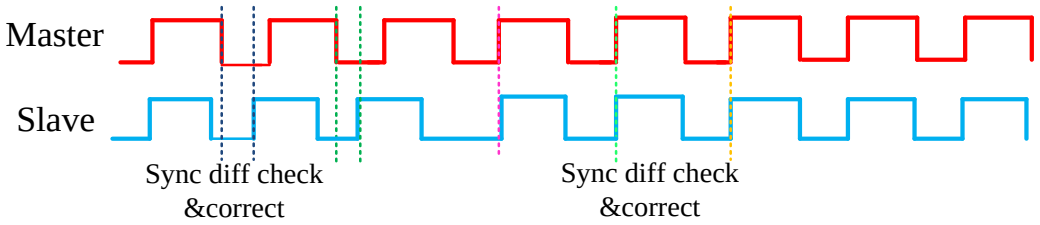
GC4653 can support hardware frame sync for dual camera application. It can be set both master and slave sensor. When use this mode, the two sensor's FSYNC pin must connect to each other.



Adjust mismatch sync



Dynamic mismatch sync control



Addr.	Register name	Description
0x027f	fsync_mode	[4]fsync_clear_counter [3]clock en [1]1 master or 0 slave [0]fsync_en
0x0282	fsync_mode_new2	[3] row count mode
0x0283	fsync_mode_new3	[7] gpio_value (gpio_mode on) or Fsync_diff_always_mode (gpio_mode off) [6:0] fsync out position
0x0284	Fsync row time	[7] position_FS_D [3] position_FS_A [2] position_FE_D [1] fsync_out_polarity [0] fsync_in_polarity
0x0285	fsync_mode_new4	[6] first vb clear [5] fsync_row_diff_mode
0x0286	fsync_row_diff_th	[5:0] fsync_row_diff_th
0x0287	Debug_mode4	[5:4] fsync_vb_gap
0x0288	fsync_row_diff_big[13:8]	[5:0] fsync_row_diff_big[13:8]
0x0289	fsync_row_diff_big [7:0]	[7:0] fsync_row_diff_big [7:0]
0x028a	fsync_row_diff_big2[13:8]	[5:0] fsync_row_diff_big2[13:8]
0x028b	fsync_row_diff_big2 [7:0]	[7:0] fsync_row_diff_big2[7:0]

9.8 OTP memory

GC4653 sensor has 2K bits embedded OTP(One Time Programmable) memory.

9.9 Frame structure

Frame structure is controlled by HB, frame length, window start, window height, window width and VB.

Frame length control

Frame length are controlled by window height, minimum VB and shutter time.

- Frame length depend shutter time.
- Minimum frame length = window height + 32 +VB (VB_min = 8)e
- If shutter time < minimum frame length:

  Actual frame length = minimum frame length
- If shutter time > minimum frame length:

  Actual frame length = shutter time + 32.

- Fix frame rate
- User can fix frame length or VB to fix frame rate.

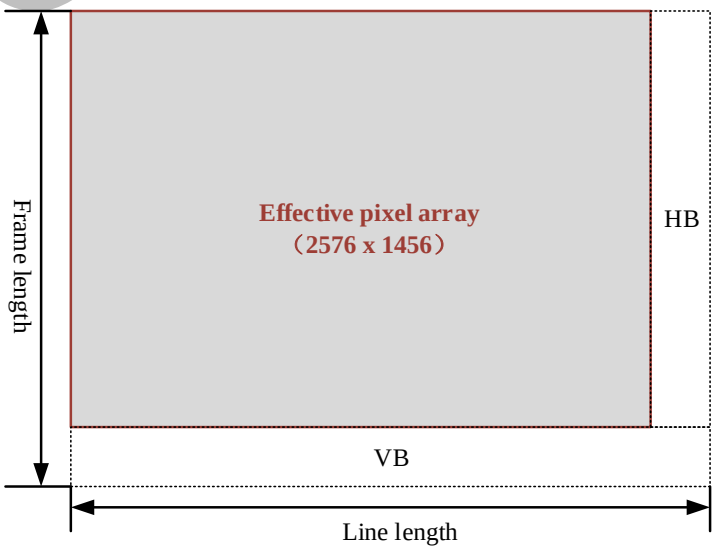
Line length control

Line length control for internal set, and not recommended to be modified.

Addr.	Register name	Description	
0x0342	Line length	[3:0] Line length[11:8]	X2
0x0343		[7:0] Line length[7:0]	X2

Blank time control

1. line blank time is controlled by HB
2. frame blank time
   - frame blank time = frame length lines – window height – 32



10. Register List

System Register

Address	Name	Width	Default Value	Description
0x03f0	Sensor_ID_high	8	0x46	Sensor_ID
0x03f1	Sensor_ID_low	8	0x53	Sensor_ID
0X033E	line_length[7:0]	8	0X94	Line_length
0X033F	line_length[15:8]	8	0X05	
0X0340	Framelength[13:8]	6	0X07	
0X0341	Framelength[7:0]	8	0X0D	
0X0342	CISCTL_hb[13:8]	6	0X02	
0X0343	CISCTL_hb[7:0]	8	0XCA	
0X0344	CISCTL_col_start[11:8]	4	0X00	
0X0345	CISCTL_col_start[7:0]	8	0X00	
0X0346	CISCTL_row_start[10:8]	3	0X02	
0X0347	CISCTL_row_start[7:0]	8	0X00	
0X0348	CISCTL_win_width[11:8]	4	0X0A	
0X0349	CISCTL_win_width[7:0]	8	0X10	
0X034A	CISCTL_win_height[10:8]	3	0X05	
0X034B	CISCTL_win_height[7:0]	8	0XC0	
0X034C	out_win_width[11:8]	4	0X0A	
0X034D	out_win_width[7:0]	8	0X00	
0X034E	out_win_height[11:8]	4	0X05	
0X034F	out_win_height[7:0]	8	0XA0	
0X0350	win_mode	1	0X01	
0X0351	out_win_y1[10:8]	3	0X00	
0X0352	out_win_y1[7:0]	8	0X00	
0X0353	out_win_x1[11:8]	4	0X00	
0X0354	out_win_x1[7:0]	8	0X00	

Analog & CISCTL

Address	Name	Width	Default Value	Description
0x0202	Exposure[13:8]	6	0x00	
0x0203	Exposure[7:0]	8	0x10	
0x020e	Auto_pregain[9:6]	4	0x01	

0x020f	Auto_pregain[5:0]	6	0x00	
0X02b3	ANALOG_PGA_gain[7:0]	8	0x00	
0X02b4	ANALOG_PGA_gain[10:8]	3	0x00	
0X02b8	col_gain[13:6]	8	0x01	
0X02b9	col_gain[5:0]	6	0x00	

CSI/PHY1.0

Address	Name	Width	Default Value	Description
0x0100		4	0x00	[3] Lane_ena [2] ULP_ena [1] line_sync_mode [0] mipi_ena
0x0101	Image_Orientation	2	0x00	[1] updown [0] mirror
0x0103	fifo_prog_full_level1[9:8] fifo_prog_full_level2[9:8]	4	0x00	[3:2] fifo_prog_full_level1[9:8] [1:0] fifo_prog_full_level2[9:8]
0x0104	fifo_prog_full_level1[7:0]	8	0x10	[7:0] fifo_prog_full_level1
0x0105	fifo_prog_full_level2[7:0]	4	0x10	[7:0] fifo_prog_full_level2
0x0106	FIFO_mode	8	0x38	[7] sram_test_mode [6] fifo_rst_mode [5] fifo1_cs_en [4] fifo2_cs_en [3] SPI_gate_SRAM [2] fifo1_clk_gate_mode [1] fifo2_wr_gate_mode [0] fifo2_rd_gate_mode
0x0107	CSI2_mode2	8	0x09	[7] virtual channel en [6] mipi input test data en [5] mipi write gate en [4] mipi hb ctl en [3:2] vc3_id [1:0] vc2_id
0x0108	CSI2_mode3	8	0x04	[3] CSO2_mode_updata_mode [2] mipi_set_auto_en [1:0] switch mode
0x010d	LWC_set[7:0]	8	0x80	
0x010e	LWC_set[15:8]	8	0x0c	Raw10：2560x5/4 must be 2x
0x010f	SYNC_set	8	0xb8	SYNC_set
0x0110	LDI_set_dummy	8	0x32	Used for first dummy line 0x31 –raw8

				0x32 –raw10 0x33 –raw12
0x0111	LP_set	8	0x2b	RAW10
0x0112	Mipi_raw_mode[15:8]	8	0x0a	0x0808 RAW8 0x0a0a RAW10 0x0a08 COMP10_8
0x0113	Mipi_raw_mode[7:0]	8	0x0a	
0x0114	Mipi_lane_num	2	0x03	00:1lane 01:2lane 10:3lane 11:4lane
0x0115	DPHY_mode	8	0x10	[7] mipi para invar when div2 [6] DATA lane gate [5] all_lane_open_mode [4:2] switch_msb_mode [1:0] clklane_mode
0x0116	LP_set	8	0x29	[7:6] hi-z [5:4] use define [3:2] 1 [1:0] 0
0x011b	fifo2_prog_full_level	6	0x0c	[5:0] fifo2_prog_full_level
0x011c	fifo2_push_prog_full_level	6	0x10	[5:0] fifo2_push_prog_full_level
0x011d	Sram_test_mode	8	0x02	[6] raw14 compress [5] compress_predict_out_mode [4] compress_mode [3] cen [2] RF1 gata [1] RF1 gate [0]sram test
0x011f		4	--	[3] fifo 1_error_valid [2] fifo 1_full_valid [1] fifo_pop_error_valid [0] fifo_push_error_valid
0x0120	T_init_set	8	0x80	more than 100 us
0x0121	T_LPX_set	8	0x10	more than 50ns
0x0122	T_CLK_HS_PREPARE_set	8	0x05	38ns ~95ns LP00
0x0123	T_CLK_zero_set	8	0x20	more than 300ns
0x0124	T_CLK_PRE_set	8	0x02	more than 8UI
0x0125	T_CLK_POST_set	8	0x20	60ns +52UI
0x0126	T_CLK_TRAIL_set	8	0x08	60ns
0x0127	T_HS_exit_set	8	0x10	more than 100ns
0x0128	T_wakeup_set	8	0xa0	1 ms

0x0129	T_HS_PREPARE_set	8	0x06	45+4UI ~85+5UI
0x012a	T_HS_Zero_set	8	0x0a	140ns
0x012b	T_HS_TRAIL_set	8	0x08	60ns
0x012d	mp_reserve	4	0x00	60ns
0x0130	MIPI_Test	8	0x00	[2] line_sync_mode_patch [1] mipi_test_clk_mode [0] mipi_test
0x0136	Initial period	2	0x00	[1] initial_en [0] period_en
0x0137	Initial_time[7:0]	8	0xff	initial_time
0x0138	Initial_time[15:8]	8	0x0f	
0x0139	Period_time	8	0x7f	
0x013a	Period_start_time	8	0xfe	can not be 8'hff
0x013b	prbs_mode	8	0x20	[6] prbs11 [5] prbs_9 [4] clane prbs en [3] dlane3 prbs en [2] dlane2 prbs en [1] dlane1 prbs en [0] dlane0 prbs en
0x013c	prbs_seed[7:0]	8	0x9a	prbs_seed[7:0]
0x013d	prbs_seed[15:8]	8	0x78	prbs_seed[15:8]
0x013e	prbs_LDI	8	0x3d	
0x014c	MIPI_TSEL	2	0x01	
0x0180	DPHY_analog_mode1	8	0x06	[6] mipi_en [5:4] disable_set [3:0] mipi_diff
0x0181	DPHY_analog_mode2	8	0x00	[7] dphy_data3_en [6] dphy_data2_en [5] dphy_data1_en [4] dphy_data0_en [3] data3delay1s [2] data2delay1s [1] data1delay1s [0] data0delay1s
0x0182	DPHY_analog_mode3	8	0x00	[7:6] data3lp_drv_10 [5:4] data2lp_drv_10 [3:2] data1lp_drv_10 [1:0] data0lp_drv_10
0x0183	DPHY_analog_mode4	8	0x55	[7:6] data3ctr [5:4] data2ctr [3:2] data1ctr

				[1:0] data0ctr
0x0184	DPHY_analog_mode5	8	0xaa	[7:6] dat3hs_ph [5:4] dat2hs_ph [3:2] dat1hs_ph [1:0] dat0hs_ph
0x0185	DPHY_analog_mode6	8	0x00	[7] data3lp_drv_2 [6] data2lp_drv_2 [5] data1lp_drv_2 [4] data0lp_drv_2 [3] clkip_drv_2 [2:1] NA [0] dphy_clk_en
0x0186	DPHY_analog_mode7	8	0x63	[7:6] clkctr [5:4] clkhs_ph [3:2] clklp_drv_10 [1] clklane_p2s_sel NA clkp2s_en [0] clkdelay1s