GC2083 CSP

1/3.02’’2Mega CMOS Image Sensor

Data Sheet

Preliminary

V0.2

2021-11-22

Ordering Information

◆ **GC2083-C51YA**

(Colored, 50PIN-CSP)

GENERATION REVISION HISTORY

REV.	EFFECTIVEDATE	DESCRIPTION OFCHANGES	PREPARED BY
V0.0	*2020-10-28*	*Document Release*	*DSC-AE Dept.*
V0.1	*2021-11-22*	*Update P10 pin diagram;P13 package specification;P23 operation mpde*	*DSC-AE Dept.*
V0.2	*2022-01-20*	*Update P2 Ordering Information*	*DSC-AE Dept.*

Galaxycore Incorporation

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Content

1. Sensor Overview

1.1 General Description

GC2083 is a high quality 1080P CMOS image sensor, for security camera products, digital camera products and mobile phone camera applications. GC2083 incorporates a 1920H x 1080V pixel array, on-chip 10-bit ADC, and image signal processor.

The full scale integration of high-performance and low-power functions makes the GC2083 best fit the design, reduce implementation process, and extend the battery life of Motion Camera, Car DVR, and a wide variety of mobile applications.

It provides RAW10 and RAW8 data formats with MIPI and DVP interface. It has a commonly used two-wire serial interface for host to control the operation of the whole sensor.

1.2 Features

- Standard optical format of 1/3.02 inch
- 2.7μm*2.7μm
- Output formats: Raw Bayer 10bit/8bit
- Power supply requirement: AVDD28: 2.7~2.9V(Typ.2.8V)
  DVDD12: Generated by the internal LDO(Typ.1.2V)
  IOVDD: 1.7~1.9V(Typ.1.8V)
- PLL support
- Support frame sync
- DVP /MIPI (2lane) interface support
- Horizontal/Vertical mirror
- Image processing module
- Package: CSP

1.3 Application

- Security cameras
- Automotive
- Cellular Phone Cameras
- Digital still cameras and camcorders
- Video telephony and conferencing equipment

1.4 Technical Specifications

Parameter	Typical value
Optical Format	1/3.02inch
Pixel Size	2.7μm×2.7μm
Active pixel array	1920×1080
Shutter type	Electronic rolling shutter
ADC resolution	10 bit ADC
Max Frame rate	30fps@full size
Power Supply	AVDD28: 2.8V DVDD12: Generated by the internal LDO IOVDD: 1.8V
Power Consumption	TBD
MAX SNR	37dB
Dark Current	TBD
Sensitivity	3.24v/lux.s
Dynamic range	74 dB
Operating temperature:	-30~85℃
Stable Image temperature	-20~60℃
Storage temperature	-40~125℃
Optimal lens chief ray angle(CRA)	12°(linear)
Package type	CSP
Input clock frequency	6~36MHz

2. DC Parameters

2.1 Standby Current

Item	Symbol	Min	Typ	Max	Unit
Analog	I_{AVDD}	—	TBD	—	mA
I/O	I_{IOVDD}	—	TBD	—	mA

XSHUTDOWN : L
Typ. Analog: 2.8V, Digital: 1.2V, I/O:1.8V, T_j=25℃

2.2 Power off Current

Item	Symbol	Min	Typ	Max	Unit
Analog	I_{AVDD}	—	0	0	mA
I/O	I_{IOVDD}	—	0	0	mA

Power off, T_j=25℃

2.3 Operation current

Full size (DVP)

Item	Symbol	Min	Typ	Max	Unit
Analog	I_{AVDD}	—	TBD	—	mA
I/O	I_{IOVDD}	—	TBD	—	mA

Input clock: 27MHz, Frame rate: 30FPS, RAW 10,

Typ. Analog: 2.8V, Digital: 1.2V, I/O:1.8V, T_j=25℃

Full size (MIPI 2 Lane)

Item	Symbol	Min	Typ	Max	Unit
Analog	I_{AVDD}	—	TBD	—	mA
I/O	I_{IOVDD}	—	TBD	—	mA

Input clock: 27MHz, Frame rate: 30FPS, RAW 10,

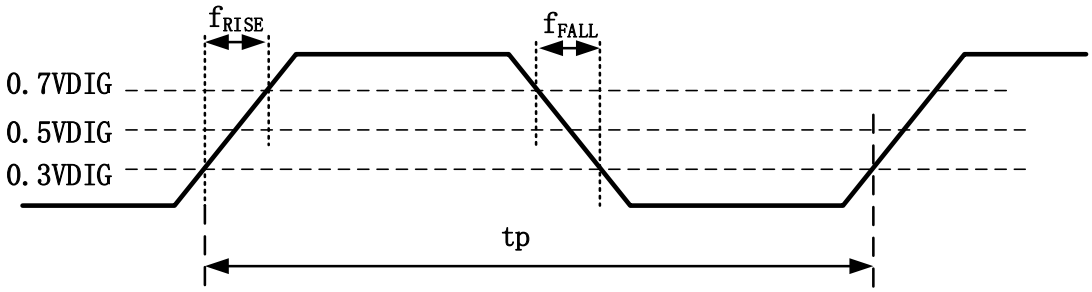
Typ. Analog: 2.8V, Digital: 1.2V, I/O:1.8V, T_j=25℃

2.4 DC Characteristics

Item	Symbol	Min	Typ	Max	Unit
Power supply	**V_{AVDD}**	2.7	2.8	2.9	V
	V_{DVDD}	1.1	1.2	1.3	V
	V_{IOVDD}	1.7	1.8	1.9	V
Digital Input(Conditions: AVDD = 2.8V, DVDD =1.2V, IOVDD = 1.8V)					
Input voltage HIGH	**V_{IH}**	0.7*VIF			V
Input voltage LOW	**V_{IL}**			0.3*VIF	V
Digital Output(Conditions: AVDD =2.8V, IOVDD = 1.8V, standard Loading 25PF)					
Output voltage HIGH	**V_{OH}**	0.8*VIF			V
Output voltage LOW	**V_{OL}**			0.2*VIF	V

3. AC Characteristics

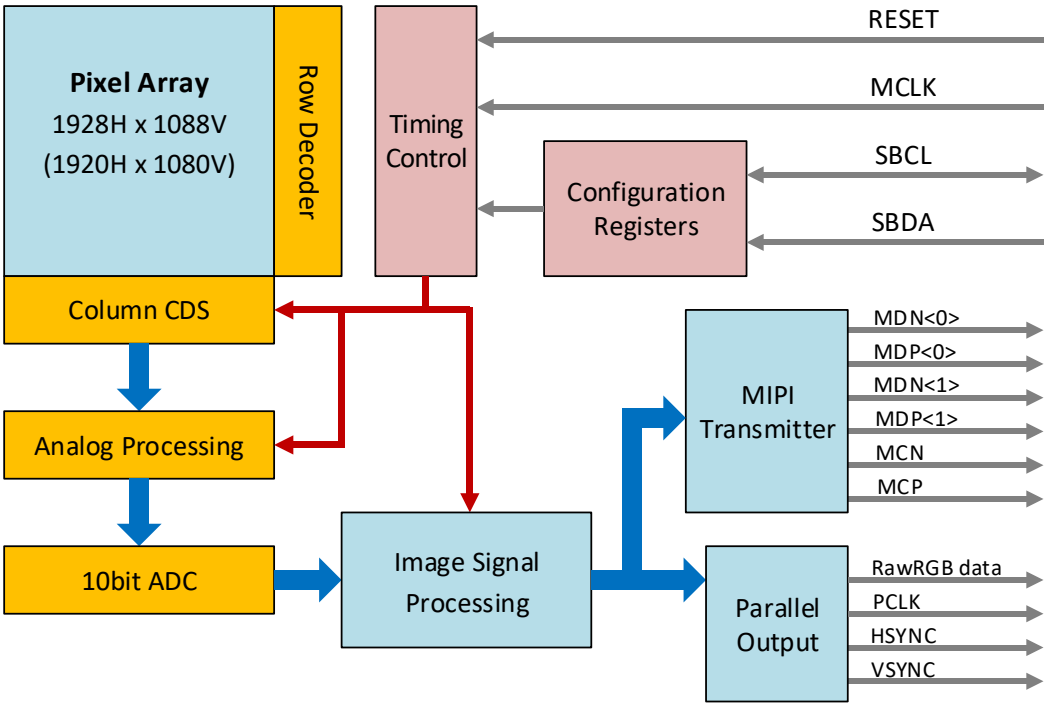
Master clock wave diagram



Input clock square waveform specifications：

Item	Symbol	Min	Typ	Max	unit
Frequency	f_{SCK}	6	27	36	MHz
jitter (period, peak-to-peak)	T_{jitter}			600	ps
Rise Time	f_{RISE}	1		15	ns
Fall Time	f_{FALL}	1		15	ns
Duty Cycle	f_{DUTY}	40		60	%
Input Leakage	f_{ILEAK}	-10		10	μA

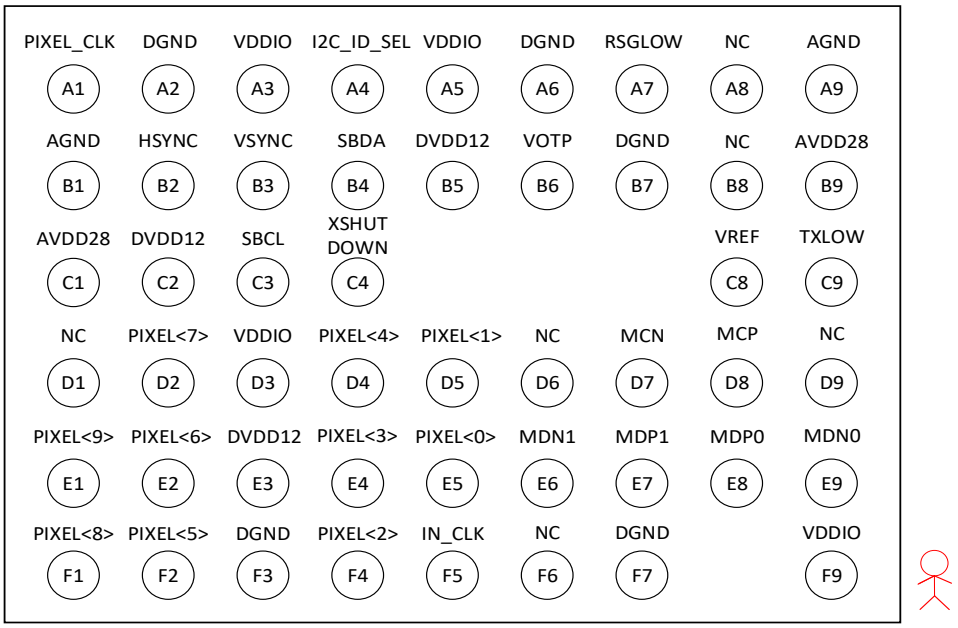
4. Block Diagram



GC2083 has an active image array of 1920x1080 pixels. The active pixels are read out progressively through column/row driver circuits. In order to reduce fixed pattern noise, CDS circuits are adopted. The analog signal is transferred to digital signal by 10 bit A/D converter. The digital signals are processed in the ISP Block. Users can easily control these functions via two-wire serial interface bus.

5. CSP Package Specifications

5.1 Pin Diagram (CSP)



Top View

5.2 Pin Descriptions

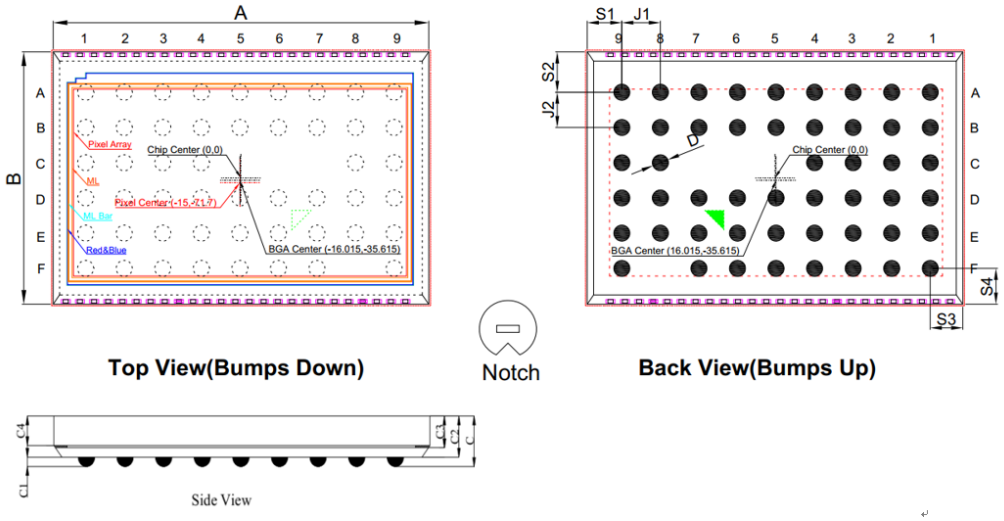
Pin	Name	Pin Type	Description
A1	PIXEL_CLK	OUTPUT	DVP clock
A2	DGND	GROUND	Ground for Digital.
A3	VDDIO	POWER	I/O POWER:1.8V
A4	I2C_ID_SEL	INPUT	ID_SEL（floating forbidden）. 0:0x6e, 1:0x7e
A5	VDDIO	POWER	I/O POWER:1.8V
A6	DGND	GROUND	Ground for Digital.
A7	RSGLOW	POWER	Internal power supply.
A8	NC	NC	NC
A9	AGND	GROUND	Ground for analog.
B1	AGND	GROUND	Ground for analog.
B2	HSYNC	OUTPUT	DVP HSYNC.

B3	VSYNC	I/O	DVP VSYNC.
B4	SBDA	I/O	Two-wire serial bus, data.
B5	DVDD12	POWER	DIGITAL POWER:1.2V Generated by the internal LDO of the chip
B6	VOTP	POWER	2.8V OTP burning power supply（floating available）
B7	DGND	GROUND	Ground for Digital.
B8	NC	NC	NC
B9	AVDD28	POWER	ANALOG POWER: 2.8V
C1	AVDD28	POWER	ANALOG POWER: 2.8V
C2	DVDD12	POWER	DIGITAL POWER: 1.2V Generated by the internal LDO of the chip
C3	SBCL	I/O	Two-wire serial bus, clock.
C4	XSHUTDOWN	INPUT	Sensor power down control: (floating forbidden) 0: reset&standby 1: normal work
C5	\	\	\
C6	\	\	\
C7	\	\	\
C8	VREF	POWER	Internal power supply.
C9	TXLOW	POWER	Internal power supply.
D1	NC	NC	NC
D2	PIXEL<7>	OUTPUT	DVP07
D3	VDDIO	POWER	I/O POWER: 1.8V
D4	PIXEL<4>	OUTPUT	DVP04

D5	PIXEL<1>	OUTPUT	DVP01
D6	NC	NC	NC
D7	MCN	OUTPUT	MIPI clock (+).
D8	MCP	OUTPUT	MIPI clock (-).
D9	NC	NC	NC
E1	PIXEL<9>	OUTPUT	DVP09
E2	PIXEL<6>	OUTPUT	DVP06
E3	DVDD12	POWER	DIGITAL POWER: 1.2V Generated by the internal LDO of the chip
E4	PIXEL<3>	OUTPUT	DVP03
E5	PIXEL<0>	OUTPUT	DVP00
E6	MDN1	OUTPUT	MIPI data <1> (-).
E7	MDP1	OUTPUT	MIPI data <1> (+).
E8	MDP0	OUTPUT	MIPI data <0> (+).
E9	MDN0	OUTPUT	MIPI data <0> (-).
F1	PIXEL<8>	OUTPUT	DVP08
F2	PIXEL<5>	OUTPUT	DVP05
F3	DGND	GROUND	Ground for Digital.
F4	PIXEL<2>	OUTPUT	DVP02
F5	IN_CLK	INPUT	Sensor input clock.
F6	NC	NC	NC
F7	DGND	GROUND	Ground for Digital.
F8	\	\	\
F9	VDDIO	POWER	I/O POWER: 1.8V

5.3 Package Specification (unit: μm)

Mechanical Drawing



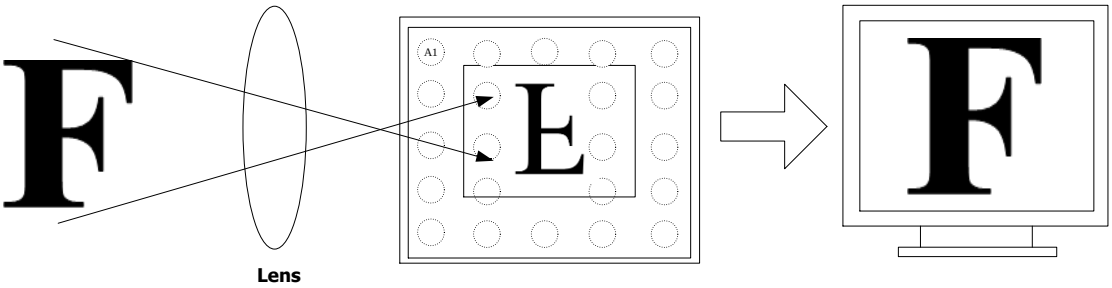
Description	symbol	Nominal	Min	Max
		Millimeters		
Package Body Dimension X	A	5.8440	5.8190	5.8690
Package Body Dimension Y	B	3.9380	3.9130	3.9630
Package Height	C	0.6500	0.5950	0.7050
Ball Height	C1	0.1300	0.1000	0.1600
Package Body Thickness	C2	0.5200	0.4850	0.5550
Thickness from top glass surface to wafer	C3	0.3450	0.3300	0.3600
Glass Thickness	C4	0.3000	0.2900	0.3100
Ball Diameter	D	0.2500	0.2200	0.2800
Total Ball Count	N	50（6NC）		
Ball Count X axis	N1	9		
Ball Count Y axis	N2	6		
Pins pitch X axis	J1	0.6000	0.5900	0.6100
Pins pitch Y axis	J2	0.5500	0.5400	0.5600

BGA ball center to package center offset in X-direction	X	0.016015	-0.0090	0.0410
BGA ball center to package center offset in Y-direction	Y	0.035615	0.0106	0.0606
BGA ball center to chip center offset in X-direction	X1	0.016015	-0.0090	0.0410
BGA ball center to chip center offset in Y-direction	Y1	0.035615	0.0106	0.0606
Edge to Pin Center Distance along X1	S1	0.538015	0.5080	0.5680
Edge to Pin Center Distance along Y1	S2	0.629615	0.5996	0.6596
Edge to Pin Center Distance along X2	S3	0.505985	0.4760	0.5360
Edge to Pin Center Distance along Y2	S4	0.558385	0.5284	0.5884

6. Optical Specifications

6.1 Readout Position

The GC2083 default status is readout from the lower left corner with pin A1 located in the upper left corner. The image is inverted vertically and horizontally by the lens, so proper image output results when Pin A1 is located in the upper left corner.

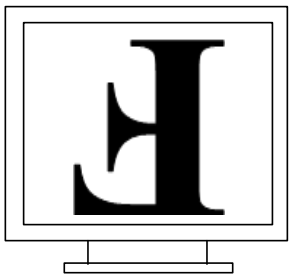


Readout direction can be set by the registers.

Function	Register Address	Register Value	First Pixel
Normal	0x0015[0]、0x0d15[0]	00	R
Horizontal mirror	0x0015[0]、0x0d15[0]	10	Gr
Vertical Flip	0x0015[0]、0x0d15[0]	01	Gb
Horizontal Mirror and Vertical Flip	0x0015[0]、0x0d15[0]	11	B

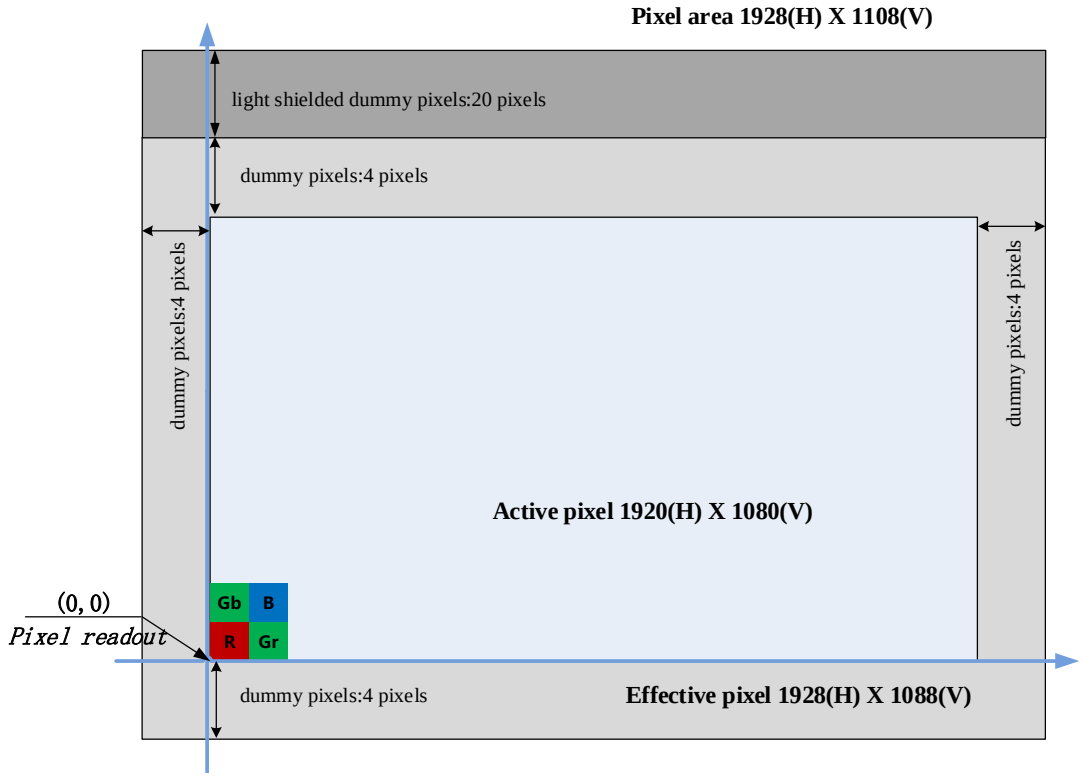
Horizontal Mirror

Vertical Flip



Horizontal Mirror and Vertical Flip

6.2 Pixel Array



Pixel array is covered by Bayer pattern color filters. The primary color GR/BG array is arranged in line-alternating way.

If no flip in column, column is read out from 0 to 1919. If flip in column, column is read out from 1919 to 0.

If no flip in row, row is read out from 0 to 1079.If flip in row, row is read out from 1079 to 0.

6.3 Lens Chief Ray Angle (CRA)

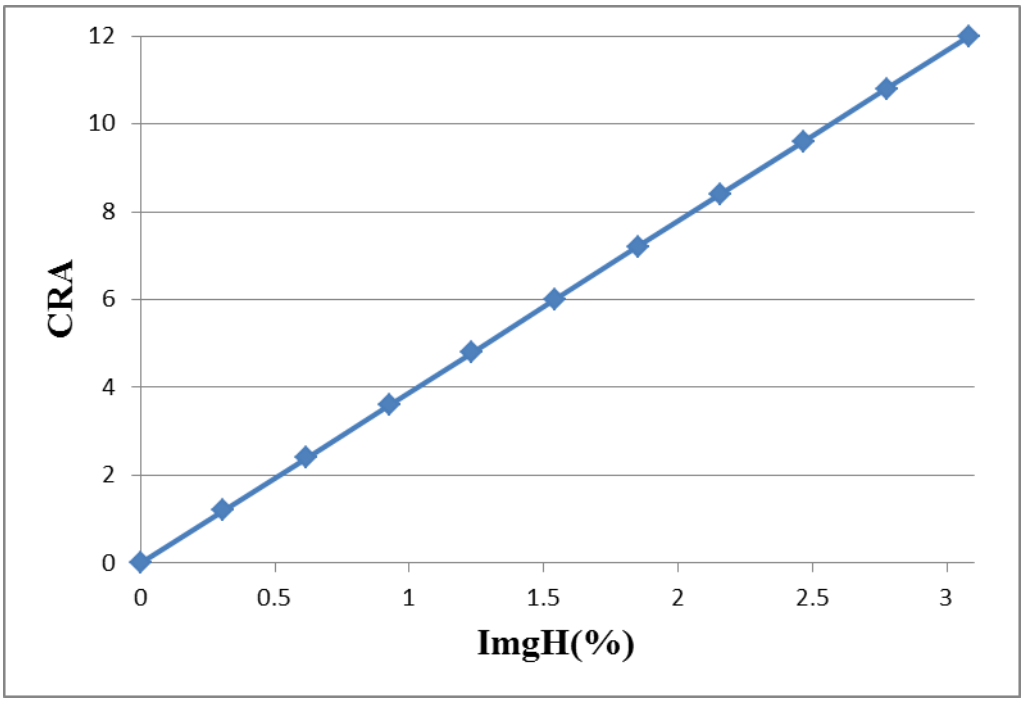
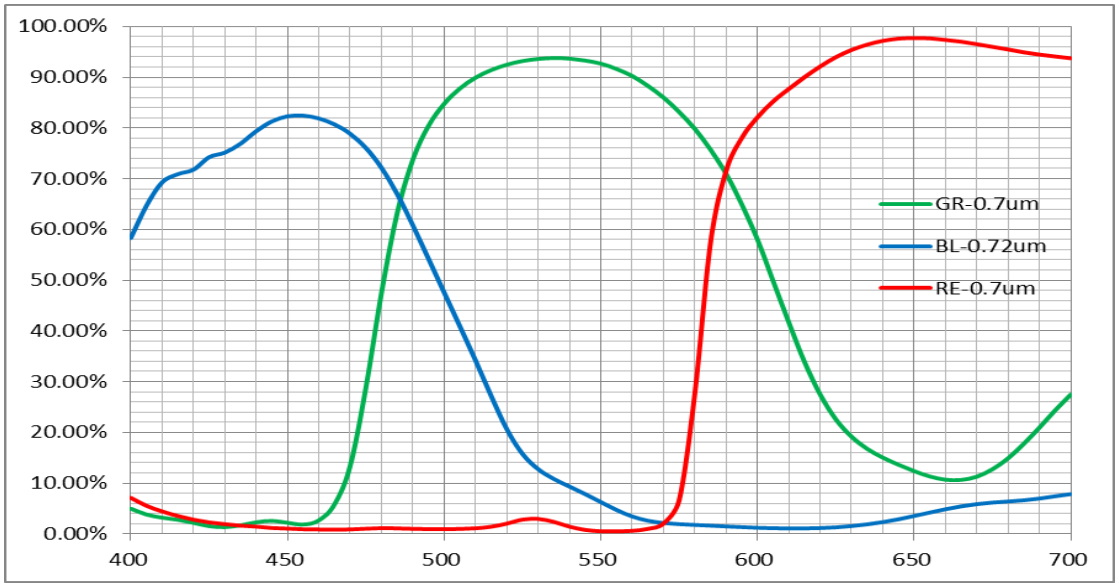


Image Height (%)	Image Height (mm)	CRA (degree)
0	0	0
10	0.3085	1.2
20	0.617	2.4
30	0.9255	3.6
40	1.234	4.8
50	1.5425	6
60	1.851	7.2
70	2.1595	8.4
80	2.468	9.6
90	2.7765	10.8
100	3.085	12

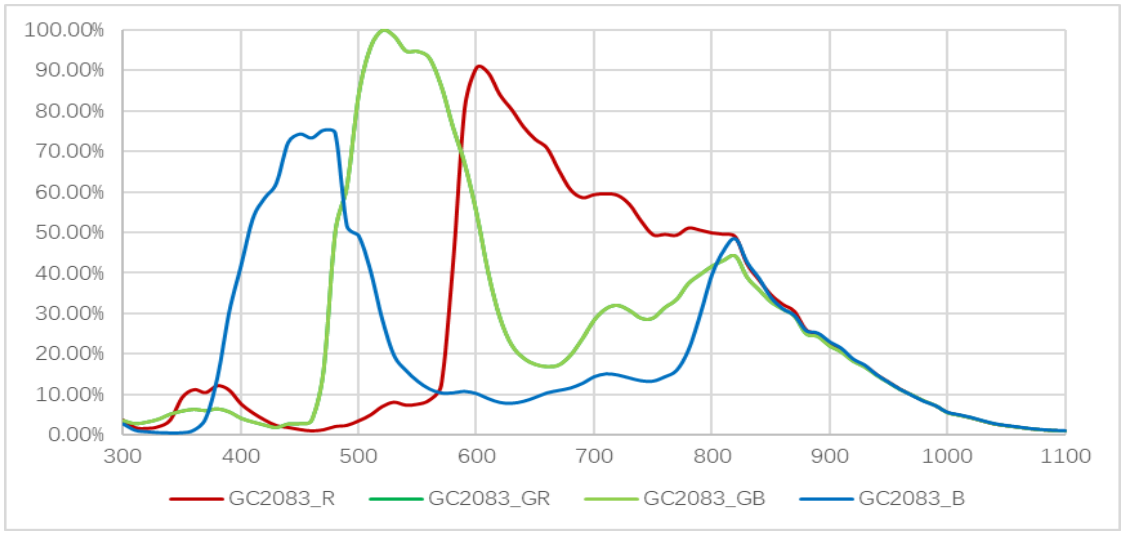
6.4 Color Filter Spectral Characteristics

The optical spectrum of color filters is shown below



6.5 QE Spectral Characteristics

The optical spectrum of QE is below



7. Two-wire Serial Bus Communication

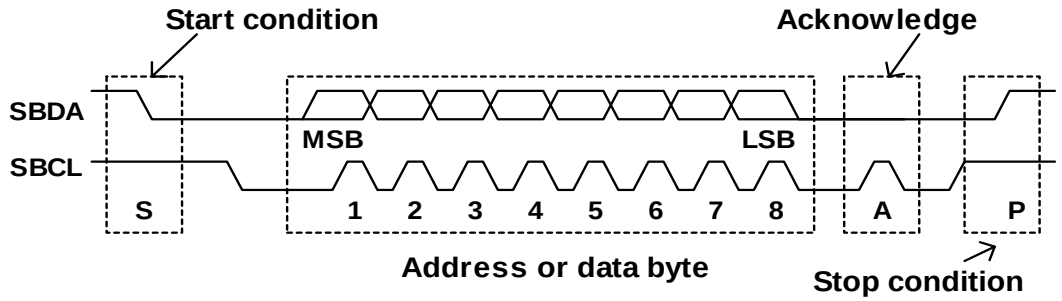
GC2083 Device Address:

ID_SEL	Slave address write mode	Slave address read mode
0(default)	**0x6e**	**0x6f**
1	**0x7e**	**0x7f**

7.1 Protocol

The host must perform the role of a communications master and GC2083 acts as either a slave receiver or transmitter. The master must do

- Generate the **Start(S)/Stop(P)** condition
- Provide the serial clock on **SBCL**.



Single Register Writing:

S	6eH	A	Register Address	A	Data	A	P

Incremental Register Writing:

S	6eH	A	Register Address	A	Data(1)	A	……	Data(N)	A	P

Single Register Reading:

S	6eH	A	Register Address	A	S	6fH	A	Data	NA	P

Notes:

From master to slave

From slave to master

S: Start condition

P: Stop condition

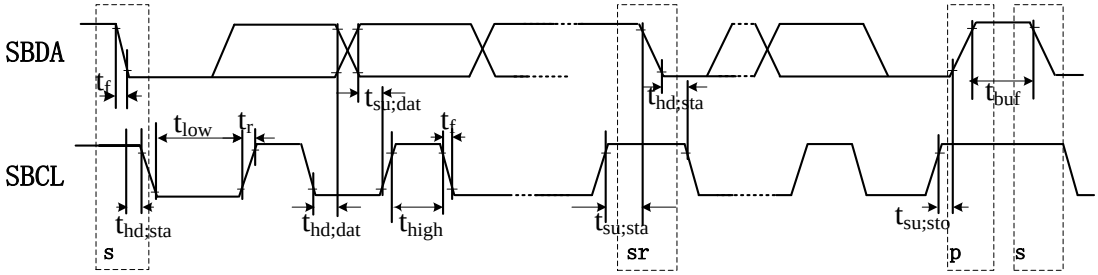
A: Acknowledge bit

NA: No acknowledge

Register Address: Sensor register address

Data: Sensor register value

7.2 Serial Bus Timing

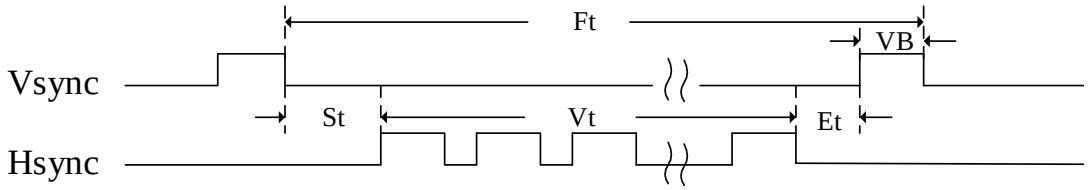


Parameter	Symbol	Min.	Typ.	Max.	Unit
SBCL clock frequency	F_{scl}	0	--	400	KHz
Bus free time between stop and start condition	t_{buf}	1.3	--	--	μs
Hold time for a repeated start	$t_{hd;sta}$	0.6	--	--	μs
LOW period of SBCL	t_{low}	1.3	--	--	μs
HIGH period of SBCL	t_{high}	0.6	--	--	μs
Set-up time for a repeated start	$t_{su;sta}$	0.6	--	--	μs
Data hold time	$t_{hd;dat}$	0	--	0.9	μs
Data Set-up time	$t_{su;dat}$	100	--	--	Ns
Rise time of SBCL, SBDA	t_r	--	--	300	Ns
Fall time of SBCL, SBDA	t_f	--	--	300	Ns
Set-up time for a stop	$t_{su;sto}$	0.6	--	--	μs
Capacitive load of bus line (SBCL, SBDA)	C_b	--	--	--	Pf

8. Applications

8.1 DVP timing

Suppose Vsync is low active and Hsync is high active, and output format is RAW Bayer 10bit/8bit, then the timing of Vsync and Hsync is bellowing:



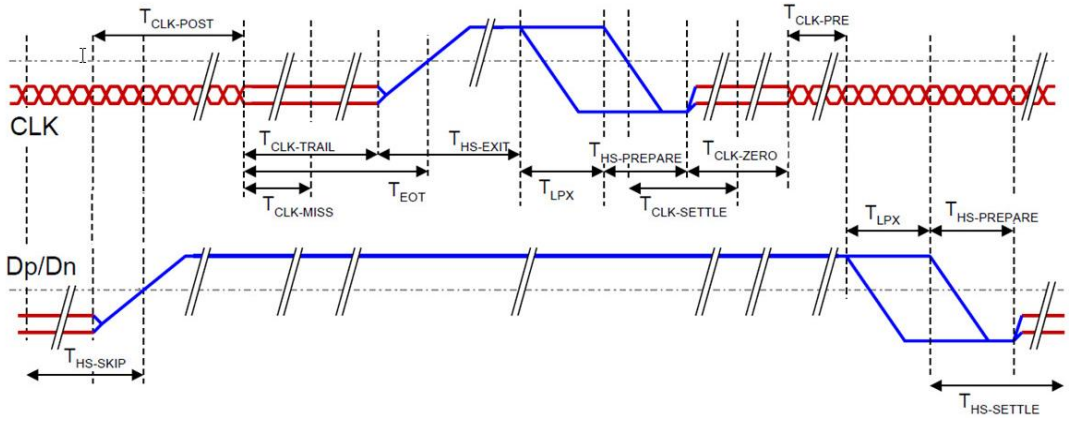
Ft = Vt + 16 + VB；(St + Et < 16+VB)

Ft -> Frame time, one frame time.

Vt -> valid line time. Vt = win_height, win_height is setting by register 0x0d0d and 0x0d0e.

VB->Vblank,setting by register 0x0d07 and 0x0d08

8.2 Clock lane low-power



Notice:

- Clock must be reliable during high speed transmission and mode-switching.
- Clock can go to LP only if data lanes are in LP (and nothing relies on it).
- In Low-Power data lanes are conceptually asynchronous (independent of the high

speed clock).

$T_{CLK\_HS\_PREPARE}$: setting by Register 0x0222

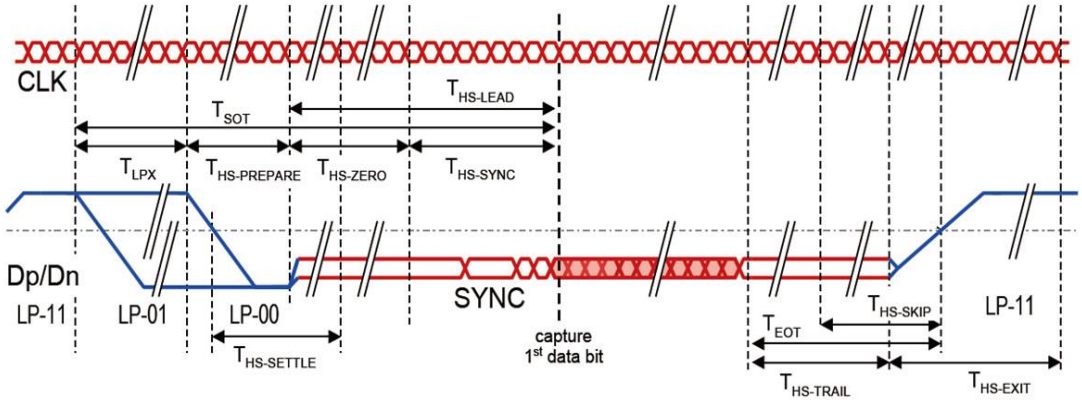
T_{CLK_ZERO}: setting by Register 0x0223

T_{CLK_PRE}: setting by Register 0x0224

T_{CLK_POST}: setting by Register 0x0225

T_{CLK_TRAIL}: setting by Register 0x0226

8.3 Data Burst



Notice:

- Clock keeps running and samples data lanes (except for lanes in LPS).
- Unambiguous leader and trailer sequences required to distill real bits.
- Trailer is removed inside PHY (a few bytes).
- Time-out to ignore line values during line state transition.

T_{LPX}: setting by Register 0x0221

$T_{HS\_PREPARE}$: setting by Register 0x0229

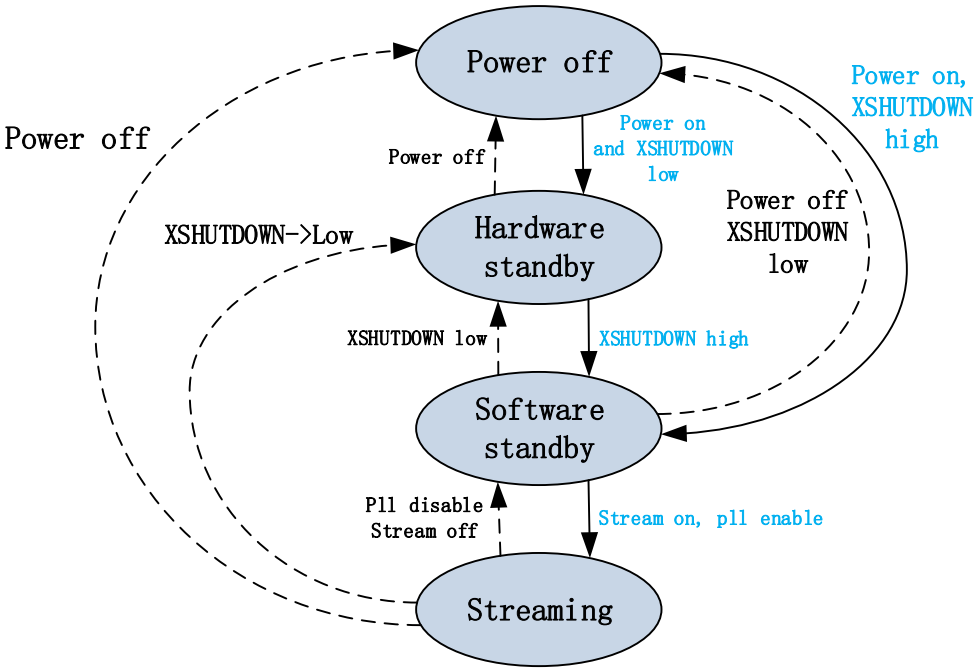
T_{HS_ZERO}: setting by Register 0x022a

T_{HS_TRAIL}: setting by Register 0x022b

T_{HS_EXIT}: setting by Register 0x0227

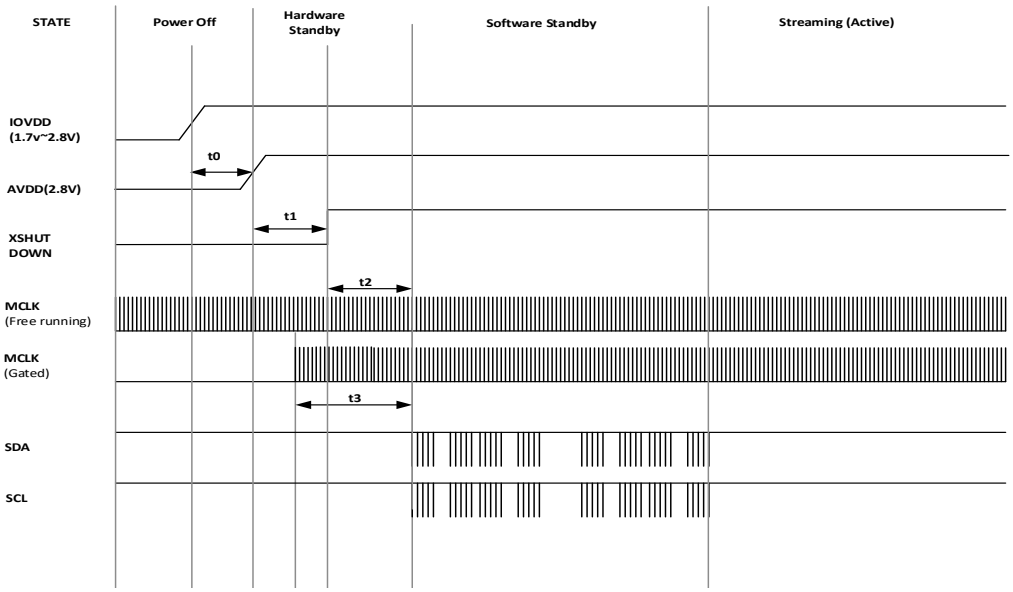
9. Function description

9.1 Operation mode



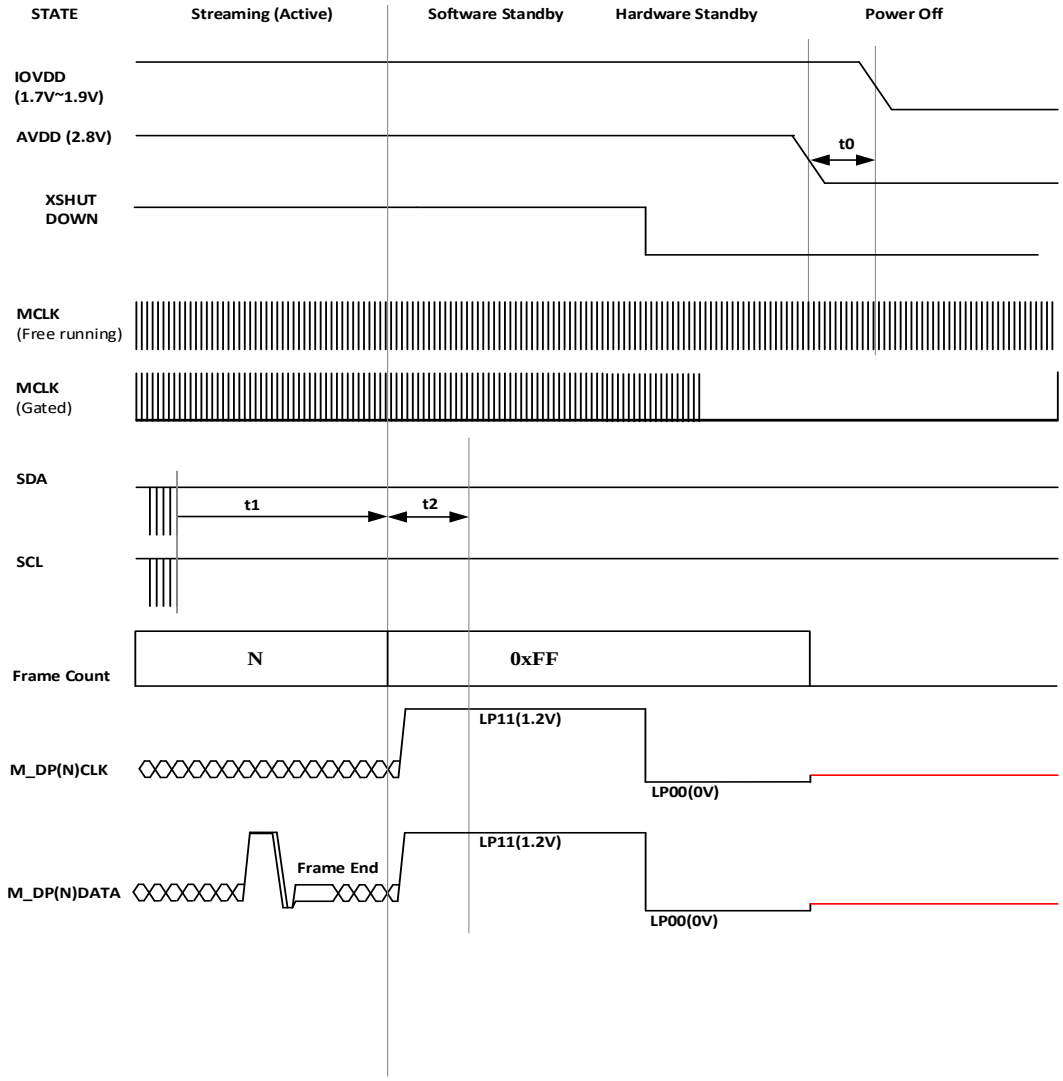
Power state	Description	Activate
Power off	Power supplies are turned off	None
Hardware standby	No communication with sensor, low level on XSHUTDOWN, and stop MCLK	XSHUTDOWN high
Software standby	Two- wire serial communication with sensor, pll is ready for fast return to streaming mode	Stream mode off PLL disable XSHUTDOWN high
Streaming	Sensor is fully powered and is streaming image data on the MIPI CSI-2 bus	All

9.2 Power on Sequence



Parameter	Description	Min.	Max.	Unit
t0	From IOVDD to AVDD28	50	-	μs
t1	From AVDD28 to XSHUTDOWN pull high	0	-	μs
t2	XSHUTDOWN rising to first I2C transaction	50	-	μs
t3	Minimum No. of MCLK cycles prior to the first I2C transaction	1200	-	MCLK

9.3 Power off Sequence



Parameter	Description	Min.	Max.	Unit
t0	From IOVDD pull down to AVDD28 pull down	0	-	μs
t1	Enter Software Standby CCI command – Device in Software Standby mode	0	-	μs
t2	Minimum number of MCLK cycles after the last CCI transaction or MIPI frame end code.	2000		MCLK

- If the sensor’s power cannot be cut off, please keep power supply, then set XSHUTDOWN pin low. It will make sensor standby
- Register should be reloaded before works.
- If the standby sequence needs to be modified, please contact FAE of *Galaxycore Inc.wo dianli*

9.4 Black level calibration

Black level is caused by pixel characteristics and analog channel offset, which makes poor image quality in dark condition and color balance, to reduce these, sensor automatically calibrates the black level every frame with light shield pixel array.

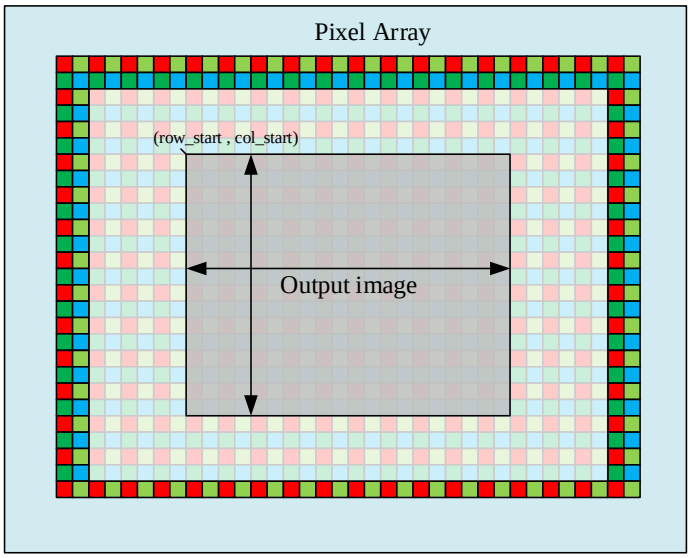
9.5 Integration time

The integration time is controlled by the integration time registers

Addr.	Register name	Description
0x0d03	Shutter time	[5:0] shutter time[13:8]
0x0d04		[7:0] shutter time[7:0]
0x0d41	Frame length	[5:0] frame length[13:8]
0x0d42		[7:0] frame length[7:0]

9.6 Windowing

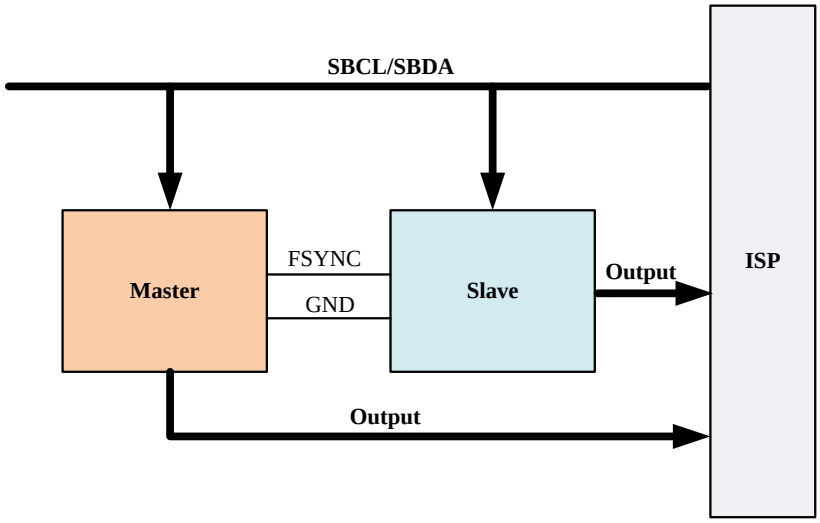
GC2083 has a rectangular pixel array 1920 x 1080, it can be windowed by output size control, the output image windowing can be used to adjust output size, and it will affect field angle.



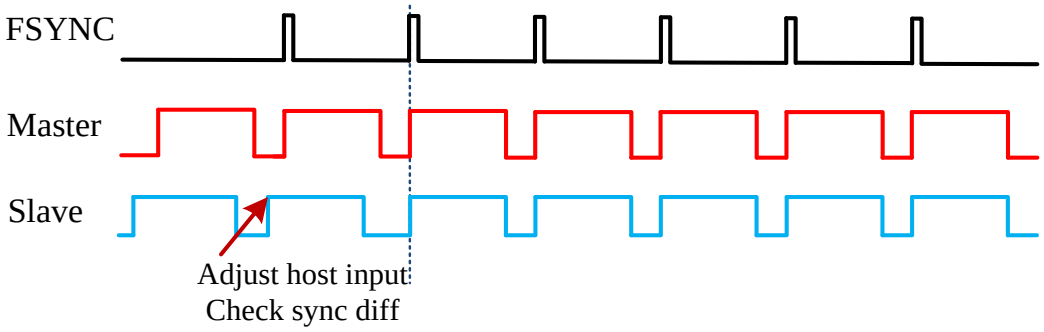
Addr.	Register name	Description
0x0d0d	win_height	[2:0]win_height[10:8]
0x0d0e		[7:0]win_height[7:0]
0x000f	win_width	[3:0]win_width[11:8]
0x0010		[7:0]win_width[7:0]
0x0d09	Row start	[2:0]row_start[10:8]
0x0d0a		[7:0]row_start [7:0]
0x000b	Col start	[2:0]col_start[10:8]
0x000c		[7:0]col_start[7:0]

9.7 Frame sync mode

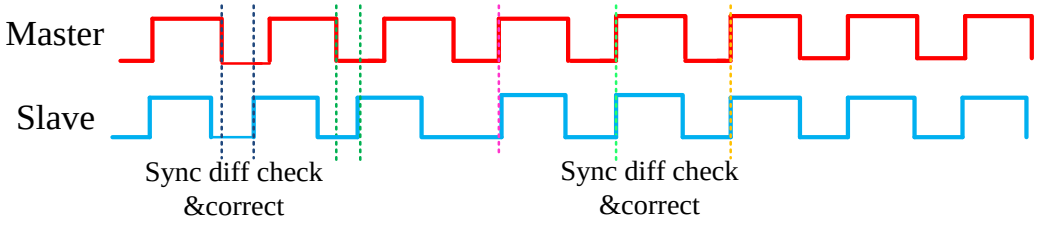
GC2083 can support hardware frame sync for dual camera application. It can be set both master and slave sensor. When use this mode, the two sensor’s FSYNC pin must connect to each other.



Adjust mismatch sync



Dynamic mismatch sync control



Addr.	Register name	Description
0x0068	fsync_mode	[4]fsync_clear_counter [3:0]fsync_mode
0x0069	fsync_mode_global	
0x0d69	fsync_mode_new3	
0x0d6a	Fsync row time	
0x0d6b	fsync_mode_new4	
0x0d6c	fsync_row_diff_th	[5:0] fsync_row_diff_th
0x006b	Debug_mode4	[5:4] fsync_vb_gap
0x0d6e	fsync_row_diff_big[13:8]	[5:0] fsync_row_diff_big[13:8]
0x0d6f	fsync_row_diff_big [7:0]	[7:0] fsync_row_diff_big [7:0]
0x0d70	fsync_row_diff_big2[13:8]	[5:0] fsync_row_diff_big2[13:8]
0x0d71	fsync_row_diff_big2 [7:0]	[7:0] fsync_row_diff_big2[7:0]

9.8 Frame structure

Frame structure is controlled by HB, frame length, window start, window height, window width and VB.

Frame length control

Frame length are controlled by window height, minimum VB and shutter time.

- Frame length depend shutter time.

- Minimum frame length = window height + 16 +VB (VB_min = 16)
- If shutter time < minimum frame length:

  Actual frame length = minimum frame length
- If shutter time > minimum frame length:

  Actual frame length = shutter time + 16 (recommended).

- Fix frame rate

- User can fix VB to fix frame rate.

Line length control

Line length = 1200 (not recommended to be modified)

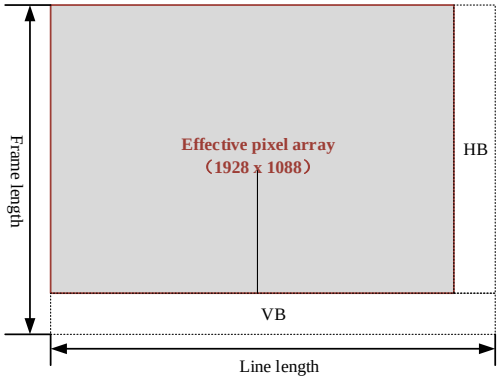
Addr.	Register name	Description
0x0d05	Line length	[3:0] Line length[11:8] X2
0x0d06		[7:0] Line length[7:0] X2

Output window array control

Addr.	Register name	Description
0x0191	Out_window_y1	[2:0] Out_window_y1[10:8]
0x0192		[7:0] Out_window_y1[7:0]
0x0193	Out_window_x1	[3:0] Out_window_x1[11:8]
0x0194		[7:0] Out_window_x1[7:0]
0x0195	Out window height	[2:0] Out window height[10:8]
0x0196		[7:0] Out window height[7:0]
0x0197	Out window width	[3:0] Out window width[11:8]
0x0198		[7:0] Out window width[7:0]

Blank time control

1. line blank time is controlled by HB
2. frame blank time
   - frame blank time = frame length lines – window height – 16



10. Register List

System Register

Address	Name	Width	Default Value	R/W	Description
0x03f0	**Sensor_ID_HIGH**	**8**	**0x20**	**RO**	**Sensor_ID**
0x03f1	**Sensor_ID_LOW**	**8**	**0x83**	**RO**	**Sensor_ID**

Analog & CISCTL

Address	Name	Width	Default Value	R/W	Description
0x0d03	Exposure time[13:8]	6	0x00	RW	[7:6] NA [5:0] exposure time[13:8]
0x0d04	Exposure time [7:0]	8	0x10	RW	[7:0] exposure time[7:0]
0x0d05	CISCTL _HB[11:8]	4	0x04	RW	CISCTL_HB
0x0d06	CISCTL_HB [7:0]	8	0x48	RW	
0x0d07	CISCTL_vb [13:8]	6	0x00	RW	VB
0x0d08	CISCTL_vb [7:0]	8	0x20	RW	
0x0d09	CISCTL_row_start[10:8]	3	0x00	RW	[7:3] reserved [2:0] Row Start[10:8]
0x0d0a	CISCTL_row_start [7:0]	8	0x00	RW	Row Start[7:0]
0x000b	CISCTL_ col_start [10:8]	3	0x00	RW	[7:3] reserved [2:0] colstart[10:8]
0x000c	CISCTL_ col_start [7:1]	8	0x00	RW	[7:0] colstart
0x0d0d	CISCTL_ win_height[10:8]	3	0x04	RW	[7:3] NA [2:0] Window height[10:8]
0x0d0e	CISCTL_ win_height [7:0]	8	0x48	RW	[7:0] Window height
0x000f	CISCTL_win_width [10:8]	3	0x07	RW	[7:3] NA [2:0] Window width[11:8]
0x0010	CISCTL_win_width [7:0]	8	0x90	RW	[7:0] window width
0x0d41	Framelength	6	0x04	RW	[5:0]: framelength[13:8]
0x0d42		8	0x65	RW	[7:0]: framelength[7:0]
0x0d13	CISCTL_vs_st	8	0x10	RW	vs_st
0x0d14	CISCTL_vs_et	8	0x04	RW	vs_et
0x0068	fsync_clear_counter fsync_mode	5	0x08		[4]fsync_clear_counter [3:0]fsync_mode

0x0069	Fsync_mode_global	8	0x00		[7]fsync_vb_gap_lasts [6]strobe_output [5]fsync_out_polarity [4]fsync_in_polarity [3]gpio_mode [2]gpio_value [1]vsync_out_mode [0]fsync_every_frame_slave
0x0d67	Fsync_mode_global_r	8	0x00		
0x0d69	Fsync_mode_new3	8	0x04		
0x0d6a	Fsync_rowtime	8	0x00		
0x0d6b	Fsync_mode_new4	8	0x01		[7]fsync_vb_gap_mode_tmp [6]fsync_vb_first_mode_tmp [5]fsync_row_diff_mode [4]fsync_vb_mode
0x0d6c	Fsync_row_diff_th	8	0x02		
0x0d6d	Debug_mode4	8	0x58		[7] exp_change_retime [5:4] fsync_vb_gap [1:0] fsync_vb_old
0x0d6e	Fsync_row_diff_big[13:8]	6	0x00		[13:8] fsync_row_diff_big
0x0d6f	Fsync_row_diff_big[7:0]	8	0x04		[7:0] fsync_row_diff_big
0x0d70	Fsync_row_diff_big2[13:8]	6	0x00		[5:0] Fsync_row_diff_big2
0x0d71	Fsync_row_diff_big2[7:0]	8	0x10		

CSI/PHY1.0

Address	Name	Width	Default Value	R/W	Description
0x0201	DPHY_analog_mode1	8	0x20	RW	
0x0202	DPHY_analog_mode2	8	0x16	RW	
0x0203	DPHY_analog_mode3	8	0xca	RW	
0x0204	FIFO_prog_full_level[7:0]	8	0x08	RW	[7:0]FIFO_prog_full_level[7:0]
0x0206	FIFO_mode	8	0x00	RW	
0x0211	LDI_set	8	0x2b	RW	
0x0212	LWC_set[15:87:0]	8	0x07	RW	
0x0213	LWC_set[7:0]	8	0x80	RW	
0x0214	SYNC_set	8	0xb8	RW	SYNC_set
0x0215	DPHY_mode	8	0x10	RW	
0x0216	LP_set	8	0x29	RW	
0x021b	fifo2_prog_full_level	5	0x08	RW	[4:0]fifo2_prog_full_level
0x021c	fifo2_push_prog_full_level	5	0x08	RW	[4:0]fifo2_push_prog_full_level

0x021d	sram_test_mode	4	0x02	RW	[3]RF1_not_split [2]RF1 cen [1]RF1 gate [0]NA sram test
0x0220	T_init_set	8	0x80	RW	
0x0221	T_LPX_set	8	0x10	RW	
0x0222	T_CLK_HS_PREPARE_set	8	0x05	RW	
0x0223	T_CLK_zero_set	8	0x20	RW	
0x0224	T_CLK_PRE_set	8	0x02	RW	
0x0225	T_CLK_POST_set	8	0x20	RW	
0x0226	T_CLK_TRAIL_set	8	0x08	RW	
0x0227	T_HS_exit_set	8	0x10	RW	
0x0228	T_wakeup_set	8	0xa0	RW	
0x0229	T_HS_PREPARE_set	8	0x06	RW	
0x022a	T_HS_Zero_set	8	0x0a	RW	
0x022b	T_HS_TRAIL_set	8	0x08	RW	
0x0230	MIPI_test	2	0x00	RW	[1:0]MIPI_Test
0x0235	OUT_pad_test_data	8	0x00		
0x0236	clklp_drv	2	0x00		[1:0]clklp_drv
0x0237	lp_drv	4	0x00		[3:2] data1lp_drv [1:0] data0lp_drv
0x0238	prbs_mode	8	0x20		
0x0239	prbs_LDI	8	0x3d		
0x024a	prbs_seed[7:0]	8	0x9a		
0x024b	prbs_seed[15:8]	8	0x78		
0x024c	MIPI_TSEL	2	0x01		[1:0] MIPI_TSEL
0x0290	dvp_out_mode	6	0x00		[7] o_vsync_pola [6] o_hsync_pola
0x0291	pad_test_valid[11:8]	4	0x00		
0x0292	pad_test_valid[7:0]	8	0x00		
0x0293	pad_test_data[11:8]	4	0x00		
0x0294	pad_test_data[7:0]	8	0x00		

OUT

Address	Name	Width	Default Value	R/W	Description
0x018c	Test image	1	0x10		[2] input test image
0x0191	out_win_y1[10:8]	11	0x00		[7:3]NA [2:0] out_win_y1
0x0192	out_win_y1[7:0]	11	0x00		Out_win_y1

0x0193	Out_win_x1[11:8]	12	0x00		[7:4]NA [3:0]out_win_x1
0x0194	Out_win_x1[7:0]	12	0x00		
0x0195	Out_win_height[10:8]	11	0x04		[7:3]NA [2:0] out_win_helght[10:8]
0x0196	Out_win_height[7:0]	11	0x38		out_win_helght[7:0]
0x0197	Out_win_width[11:8]	12	0x07		[7:4]NA [3:0]out_win_width[11:8]
0x0198	Out_win_width[7:0]	12	0x38		Out_win_width[7:0] must be 8X when raw10
0x0199	Out_win_offset	4	0x05		[7:4]NA [3:0] Out_win_offset for auto_updown[3:2] out_offset_y1=2 for auto_mirror[1:0] out_offset_x1=2

DARK OFFSET

Address	Name	Width	Default Value	R/W	Description
0x0170	WB_offset_G1	8	0x40	RW	WB_offset_G1
0x0171	WB_offset_R1	8	0x40	RW	WB_offset_R1
0x0172	WB_offset_B1	8	0x40	RW	WB_offset_B1
0x0173	WB_offset_G2	8	0x40	RW	WB_offset_G2

GLOBAL/PRE/POSTGAIN

Address	Name	Width	Default Value	R/W	Description
0x00b1	auto_pregain_sync[9:6]	4	0x01	RW	[7:4] NA [3:0] Auto_pregain[9:6] 4.6 精度
0x00b2	auto_pregain[5:0]	8	0x00	RW	[7:2] Auto_pregain[5:0] [1:0]NA
0x00d0	Analog_PGA_gain[7:0]	8	0x00	RW	
0x0dc1	Analog_PGA_gain[8]	1	0x00	RW	[0] analog_gain
0x00b8	Col_gain[11:6]	8	0x00	RW	[7:6]NA [5:0]col_gain[11:6]
0x00b9	Col_gain[5:0]	8	0x00	RW	[7:6]NA [5:0]col_gain[5:0]
0x007a	Global gain	8	0x40	RW	[7:6] global gain 2.6 精度