Full Adder Design Using Reversible Logic with Different Tools for Low Power VLSI

A PROJECT REPORT

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BONAFIDE CERTIFICATE

Certified that this project report "**Full Adder Design Using Reversible Logic with Different Tools for Low Power VLSI**" is the bonafide work of "**Caprio Mistry, Ashis Paul, Sugoto Roy Chowdhury, Swarnali Mitra**" who carried out the project work under my supervision.

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ABSTRACT

In this work we propose a study to the logic design synthesis of different circuit by using reversible computing. This study is based on the use of full adder circuit using reversible logic synthesis. The idea is designing an adder circuit with low power dissipation and low power consumption. Among the properties of reversible gate, we have a minimum of input constant number of gate and number of garbage output. Garbage output are those output which is not using for any consumption.

Full adder cell is one of the most frequently used digital circuit component in arithmetic logic unit (ALU) and it is the essential functional unit of all computational circuit. Till now lots of improvement has been done in this area to refine the architecture and performance of full adder circuit design. In this project, designs of novel full adder cell at 90nm CMOS technology are implemented by using CMOS transistors along with the existing full adder cell using reversible computing.

1.INTRODUCTION

Scientist R. Landauer proved in 1961 that energy dissipation is caused by the loss of each bit of information. The amount of energy dissipated for one bit of information loss is KTln2 joules, where K is the Boltzmann's constant and T is the operating temperature. At ambient temperature, the heat released by the loss of one bit of information is extremely tiny, but in the case of high computational tasks, when the number of bits is greater, the heat dissipated by them is so significant that it impacts performance and reduces component lifespan. C. H. Bennett demonstrated in 1973 that reversible logic gates must be used in a logic circuit to prevent KTln2 energy loss.

1.1 Overview

The use of battery-powered portable electronic systems is becoming more popular. Because these gadgets are portable, they require a battery to power them. As a result, power consumption and speed become the primary concerns in the design of devices such as laptops, tablets, mobile phones, notebooks, and a variety of other personal communication devices. In VLSI technology, power consumption is critical. More power consumption causes more heating, which reduces battery life and necessitates the use of a cooling fan to cool the circuitry. As a result, power consumption influences battery life and overall system cost. Most digital communication devices and the devices listed above are utilized in applications such as digital signal processing, image and video processing, microcontrollers, and these applications require different arithmetic and logic operations to execute addition, subtraction, multiplication, and so on. All of these operations, such as addition, subtraction, and multiplication, could be done internally using only adder cells. Since adder circuit (cell) plays most important role in designing these digital communication devices.

1.2 What is reversible computing?

Reversible computing refers to any type of computation in which the computational process is time-reversible to some extent. A required criterion for reversibility in a model of computation that employs deterministic transitions from one state of the abstract machine to another is that the mapping between states to their successors be one-to-one. Reversible computing is a type of unusual computing.

1.3 Need of reversible computing

As we pack more and more logic elements into smaller and smaller volumes and clock them at higher and higher frequencies, we dissipate more and more heat. This creates at least three problems:

- Energy costs money.
- Portable systems exhaust their batteries.
- Systems overheat.

An alternative is to use logic operations that do not erase information. These are called reversible logic operations, and in principle they can dissipate arbitrarily little heat. As the energy dissipated per irreversible logic operation approaches the fundamental limit of ln 2 x kT, the use of reversible operations is likely to become more attractive. If current trends continue this should occur sometime in the 2010 to 2020 timeframe. If we are to reduce energy dissipation per logic operation below ln 2 x kT we will be forced to

use reversible logic.

Nanotechnology should let us build mole quantities of logic elements. Unless energy dissipation per logic operation can be reduced below kT, the raw cost of electricity might well prove prohibitive and the system might quickly overheat

To reduce the area of chip, the complexity in the circuits has increased significantly, because of that the power dissipation and performance of the adder circuit are being affected. So, there is concern towards circuits design in low power VLSI design to reduce the chip size and power dissipation. There are two types of power dissipations in MOSFET technology i.e., static power dissipation and dynamic power dissipation. In Static power dissipation there are few parameters which effect operation of device like sub threshold leakage, reverse-biased junction leakage, gate direct tunneling leakage and gate induced drain leakage shows the major effect in various scaling parameters. In Dynamic power dissipation mainly switching and short circuit power is considered.

1.4 Technical requirement for reversable computing

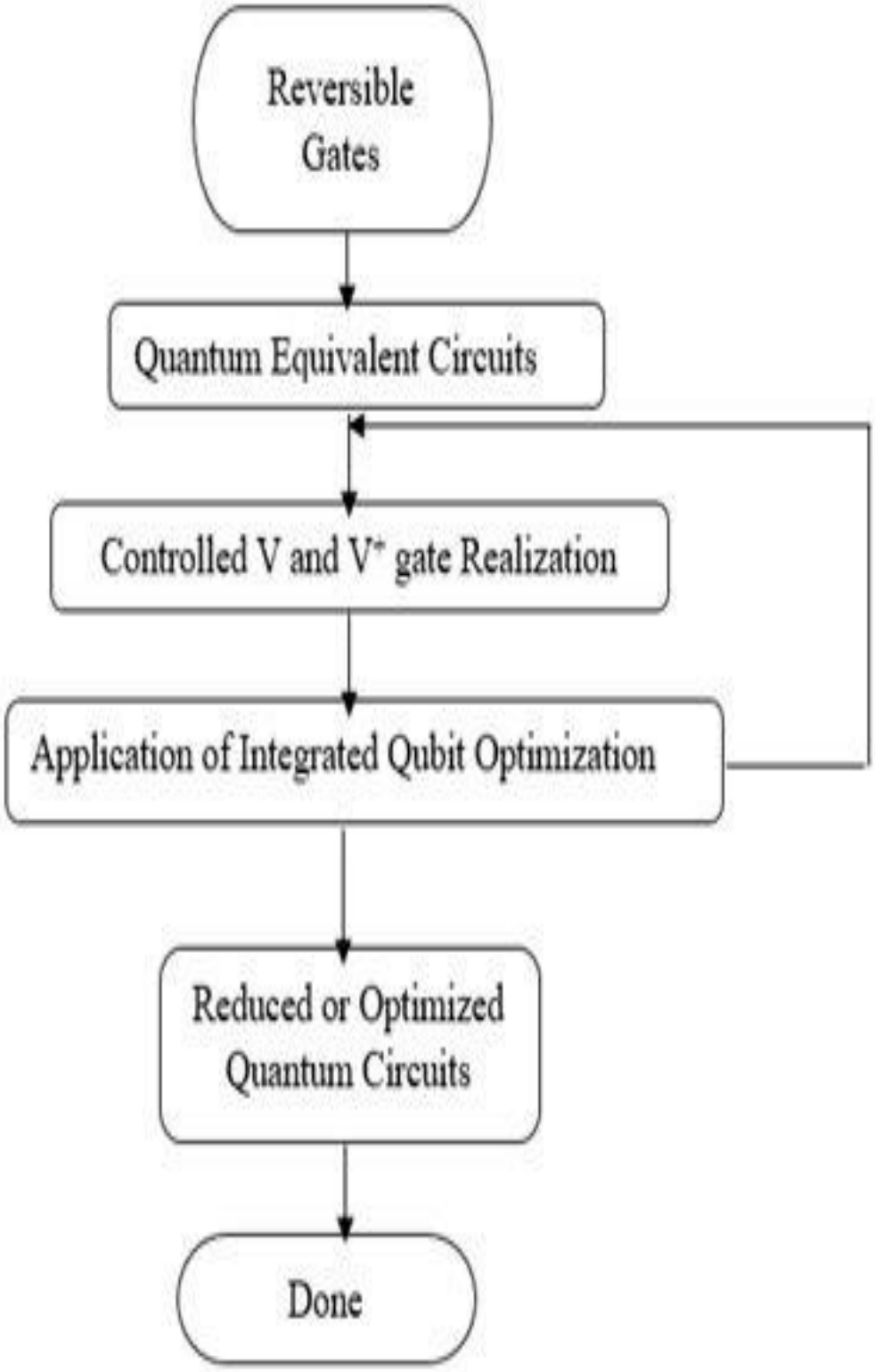


Fig a.

2.LITERATURE REVIEW

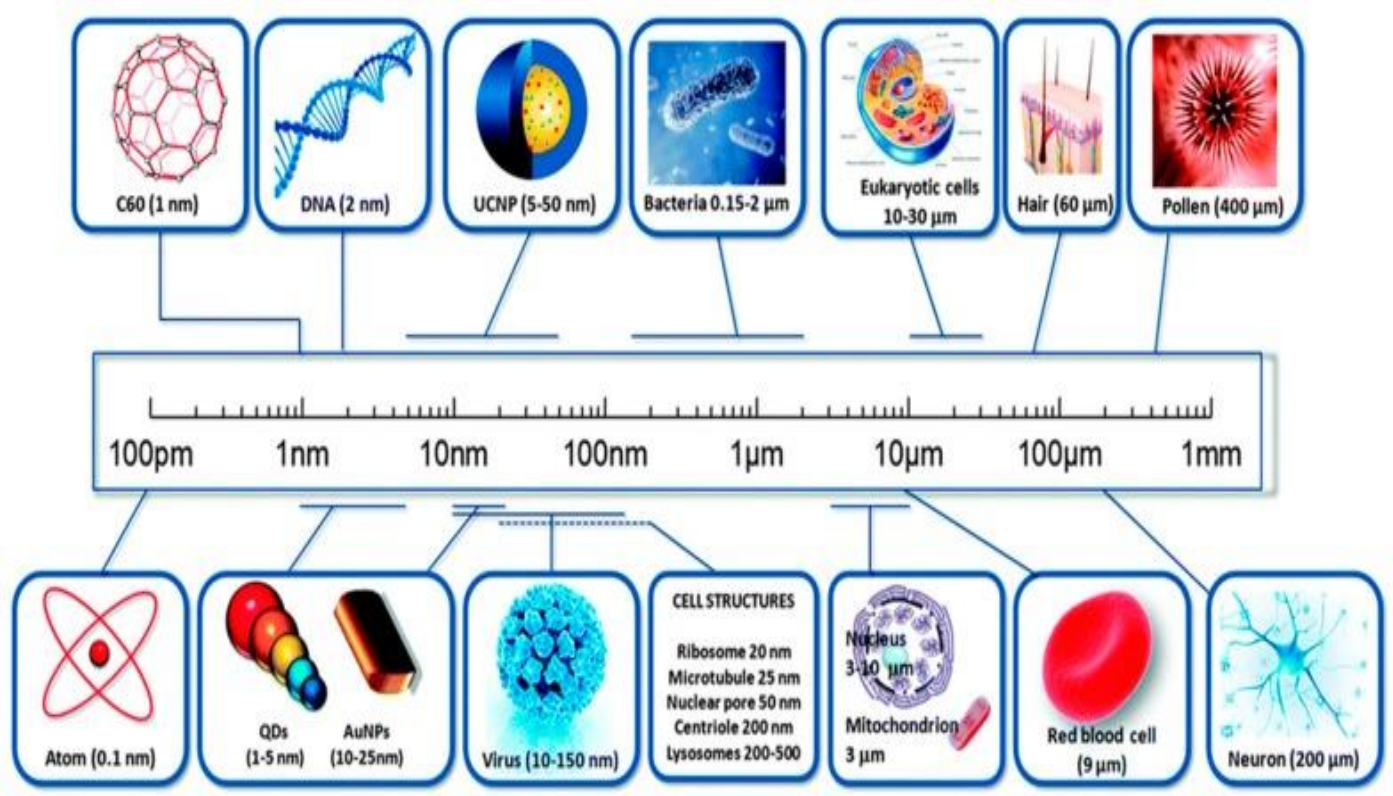
In this work, we offer a study of logic design synthesis of various circuits utilizing reversible computing. This research is based on the utilization of a complete adder circuit with reversible logic synthesis. The objective is to create an adder circuit with minimal power dissipation and usage. We have a minimum of input constant number of gate and number of garbage output among the reversible gate attributes. Garbage output is any output that is not being consumed.

Full adder cells are one of the most often utilized digital circuit components in arithmetic logic units (ALUs), and they are the fundamental functional unit of all computational circuits. Power consumption and speed have emerged as important factors in the design of devices such as laptops, tablets, mobile phones, notebook computers, and a range of other personal communication devices. Power consumption is crucial in VLSI technology.

More power consumption results in increased heating, which affects battery life and needs the usage of a cooling fan to keep the circuitry cool. As a result, power consumption has an impact on battery life as well as overall system cost. The majority of digital communication devices and the devices listed above are used in applications such as digital signal processing, image and video processing, and microcontrollers, and these applications require various arithmetic and logic operations to perform addition, subtraction, multiplication, and so on. Internally, all of these operations, such as addition, subtraction, and multiplication, may be performed.

Till now in digital world different types of full adder cells are designed with different logic styles. Some of them are good for low power application, some of them for high speed, few of them full fill minimum area requirement but all these designs have its own merits and demerits. According to requirement of applications these adders are used. Few full adder cells which are already implemented are conventional full adder cell, Static Energy Recovery Full adder cell (SERF), Gate Diffusion Input (GDI) full adder Cell etc. Most of the complex computational circuit requires full adder circuitry hence the whole power consumption and speed of computational circuit can be managed by the implementing the low power and high-speed adder cell, so overall performance of computational circuits is totally depending on the adder cell.

The word 'nano' refers to a Greek prefix that means 'dwarf' or ‘very little,' and it represents a thousand millionth of a meter (10.9). The terms "nanoscience" and "nanotechnology" should be differentiated. Nanoscience is the study of structures and substances on nanometer sizes ranging from 1 to 100 nm, while nanotechnology is the technology that applies this knowledge to practical applications such as electronics. A single human hair is 60,000 nanometers thick, but the DNA double helix has a radius of 1 nanometer. Nanoscience may be traced back to the 5th century B.C., when scientists debated whether matter is continuous.



The technique of embedding or integrating hundreds of thousands of transistors onto a single silicon semiconductor microchip is known as very large-scale integration. VLSI technology was first developed in the late 1970s, about the same time as high level processor (computer) microchips were being developed. Microprocessors and microcontrollers are two of the most prevalent VLSI devices.

The advancements in large-scale integration technologies are principally responsible for the electronics industry's extraordinary growth. The number of options for ICs in control applications, telecommunications, high-performance computing, and consumer electronics as a whole continues to grow with the emergence of VLSI designs.

Due to VLSI technology, today's devices like as smartphones and cellular communications provide unparalleled mobility, processing capacity, and application access. As demand continues to rise, the projection for this trend implies a quick growth.

In this year, reversible logic has emerged as a potential technique in low-power VLSI design, nanotechnology, quantum computing, and optical computing in recent years. The performance and dependability of digital systems that are now implemented with traditional logic gates can be improved by employing reversible logic gates, which allow for lower power consumption and shorter quantum delays, boosting computing speed. The essential block in the arithmetic and logic unit of processors and other digital logic programmable devices is the adder/subtractor circuit.

VLSI Technology's Advantages

VLSI technology has the following major benefits:

- Circuits have been made smaller.
- Devices have become more cost-effective.
- In terms of circuit operating speed, the performance has improved.
- When compared to separate components, it consumes less energy.
- Devices that are more dependable

3.OBJECTIVE

To design, simulate and synthesize a full adder circuit with implementing the concept of reversible computing. Nanotechnology should enable us to construct mole amounts of logic components. Unless the energy dissipation per logic operation is decreased to less than petajoules, the raw cost of power may become prohibitive, and the system may soon overheat.

4.PLANNING

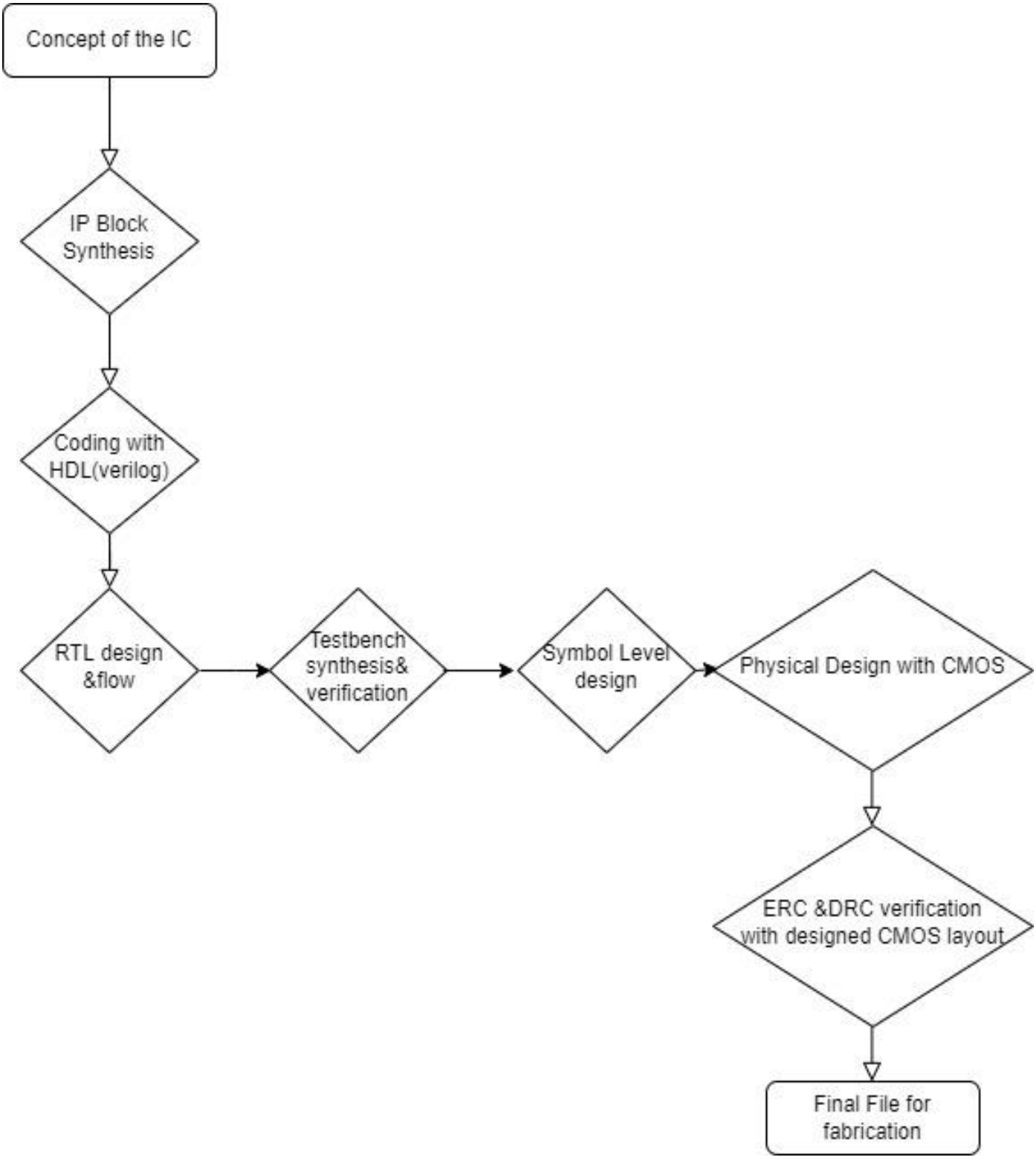


Fig b: Roadmap of Ic Design

5.REQUEREMENT ANALYSIS

5.1 Low Power VLSI

Reversible computing spans computational models that are both forward and backward deterministic. These models have applications in program inversion and bidirectional computing, and are also interesting as a study of theoretical properties. A reversible computation does, thus, not have to use energy, though this is impossible to avoid in practice, due to the way computers are build. It is, however, not always obvious how to implement reversible computing systems. The restriction to avoid information loss imposes new design criteria that need to be incorporated into the design; criteria that do not follow directly from conventional models.

5.2 Over Heating

Whenever we use any handheld device like our smartphones, laptops or computers, the logic gates which are designed using the transistors start to work. The use of transistors for designing the logic gates is as fast as switches. But the debating point is about the heating of the devices. We all face the fact that our processors and mobile devices discharge lots of heat. The reason behind it is the increase of transistors on-chip (TOC).

5.3 I/O BIT LOSS

A reversible circuit has exactly as many outputs as inputs. Each input can be reconstructed from the output; no bits are lost but in conventional logics cannot reconstruct the input from the output, so reversible circuits will not give off heat from bit loss.

A. Tools required and used

1. DSCH. (National Instruments Corps.)
2. Microwind 3.1. (National Instruments Corps.)

6.SYSTEM FLOW

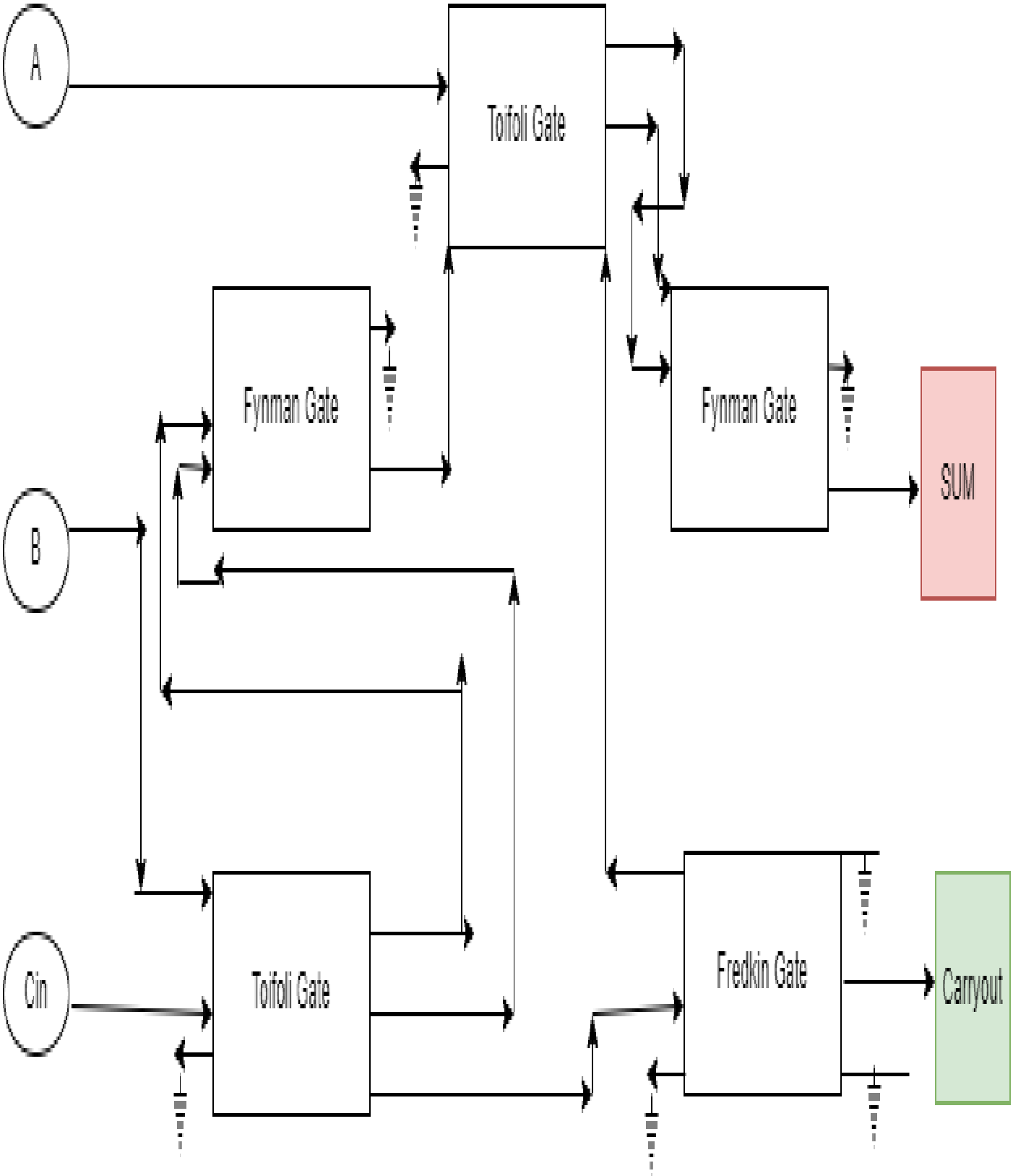


Fig c.

7.PROPOSED DESIGN

7.1 Gate level designs of Reversible circuits using DSCH.

Feynman Gate (FG)

Feynman gate is a 2 inputs 2 outputs (2x2) reversible gate. Another name for Feynman gate is Controlled NOT gate having the mapping (A, B) to (P=A, Q=A⊕B) where A, B are the inputs and P, Q are the outputs, respectively. This gate is useful for copying the required outputs. Therefore, it can be known as a copying gate. It has a quantum cost of one. Its logic circuit is shown in below.

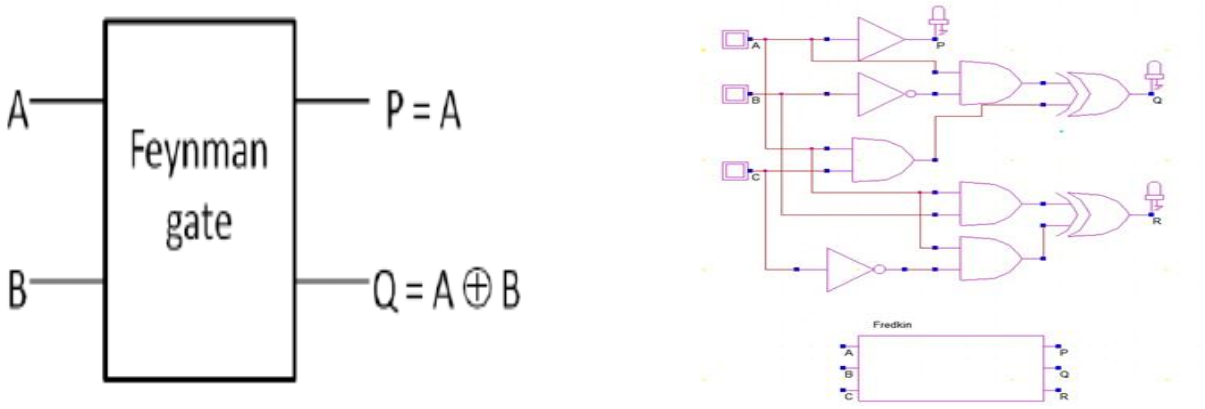


Fig d.

Fredkin Gate (FRG)

Fredkin gate is a 3 inputs 3 outputs (3x3) reversible gate having the mapping (A, B, C) to (P=A, Q=A'B⊕AC, R=AB⊕A'C), where A, B, C are the inputs and P, Q, R are the outputs, respectively. It is also known as a Controlled Permutation gate. It has a quantum cost of five. Its logic circuit is shown in below.

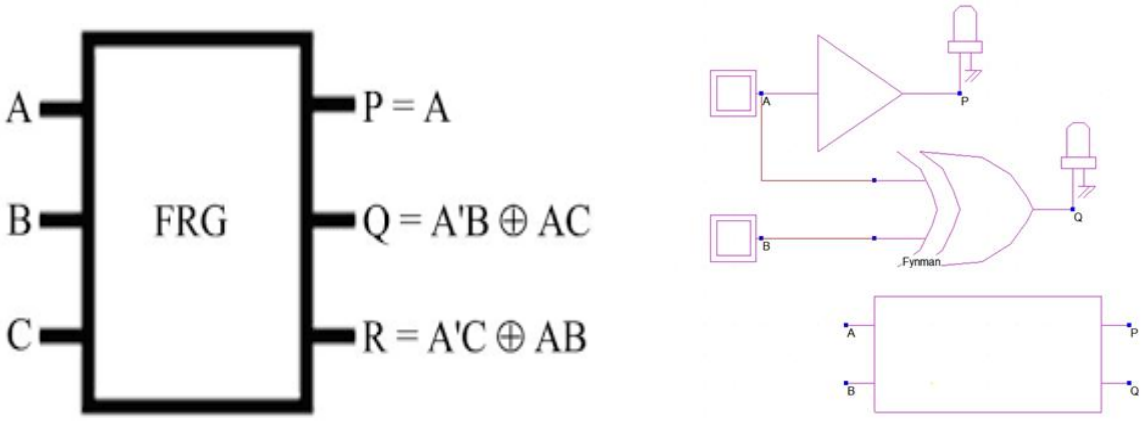
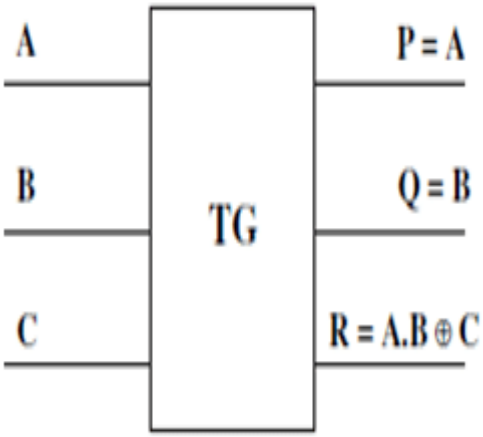


Fig e.

Toffoli Gate (TG)

Toffoli Gate is a 3 inputs 3 outputs (3x3) reversible gate having the mapping (A, B, C) to (P=A, Q=B, R=A.B⊕C). The other name for Toffoli gate is controlled controlled-NOT gate. It has a quantum cost of five. Its logic circuit is shown in below.



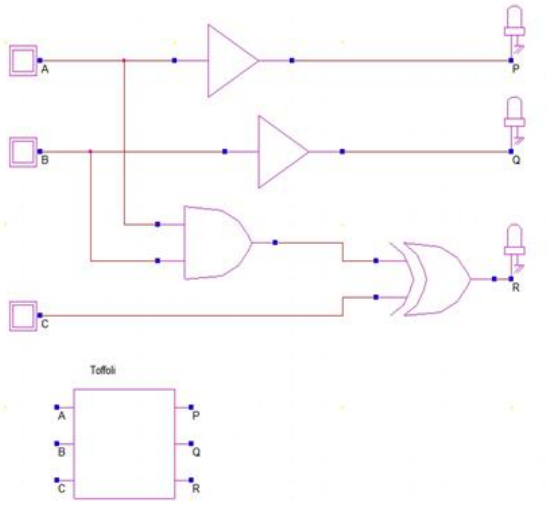


Fig f.

7.2 Symbol level IC design for Full adder circuit using reversible gates with DSCH.

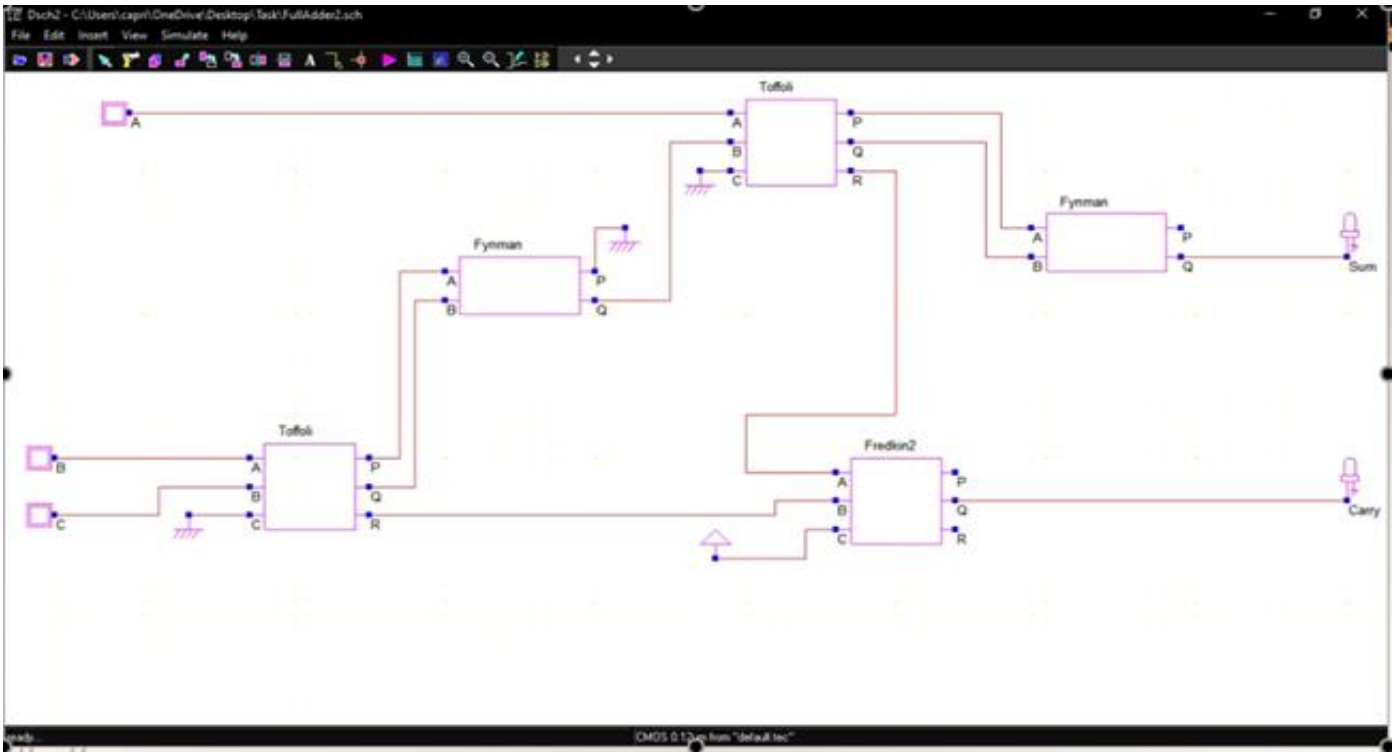


Fig g:

7.3 Physical design with CMOS 90 nm Technology with reversible logic using Microwind.

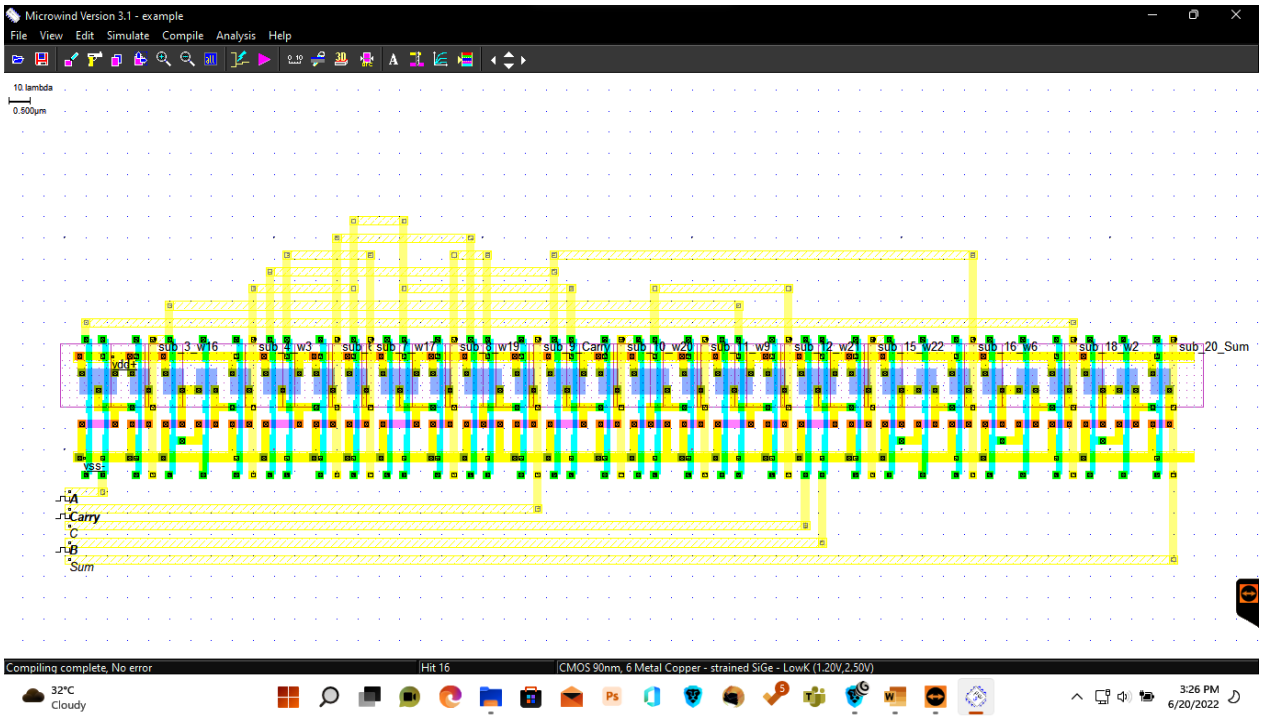


Fig h.

Corresponding Verilog code for the above circuits Fig f.& Fig e.

```
module FULLADDER2(A,B,C,Sum,Carry);
input A,B,Carry;
wire w16,w17,w18,w19, w20, w21, w22;
and #(15) sub_3(w16, w2, A);
xor #(36) sub_4(w3, w16, vss);
and #(15) sub_6(w18, w6, w17);
not #(23) sub_7(w17, w3);
and #(15) sub_8(w19, vdd, w3);
or #(15) sub_9(Carry, w18, w19);
and #(15) sub_10(w20, w6, w3);
or #(8) sub_11(w9, w20, w21);
and #(15) sub_12(w21, vdd, w16);
and #(15) sub_15(w22, C, B);
xor #(22) sub_16(w6, w22, vss);
xor #(22) sub_18(w2, w12, w13);
xor #(15) sub_20(Sum, w4, w5);
endmodule
```

8.EXPERIMENTAL RESULT

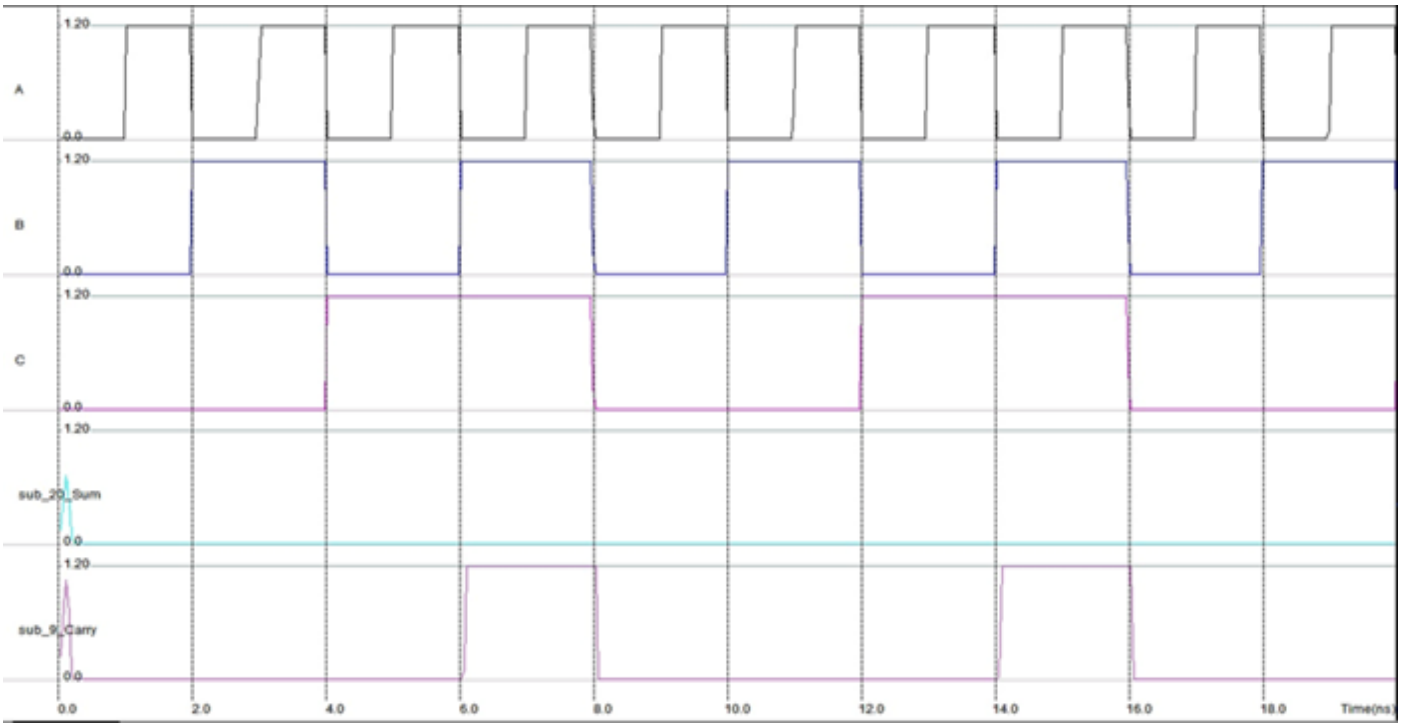


Fig i:

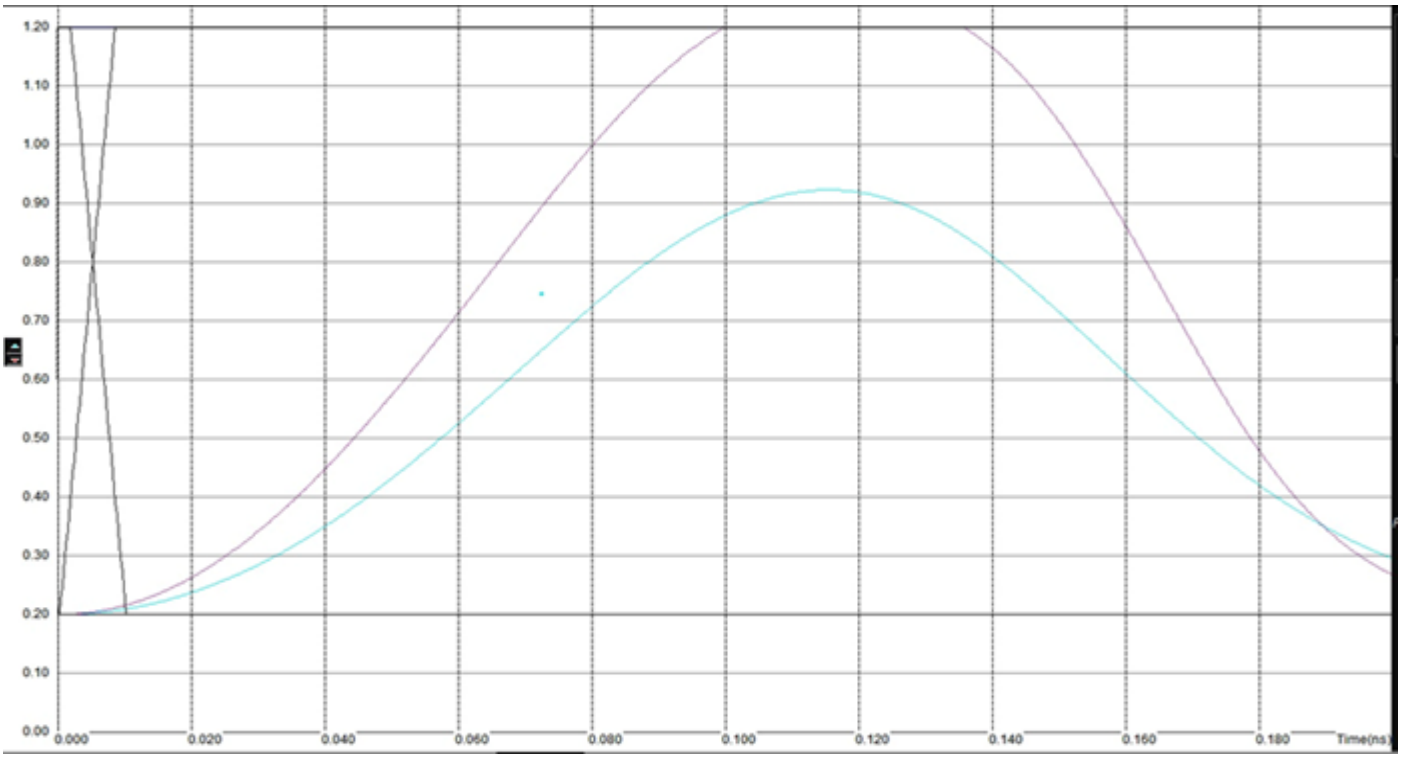


Fig j:

9.FUTURE SCOPE

Reversible engineering has been one of the thrust areas ensuring that continual process of the innovation trends that explore and sustain the resources of the nature. This reversible engineering is used in many fields like quantum computing, low power CMOS design, nanotechnology, optical information processing, digital signal processing, cryptography, etc. These are the digital domain implementations of Reversible and Fault-Tolerant logic gates. Any arbitrary Boolean function can be synthesized by using the proposed parity preserving reversible gates. Not only the possibility of detecting errors is induced inherently in the proposed high-speed adders at their output side but also it allows any fault that affects no more than a single signal that is detectable. The fault tolerant reversible full adder circuits are realized by using two IG gates only. The derived fault tolerant full adder is used for designing other arithmetic- logic circuit by using it as fundamental building block. The proposed reversible gate is designed to have less hardware complexity and efficiency in terms of gate count, garbage outputs and constant input. In this paper, we design BCD adder using carry select logic, Carry-select and Bypass adders using FG gates, and newly designed TG gates.

10. CONCLUSION

The proposed parity preserving reversible New TG gate is better than the existing reversible gates in terms of hardware complexity, gate count, garbage outputs, unit delay and constant inputs. Finally, this paper presents a novel implementation and realization of fault tolerant reversible circuits and demonstrates its superiority than the existing designs in terms of computational complexity. All the circuits are synthesized and verified using DSCH & Microwind software tool from National Instruments corps.

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