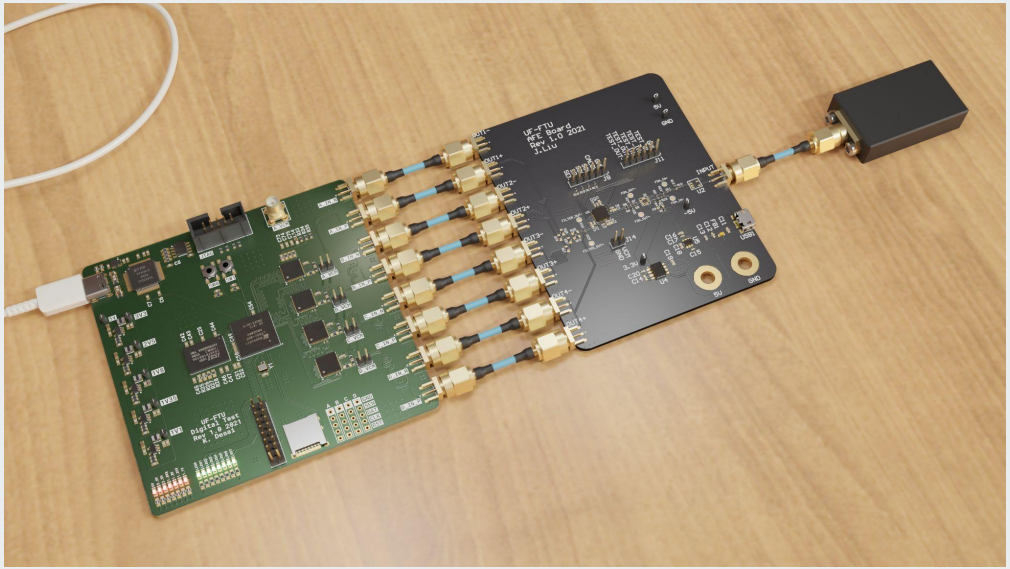
Ultra-Fast CMOS Failure Test Unit (UF-FTU)



Group TL-012
Milestone 4 - Product Review

Showcase Video

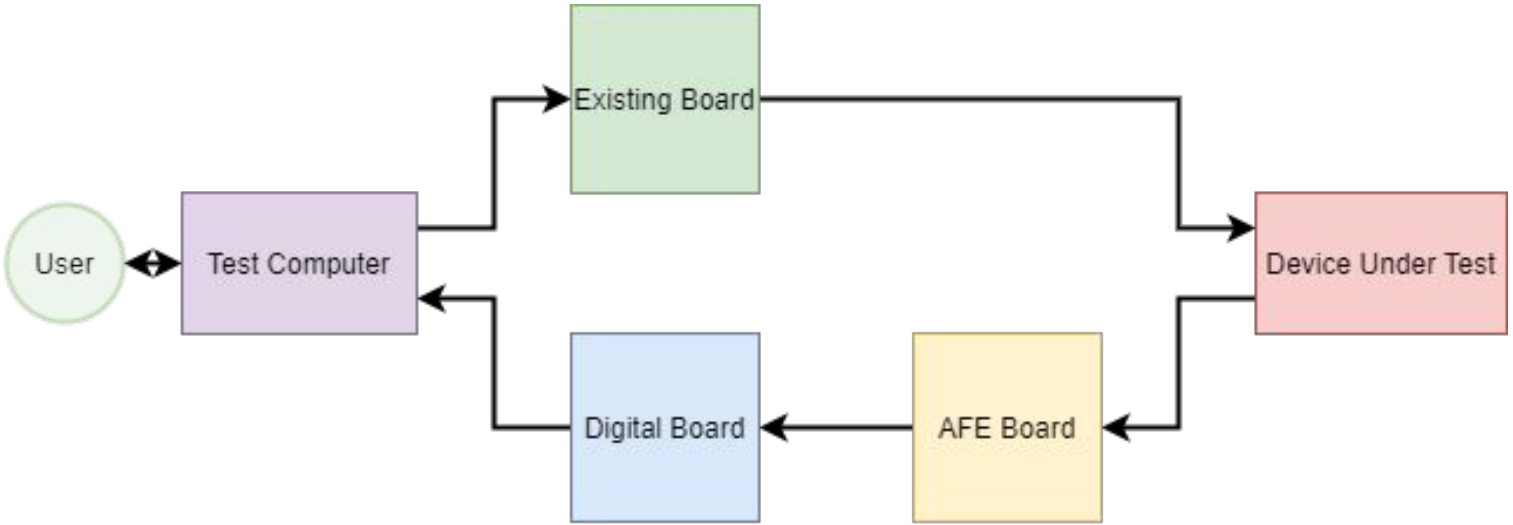
Executive Summary

- UBC System on Chip lab are studying the causes of transistor healing
- Our solution provides a flexible platform for these studies
- Focus on adaptability and performance per dollar
- Allow the client to reduce resources needed to perform these studies

Background and Context

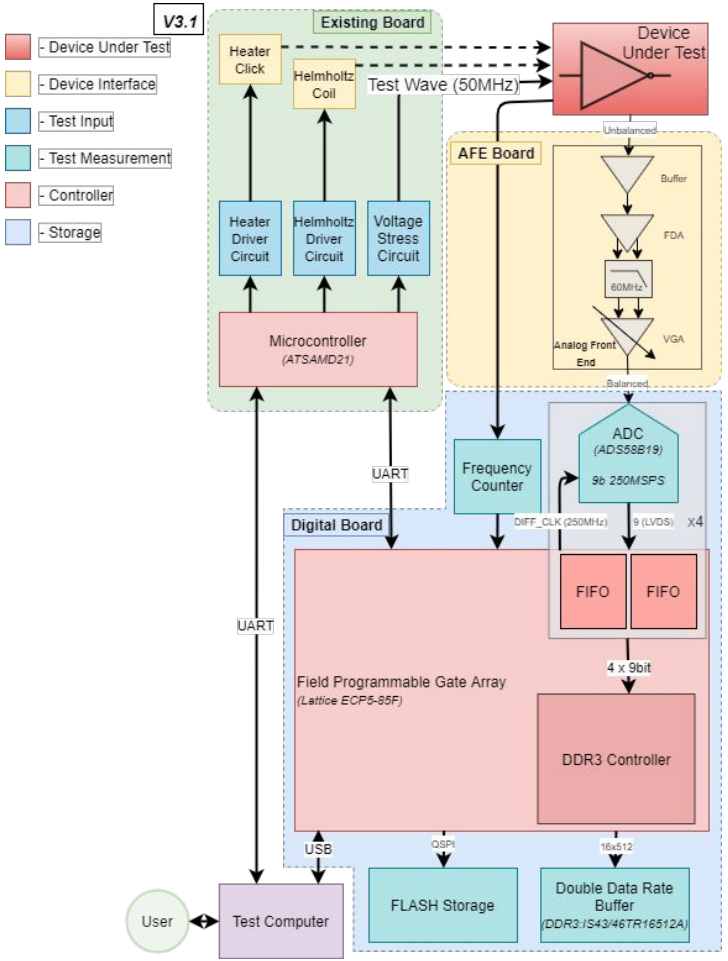
- Transistor Healing: Restoration of transistor performance
- Purpose: Provide a device capable of measuring transistor healing
- Requirements:
    - Sample DUT's output voltage at 1GSPS for half a second
    - Provide 10mV of resolution
    - Present data ready for processing

Design Overview



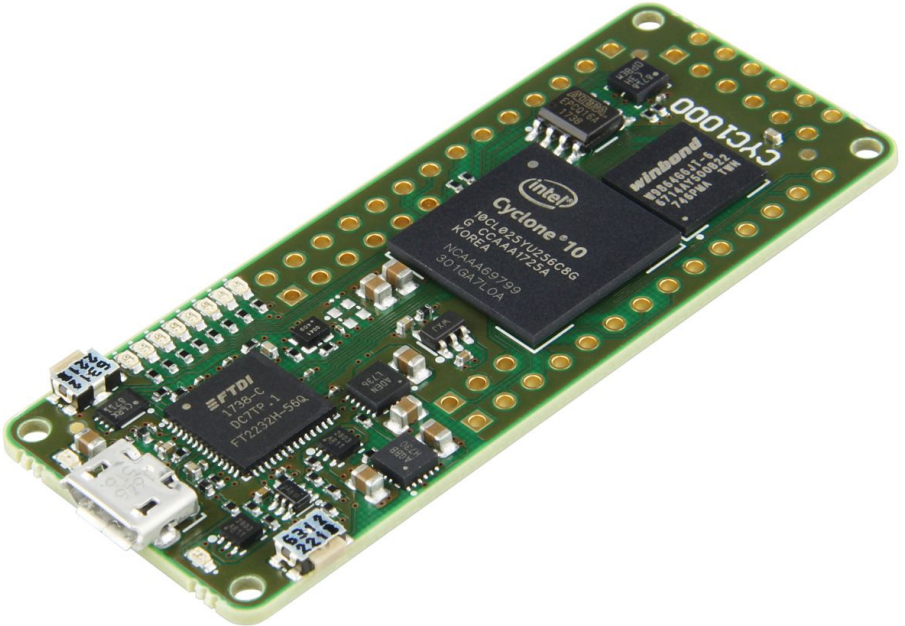
Design Overview

- System consists of 3 boards:
  - Existing Board
    - Developed by SoC Lab
  - AFE Board
  - Digital Board



Device Under Test

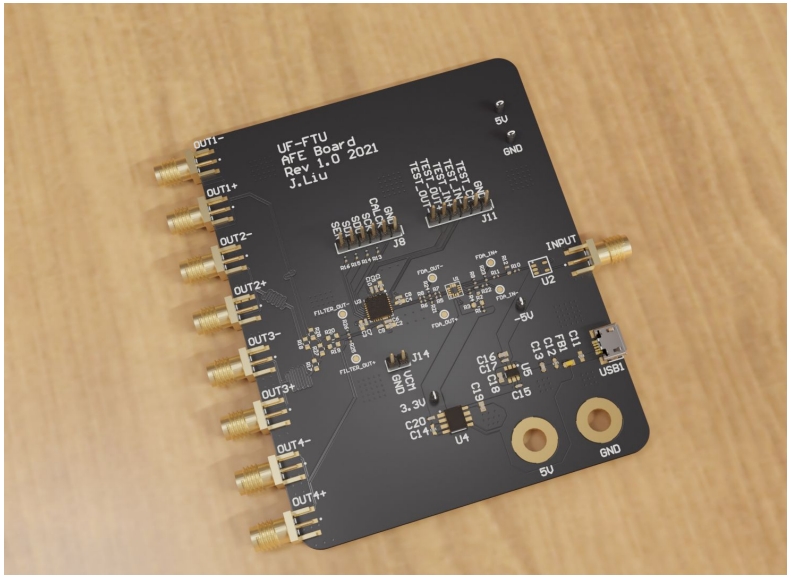
- DUT Specifications
  - Intel Cyclone 10 FPGA
  - Configured as a CMOS Buffer
- Goal
  - Understand buffer performance after aging
  - Attempt to regain performance with transistor healing



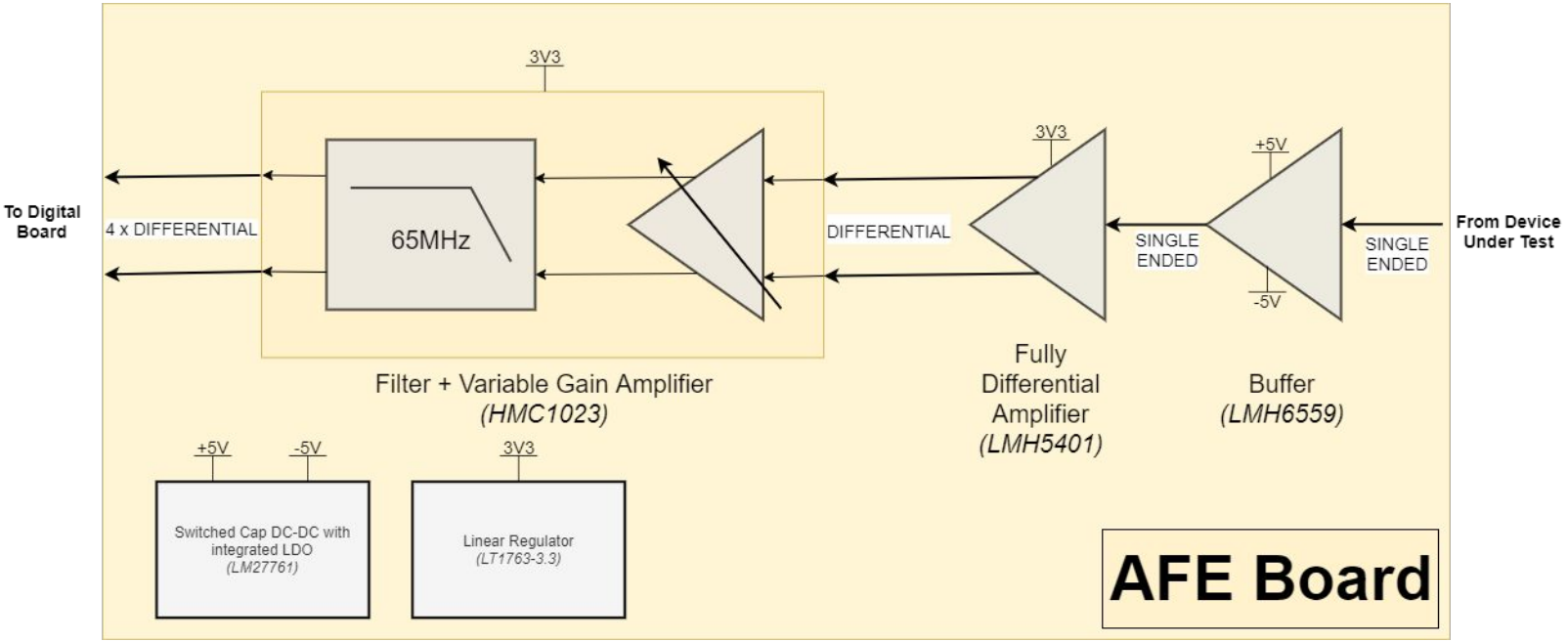
Cyclone 10 Dev Board
(https://shop.trenz-electronic.de/)

Analog Front End (AFE) Board

- Performs
  - Input signal single-ended to differential signaling conversion
  - Input signal scaling and biasing
  - Noise filtering
- Design
  - 4 Layer PCB
  - Onboard power supplies
  - Controlled Impedance and Length Matched Traces

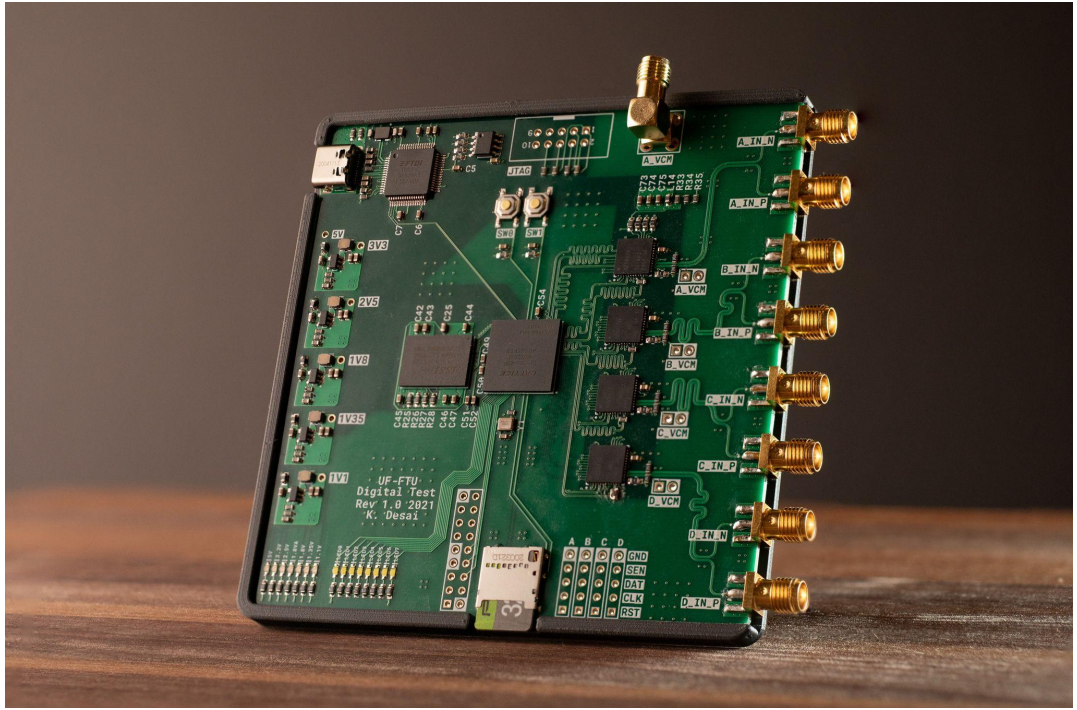


Analog Front End (AFE) Design

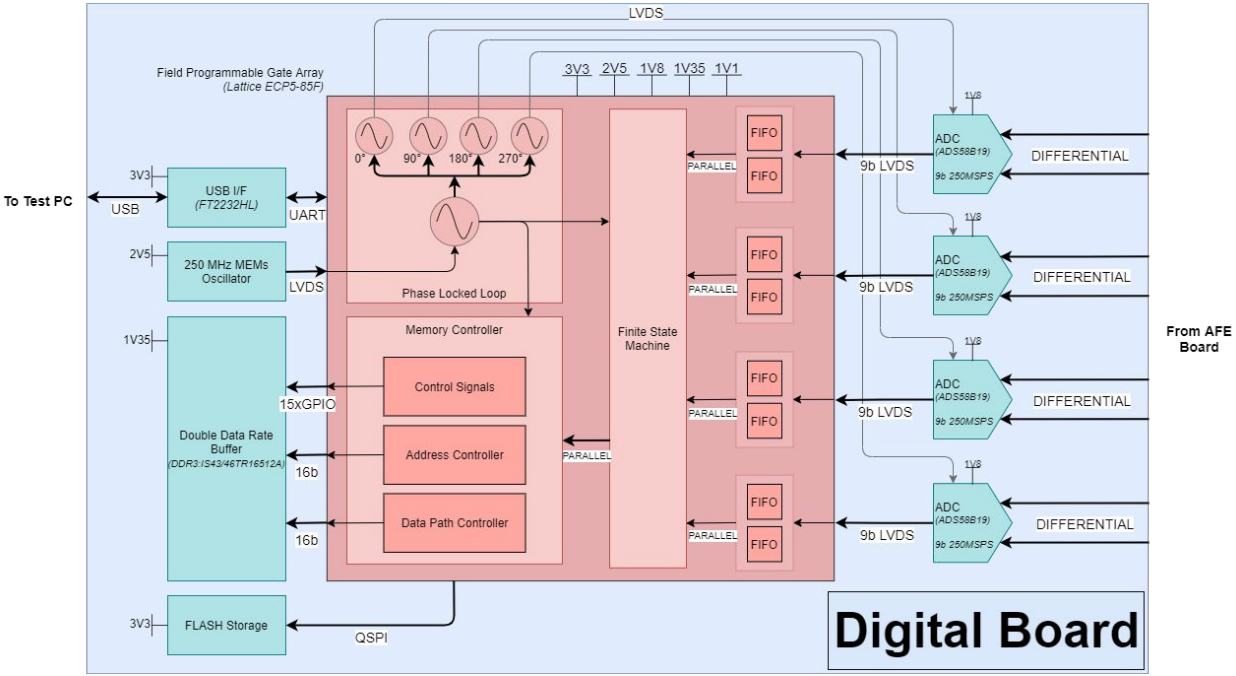


Digital Board

- Performs
  - Digitization of samples
  - Storage of samples
  - Clock Generation
- Design
  - 6 Layer PCB
  - Controlled Impedance and Length Matched Traces
  - Onboard power supplies

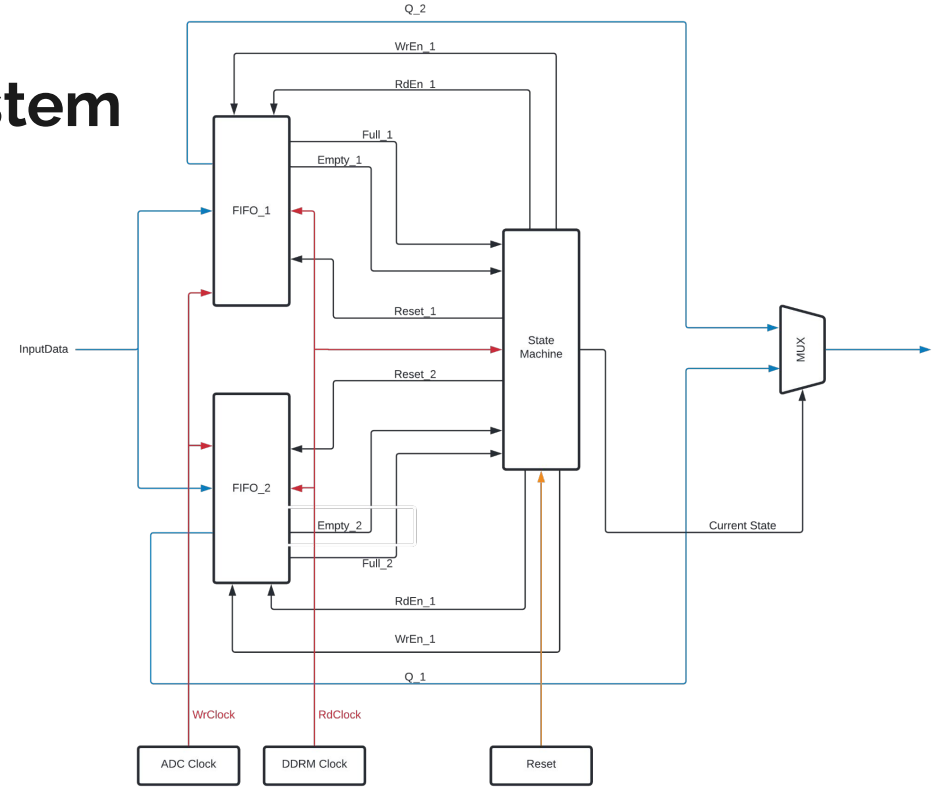


Digital Board



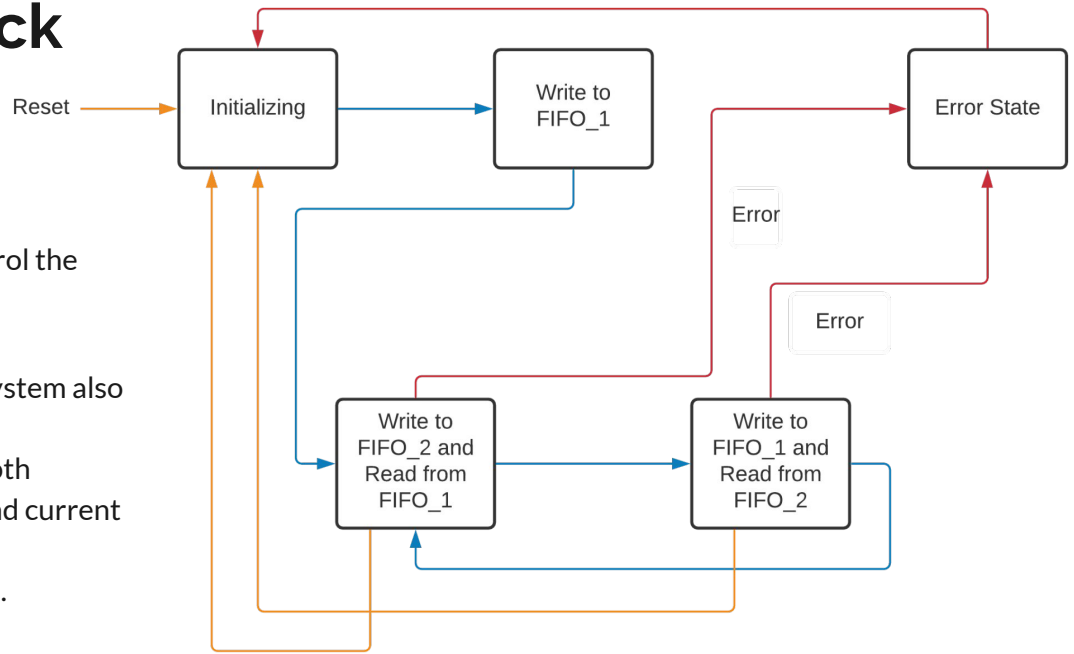
Clock Domain Buffering System

- Performs
  - High speed clock domain crossing.
  - Transferring data collected by ADC to DDR memory.
- Design
  - Use FIFOs are buffers.
  - Control the read/write sequence of the FIFOs and the data flow using a state machine.



Control Logics of Clock Buffering System

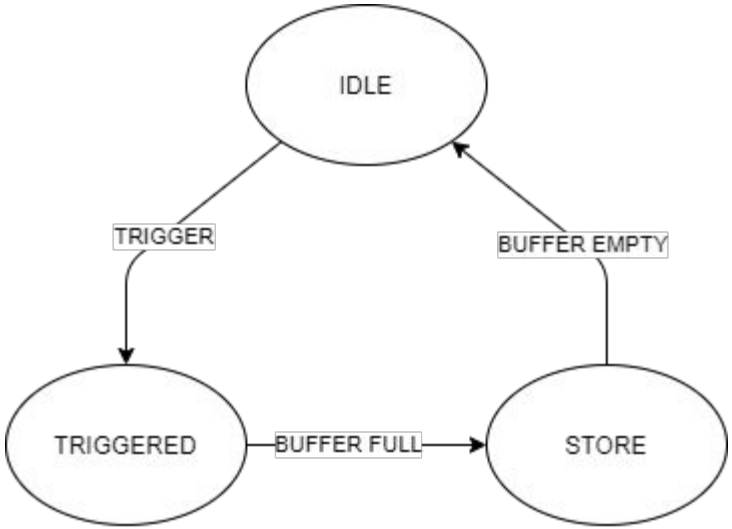
- Perform
  - Working as a control logic to control the Clock Domain Buffering System.
- Design
  - Trigger of the reset of the whole system also resets the state machine
  - The state transition depends on both received feedbacks from FIFOs and current state
  - Error state is also the default state.



System Controller

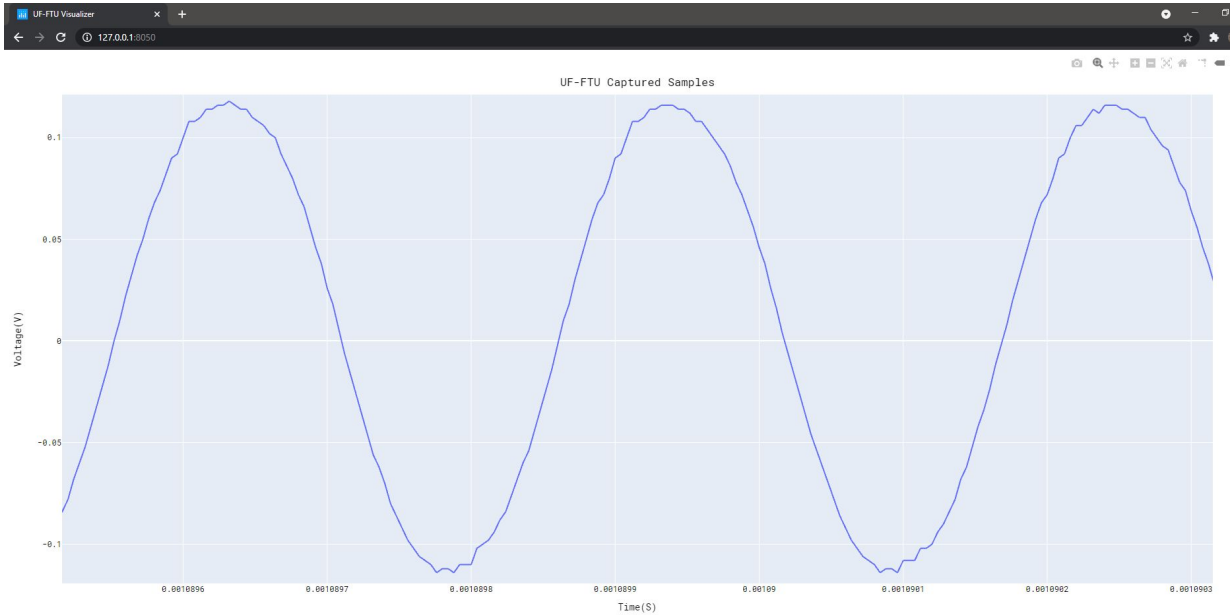
Consists of 3 major states

- Idle
  - The device is waiting a trigger event
- Triggered
  - The device has received the trigger command
  - Fill the buffer until buffer full
- Store
  - Buffer full
  - Transfer data to the mass storage



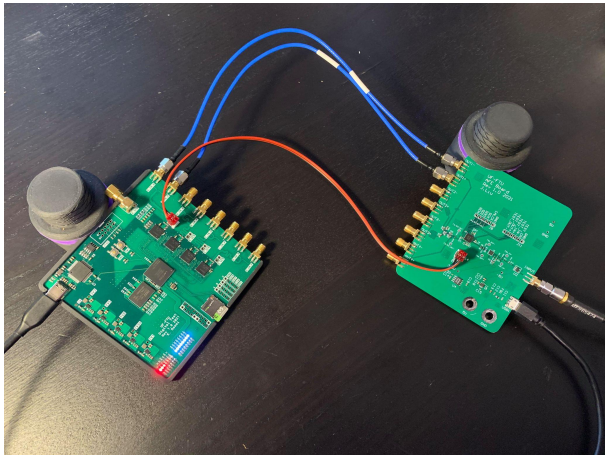
Visualizer

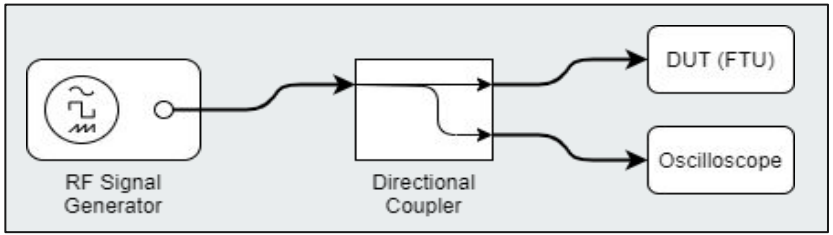
- Performs
  - Easy display of samples
  - Allows data dissection
  - Runs live and stored samples
- Design
  - Automatic SD Card detection
  - End user customizable
  - Written in Python



Validation & Verification

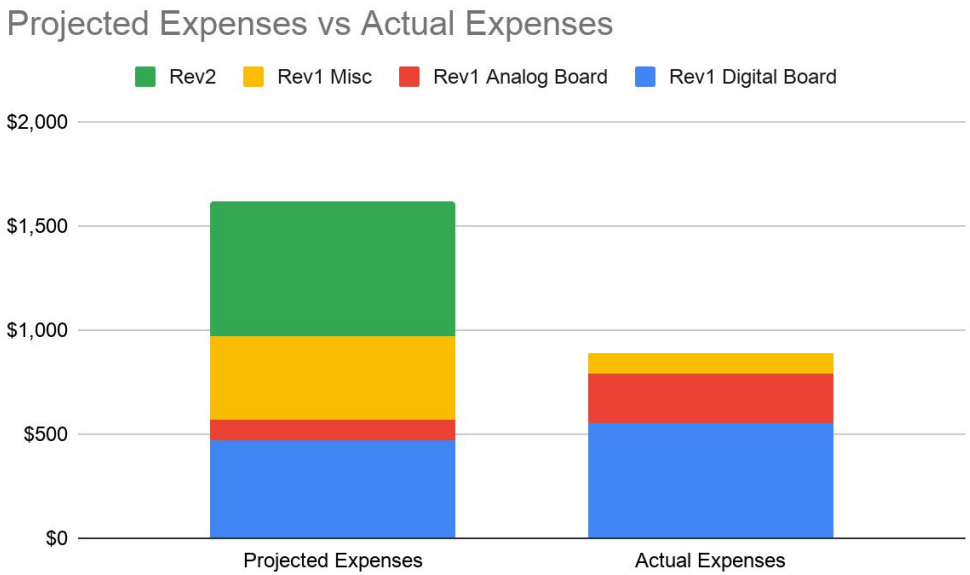
- Subsystems have all gone through simulation & functional testing
- Hardware verification for subsystems successful
- Design has been validated using lab equipment to show design requirements are met





Budget & Resources

- $1,650 budget available
- Initial projected cost of $1,621
- Final cost of $886
- Saved $735 from initial projection
- Equipment
  - Ketan's Lab
  - Remote desktop



Results and Next Steps

- The device is capable of meeting all the requirements
- Client can begin testing transistor healing
- The next steps are:
  - Continued development of the verilog gateware
  - Integration with the existing system

Live Demonstration

Questions?

Appendices

Analog Front End (AFE) Design - ADC Calcs

ADS58B19

Range:

V_in,cm = 1.7V

V_in,diff = 1.5Vpk-pk

- 0.75Vpk-pk swing per input
- +/- 0.375V per input

V_in, + or - = [1.325V to 2.075V]

AFE Design:

Output V_diff = 1.3Vpk-pk max to leave some headroom (0.2V) for ADC

1.3V/(2^9) = 2.5mV/bit resolution, meeting the 10mV resolution requirement

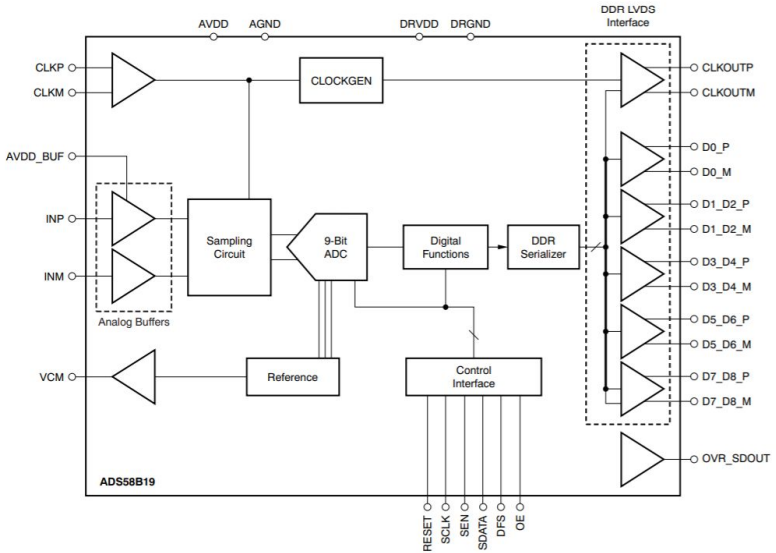
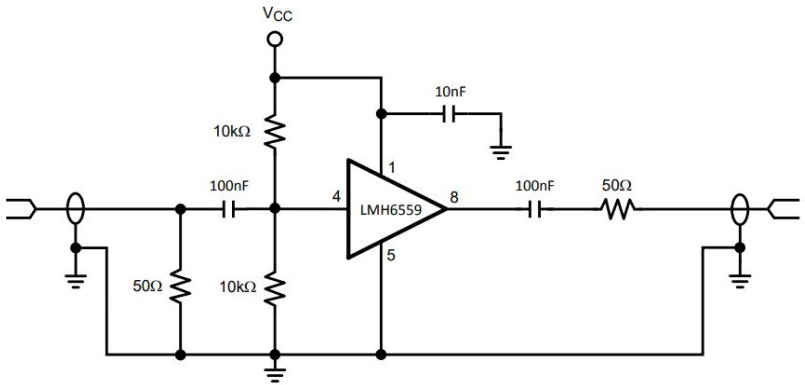


Figure 6. ADS58B19 Block Diagram

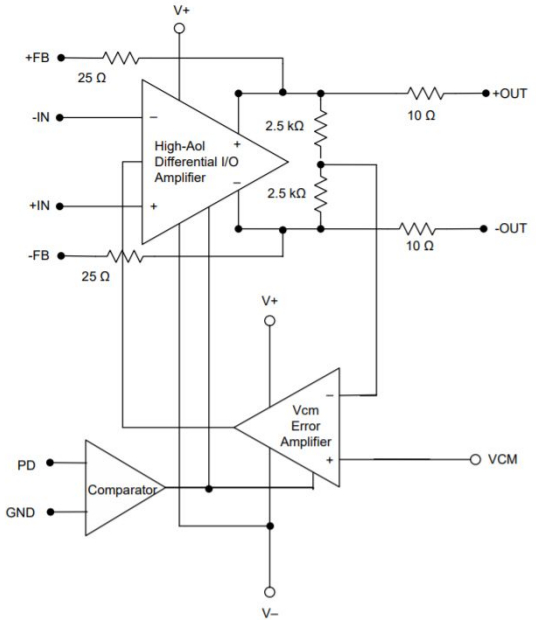
Analog Front End (AFE) Design - Buffer

LMH6559
200kΩ Input impedance
1050MHz large signal bandwidth



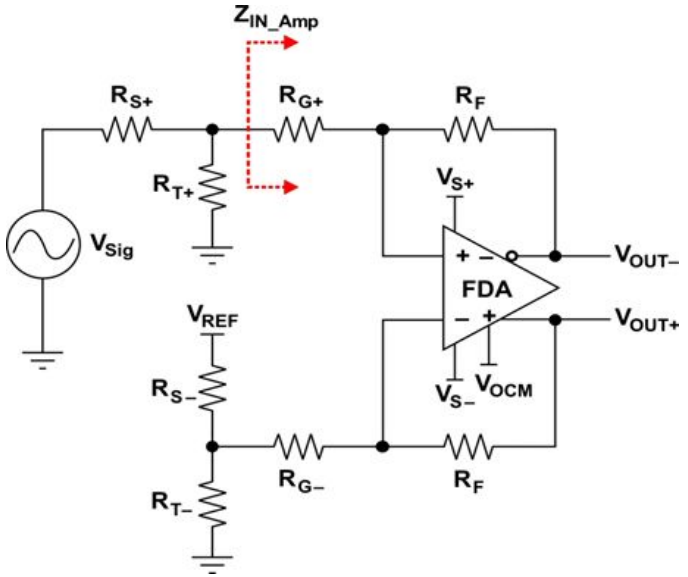
Analog Front End (AFE) Design - FDA

LMH5401
4.4GHz large signal bandwidth
2.8V maximum differential output voltage swing



Analog Front End (AFE) Design - Scaling and Biasing

	A	B	C	D	E
1	Design Inputs (enter values)				
2	V_{Sig_min}	V_{Sig_max}	V_{Out_Diff}	CM	V_{REF}
3	0	2.5	1.3	1.7	3.3
4	Design Choices (enter values)				
5	R_{S+}	R_F	R_{S-}		
6	1000	1000	1000		
7	Calculated Values				
8	V_{OUT}/V_{Sig}	R_{T+}	R_{G+}	R_{T-}	R_{G-}
9	0.52	1083.33	480.00	245.28	803.03
10	Nearest Standard Values				
11	R_{T+}	R_{G+}	R_{T-}	R_{G-}	
12	1070.0	475.0	243.0	806.0	
13	Attenuation and Feedback Factors with Standard Values				
14	B+	B–	Atten+	Atten–	Z_{IN}
15	0.498	0.500	0.517	0.195	1460.177
16	Output Voltages with Standard Values				
17		Min	Mid	Max	V_{OUT_Diff}
18	V_{OUT+}	1.373	1.698	2.023	1.300
19		Max	Mid	Min	Offset
20	V_{OUT-}	2.027	1.702	1.377	-0.004
21					



Analog Front End (AFE) Design - Filter

HMC1023
6th order butterworth low pass filter
5MHz to 72MHz programmable cutoff frequency
0 to 10dB programmable gain
One-time-programmable default setting
SPI interface (<30MHz)

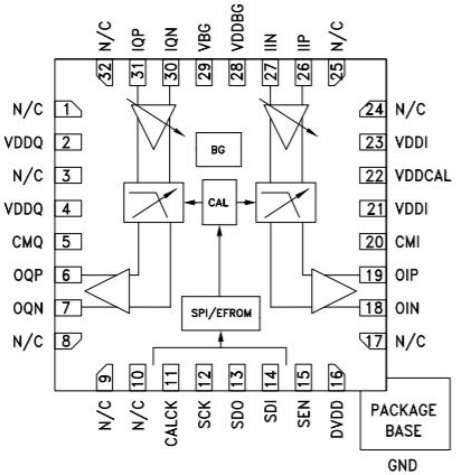
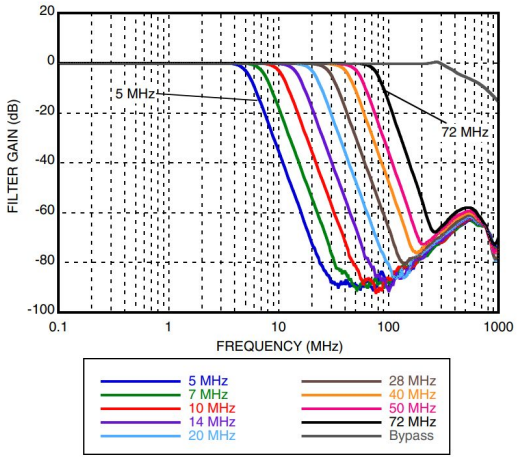


Figure 1. Filter Attenuation (all Bandwidths) [1]

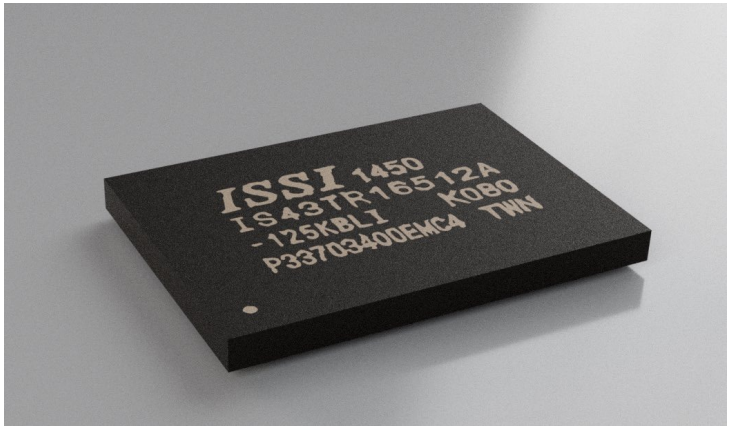


Clock Domain Buffering System

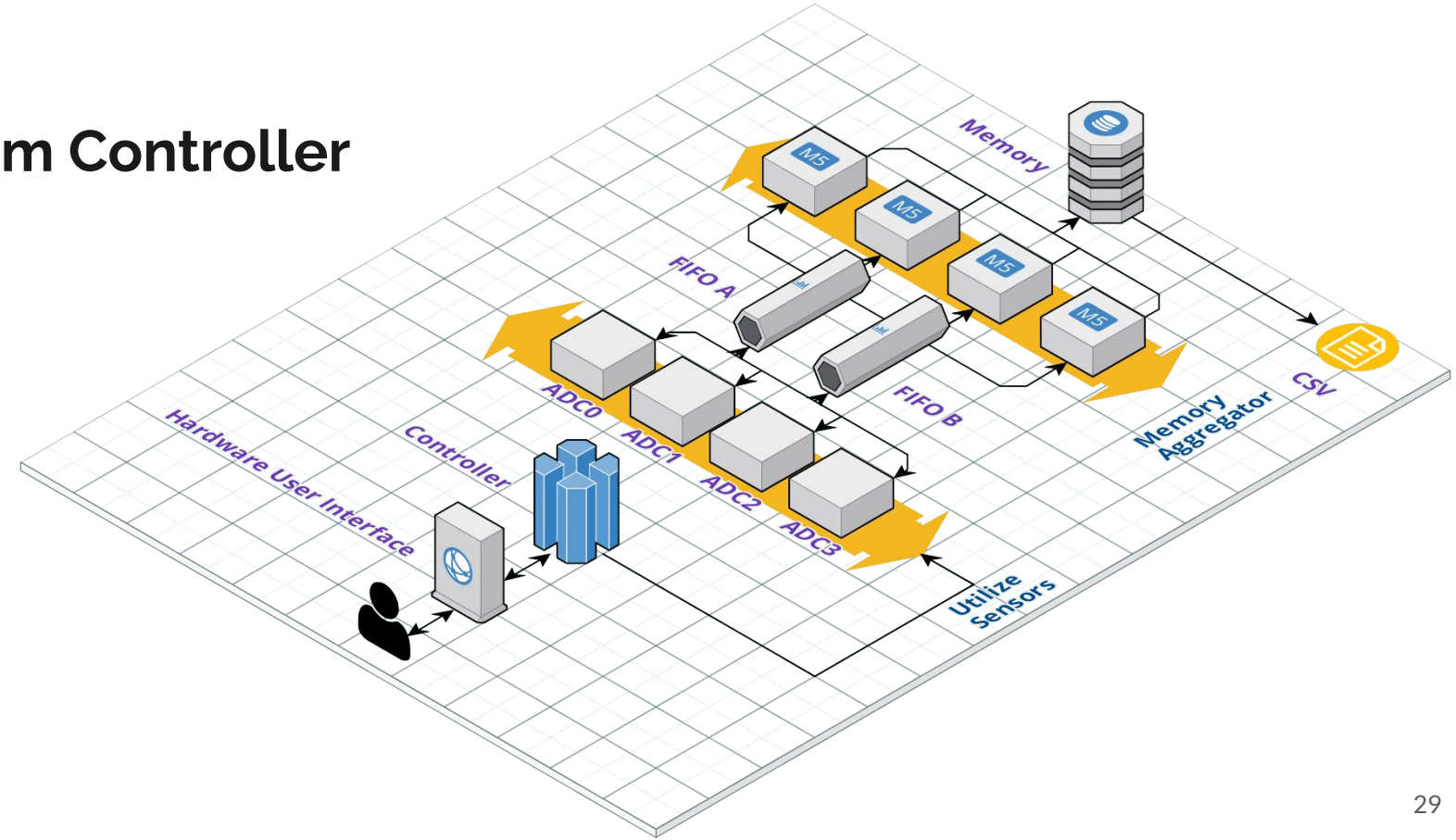
```
casex({current_stage, full_1, full_2, empty_1, empty_2})
  {2'b00, 2'b00, 2'b11} : {reset_1, reset_2, RdEn_1, RdEn_2, WrEn_1, WrEn_2, next_stage} = {2'b00, 2'b00, 2'b10, 2'b00};//Reset successed, start filling FIFO_1
  {2'b00, 2'b00, 2'b01} : {reset_1, reset_2, RdEn_1, RdEn_2, WrEn_1, WrEn_2, next_stage} = {2'b00, 2'b00, 2'b10, 2'b00};//Data recived by FIFO_1, but FIFO_1 is not filled yet
  {2'b00, 2'b10, 2'b01} : {reset_1, reset_2, RdEn_1, RdEn_2, WrEn_1, WrEn_2, next_stage} = {2'b00, 2'b00, 2'b00, 2'b01};//FIFO_1 is filled. FIFO_2 is still at initial stage.
  //Start read from FIFO_1 while write to FIFO_2
  {2'b01, 2'b10, 2'b01} : {reset_1, reset_2, RdEn_1, RdEn_2, WrEn_1, WrEn_2, next_stage} = {2'b00, 2'b10, 2'b01, 2'b01};//Start read from FIFO_1 while write to FIFO_2
  {2'b01, 2'b00, 2'b00} : {reset_1, reset_2, RdEn_1, RdEn_2, WrEn_1, WrEn_2, next_stage} = {2'b00, 2'b10, 2'b01, 2'b01};//Read from FIFO_1 and remove data from FIFO_1. FIFO_2 is not empty anymore
  {2'b01, 2'b00, 2'b10} : {reset_1, reset_2, RdEn_1, RdEn_2, WrEn_1, WrEn_2, next_stage} = {2'b00, 2'b00, 2'b01, 2'b00};//FIFO_1 is emptied and FIFO_2 is not filled yet> (Read speed is faster than write).Pause sending data to DDR until FIFO_2is filled
  {2'b01, 2'b01, 2'b10} : {reset_1, reset_2, RdEn_1, RdEn_2, WrEn_1, WrEn_2, next_stage} = {2'b00, 2'b00, 2'b00, 2'b10};//FIFO_2 is filled and FIFO_1 is emptied. Ready to switch to read-FIFO_2 and write-FIFO_1
  ///Start read from FIFO_2 while write to FIFO_1
  {2'b10, 2'b01, 2'b10} : {reset_1, reset_2, RdEn_1, RdEn_2, WrEn_1, WrEn_2, next_stage} = {2'b00, 2'b01, 2'b10, 2'b10};
  {2'b10, 2'b00, 2'b00} : {reset_1, reset_2, RdEn_1, RdEn_2, WrEn_1, WrEn_2, next_stage} = {2'b00, 2'b01, 2'b10, 2'b10};//Read from FIFO_2 and remove data from FIFO_2. FIFO_1 is not empty anymore
  {2'b10, 2'b00, 2'b01} : {reset_1, reset_2, RdEn_1, RdEn_2, WrEn_1, WrEn_2, next_stage} = {2'b00, 2'b00, 2'b01, 2'b00};//FIFO_2 is emptied and FIFO_1 is not filled yet (Read speed is faster than write).Pause sending data to DDR until FIFO_2is filled
  {2'b01, 2'b10, 2'b01} : {reset_1, reset_2, RdEn_1, RdEn_2, WrEn_1, WrEn_2, next_stage} = {2'b00, 2'b00, 2'b00, 2'b01};//FIFO_1 is filled and FIFO_2 is emptied. Ready to switch to read-FIFO_1 and write-FIFO_2

  default : {reset_1, reset_2, RdEn_1, RdEn_2, WrEn_1, WrEn_2, next_stage} = {2'b11, 2'b00, 2'b00, 2'b11};//2'b11 is the error stage. We are not supposed to trigger the default stage unless some unexpected feedbacks from FIFOs are recived.
```

DDR3 Memory

- Performs
  - Stores all test data received from the ADC buffers
  - 8 Gb DDR3 RAM for multiple cycles
  - Performance oriented memory controller at upto 12.8 Gb/s
- Design
  - Programmed in SystemVerilog
  - Uses Lattice Diamond DDR3 Controller
  - Validated functionally

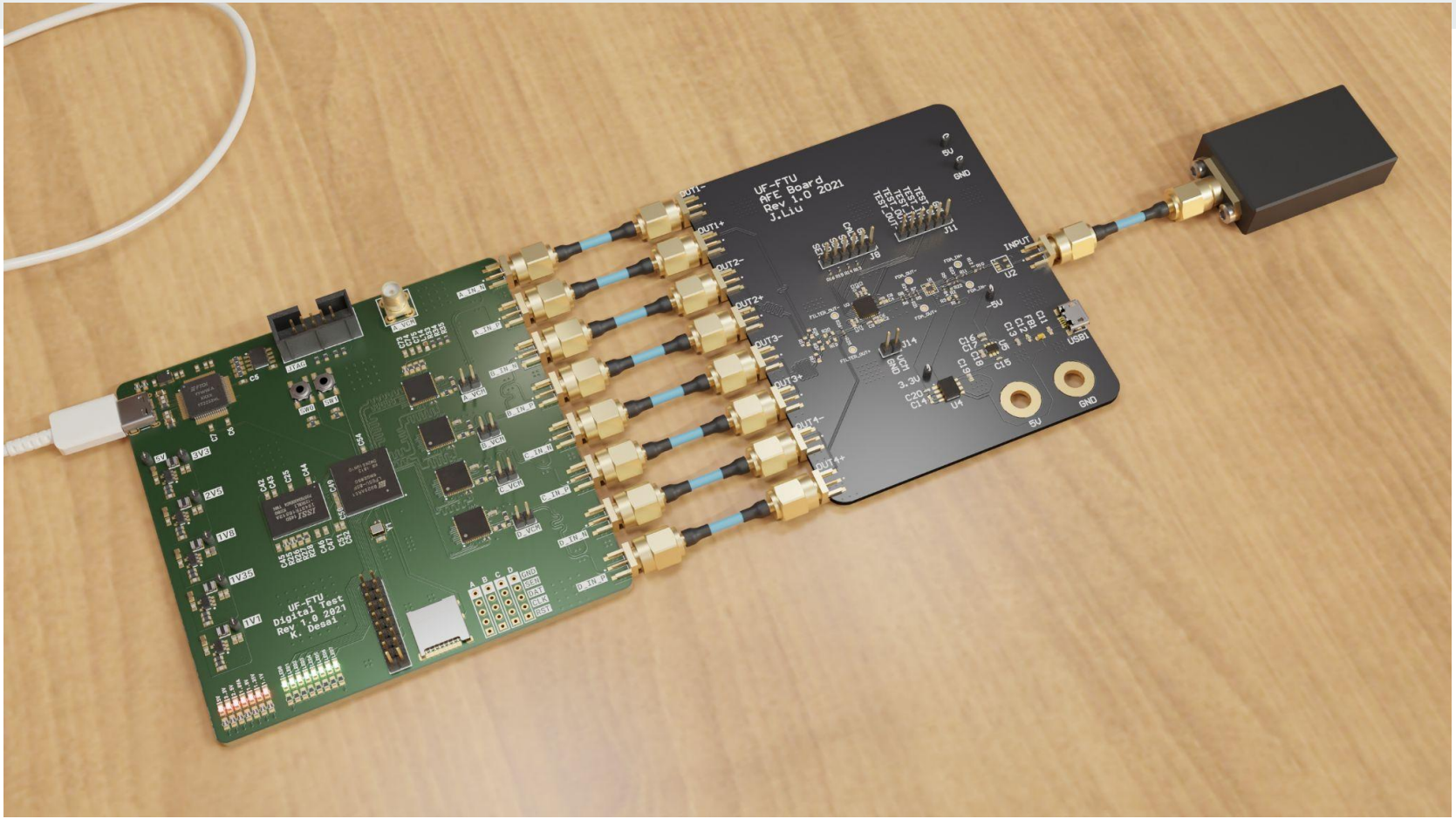


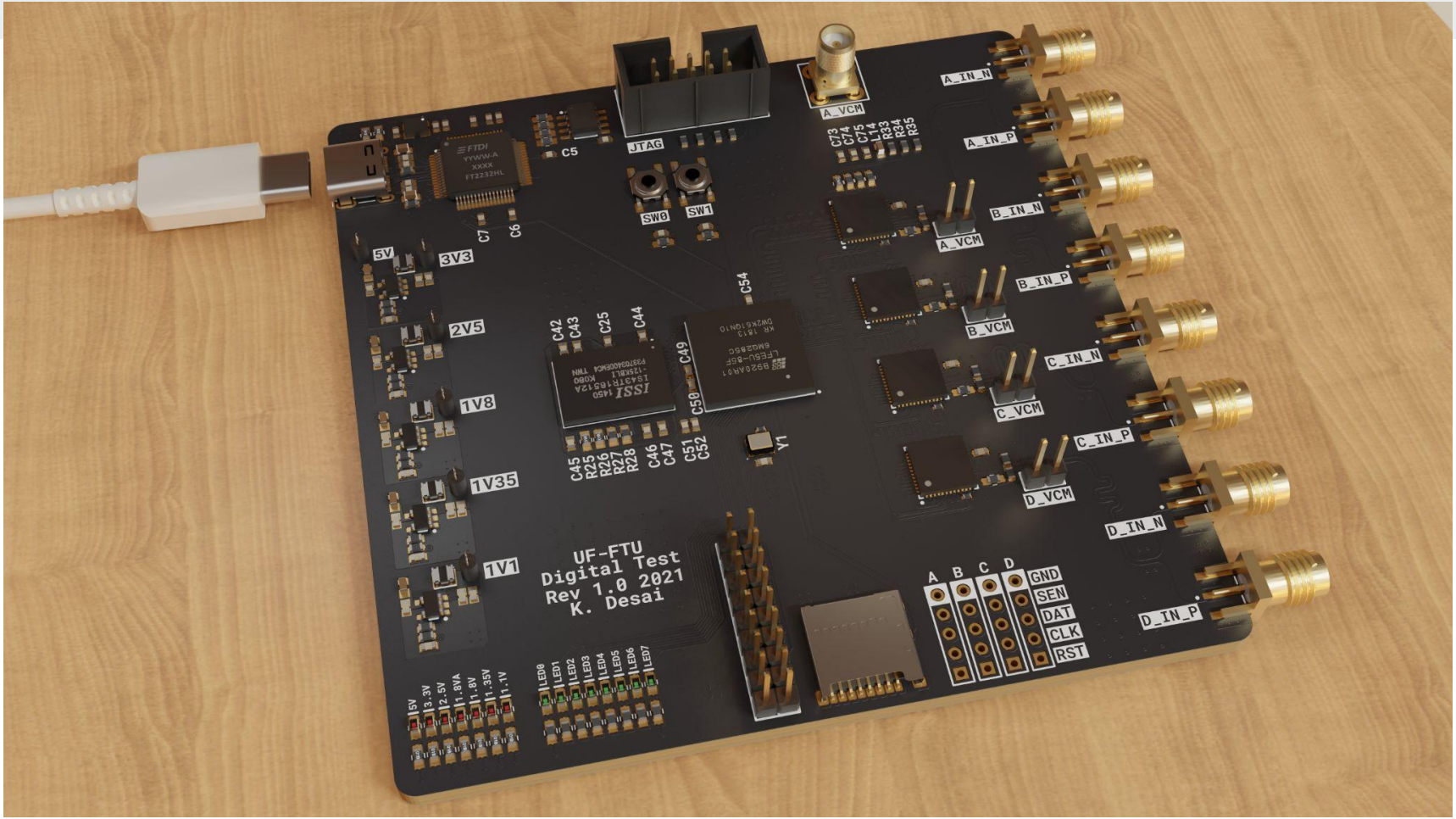
System Controller

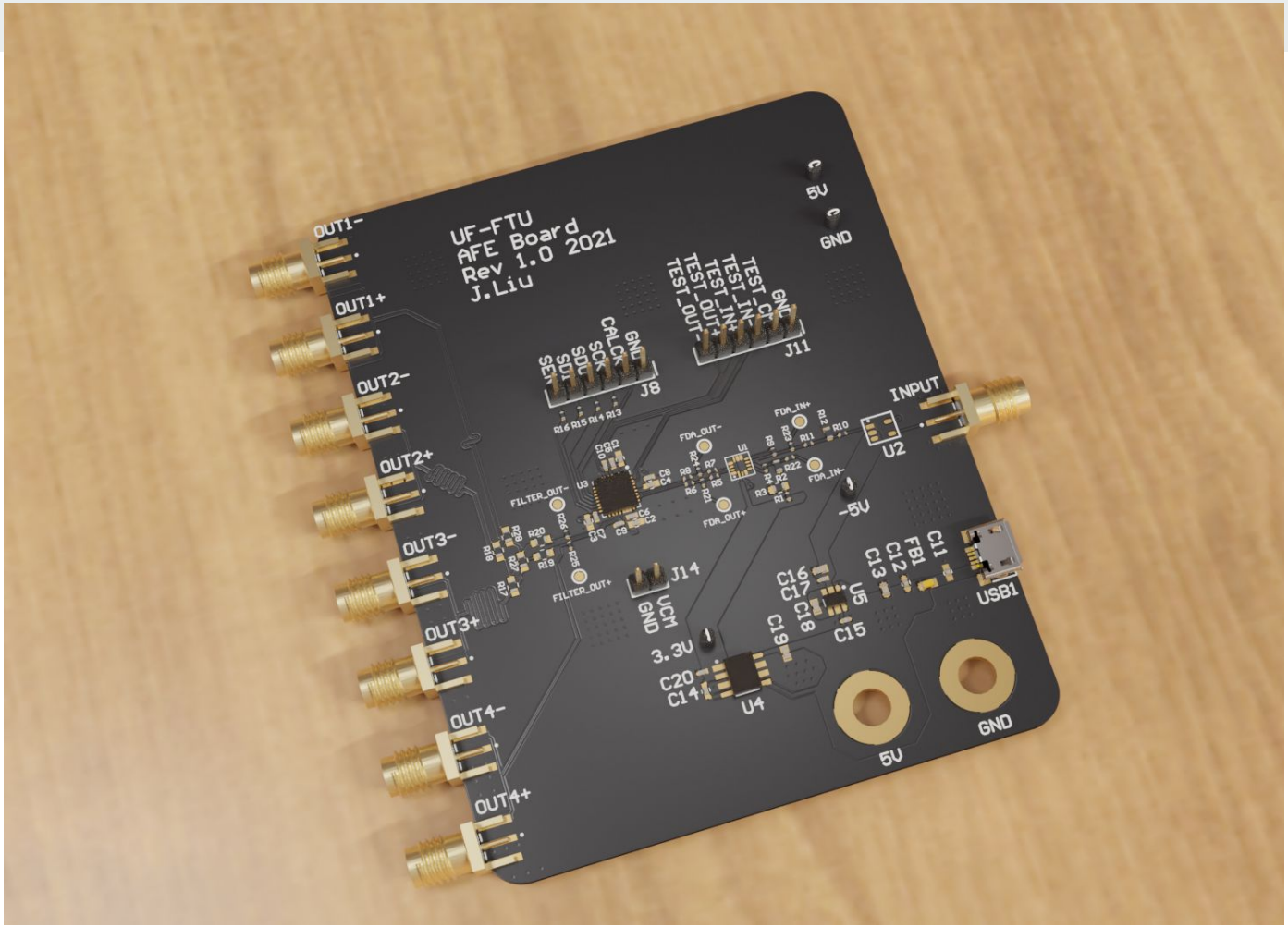


Visualizer

```
def triangle(length, amplitude):
    section = length // 4
    for direction in (1, -1):
        for i in range(section):
            yield i * (amplitude / section) * direction
        for i in range(section):
            yield (amplitude - (i * (amplitude / section))) * direction


@app.callback(
            [Output('live-graph', 'figure'), Output('live-graph','animate'), Output('graph-update','disabled')],
            [Input("graph-update", "n_intervals"), Input('submit-val', 'n_clicks')]
            )
def update_graph_scatter(input_data, click):
    global counter
    global X
    global Y
    global old_clicks

    #reset waveform
    if old_clicks != click:
        X = deque()
        Y = deque()
        counter = 0
        old_clicks = click
        data = plotly.graph_objs.Scatter(
            x=list(X),
            y=list(Y),
            name='Scatter',
            mode= 'lines+markers'
        )
        return [
                    {
                        'data': [data],
                        'layout' : go.Layout(
                                                xaxis=dict(range=[0,0], title="Time (Milliseconds)"),
                                                yaxis=dict(range=[0,0], title="Measured Voltage (Millivolts)"),
                                                title="UF-FTU Captured Waveform",
```


UF-FTU
AFE Board
Rev 1.0 2021
J.Liu
UF-FTU
Digital Test
Rev 1.0 2021
K. Dessai
INPUT
USB1
5V
GND
3.3V


UF-FTU
Digital Test
Rev 1.0 2021
K. Desai
A_IN_N
A_IN_P
B_IN_N
B_IN_P
C_IN_N
C_IN_P
D_IN_N
D_IN_P
A_VCM
B_VCM
C_VCM
D_VCM
JTAG
SW0
SW1
5V
3V3
2V5
1V8
1V35
1V1
GND
SEN
DAT
CLK
RST


UF-FTU
AFE Board
Rev 1.0 2021
J.Liu
OUT1-
OUT1+
OUT2-
OUT2+
OUT3-
OUT3+
OUT4-
OUT4+
5V
GND
SEN
SDI
SDO
SCK
CAL
GND
J8
TEST_OUT-
TEST_OUT+
TEST_IN-
TEST_IN+
TEST_CAL
GND
J11
INPUT
U2
FDA_IN+
FDA_IN-
FDA_OUT-
FDA_OUT+
-5V
FILTER_OUT-
FILTER_OUT+
U3
J14
VCM
GND
3.3V
U4
U5
USB1
FB1
5V
GND