Project Overview

ULTRA-FAST CMOS FAILURE TEST UNIT

Ivanov Group at UBC SoC Lab

Capstone Group 12

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Executive Summary

The Ivanov Group at the University of British Columbia's System-on-a-Chip lab required an integrated solution to perform the study of transistor healing in CMOS Integrated Circuits. Such studies consist of applying high stress to a device under test and observing the transistor behavior when stresses are removed. Inside the transistor these stresses cause defects in the Silicon Dioxide layer between the gate and the channel. The result of this is increased current leakage and reduced performance. Upon removing the stresses these defects can be removed, recovering some of the original performance [1], the small timeframe in which this occurs necessitates ultra fast sampling rates.

Our team has created a modular integrated system consisting of two boards; an analog front end and a digital board back end to automate the entire testing procedure. The solution interfaces with various testing elements to apply desired stresses such as temperature stresses, magnetic stresses, and voltage stresses. Simultaneously the front end converts the input signal into differential signals and scales it appropriately to match the high speed ADCs input signal range and filters the input signal to prevent high frequency aliasing noise before it is fed into the digital board. The digital board takes high-accuracy measurements with resolutions exceeding 10mV at ultra fast speeds of 1 GSPS, and storing up to 8 gigabits of samples.

The system provides a foundation for further custom measurement and processing tools to be easily generated. Our design maximizes the performance per dollar to allow scalability and replication for industrial implementation. We have achieved this through minimizing our part count, reducing the bill of materials and decreasing production costs.

Our solution has been extensively verified and validated to consistently exceed all client requirements. This has been done throughout all stages of development from design stage to integration and finally, real world testing. This helped us ensure a fully working product and gain our client's confidence in the device and overall design.

The Ivanov Group is now able to better analyze transistor behavior, and make more informed decisions in the field of research and development. We have heavily reduced the resources needed to provide an insight into the fundamental physics of these CMOS ICs. In the future our design will be replicated for utilization by the Ivanov group's client Huawei.

List of Tables and Figures

List of Abbreviations

ADC - Analog to Digital Converter

AFE - Analog Front End

BOM - Bill of Materials

CAD - Computer Aided Design

CMOS - Complementary Metal-Oxide Semiconductor

DDR - Double Data Rate (Memory)

DUT - Device Under Test

ECE - Electrical and Computer Engineering

FPGA - Field Programmable Gate Array

GSPS - Giga Samples Per Second

GUI - Graphic User Interface

ICs - Integrated Circuits

KSPS - Kilo Samples Per Second

LVDS - Low Voltage Differential Signalling

MCU - Microcontroller Unit

PCB - Printed Circuit Board

Rev - Revision

SATA - Serial Advanced Technology Attachment

SoC - System-On-a-chip

SSD - Solid State Drive

UBC - The University of British Columbia

UF-FTU - Ultra Fast - Failure Test Unit

V&V - Verification and validation

1.0 About This Document

1.1 Purpose

The purpose of this document is to provide a high-level overview of the Capstone project titled, “Ultra-Fast CMOS Failure Test Unit”. The intention is to assist the audience in gaining an understanding of the background and context of the project; the process we undertook and finally the results our project has achieved for the Ivanov Group.

1.2 Audience

This document is intended for the following stakeholders:

Ivanov Group at UBC SoC: The group headed by Dr. Andre Ivanov, with Arash Sheikholeslam as the primary contact of the Capstone Team is responsible for setting the guidelines and overseeing the progress of the project.

UBC ECE faculty supervisors: Since this project is a part of the Capstone Program at UBC, the evaluating body of technical Capstone instructors and teaching assistants play an important role in reviewing this document and assessing the Capstone Team’s performance.

1.3 Related Documents

There are six essential documents under revision that will provide more information regarding the project. The related documents that will be included are:

1. Requirements Specifications
2. Design Specifications
3. Verification & Validation Specifications
4. List of Deliverables
5. Project Management
6. Project Retrospective

These documents elaborate on the project and provide an in-depth analysis of the decision making process through the duration of the project.

2.0 Background and Context

Transistor healing is a phenomenon that occurs when the high stresses of CMOS lifetime testing are removed. When transistors age, degradation to the oxide layer between the gate and channel causes imperfections to occur. These imperfections result in higher leakage current and reduced performance. When these transistors are allowed to heal, this oxide layer can release some of these impurities, restoring the channel performance. This can be seen in the voltage transfer characteristics of a transistor. By monitoring the output voltage we can observe factors such as gate threshold and channel length modulation to better determine the impact of this healing. To gain a better understanding of the fundamental physics associated with this phenomenon, the Ivanov Group at the UBC SoC lab are in need of a device that is capable of measuring at very high sample rates. While commercial off-the-shelf solutions exist, none are suitably tailored to this scenario and either do not fulfill the requirements or are too expensive.

To solve this problem, our team developed a system capable of performing three main tasks: generating the test environment for these CMOS ICs, performing measurements, and displaying the results in a quick and easy to use manner. The team worked alongside the FTU being developed by the Ivanov Group. The FTU developed is capable of generating the test environment consisting of a PCB heater, a Helmholtz coil and a programmable voltage source. These variables control the temperature, magnetic field strength and supply voltage seen by the DUT. Scenarios in which transistor healing occurs are generated by subjecting the DUT to high stress and then subsequently relieving it of the stress. Thus the overall test flow consists of applying an adverse environment to the DUT and allowing steady state operation to be achieved, after which the stresses are removed and a sample of the transistor output is taken to observe the characteristics of the healing in depth.

The Ivanov Group’s design has been integrated into our design with our system being focused on high performance sampling. Since the Ivanov Group would like the ability to test a variety of devices, our solution is highly configurable to the user, taking advantage of adaptable hardware such as Field Programmable Gate Arrays, high speed data converters and high speed memory. This method of configurable hardware gives a foundation for the Ivanov Group to build upon and customize the final product to a wide set of applications. Therefore, the overall project achieves an expandable, high performance, and easy to use data acquisition device with additional results processing system to comprehensively facilitate and automate failure testing.

3.0 Goals, Objectives and Constraints

To facilitate the Ivanov Group's research, a UF-FTU is needed to further analyze transistor healing. Based on the requirements set by the client, the following goals, objectives and constraints are defined.

3.1 Goals

To deliver a device capable of:

- Controlling test environment
- Measuring the DUT's outputs
- Measuring Random Telegraphic Noise
- Displaying the results to a user

3.2 Objectives

- To control the test environment, such as the temperature, magnetic field and voltage
- To measure DUT outputs at 1 GSPS for 500 milliseconds
- To measure with a resolution of 10 mV or higher
- To measure at frequencies of 50 MHz or higher
- To measure Random Telegraphic Noise at frequencies around the fundamental output frequency of 50MHz

3.3 Constraints

- $1650 total budget
- 7 month project timeline
- Compatibility with the Ivanov group's test environment generation system
- User Interface on Personal Computer
- Test setup via JSON interface

4.0 Outcome

The client currently has a limited testing setup with the main problem being that it operates at significantly low speeds and is not automated, limiting their overall testing throughput. The data collected by the current system is not detailed enough to develop proper understanding of the underlying physical phenomenon experienced by the CMOS transistors under test.

Our project is a standalone product which directly allows the client's organization to rapidly test their current CMOS transistors to standards higher than typical industrial testing systems. The data that will be acquired by our UF-FTU will be used by the client to develop the physical models of transistor healing.

The product is a modular integrated system consisting of two boards; an analog front end and a digital board back end. At a high level, these blocks include the ADCs, the AFE, the FPGA and firmware subsystems, DDR3 Memory and finally SSD storage. The firmware blocks include the clock domain buffering system and memory controller. The system provides a foundation for further custom measurement and processing tools to be easily generated. Our design has successfully maximized the performance per dollar to allow scalability and replication for industrial implementation. We have achieved this through minimizing our part count, reducing the bill of materials and decreasing production costs.

Further details on our design can be found in our Design Specifications document where a high level diagram as well as detailed block by block breakdown is present.

Overall our project has been executed with emphasis on scalability and replicability, our design can be utilized to easily manufacture more UF-FTUs as needed by the organization internally or if the organization wishes to expand externally as a consumer facing product.

5.0 Deliverables

The main project deliverable for the client was to provide a functionally verified and validated design that meets the design requirements. We have successfully achieved all required deliverables and also our stretch goals by delivering a complete functional hardware board.

The required and “stretch goal” deliverables are listed below in Table 1 and Table 2:

Deliverable Category	Deliverable Name	Method of Delivery
Documentation	User manual	Word document
	Design process	Word document
	BOM	Excel spreadsheet
Design Files	PCB design files	Altium design files
	Gerber manufacturing files	Altium gerber files
	PCB renders	Image & CAD files
	Simulations	SPICE simulation files
	State diagrams	Diagram
Firmware & Gateware	Firmware source code	C source code
	Gateware source code	Verilog source code
	Gateware simulation	Verilog testbench files

Table 1: Required project deliverables

Deliverable Category	Deliverable Name	Method of Delivery
Software	Host PC side software for data analysis and visualization	Python source code
Hardware	Physical prototype	Fabricated and assembled PCBs
		Mechanical enclosure

Table 2: Stretch goal project deliverables

6.0 Verification and Validation

To ensure our product successfully met and exceeded all of our client's needs we subjected it to strict verification and validation phases. A high level overview is provided here, for more details please refer to our Verification and Validation document.

In our design stage we utilized SPICE simulation software such as LTSpice to understand and develop the fundamental behaviours of the board. For the hardware stage, we incorporated commercial test equipment such as Spectrum Analyzers and Oscilloscopes to confirm the simulation results. Finally, we carried out system calibration to account for manufacturing tolerances.

The gateware and firmware blocks that include the clock domain buffering system and memory controller had their own sets of tests, including functional testing through test benches and compliance testing in accordance with vendor specifications. We overcame difficulties in testing which arose because of a lack of viable solutions for robust testing while not having the physical board and components present by designing multiple backup firmware solutions leading us to deliver a fully functional system.

Our design is based around distinct subsystems, which allowed verification to be performed at several stages of the design process independently. This incremental approach allowed for continuous improvement and ensured our design remained agile to requirement changes. Steps were also taken to assess the effectiveness of the implemented solution, leading to exceeding all client requirements and completing our stretch goals in the final product.

We performed regular process health checks to assess the effectiveness of our overall development process using a continuous improvement methodology such as plan-do-check-adjust (six-sigma), these checks included assessing PCB board quality barriers.

Finally we tracked and reviewed our device's performance by using product quality KPIs, these included time taken to complete a full test, overall data bandwidth, overall digitized accuracy, and maximum number of tests that could be performed before storage overflow occurs. Our client was kept in the loop through and we had an established audit programme with them to discuss the design regularly and identify potential weaknesses and additional improvements.

7.0 Budget

The Capstone Team had an initial budget of $650 that was allocated by UBC ECE. In addition to these funds, UBC SoC also provided a preliminary budget of $1,000.

All of the costs incurred by the team were used for purchasing and fabrication, namely for manufacturing a PCB, purchasing an ADC, an FPGA and other components.

Initially our team had planned 2 revisions for our project, our initial planned cost breakdown is shown in Table 3 below. However due to our extensive testing at the design stage, we managed to achieve a successful solution in only one revision.

Category	Cost (per board)
Rev1 Digital Board	$468.00
Rev1 AFE Board	$100.00
Rev1 Assembly & Shipping	$100.00
Rev2 Combined Board	$553.00
Rev2 Assembly & Shipping	$100.00
Development Rev	$300.00
Total	**$1,621.00**
Projected Remaining Budget	**$29.00**

Table 3: Planned Cost Breakdown

By achieving a fully functional system in one revision we have saved $734.87 and our actual expenses are shown below in Table 4:

Category	Cost (per board)
Digital Board	$606.23
AFE Board	$279.90
Total	**$886.13**
Remaining Budget	**$763.87**
Project Savings	**$734.87**

Table 4: Actual Cost Breakdown

8.0 Project Management

8.1 Major Milestones

In addition to the four milestones outlined by the Capstone course, the project was divided into design revisions. It was based on an iterative process that allows for adjustments based on problems/changes that may arise as the project proceeds. The first design revision consists of a segmented design, splitting up the system into analog and digital sections. This also helped us isolate each section for rapid development and testing.

As this project was primarily hardware based, we initially developed a stringent timeline (see Appendix 1). For instance, variables such as shipping and fabrication needed to be accounted for within each stage of the project. However our project went much better than we had planned for and we managed a successful working system in just one revision instead of the two we had planned.

The key hardware milestones were PCB, component ordering, and testing, as this process can take several weeks to complete. For the project to have remained on track, these milestones were crucial to meet. Final integration and validation is also an important milestone as it is necessary to ensure the product will meet the client's expectations. Verification deadlines were dependent on borrowing/acquiring testing gear which additionally forced us to be very careful with our timeline to be able to arrange it with our client.

Overall we managed to achieve all requirements and deliverables ahead of time and so were able to deliver on our stretch goals as well to exceed all client requirements.

8.2 Major Responsibilities

The project was broken down into technical and non-technical tasks. Each task had an associated lead member, with several more supporting members. This approach ensured that members were aware of the functioning of all portions of the project, as well as ensuring that no member is unable to work due to delays. The major responsibilities we had are outlined below:

Technical Task	Lead	Support
Test Input System	Jerry	Ketan, Keerthana
Sampling System	Ketan	Jerry, Jiaqi
FPGA Gateware	Jiaqi	Abdullah, Ketan
Storage System	Ketan	Abdullah
Processing System	Abdullah	Jiaqi, Jerry, Keerthana

Table 5: Technical Tasks Distribution

Non-technical Task	Lead	Support
Project Management	Keerthana	Jiaqi
Communications	Jerry	Ketan
Administration	Ketan	Abdullah
Safety	Ketan	Jerry

Table 6: Non-Technical Tasks Distribution

8.3 Safety & Risk Assessment

Safety is paramount to our team and our profession. Our product involved interacting with bare PCBs and components that have hazards such as high temperatures, or electrical shocks. To prevent injuries we needed to identify hazards and have strong barriers, and it involved recognizing that those who do the work understand the risk and are therefore key to keeping our barriers strong.

We worked in accordance with the new rules set out by the Capstone teaching team for COVID-19 and other safety risks. As such we opted for all board fabrications to be completed at certified JLC PCB production facility thus removing any need for potentially dangerous physical prototyping tasks to be done by our team.

Our methodology of risk-based sampling and testing enabled our team to make risk-based decisions for our design and testing across the entire development cycle. All product quality risks with potential impacts to our delivery timeline were controlled with one or more mandatory controls and recovery measures, e.g. backup components,

sampling and testing, an agreed upon process for resolving and managing client changes, etc. In all cases, the level of control reflected the magnitude of the risk determined by our team.

1. Identify - hazard and risk identification

2. Assess - risk assessment

3. Control - implement controls

4. Recover - implement recovery measures

Thus, risk control was an active focus for our team, as working on a hardware based project without lab access and requiring relatively expensive components with a limited budget made this vital for project success.

Below was a high-level overview of our top quantitative risks:

Quantitative Risk Assessment						
Risk	Insufficient Funds	PCB Damage	Component Damage	Delivery Delays	Production Delays	Assembly Mistakes
Probability	High	Medium	Medium	Low	Low	Medium
Severity	Catastrophic	Very High	High	Medium	Medium	Low
Priority	1	2	3	4	5	6

Table 7: Quantitative Risk Assessment Summary

There were additional vertical risks identified, related to team management and individual tasks. Our coherent support structure with additional time buffers and appointed add-on members for critical tasks allowed us to successfully complete our project ahead of time, meeting and exceeding all client requirements and with major savings on our budget. Through our risk assessment methodology we were able to make a more coherent decision between our proposed solutions.

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8.4 Team Management

Our team's philosophy was to allow as much autonomy as possible and support individual compartmentalization. In order to support this we had broken the project into subsystems which for the most part can be designed, developed, tested and validated separately. These subsystems then each had assigned team members based on individual interests and experience with a team lead to monitor progress. As soon as two or more subsystems could be incorporated together the two teams were unified and split into validation and verification groups to achieve smooth integration from the base up.

We also operated under the agile approach:

- A Sprint is a period of development, for which a Product backlog (requirements) is collected from the stakeholders and prioritized into a smaller Sprint backlog
- The week is then all about getting that backlog successfully completed
- The Sprint officially comes to an end with a Sprint Review where stakeholders are consulted for feedback on the work completed and adaptations are taken to optimize value

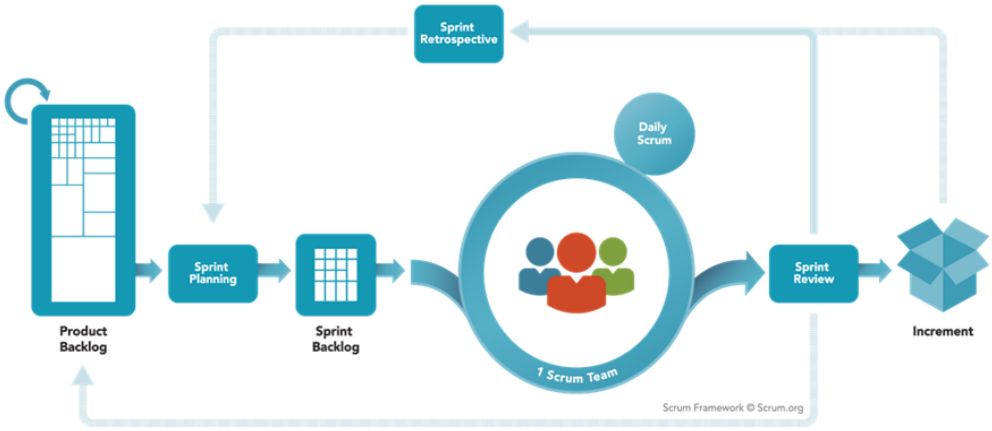
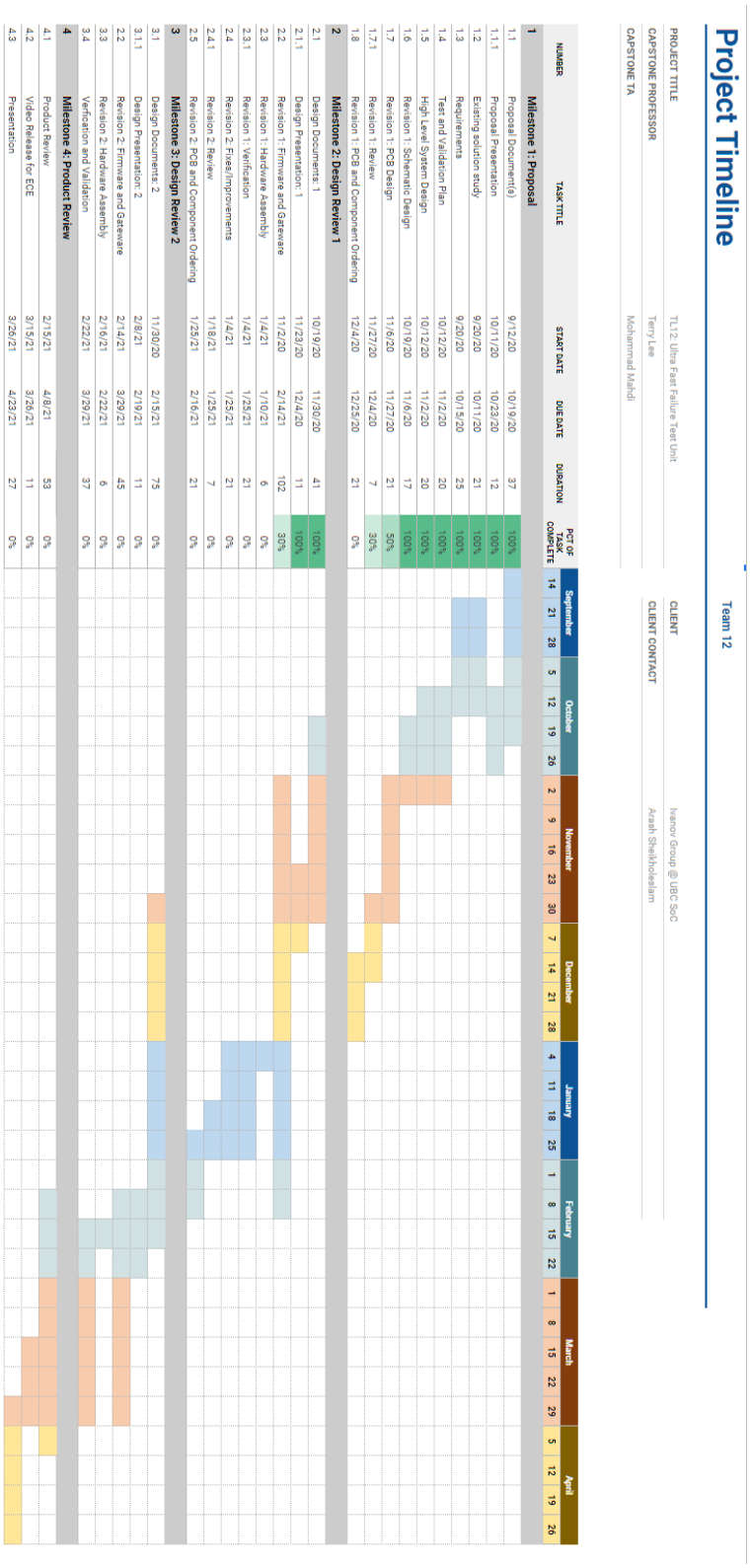


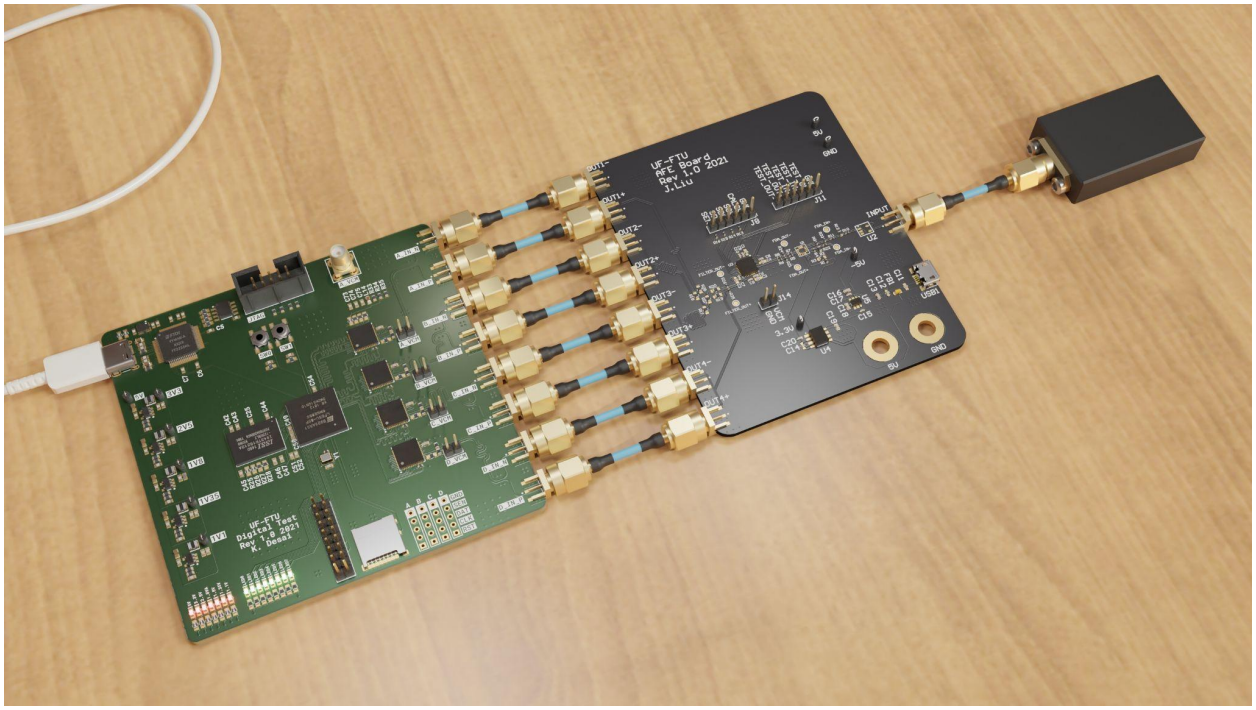
Figure 1: Agile Framework (from scrum.org)

In accordance with COVID-19 policies the team worked completely online, with no physical meetings whatsoever throughout the project. For our hardware project it had made it harder to work together on the physical subsystems. We overcame this by setting up a dedicated server for our teammates to remotely connect to in order to tinker with hardware physically located at one place. We utilized services like Github, Atom Teletype, Altium Live and Google Drive to successfully collaborate online.

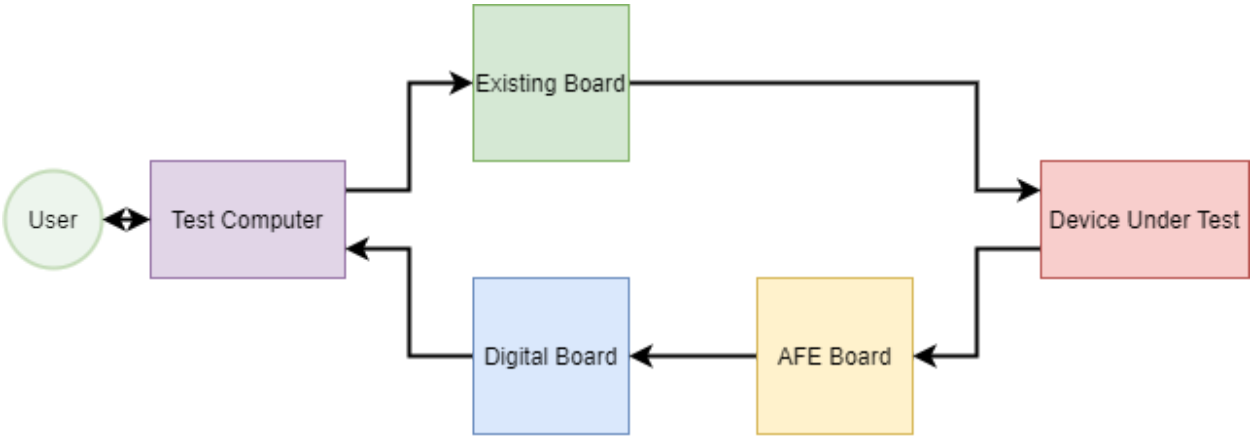
APPENDICES



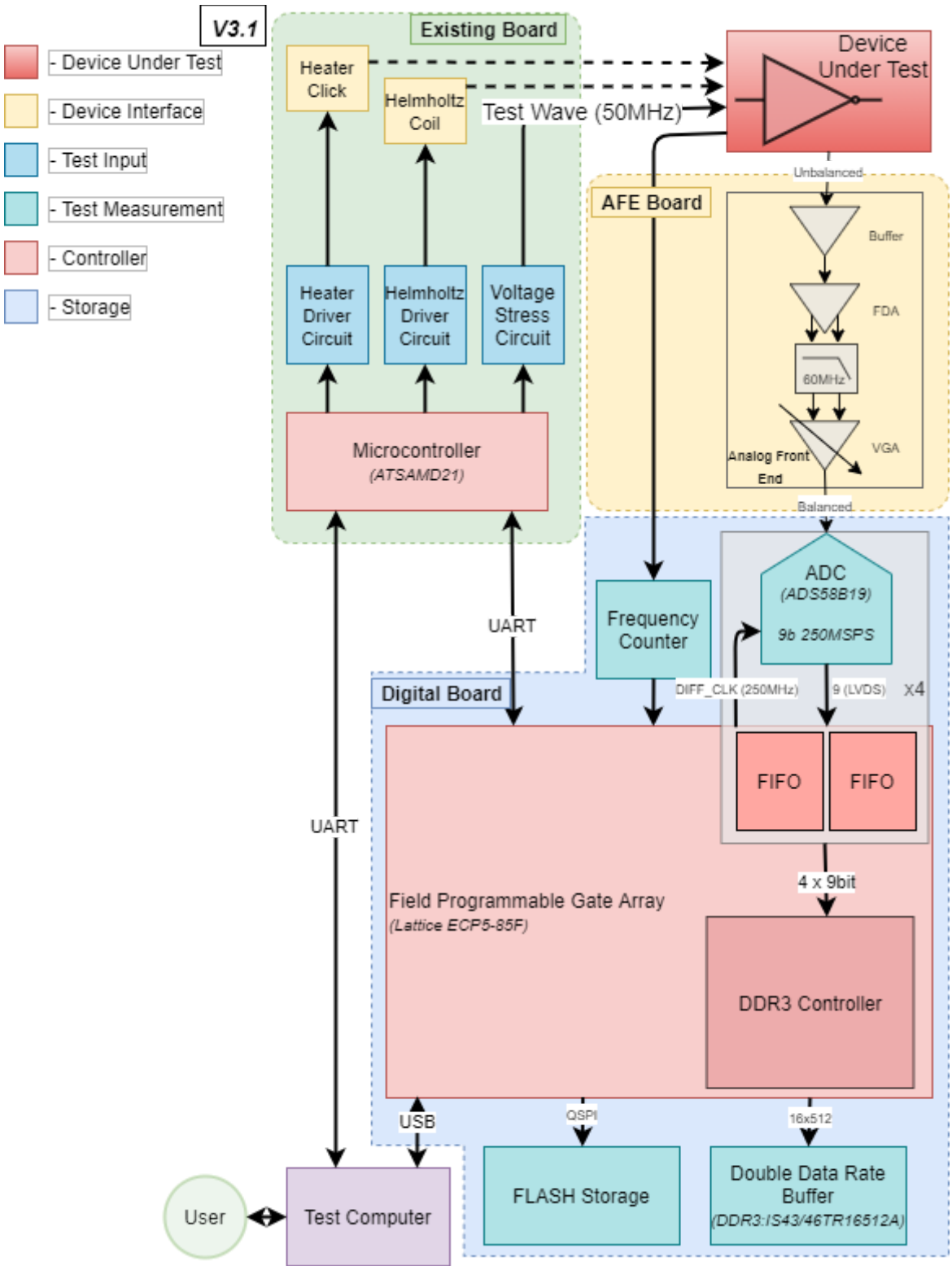
Appendix 1 - Project Timeline



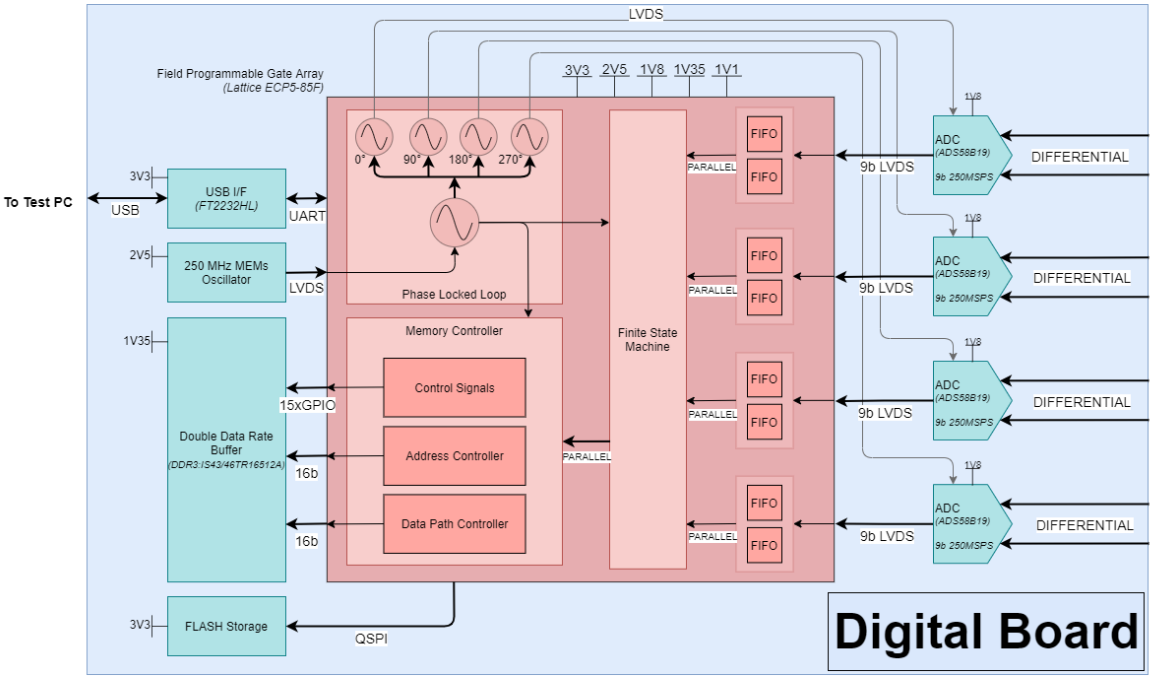
Appendix 2 - Complete System Render



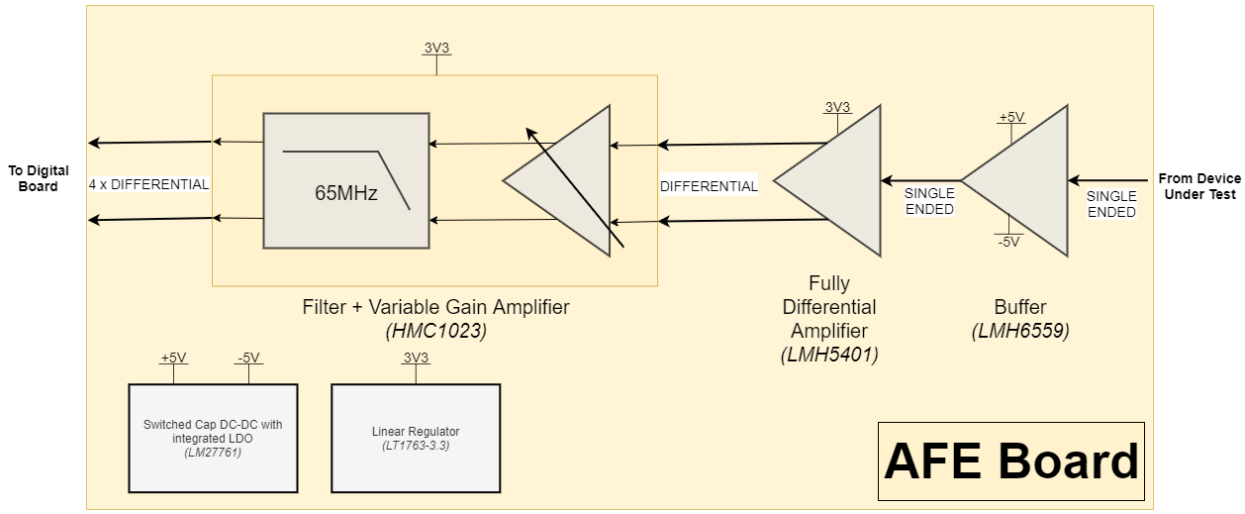
Appendix 3 - High Level System View



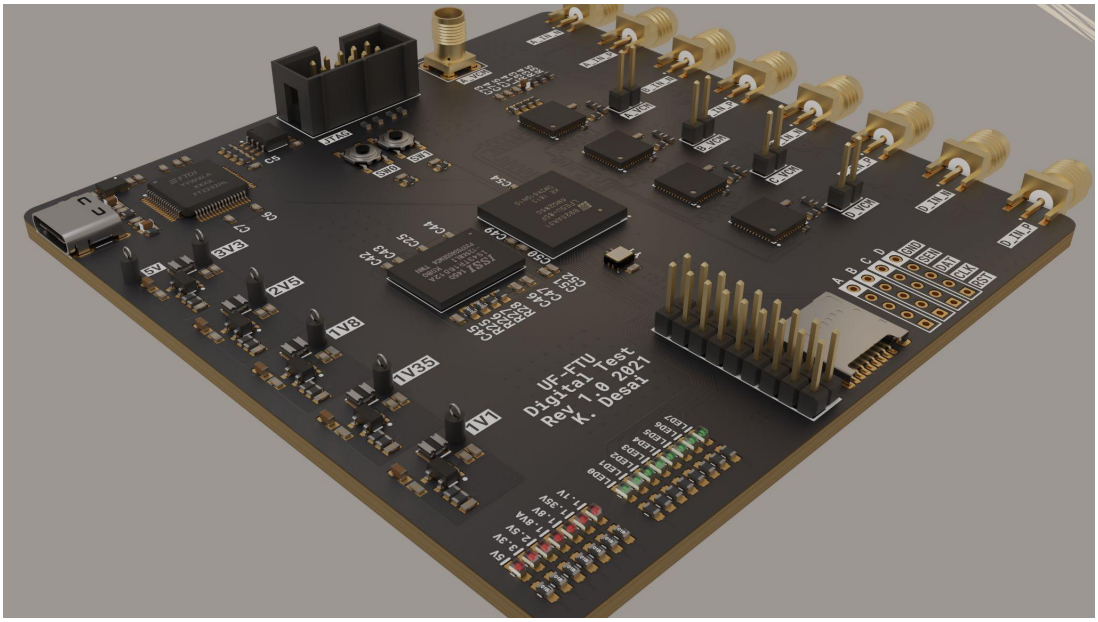
Appendix 4 - Detailed System View



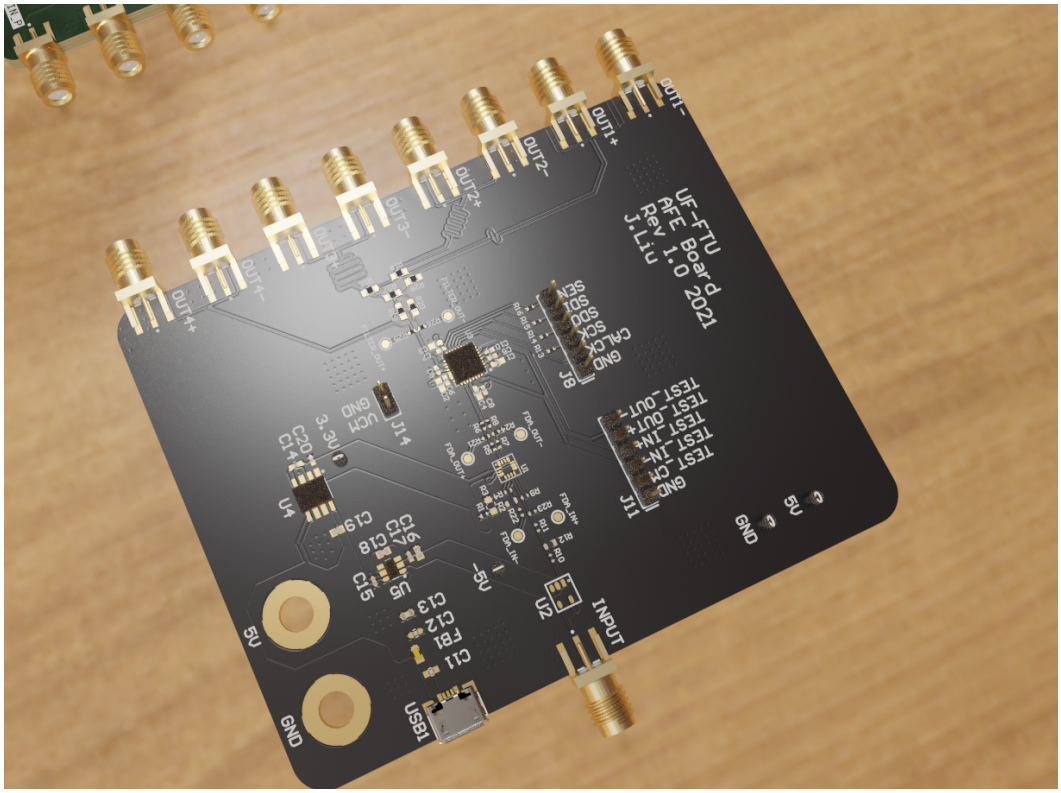
Appendix 5 - Digital Board Overview



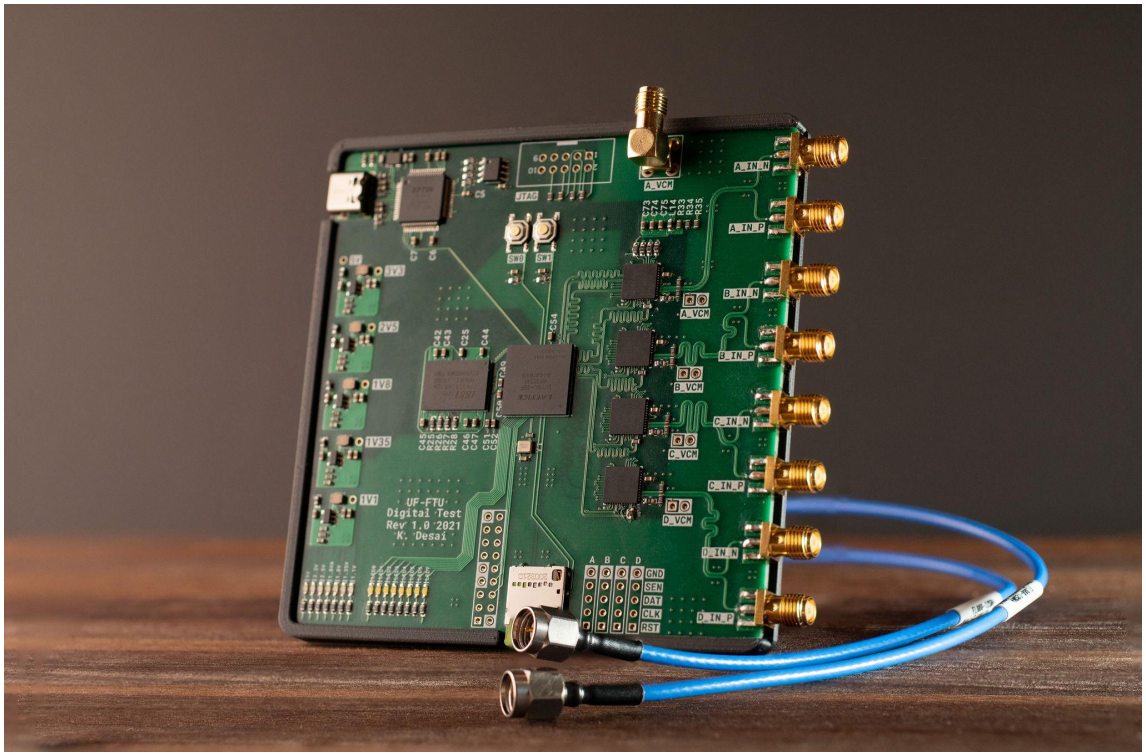
Appendix 6 - AFE Board Overview



Appendix 7 - Digital Test Board Render



Appendix 8 - AFE Board Render



Appendix 9 - Digital Board Photo

References

[1] A. H. Baba and S. Mitra, "Testing for Transistor Aging," *2009 27th IEEE VLSI Test Symposium*, Santa Cruz, CA, 2009, pp. 215-220, doi: 10.1109/VTS.2009.56.

[2] A. J. Jerri, "The Shannon sampling theorem—Its various extensions and applications: A tutorial review," in Proceedings of the IEEE, vol. 65, no. 11, pp. 1565-1596, Nov. 1977, doi: 10.1109/PROC.1977.10771.1