Timing is Everything: Understanding LVPECL and a newer LVPECL-like output driver

Welcome to our Timing is Everything series! Today we will talk about the low-voltage positive emitter-coupled logic (LVPECL) since it's a very popular signal type. In this blog, we'll go through some key features of LVPECL, its advantages and disadvantages, as well as a newer clock driver architecture that overcomes some disadvantages of conventional LVPECL drivers.

In general, LVPECL operates with a large differential voltage swing but tends to be less power-efficient than other signal types such as LVDS and HCSL. Due to its emitter-coupled logic (ECL) characteristics, LVPECL has fast rise and fall time as well as large swing, which is useful for driving high-frequency signals over lossy PCB traces compared to other signal types.

The typical output of an LVPECL driver consists of a differential pair with the emitters connected to ground via a current source, as shown in Figure 1. This differential pair drives a pair of emitter-followers which provide the current to output+ and output – through the external biasing resistors to set the emitter currents, which control the output swing, switching speed, and power consumption.

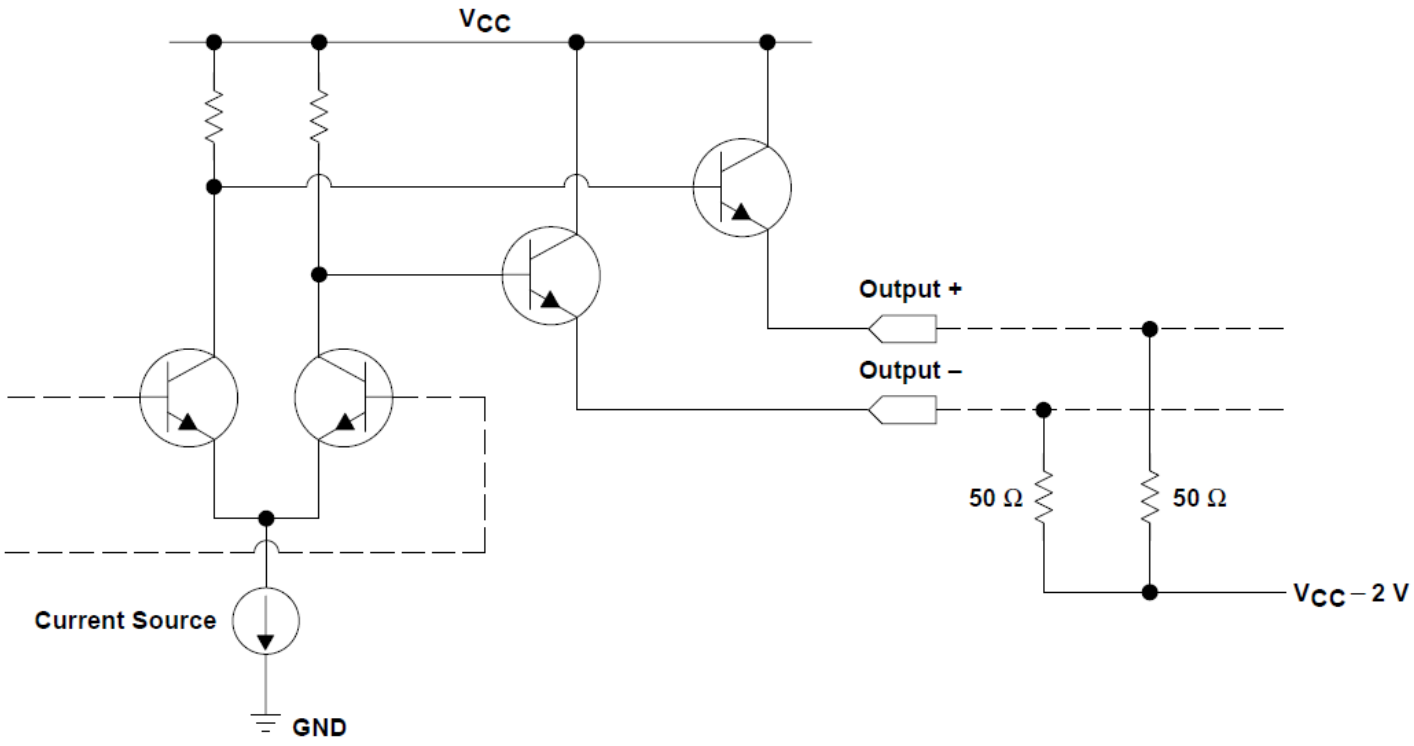

Figure 1. LVPECL output topology

LVPECL output could be terminated with 50 Ω resistor to the termination voltage VDD-2V, as shown in Figure 2. When a separate termination voltage is not available, the LVPECL output could also be terminated using the Thevenin Equivalent network. However, the equivalent network increases the power consumption in the external resistors. As shown in Figure 3, AC coupling is more widely used. Two 150-ohm resistors are used for DC biasing the LVPECL output emitter follower, and the values are calculated based on setting the output transistor emitter current at the switching threshold. Because the output biasing resistor is placed at the driver side before the coupling capacitors, the line termination resistors and input biasing must be provided at the receiver side. The power consumption in 150 ohm pull down resistors is less than Thevenin equivalent termination.

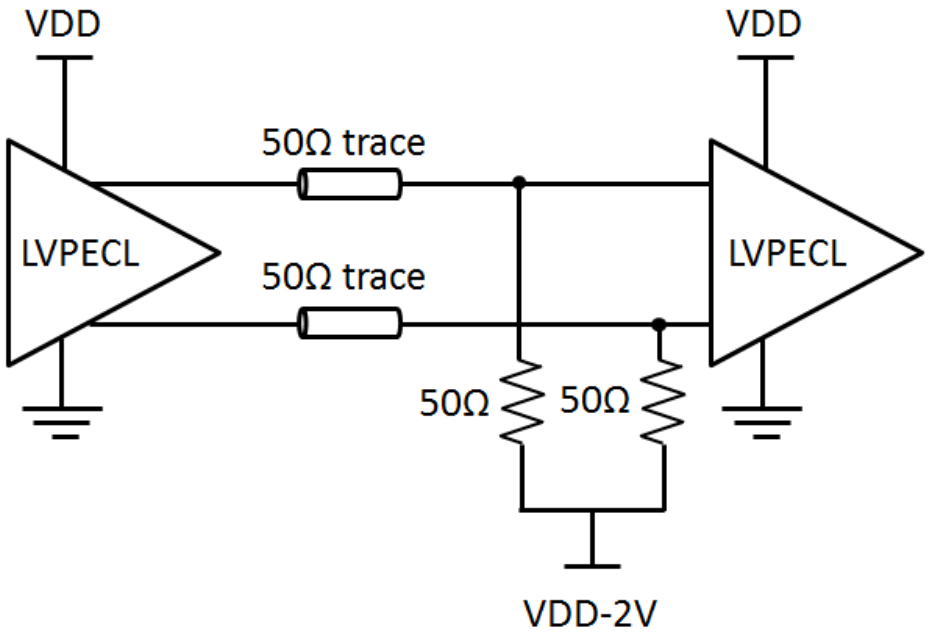

Figure 2. LVPECL standard load termination

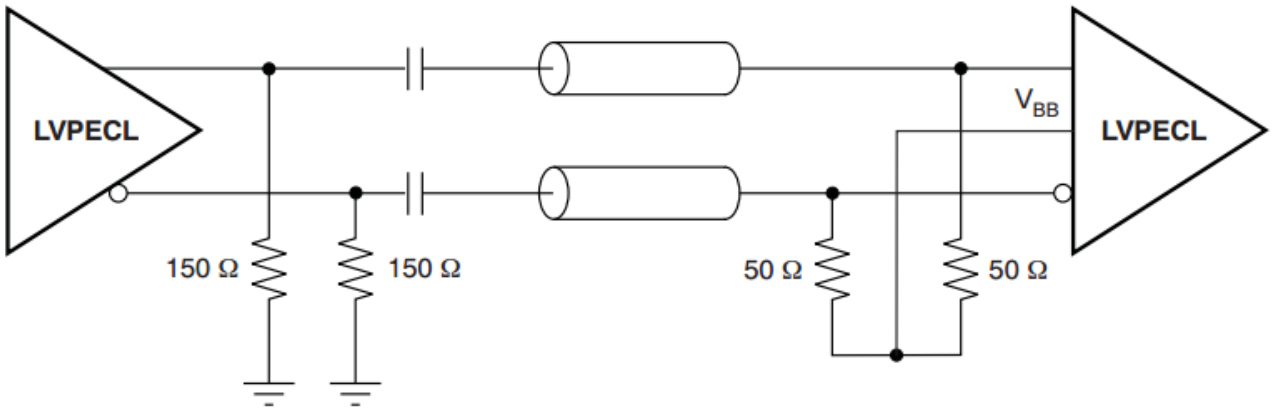

Figure 3. LVPECL AC-coupled interface with termination and biasing at the receiver

LVPECL output produces an 800 mV swing through the 50 Ω resistor. The swing of LVPECL is the largest one of all differential signal types, as shown in Table 1. LVPECL drivers are most flexible to interface with other differential receivers when using AC coupling for DC blocking and isolating different common voltage of the driver and receiver (AC coupling is common for clock interfaces due to 50% duty cycle).

Table 1. Typical swing of different signal types

	LVPECL	LVDS	HCSL	CML
Swing (mV)	800	400	750	400

LVPECL can offer the best jitter performance because the slew rate of LVPECL is very fast compared to other differential signal types. Table 2 compares the output slew rate of LVPECL, LVDS and CML drivers from two TI clock drivers, CDCM61004 and CDCM6208. Because the slew rate of LVPECL is fast, it makes the LVPECL signal less sensitive to the noise, which leads to lower jitter.

Table 2. Slew rate of different signal types

	LVPECL (CDCM61004)	LVDS (CDCM61004)	CML (CDCM6208)
Swing (mV)	800	400	400
Rise/fall time (20% to 80%) (ps)	175	255	143
Slew rate (V/ns)	2.74	0.94	1.68

However, power consumption is the primary disadvantage of LVPECL (driver emitter current, external biasing resistor currents, and 3.3 V operating supply). Below is the comparison among LVPECL and LVDS for CDCM61004 and CDCM6208. The CML consumes more current but can support lower supply voltages, like 1.8 V, which reduces the power consumption.

Table 3. Power consumption of different output drivers

	LVPECL (CDCM61004)	LVDS (CDCM61004)	CML (CDCM6208)
Current (mA)	28	20	24.25
Voltage (V)	3.3	3.3	1.8
Power consumption (mW)	92.4	66	43.65

In addition, traditional LVPECL drivers can sometimes suffer from signal integrity problems when driving a non-uniform transmission line environment. As seen in Figure 1, the emitter follower output impedance of the driver is very low, which is not well matched to a 50 Ω transmission line. If any incident signal is reflected back due to any impedance discontinuity or

mismatch along a 50 Ω transmission line, the reflected signal could not be absorbed by the source side because the impedance is unmatched at the source side, then a large portion would reflect back to load and impact signal integrity.

The CDCM6208 output stage maintains the advantages of traditional LVPECL while overcoming the disadvantages. The output stage uses a high-swing CML structure (HS-CML) but drives the same signal amplitude and rise time as the traditional LVPECL output, as shown in Figure 4. The HS-CML output stage integrates two 50 Ω resistors on chip, leading to reduced bill of materials and simplified layout. Because the HS-CML output impedance is 50 Ω, it provides good source impedance matching to terminate reflections in a 50 Ω transmission line environment compared to traditional LVPECL outputs. Meanwhile, the power supply voltage for it could be as low as 1.8 V when the traditional LVPECL output is limited to 2.5 V or 3.3 V. The power consumption is much lower, as shown in Table 4.

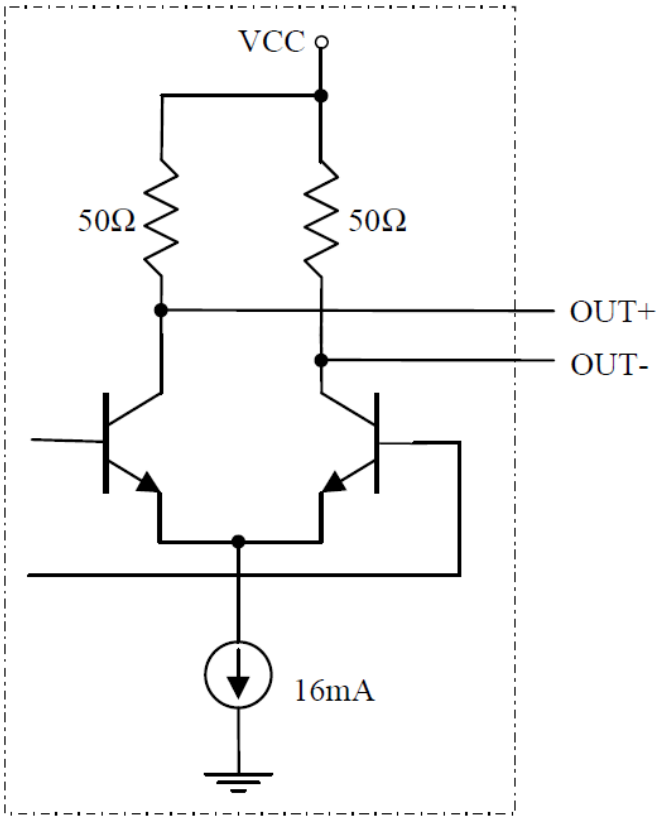

Figure 4. CDCM6208 LVPECL-like output stage

Figure 5 shows the typical CDCM6208 LVPECL-like output AC-coupled termination. The receiver is terminated internally. As CDCM6208 integrates pull up resistors on-chip, there's no need for external resistors, which reduces the bill of materials.

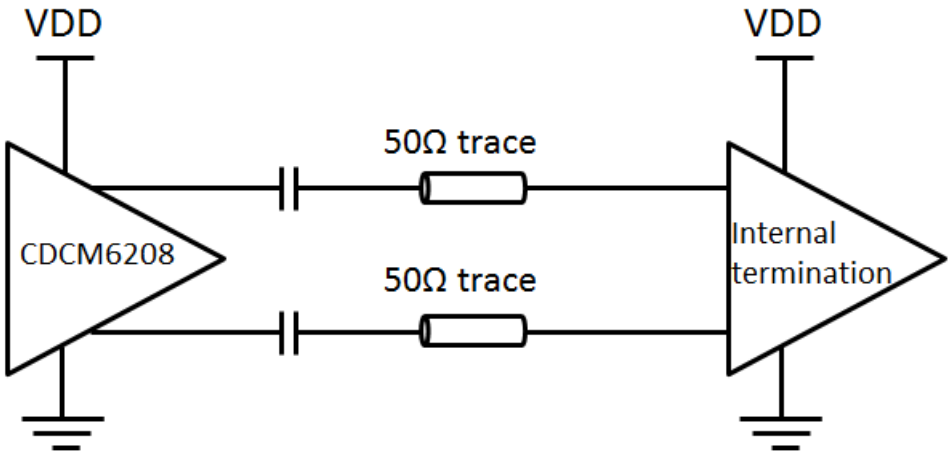

Figure 5. CDCM6208 LVPECL-like output termination

Table 4 gives a detailed comparison between traditional LVPECL driver (CDCM61004) and CML driver with LVPECL-like swing (CDCM6208). It shows the great advantages of this LVPECL-like output.

Table 4

	LVPECL (CDCM61004)	**LVPECL-like (CDCM6208)**
Topology	Emitter follower	CML (High swing)
Typical swing (mV)	800	800
Typical rise/fall time (ps)	175	211
Driver VCC (V)	3.3	3.3, 2.5, 1.8
Typical driver power (mW)	92.4 @3.3 V	72 @1.8 V
Output impedance	Low	50 Ω on-chip
Output biasing resistors	External 150 Ω pulldowns	None

In conclusion, choosing a proper signal type is important for your design. I hope you now have a better understanding of LVPECL and the newer LVPECL-like drivers. Thanks for joining me on Timing is Everything!

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Application notes for further reading

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Interfacing Between LVPECL, VML, CML, and LVDS Levels

LVPECL and LVDS Power Comparison

AC-Coupling Between Differential LVPECL, LVDS, HSTL, and CML