AN4550

USB7206/USB7216/USB7252 FlexConnect Operation

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1.0 INTRODUCTION

The Microchip USB7206, USB7216, and USB7252 smart hubs allow one of the downstream ports to be swapped with the upstream port to assume the role of USB host during hub operation. This port exchange feature is called FlexConnect.

This feature can be used in two primary ways:

1. **Host Swapping:** This functionality can be achieved through a hub wherein a host and device can agree to swap the host/device relationship. The host becomes a device, and the device becomes a host.
2. **Host Sharing:** A USB ecosystem can be shared between multiple hosts. Note that only one host may access the USB tree at a time.

FlexConnect can be enabled through any of the following methods:

1. **Register Control:** An embedded SMBus controller can configure and initiate the FlexConnect through SMBus commands during runtime.
2. **USB Command:** A USB host can initiate FlexConnect via a special command to hub's internal Hub Feature Controller.
3. **Direct Pin Control:** A select number of available GPIO pins on the device can be assigned the role of a FlexConnect control pin.

1.1 Sections

This application note covers the following sections:

1.2 References

The following documents should be referenced when using this application note:

- *Microchip USB7206 Data Sheet*
- *Microchip USB7216 Data Sheet*
- *Microchip USB7252 Data Sheet*
- *Microchip AN2935 Configuration of USB7202/USB7206/USB725x Application Note*

2.0 FUNCTIONAL OVERVIEW

The USB7206/USB7216/USB7252 has an internal USB device called Hub Feature Controller, which can be used to initiate the FlexConnect feature. The Hub Feature Controller is a generic class USB device. It is permanently connected to the last USB2 port of the hub as a non-removable port. The internal block diagrams of USB7216 and USB7206 are shown below in Figure 1 and Figure 2, respectively.

FIGURE 1: USB7216 INTERNAL BLOCK DIAGRAM

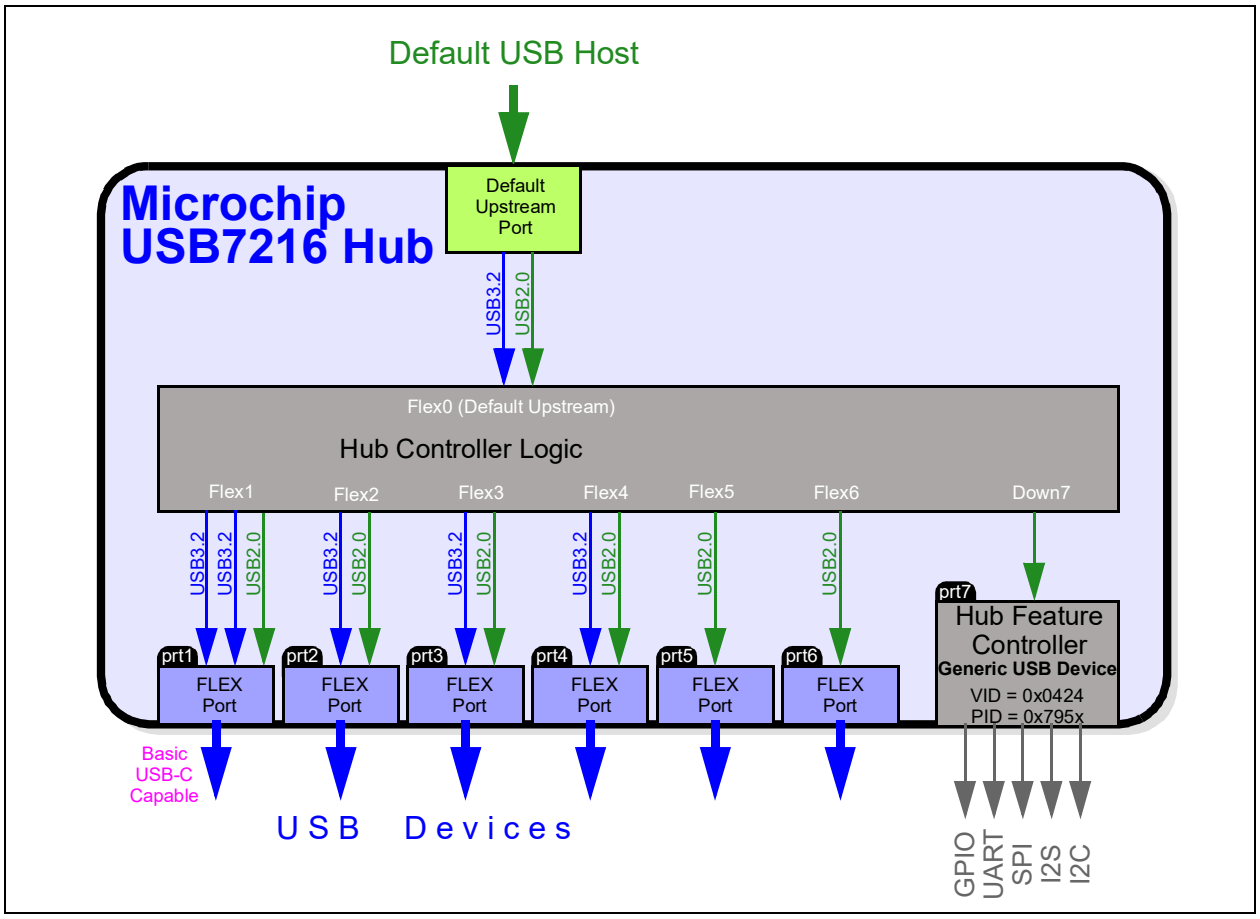
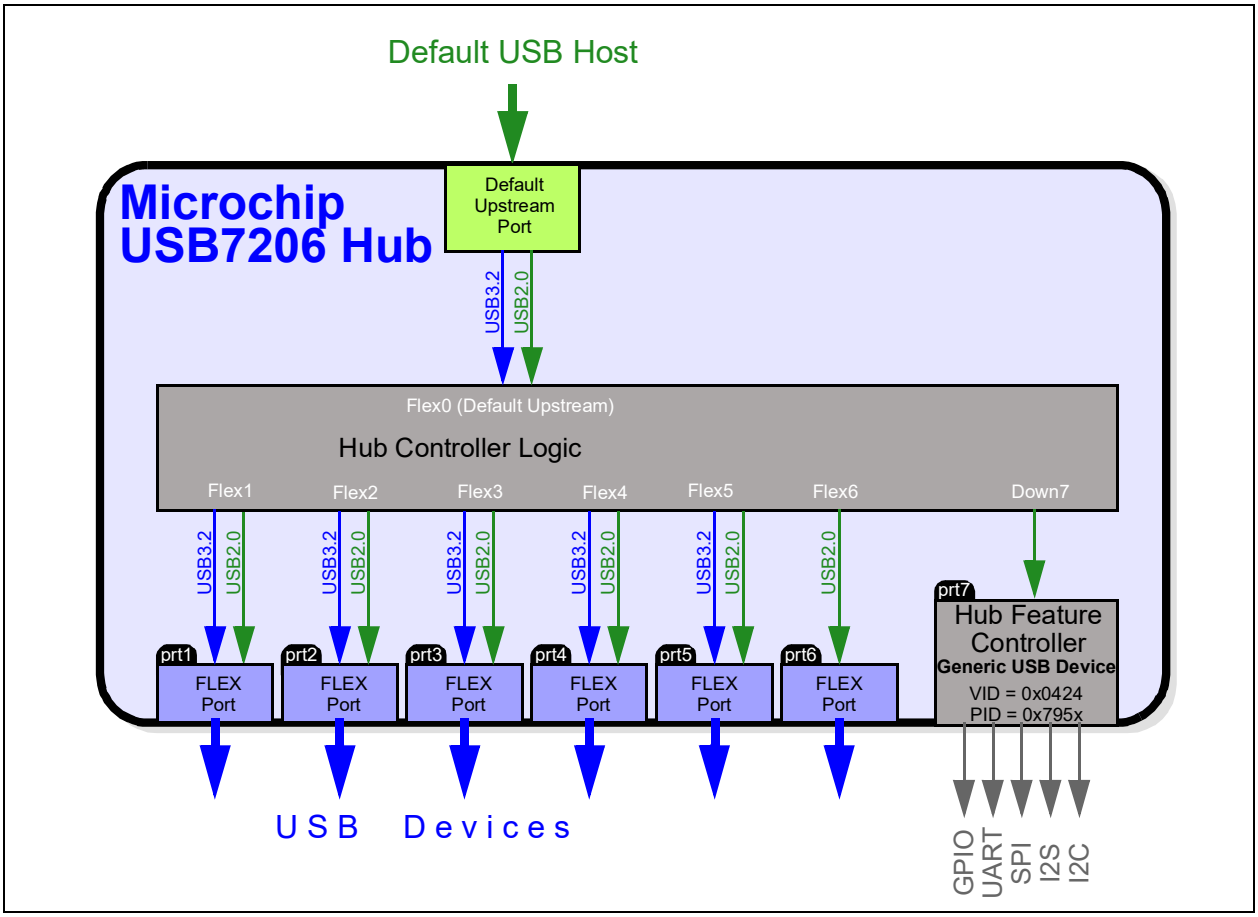
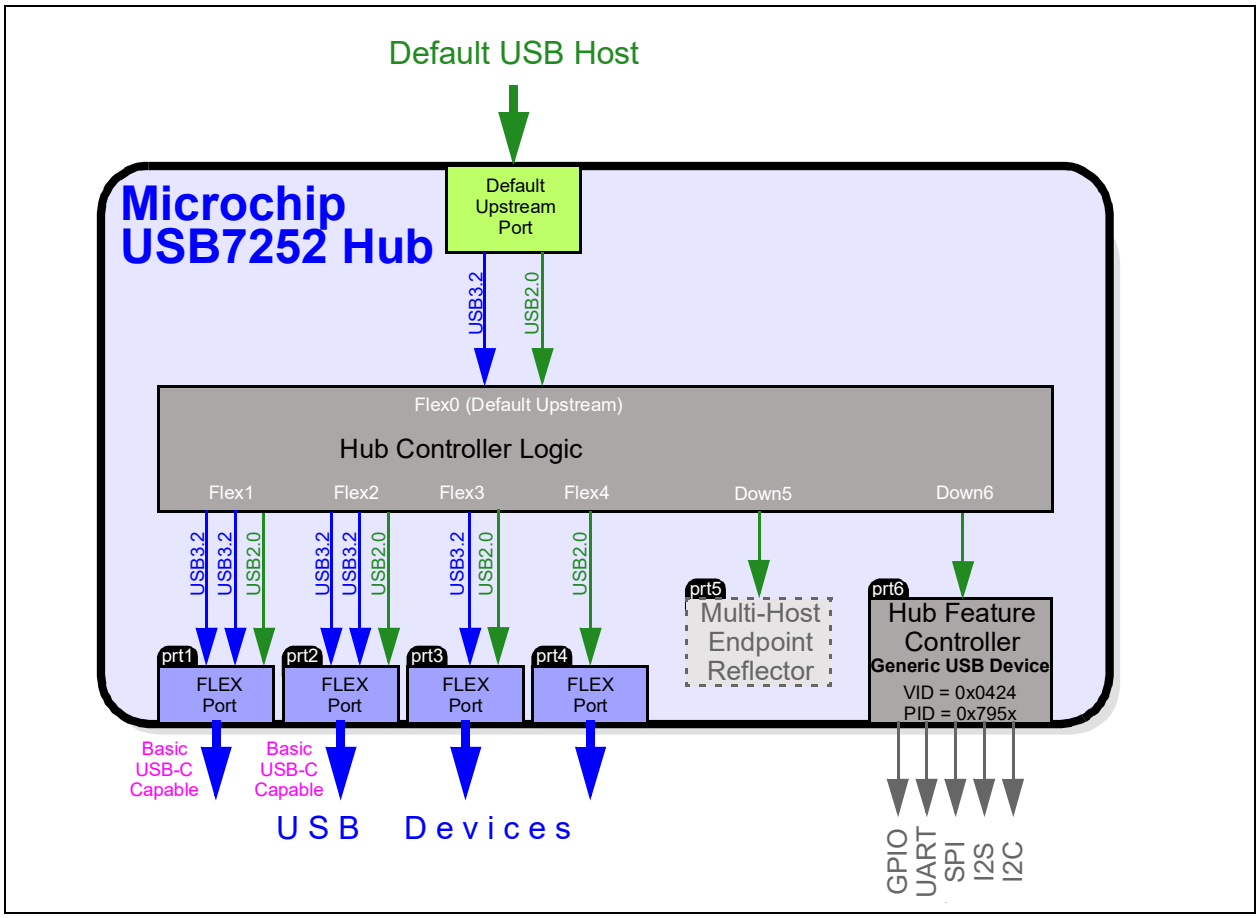


FIGURE 2: USB7206 INTERNAL BLOCK DIAGRAM



The internal block diagram of Microchip USB7252 is shown below in Figure 3.

FIGURE 3: USB7252 INTERNAL BLOCK DIAGRAM



2.1 FlexConnect Initiation

The Hub Feature Controller provides the following methods to configure the hub controller to initiate FlexConnect:

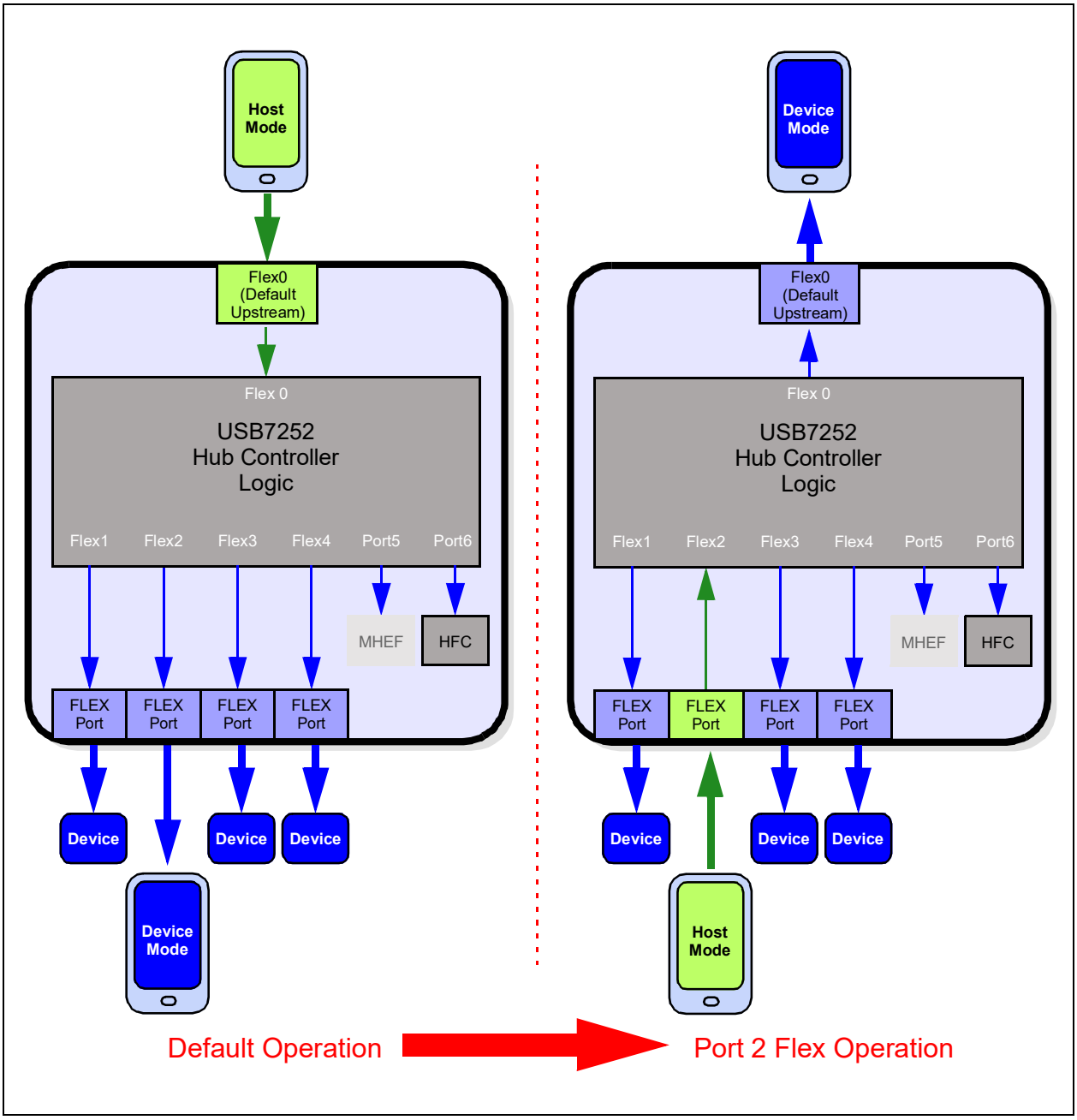
1. **Register Control** (via SMBus or OTP)
- Refer to Section 3.0, FlexConnect Register Control.
2. **Vendor-Specific Command** SET_ROLE_SWITCH to the embedded Hub Feature Controller.
- Refer to Section 4.0, FlexConnect USB Command Details.
3. **GPIO-Based Pin Control** after GPIO settings are programmed to hub OTP configuration memory.
- Refer to Section 5.0, FlexConnect Pin Control.

When FlexConnect is initiated, the current upstream port will change to a downstream port, and the designated port will change into an upstream port. This can be used for host-swapping type applications or host-sharing type applications.

2.2 Host Swapping

In a host-swapping application, the role of the host is exchanged between two dual-role capable devices through ID pin control, protocol handshake, or some other proprietary method. An example is shown in Figure 4.

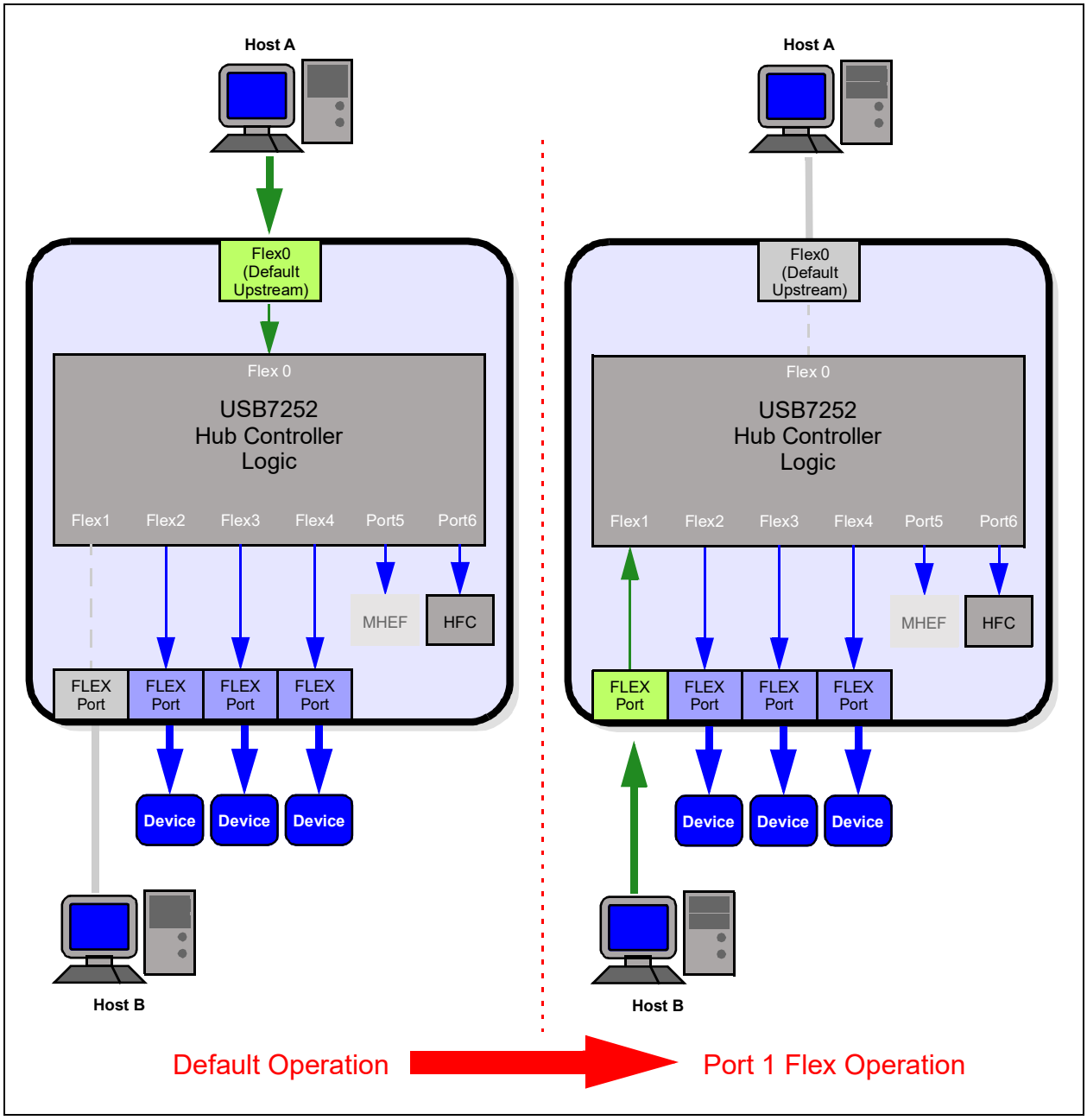
FIGURE 4: FLEXCONNECT HOST-SWAPPING EXAMPLE



2.3 Host Sharing

In a host-sharing application, multiple hosts are connected to the hub. Only one of these hosts has access to the USB device tree at a time. All other hosts are effectively disconnected from the USB tree when they do not control the host port. An example of “Host Sharing” is shown in Figure 5.

FIGURE 5: FLEXCONNECT HOST-SHARING EXAMPLE



3.0 FLEXCONNECT REGISTER CONTROL

The FlexConnect registers can be configured via SMBus to initiate FlexConnect during runtime. (See **Note 1**.) While flexed, the hub will automatically revert to the default state if one of the following conditions is met:

- If the new flex host sends a USB command which commands the hub to return to the default state
- If the new flex host is disconnected any time after the flex host has enumerated the hub
- If the hub has not yet been enumerated by the flex host after the ENUM_TIMEOUT expires
- If VBUS_DET signal on either the default host port or the new flex host port goes low

3.1 SMBus/I2C Target Pin Assignment

Based on CFG_STRAP configuration selected, the SMBus/I2C Target pins are shown in Table 1. The firmware will check the presence of external 1 kΩ to 10 kΩ pull-up resistors on both pins during SMBUS_CI2C ControllerHECK stage (See **Note 2**.) and stay in this stage indefinitely for SMBus/I2C configuration. The external SMBus/I2C controller must write SMBus command USB_ATTACH (0xAA5500) or USB_ATTACH_WITH_SMBUS (0xAA5600) to finish the configuration and exit the stage.

Note 1: For SMBus command format, refer to *AN2935 Configuration of USB7202/USB7206/USB725x Application Note*.

2: For details on boot sequence, refer to the corresponding data sheet.

TABLE 1: SMBUS/I2C TARGET PIN ASSIGNMENT

	USB7206	USB7216	USB7252
CFG_STRAP	**Configuration 3**	**Configuration 1 (SMBus/I2C)**	**Configuration 1 (SMBus/I2C)**
I2C Clock	PF26	PF26	PF26
I2C Data	PF27	PF27	PF19

3.2 Initiating FlexConnect via SMBus/I2C Command

To initiate FlexConnect via SMBus, modify the registers defined below to flex USB2 port and USB3 ports.

TABLE 2: USB2 SYSTEM CONFIGURATION REGISTER

USB2_SYS_CONFIG (BF80_0808h) RESET = 00h			**USB2 System Configuration Register**
Bit	**Name**	**R/W**	**Description**
7:3	Masked	R	For internal use only. Do not modify the value.
2:0	USB2_HUB_FLEX	R/W	This register is for initiating USB2 hub FlexConnect. 001 = Port 1 010 = Port 2 011 = Port 3 100 = Port 4 101 = Port 5 (for USB7206/USB7216) 110 = Port 6 (for USB7206/USB7216) All others = ***Invalid***

TABLE 3: USB3 SYSTEM CONFIGURATION REGISTER

USB3_SYS_CONFIG (BF80_0828h) RESET = 00h			USB3 System Configuration Register
Bit	**Name**	**R/W**	**Description**
7:3	Masked	R	For internal use only. Do not modify the value.
2:0	USB3_HUB_FLEX	R/W	This register is for initiating USB3 hub FlexConnect. 001 = Port 1 010 = Port 2 011 = Port 3 100 = Port 4 101 = Port 5 (for USB7206 only) 110 = Port 6 (for USB7206 only) All others = ***Invalid***

3.3 VBUS Status Detection

The implementation of FLEXCONNECT requires that the system designer be responsible for routing the correct host VBUS signal to the USB72xx VBUS_DET or VBUS_MON_UP pins. (See Figure 6.) The VBUS input signal to the USB2 and USB3 hub cores can be chosen through VBUS_PASS_THRU register. The default option for USB7206 is directly from VBUS_DET device pin, and VBUS_MON_UP for USB7216 and USB7252. Alternatively, the internal controller can supply the signal via PIO24 and PIO32 to USB3 and USB2 hub cores.

FIGURE 6: VBUS STATE DETECTION ON UPSTREAM PORT

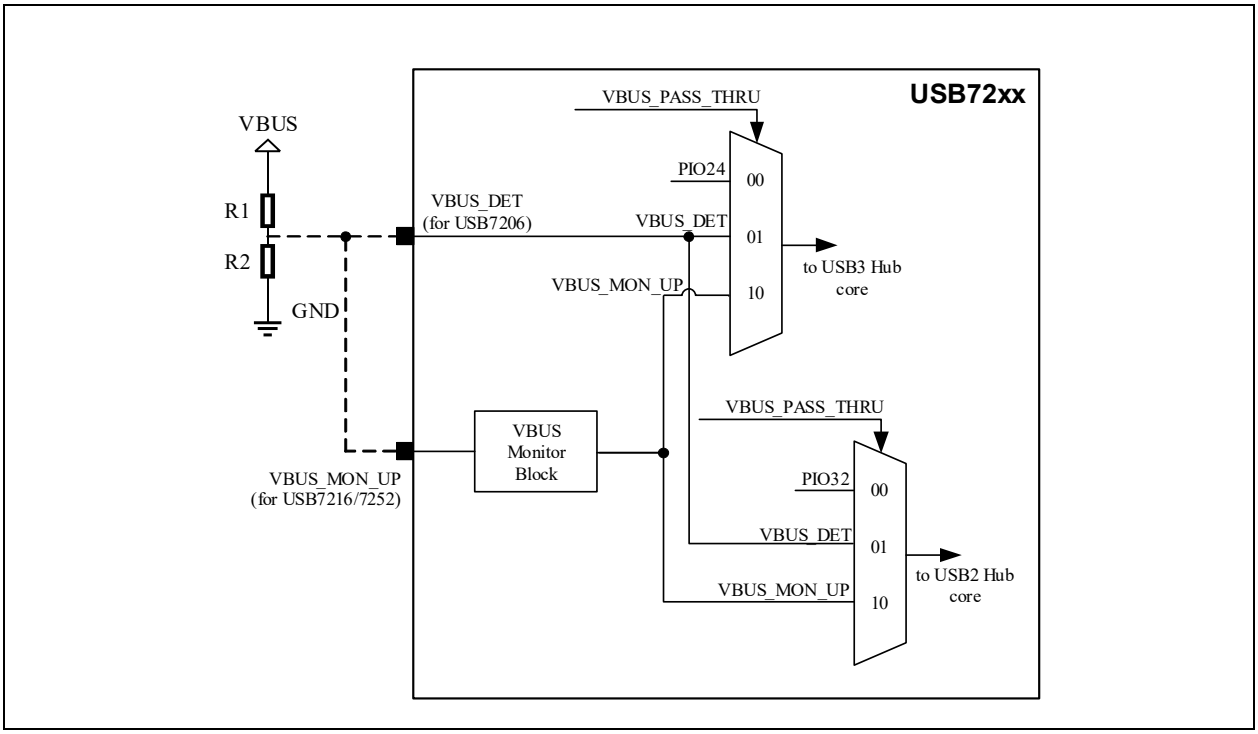


TABLE 4: VBUS PASS THROUGH REGISTER

VBUS_PASS_THRU (BF80_3C40h) RESET = 05h (UBS7206) RESET = 0Ah (USB7252/USB7216)			VBUS Pass Through Register
Bit	**Name**	**R/W**	**Description**
7:4	Masked	R	For internal use only. Do not modify the value.
3:2	USB3_PASS_THRU	R/W	00 = The VBUS to USB3 Hub comes from Internal PIO24. 01 = The VBUS to USB3 Hub comes from device pin (PF30). 10 = The VBUS to USB3 Hub comes from VBUS_MON_UP (not available on USB7206). 11 = Reserved
1:0	USB2_PASS_THRU	R/W	00 = The VBUS to USB2 Hub comes from Internal PIO32. 01 = The VBUS to USB2 Hub comes from device pin (PF30). 10 = The VBUS to USB2 Hub comes from VBUS_MON_UP (not available on USB7206). 11 = Reserved

TABLE 5: PIO[31:0] OUTPUT ENABLE REGISTER

PIO32_OUT_EN (BF80_0900h) RESET = 00000000h			PIO Output Enable Register
Bit	**Name**	**R/W**	**Description**
31:0	PIO[31:0]	R/W	Output: 0 = Disabled, 1 = Enabled

TABLE 6: PIO[63:32] OUTPUT ENABLE REGISTER

PIO64_OUT_EN (BF80_0904h) RESET = 00000000h			PIO Output Enable Register
Bit	**Name**	**R/W**	**Description**
31:0	PIO[63:32]	R/W	Output: 0 = Disabled, 1 = Enabled

TABLE 7: PIO[31:0] OUTPUT DATA REGISTER

PIO32_OUT (BF80_0920h) RESET = 00000000h			PIO Data Output Register
Bit	**Name**	**R/W**	**Description**
31:0	PIO[31:0]	R/W	Output Buffer Data

TABLE 8: PIO[63:32] OUTPUT DATA REGISTER

PIO64_OUT (BF80_0924h) RESET = 00000000h			PIO Data Output Register
Bit	**Name**	**R/W**	**Description**
31:0	PIO[63:32]	R/W	Output Buffer Data

EXAMPLE 1: FLEXCONNECT VIA SMBUS/I2C COMMAND

An example of FlexConnect Port 3 on USB7206 through SMBus/I2C controller is shown below:

1. Write 0x03 to **0xBF80_0808** to flex USB2 Port 3.
   - 0x00 0x00 0x07 0x00 0x01 **0xBF 0x80 0x08 0x08** 0x03
   - 0x99 0x37 0x00
2. Write 0x03 to **0xBF80_0828** to flex USB3 Port 3.
   - 0x00 0x00 0x07 0x00 0x01 **0xBF 0x80 0x08 0x28** 0x03
   - 0x99 0x37 0x00
3. Send attach command.
   - 0xAA 0x56 0x00
4. Write 0x00 to **0xBF80_3C40** to specify VBUS signal is from internal PIO24 and PIO32.
   - 0x00 0x00 0x07 0x00 0x01 **0xBF 0x80 0x3C 0x40** 0x00
   - 0x99 0x37 0x00
5. Configure **0xBF80_0903** and **0xBF80_0904** to set the direction of PIO24 and PIO32 as OUTPUT.
   - 0x00 0x00 0x08 0x00 0x02 **0xBF 0x80 0x09 0x03** 0x01 0x01
   - 0x99 0x37 0x00
6. Configure **0xBF80_0923** and **0xBF80_0924** to set the PIO24 and PIO32 as output HIGH.
   - 0x00 0x00 0x08 0x00 0x02 **0xBF 0x80 0x09 0x23** 0x01 0x01
   - 0x99 0x37 0x00

Note: The configuration for VBUS_PASS_THRU and PIO registers need to be done after the attach command.

3.4 FlexConnect on Type C Downstream Port

While flexing a USB-Type C® downstream port, the corresponding cc control logic to the port must be configured as upstream device role. The device role can be assigned through CC_HW_CTL_x register.

TABLE 9: PORT 1 CC HARDWARE CONTROL REGISTER

CC_HW_CTL_1 (BF80_5400h) RESET = 0005h			Port 1 CC Hardware Control Register (USB7252/USB7216 Only)
Bit	**Name**	**R/W**	**Description**
15:11	Reserved	R	Always read as ‘0.’
10	DEVICE_MODE	R	Status bit 0b = Device is in Companion mode. 1b = Device is in Standalone mode.
9:3	Reserved	R	Always read as ‘0.’
2	DEVICE_ROLE	R/W	Device role 0b = Device is configured as UFP. 1b = Device is configured as DFP.
1	Reserved	R	Always read as ‘0.’
0	STANDALONE	R/W	0b = Companion mode 1b = Standalone mode

TABLE 10: PORT 2 CC HARDWARE CONTROL REGISTER

CC_HW_CTL_2 (BF80_5800h) RESET = 0005h			Port 2 CC Hardware Control Register (USB7252 Only)
Bit	**Name**	**R/W**	**Description**
15:11	Reserved	R	Always read as ‘0.’
10	DEVICE_MODE	R	Status bit 0b = Device is in Companion mode. 1b = Device is in Standalone mode.
9:3	Reserved	R	Always read as ‘0.’
2	DEVICE_ROLE	R/W	Device role 0b = Device is configured as UFP. 1b = Device is configured as DFP.
1	Reserved	R	Always read as ‘0.’
0	STANDALONE	R/W	0b = Companion mode 1b = Standalone mode

EXAMPLE 2: SMBUS/I2C COMMAND FOR FLEXING TYPE C PORT

The following example shows a sequence of the SMBus command for flexing Type C Port 1 on USB7216/USB7252:

1. Write 0x01 to **0xBF80_0808** to flex USB2 Port 1.
   - 0x00 0x00 0x07 0x00 0x01 **0xBF 0x80 0x08 0x08** 0x01
   - 0x99 0x37 0x00
2. Write 0x01 to **0xBF80_0828** to flex USB3 Port 1.
   - 0x00 0x00 0x07 0x00 0x01 **0xBF 0x80 0x08 0x28** 0x01
   - 0x99 0x37 0x00
3. Write 0x01 to **0xBF80_5400** to change the device role for Port 1 CC Logic.
   - 0x00 0x00 0x07 0x00 0x01 **0xBF 0x80 0x54 0x00** 0x01
   - 0x99 0x37 0x00
4. Send attach command.
   - 0xAA 0x55 0x00

4.0 FLEXCONNECT USB COMMAND DETAILS

A special USB command SET_ROLE_SWITCH can be issued by the USB host to the internal Hub Feature Controller to initiate the FlexConnect. After the FlexConnect is initiated, the hub will automatically revert to the default Port 0 host state if one of the following conditions is met:

- If the new flex host sends a USB command which commands the hub to return to the default state
- If the new flex host is disconnected any time after the flex host has enumerated the hub
- If the hub has not yet been enumerated by the flex host after the ENUM_TIMEOUT expires
- If VBUS_DET signal on either the default host port or the new flex host port goes low

The USB command is a NO DATA Control transfer sent to Endpoint 0 of the internal Hub Feature Controller. On USB7216, the Hub Feature Controller is the internal device located on Port 6. On USB7206/USB7216, the Hub Feature Controller is the internal device located on Port 7. The SETUP command format is shown in Table 11.

TABLE 11: FLEXCONNECT SETUP PACKET

Setup Parameter	Value	Description
bmRequestType	0x41	Host to device, vendor class, targeted to interface
bRequest	0x90	SET_ROLE_SWITCH
wValue	0xYYYY	Refer to Table 12.
wIndex	0x0000	Reserved
wLength	00	No data

TABLE 12: WVALUE DETAIL OF FLEXCONNECT COMMAND SETUP PACKET

Bit	Name	Description
15:12	FLEX_USB3_PORT	LOGICAL downstream port to initiate or terminate FlexConnect 0001 = Port 1 0010 = Port 2 0011 = Port 3 0100 = Port 4 0101 = Port 5 (USB7206/USB7252 only) 0110 = Port 6 (USB7206/USB7252 only) All others = ***Invalid***
11	FLEX_USB3_ON	1 = Flex USB3 portion of hub. 0 = Unflex USB3 portion of hub or no change if hub is already unflexed.
10:8	ENUM_TIMEOUT	These bits control a timer which is started after FlexConnect is initiated. The hub will revert to unflexed state after timeout if the flex host does not enumerate the hub. 000 = No timeout defined (hub waits for enumeration indefinitely) 001 = 10 ms 010 = 100 ms 011 = 500 ms 100 = 1s 101 = 5s 110 = 10s 111 = 20s
7:6	Reserved	Always ‘0’
5	FLEX_CONNECT	Always 1 for selection of FlexConnect mode.
4	FLEX_USB2_ON	1 = Flex USB2 portion of hub. 0 = Unflex USB2 portion of hub or no change if hub is already unflexed.

TABLE 12: WVALUE DETAIL OF FLEXCONNECT COMMAND SETUP PACKET (CONTINUED)

Bit	Name	Description
3:0	FLEX_USB2_PORT	LOGICAL downstream port to initiate or terminate FlexConnect 0001 = Port 1 0010 = Port 2 0011 = Port 3 0100 = Port 4 0101 = Port 5 (USB7206/USB7252 only) 0110 = Port 6 (USB7206/USB7252 only) All others = ***Invalid***

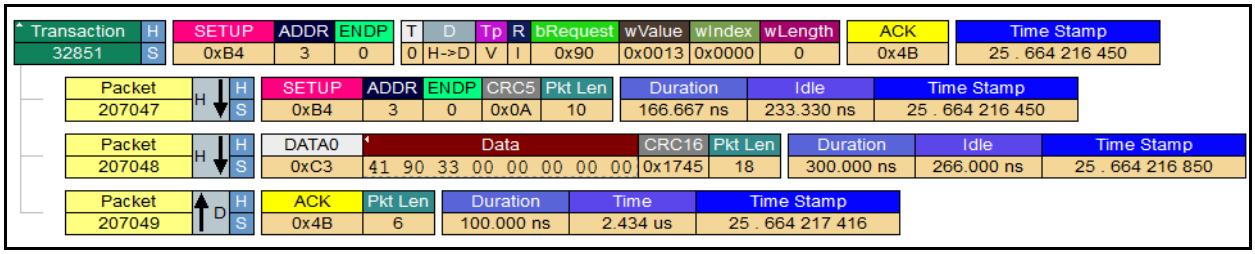
4.1 FlexConnect USB Command Example

An example of a FlexConnect initialization command for USB2 Hub to Port 3 is shown in Table 13. This command is sent to endpoint 0 of the Hub Feature Controller.

TABLE 13: FLEXCONNECT SETUP COMMAND EXAMPLE

Setup Parameter	Value	Note
bmRequestType	0x41	Host-to-device, vendor class, targeted to interface
bRequest	0x90	SET_ROLE_SWITCH
wValue	0x0033	Bits 15:12 = 0000b (No Flexing of USB3 portion of hub) Bit 11 = 0b (No Flexing of USB3 portion of hub) Bits 10:8 = 000b (No enumeration timeout) Bits 7:6 = 00b (Reserved and always 0) Bit 5 = 1b (Enter FlexConnect mode) Bit 4 = 1b (Flex of USB2 portion of hub) Bits 3:0 = 0011b (LOGICAL Port 3)
wIndex	0x0000	Reserved
wLength	00	No data

FIGURE 7: REGISTER READ SETUP TRANSACTION EXAMPLE



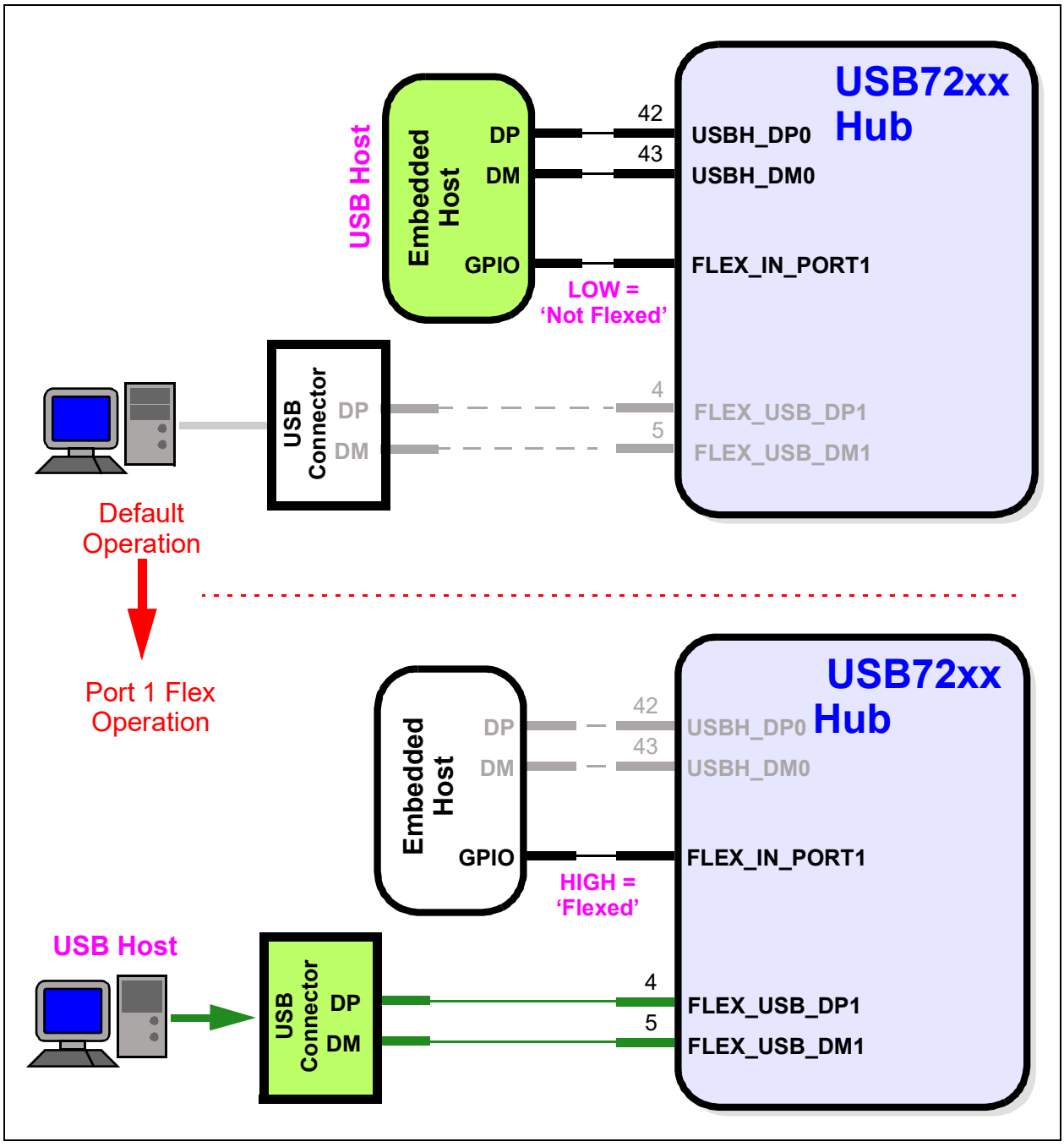
5.0 FLEXCONNECT PIN CONTROL

The FlexConnect can also be initiated through pin control by an embedded host. A selected number of available programmable function pins PFx may be assigned the role of FLEX_IN_PORTx.

If using the direct pin control method, each port which utilizes the FlexConnect feature must also be assigned its own FLEX_IN_PORTx signal. If multiple FLEX_IN_PORTx signals are triggered, the first triggered pin associated with its port will be flexed to an upstream port.

An example of how an embedded USB host may use the direct pin control method is shown in Figure 8.

FIGURE 8: FLEXCONNECT PIN CONTROL EXAMPLE



By default, FLEX_IN_PORT[1:6] pins are not assigned, and hence, not active. Only ports which are to be controlled via direct pin control must have a PF/GPIO pin assigned. Note that the assigned pins must be multiplexed to GPIO function.

Once one or more FLEX_IN_PORT[1:6] pins have been assigned, the pins will behave as shown in Table 14. Note that only one FLEX_IN_PORT[1:6] should be asserted at once.

TABLE 14: EXAMPLE FLEXCONNECT STATE TRUTH TABLE

FLEX_IN_PORT6	FLEX_IN_PORT5	FLEX_IN_PORT4	FLEX_IN_PORT3	FLEX_IN_PORT2	FLEX_IN_PORT1	FlexConnect State
0	0	0	0	0	0	Port 0 = Host Port
0	0	0	0	0	**1**	Port 1 = Host Port
0	0	0	0	**1**	0	Port 2 = Host Port
0	0	0	**1**	0	0	Port 3 = Host Port
0	0	**1**	0	0	0	Port 4 = Host Port
0	**1**	0	0	0		Port 5 = Host Port (USB7206/USB7252 Only)
1	0	0	0	0	0	Port 6 = Host Port (USB7206/USB7252 Only)
All Others						**INVALID STATE**

Note: The SMBus and USB command methods both have specific conditions wherein the hub will automatically unflex and return to the default Port 0 Host state. When using the direct pin control method, the hub will always follow the state of the pins and will never attempt to automatically unflex.

It is particularly important to understand that these control signals operated based on the hub's Logical Port assignments or how the ports are numbered as the USB host identifies the ports numbered. These control I/Os are not linked to the physical port numbering, which changes from one hub part number to another (since PHYs are grouped and remapped in various ways to form different combinations of Type-C and Type-A ports on the UFP and DFPs).

The pin assignment registers are detailed in Table 15 to Table 27. These can be modified through the hub's internal OTP memory or through the SMBus interface during hub start-up configuration. These pins cannot be modified through run-time register writes.

TABLE 15: LOGICAL PORT 2 FLEXCONNECT TRIGGER PIO CONFIGURATION REGISTER

FLEX_IN_PORT2 (BFD2_3443h)			FlexConnect Trigger PIO Configuration Register
Bit	**Name**	**R/W**	**Description**
7	USB2_FLEX_IN_EN	R/W	This bit is used for USB2.0 Hub. 1 = Enables FlexConnect trigger for the USB2.0 portion of Port 2 through GPIO control. The specific GPIO pin is selected in bits [2:0] of this register. The FlexConnect state is entered upon the rising edge of the selected GPIO. The FlexConnect state is exited upon the falling edge of the selected GPIO. 0 = Disables FlexConnect pin trigger for the USB2.0 portion of Port 2. All other bits in this register are ignored.
6:4	Reserved	R	Reserved

TABLE 15: LOGICAL PORT 2 FLEXCONNECT TRIGGER PIO CONFIGURATION REGISTER

FLEX_IN_PORT2 (BFD2_3443h)			FlexConnect Trigger PIO Configuration Register
Bit	**Name**	**R/W**	**Description**
3	USB3_FLEX_IN_EN	R/W	This bit is used for USB3.2 Hub. 1 = Enables FlexConnect trigger for the USB3.2 portion of Port 2 through GPIO control. The specific GPIO pin is selected in bits [2:0] of this register. The FlexConnect state is entered upon the rising edge of the selected GPIO. The FlexConnect state is exited upon the falling edge of the selected GPIO. 0 = Disables FlexConnect pin trigger for the USB3.2 portion of Port 2. All other bits in this register are ignored.
2:0	FLEX_IN_IO	R/W	This bit selects the GPIO to be used for the Logical Port 2 FlexConnect trigger. 000 = PF6/GPIO70 001 = PF7/GPIO71 010 = PF14/GPIO78 011 = PF19/GPIO83 100 = PF26/GPIO90 101 = PF27/GPIO91 110 = PF28/GPIO92 111 = PF29/GPIO93

TABLE 16: PORT 3 FLEXCONNECT TRIGGER PIO CONFIGURATION REGISTER

FLEX_IN_PORT3 (BFD2_3444h)			FlexConnect Trigger PIO Configuration Register
Bit	**Name**	**R/W**	**Description**
7	USB2_FLEX_IN_EN	R/W	This bit is used for USB2.0 Hub. 1 = Enables FlexConnect trigger for the USB2.0 portion of Port 3 through GPIO control. The specific GPIO pin is selected in bits [2:0] of this register. The FlexConnect state is entered upon the rising edge of the selected GPIO. The FlexConnect state is exited upon the falling edge of the selected GPIO. 0 = Disables FlexConnect pin trigger for the USB2.0 portion of Port 3. All other bits in this register are ignored.
6:4	Reserved	R	Reserved
3	USB3_FLEX_IN_EN	R/W	This bit is used for USB3.2 Hub. 1 = Enables FlexConnect trigger for the USB3.2 portion of Port 3 through GPIO control. The specific GPIO pin is selected in bits [2:0] of this register. The FlexConnect state is entered upon the rising edge of the selected GPIO. The FlexConnect state is exited upon the falling edge of the selected GPIO. 0 = Disables FlexConnect pin trigger for the USB3.2 portion of Port 3. All other bits in this register are ignored.

TABLE 16: PORT 3 FLEXCONNECT TRIGGER PIO CONFIGURATION REGISTER (CONTINUED)

FLEX_IN_PORT3 (BFD2_3444h)			FlexConnect Trigger PIO Configuration Register
Bit	**Name**	**R/W**	**Description**
2:0	FLEX_IN_IO	R/W	This bit selects the GPIO to be used for the Logical Port 3 FlexConnect trigger. 000 = PF6/GPIO70 001 = PF7/GPIO71 010 = PF14/GPIO78 011 = PF19/GPIO83 100 = PF26/GPIO90 101 = PF27/GPIO91 110 = PF28/GPIO92 111 = PF29/GPIO93

TABLE 17: PORT 4 FLEXCONNECT TRIGGER PIO CONFIGURATION REGISTER

FLEX_IN_PORT4 (BFD2_3445h)			FlexConnect Trigger PIO Configuration Register
Bit	**Name**	**R/W**	**Description**
7	USB2_FLEX_IN_EN	R/W	This bit is used for USB2.0 Hub. 1 = Enables FlexConnect trigger for the USB2.0 portion of Port 4 through GPIO control. The specific GPIO pin is selected in bits [2:0] of this register. The FlexConnect state is entered upon the rising edge of the selected GPIO. The FlexConnect state is exited upon the falling edge of the selected GPIO. 0 = Disables FlexConnect pin trigger for the USB2.0 portion of Port 4. All other bits in this register are ignored.
6:4	Reserved	R	Reserved
3	USB3_FLEX_IN_EN	R/W	This bit is used for USB3.2 Hub. 1 = Enables FlexConnect trigger for the USB3.2 portion of Port 4 through GPIO control. The specific GPIO pin is selected in bits [2:0] of this register. The FlexConnect state is entered upon the rising edge of the selected GPIO. The FlexConnect state is exited upon the falling edge of the selected GPIO. 0 = Disables FlexConnect pin trigger for the USB3.2 portion of Port 4. All other bits in this register are ignored.
2:0	FLEX_IN_IO	R/W	This bit selects the GPIO to be used for the Logical Port 4 FlexConnect trigger. 000 = PF6/GPIO70 001 = PF7/GPIO71 010 = PF14/GPIO78 011 = PF19/GPIO83 100 = PF26/GPIO90 101 = PF27/GPIO91 110 = PF28/GPIO92 111 = PF29/GPIO93

TABLE 18: PORT 5 FLEXCONNECT TRIGGER PIO CONFIGURATION REGISTER

FLEX_IN_PORT5 (BFD2_3446h)			FlexConnect Trigger PIO Configuration Register
Bit	**Name**	**R/W**	**Description**
7	USB2_FLEX_IN_EN	R/W	This bit is used for USB2.0 Hub. 1 = Enables FlexConnect trigger for the USB2.0 portion of Port 5 through GPIO control. The specific GPIO pin is selected in bits [2:0] of this register. The FlexConnect state is entered upon the rising edge of the selected GPIO. The FlexConnect state is exited upon the falling edge of the selected GPIO. 0 = Disables FlexConnect pin trigger for the USB2.0 portion of Port 5. All other bits in this register are ignored.
6:4	Reserved	R	Reserved
3	USB3_FLEX_IN_EN	R/W	This bit is used for USB3.2 Hub. 1 = Enables FlexConnect trigger for the USB3.2 portion of Port 5 through GPIO control. The specific GPIO pin is selected in bits [2:0] of this register. The FlexConnect state is entered upon the rising edge of the selected GPIO. The FlexConnect state is exited upon the falling edge of the selected GPIO. 0 = Disables FlexConnect pin trigger for the USB3.2 portion of Port 5. All other bits in this register are ignored.
2:0	FLEX_IN_IO	R/W	This bit selects the GPIO to be used for the Logical Port 5 FlexConnect trigger. 000 = PF6/GPIO70 001 = PF7/GPIO71 010 = PF14/GPIO78 011 = PF19/GPIO83 100 = PF26/GPIO90 101 = PF27/GPIO91 110 = PF28/GPIO92 111 = PF29/GPIO93

TABLE 19: PORT 6 FLEXCONNECT TRIGGER PIO CONFIGURATION REGISTER

FLEX_IN_PORT6 (BFD2_3447h)			FlexConnect Trigger PIO Configuration Register
Bit	**Name**	**R/W**	**Description**
7	USB2_FLEX_IN_EN	R/W	This bit is used for USB2.0 Hub. 1 = Enables FlexConnect trigger for the USB2.0 portion of Port 6 through GPIO control. The specific GPIO pin is selected in bits [2:0] of this register. The FlexConnect state is entered upon the rising edge of the selected GPIO. The FlexConnect state is exited upon the falling edge of the selected GPIO. 0 = Disables FlexConnect pin trigger for the USB2.0 portion of Port 6. All other bits in this register are ignored.
6:4	Reserved	R	Reserved
3	USB3_FLEX_IN_EN	R/W	This bit is used for USB3.2 Hub. 1 = Enables FlexConnect trigger for the USB3.2 portion of Port 6 through GPIO control. The specific GPIO pin is selected in bits [2:0] of this register. The FlexConnect state is entered upon the rising edge of the selected GPIO. The FlexConnect state is exited upon the falling edge of the selected GPIO. 0 = Disables FlexConnect pin trigger for the USB3.2 portion of Port 6. All other bits in this register are ignored.
2:0	FLEX_IN_IO	R/W	This bit selects the GPIO to be used for the Logical Port 6 FlexConnect trigger. 000 = PF6/GPIO70 001 = PF7/GPIO71 010 = PF14/GPIO78 011 = PF19/GPIO83 100 = PF26/GPIO90 101 = PF27/GPIO91 110 = PF28/GPIO92 111 = PF29/GPIO93

TABLE 20: PF6 CONTROL REGISTER

PF6_CTL (BF80_0C09h)			Programmable Function 6 Control Register
Bit	**Name**	**R/W**	**Description**
7:3	Reserved	R	These bits are always read as ‘0.’
2:0	Select	R	000 = GPIO70 001 = I2S_LRCK 010 = UART_RX 011 = DP1_DISCHARGE 100 = PD_SPI_CE_N0 101 = PRT_CTL1_U3

TABLE 21: PF7 CONTROL REGISTER

PF7_CTL (BF80_0C0Ah)			Programmable Function 7 Control Register
Bit	**Name**	**R/W**	**Description**
7:3	Reserved	R	These bits are always read as ‘0.’
2:0	Select	R	000 = GPIO71 001 = I2S_MCLK 010 = UART_TX 011 = DP1_DISCHARGE 100 = PD_SPI_CLK 101 = PRT_CTL2_U3

TABLE 22: PF14 CONTROL REGISTER

PF14_CTL (BF80_0C11h)			Programmable Function 14 Control Register
Bit	**Name**	**R/W**	**Description**
7:3	Reserved	R	These bits are always read as ‘0.’
2:0	Select	R	000 = GPIO78 001 = I2S_SDI 010 = UART_nCTS 011 = PRT_CTL4/OCS 100 = MSTR_I2C_CLK 101 = UART_nRTS 110 = UART_nDTR

TABLE 23: PF19 CONTROL REGISTER

PF19_CTL (BF80_0C16h)			Programmable Function 19 Control Register
Bit	**Name**	**R/W**	**Description**
7:3	Reserved	R	These bits are always read as ‘0.’
2:0	Select	R	000 = GPIO83 001 = I2S_SD0 010 = UART_nRTS 011 = SLV_I2C_DATA 100 = MSTR_I2C_DATA

TABLE 24: PF26 CONTROL REGISTER

PF26_CTL (BF80_0C1Dh)			Programmable Function 26 Control Register
Bit	**Name**	**R/W**	**Description**
7:3	Reserved	R	These bits are always read as ‘0.’
2:0	Select	R	000 = GPIO90 001 = I2S_SCK 010 = UART_nDSR 011 = Reserved 100 = SLV_I2C_CLK

TABLE 25: PF27 CONTROL REGISTER

PF27_CTL (BF80_0C1Eh)			Programmable Function 27 Control Register
Bit	**Name**	**R/W**	**Description**
7:3	Reserved	R	These bits are always read as ‘0.’
2:0	Select	R	000 = GPIO91 001 = I2S_MCLK 010 = UART_nDTR 011 = Reserved 100 = SLV_I2C_DATA 101 = PRT_CTL6/OCS 110 = UART_RX

TABLE 26: PF28 CONTROL REGISTER

PF28_CTL (BF80_0C1F)			Programmable Function 28 Control Register
Bit	**Name**	**R/W**	**Description**
7:3	Reserved	R	These bits are always read as ‘0.’
2:0	Select	R	000 = GPIO92 001 = I2S_LRCK 010 = UART_nDSD 011 = PRT_CTL6/OCS 100 = UART_TX

TABLE 27: PF29 CONTROL REGISTER

PF29_CTL (BF80_0C20h)			Programmable Function 29 Control Register
Bit	**Name**	**R/W**	**Description**
7:3	Reserved	R	These bits are always read as ‘0.’
2:0	Select	R	000 = GPIO93 Others = Reserved.

EXAMPLE 3: FLEXCONNECT VIA PIN CONTROL BY SMBUS/I2C COMMAND

An example of FlexConnect Port 5 on USB7206 through Pin Control PF29 is shown below.

1. Write 0x00 to **0xBF80_0C20** to configure PF29 as GPIO function.
   - 0x00 0x00 0x07 0x00 0x01 **0xBF 0x80 0x0C 0x20** 0x00
   - 0x99 0x37 0x00
2. Write 0x8F to **0xBFD2_3446** to flex USB2 and USB3 Port 5 through PF29.
   - 0x00 0x00 0x07 0x00 0x01 **0xBF 0xD2 0x34 0x46** 0x8F
   - 0x99 0x37 0x00
3. Write 0x00 to **0xBF80_3C40** to specify VBUS signal is from internal PIO24 and PIO32.
   - 0x00 0x00 0x07 0x00 0x01 **0xBF 0x80 0x3C 0x40** 0x00
   - 0x99 0x37 0x00
4. Configure **0xBF80_0903** & **0xBF80_0904** to set the direction of PIO24 and PIO32 as OUTPUT.
   - 0x00 0x00 0x08 0x00 0x02 **0xBF 0x80 0x09 0x03** 0x01 0x01
   - 0x99 0x37 0x00
5. Configure **0xBF80_0923** & **0xBF80_0924** to set the PIO24 and PIO32 as output HIGH.
   - 0x00 0x00 0x08 0x00 0x02 **0xBF 0x80 0x09 0x23** 0x01 0x01

- 0x99 0x37 0x00

6. Pull high the PF29 externally to flex the host.
7. Send attach command. (See Note 1.)
   - 0xAA 0x56 0x00

EXAMPLE 4: FLEXCONNECT VIA PIN CONTROL BY OTP PATCH

An example of FlexConnect Port 1 on USB7252 through Pin Control PF29 is shown below.

1. Write 0x00 to 0xBF80_0C20 to configure PF29 as GPIO function.
   - XWRE_BF800C20 = 00
2. Write 0x8F to 0xBFD2_3442 to flex USB2 and USB3 Port 1 through PF29.
   - XWRE_BFD23442 = 8F
3. Write 0x01 to 0xBF80_5400 to change the device role of Port 1 as UFP.
   - XWRE_BF805400 = 01
4. Write 0x00 to 0xBF80_3C40 to specify VBUS signal is from internal PIO24 and PIO32.
   - XWRE_BF803C40 = 00
5. Configure 0xBF80_0903 & 0xBF80_0904 to set the direction of PIO24 and PIO32 as OUTPUT.
   - XWRE_BF800903 = 01 01
6. Configure 0xBF80_0923 & 0xBF80_0924 to set the PIO24 and PIO32 as output HIGH.
   - XWRE_BF800923 = 01 01

(See Note 2.)

Note 1: The hub is reset every time FlexConnect is initiated or terminated. If the SMBus configuration channel is used in the system implementation, the hub will wait in the configuration stage until it is configured and instructed to enter the runtime stage via the SMBus Attach command. This can create conflicts if FlexConnect is triggered via Direct Pin Control or USB Command methods along with SMBus configuration. As the host controller configuring the hub, it must be aware of the change in FlexConnect state and ensure to reconfigure the hub in a timely manner.

2: A known issue for FlexConnect USB 3.0 connection appears in silicon Revision C and can be avoided by performing the following steps:

1. Run the hub using SPI Flash memory.
2. Disable the host (PC) power management. For further information, refer to the *USB72x6/USB7252 Silicon Errata*.

6.0 FLEX CONFIGURATION SPACE

The FlexConnect Configuration Space is a general configuration option which loads setting that shall only take effect while the hub is in Flexed state. Any feature which is usually configured via hub configuration registers may be included in the hub FlexConnect Configuration Space. Features such as port disable or enable, battery charging configuration and more can be programmed to take effect once in the Flexed state. The FlexConnect Configuration Space (FLEX-CFG) space utilizes the same command format as general hub configuration files (.cfg) which are generated using the MPLAB® Connect Configurator tool. The same methods used to generate these files for general configuration may also be applied here. Refer to the following registers and example for additional details on how to use the FlexConnect Configuration Space.

TABLE 28: FLEX CONFIGURATION CONTROL REGISTER

FLEX_CTL_REG (BFD2_345Bh)			Flex Configuration Control Register
Bit	**Name**	**R/W**	**Description**
7	OTP_FLEXCFG	R/W	This bit indicates if the FLEXCFG data is provided dynamically from the USB host or if FLEXCFG data is statically configured on a per-port basis via hub OTP memory. 0b = FLEXCFG area shall be dynamically populated by the host. This method allows for the highest level of flexibility, but requires software on the USB host to control FlexConnect and load new FLEXCFG data before each FlexConnect transition. 1b = Each flex port shall have its own configuration chunk within the FLEXCFG_DATA. The data for every port shall begin right at the start of the buffer only. APPLY_FLEXCFG & FLEX_CFG_LEN are all invalid in this mode of operation.
6:1	Reserved	R	Reserved
0	APPLY_FLEXCFG	R/W	1 = FLEXCFG configuration of length specified in the FLEXCFG_LEN register will be applied during the Flex state transition 0 = FLEXCFG configuration will not be applied on the next Flex state transition.

TABLE 29: FLEX CONFIGURATION DATA REGISTERS

FLEXCFG_DATA (BFD2_3800h-BFD2_3BFFh)			Flex Configuration Data Registers
BYTE	**Name**	**R/W**	**Description**
1,023:0	FLEXCFG_DATA	R/W	Bytes from the configurations for FLEXCFG are programmed here. Up to 1,024 bytes of configuration data may be loaded. The standard OTP configuration file format shall be used. See *Microchip AN2935 - Configuration of USB7202/USB7206/USB725x* for details on configuration file formatting, or use the MPLAB Connect Configurator tool to generate a '.cfg' file. The binary data within the '.cfg' file can be placed directly into these registers. When OTP_FLEXCFG = 0b, then entire FLEXCFG_DATA space may be used, and the length of the configuration data must be properly defined in FLEXCFG_LEN. When OTP_FLEXCFG = 1b, this space is chunked into portions which are allocated to logical port numbers. When FlexConnect is initiated to a logical port, the FLEXCFG data which pertains only to that logical port is loaded. Logical Port 1: Bytes 00 - 170 Logical Port 2: Bytes 171 - 340 Logical Port 3: Bytes 340 - 510 Logical Port 4: Bytes 511 - 680 Logical Port 5: Bytes 681 - 850 Logical Port 6: Bytes 851 - 1,020 Unused: Bytes 1,021 - 1,023

TABLE 30: FLEX CONFIGURATION LENGTH REGISTERS

FLEXCFG_LEN (BFD2_345Ch-BFD2_345Dh)			Flex Configuration Length Registers
Bit	**Name**	**R/W**	**Description**
15:10	Reserved	R	Reserved
9:0	FLEXCFG_LEN	R/W	This field indicates the length of the FLEXCFG data. This is only used if OTP_FLEXCFG = 0b.

6.1 Recommended Procedure for a Dynamic USB Host-Controlled FLEXCFG Data (OTP_FLEXCFG = 0b)

The recommended procedure for implementing dynamic USB Host-controlled FLEXCFG is as follows:

1) Create a configuration file with all the options that are to be applied after flexing.

2) Program the bytes from the configuration file starting at the first register of FLEXCFG_DATA (BFD2_3800h).

3) Program the length of the data in the configuration file/FLEXCFG_DATA area into the FLEXCFG_LEN register.

4) Set the APPLY_FLEXCFG bit in the FLEX_CTL_REG register.

5) Send the FlexConnect USB command SET_ROLE_SWITCH.

At this point, the data from the FLEXCFG_DATA registers of length FLEXCFG_LEN will be applied to the hub and can be seen by the new flexed host.

If the same configuration is to be programmed when the next FlexConnect occurs, simply rewrite the length of the FLEXCFG patch in FLEXCFG_LEN and send the FlexConnect USB command. If FLEXCFG_DATA is to be updated, clear out the data in the FLEXCFG_DATA area and repeat the recommended procedure.

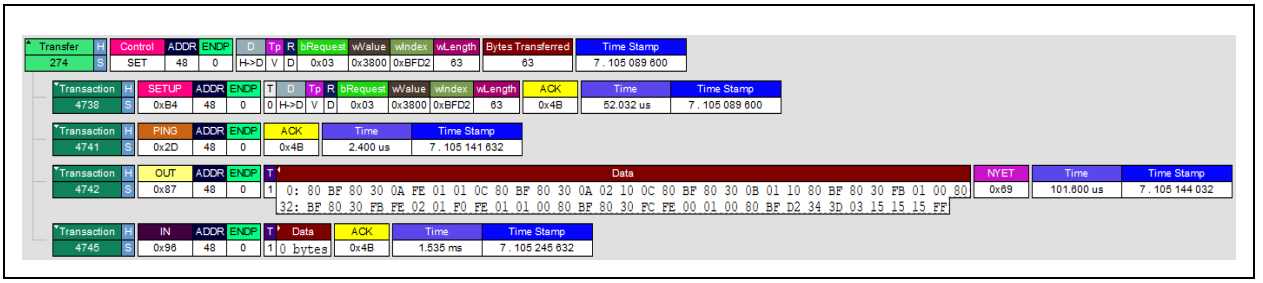
Below is an example configuration that might be programmed into the FLEXCFG space as well as a USB trace of the process.

Step 1: Create a configuration file with all the options to be applied after flexing.

In this example, FlexConnect will be sent to Port 1. This configuration file will disable Ports 2 to 4 and set them to be dedicated charging ports (DCP). After flexing, the new host will see a two-port hub with the other 3 ports set to DCP.

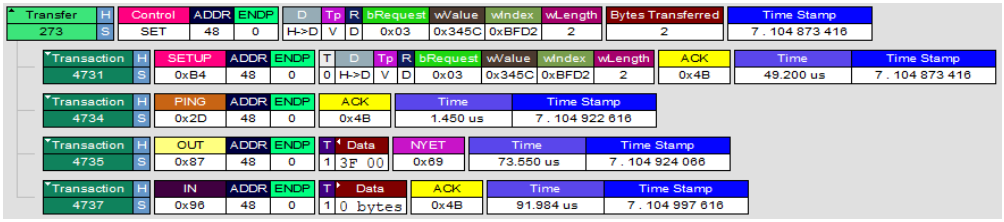
Step 2: Program the bytes from the configuration file starting at the first register of FLEXCFG_DATA. See Figure 9.

FIGURE 9: WRITING FLEXCFG_DATA TRANSACTION EXAMPLE



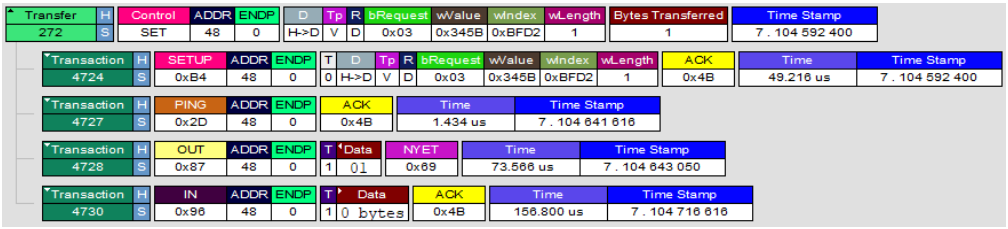
Step 3: Program the length of the data in the configuration file/FLEXCFG_DATA area into the FLEXCFG_LEN register. See Figure 10.

FIGURE 10: WRITING FLEXCFG_LEN TRANSACTION EXAMPLE



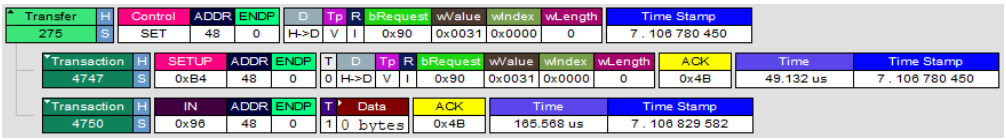
Step 4: Set the APPLY_FLEXCFG bit in the FLEXCFG_CTL_REG. See Figure 11.

FIGURE 11: WRITING FLEXCFG_CTL TRANSACTION EXAMPLE



Step 5: Send the FlexConnect command. See Figure 12.

FIGURE 12: SENDING FLEXCONNECT COMMAND TO PORT 1 TRANSACTION EXAMPLE



Note: Battery charging enabling/disabling through the FLEX_CFG space is not supported. If battery charging is to be enabled on a port via the FLEXCFG space like in the example above, battery charging **must** also be enabled via OTP or strapping in the original unflexed configuration. For example if Port 2 is to be configured as a battery charging port in the FLEXCFG space then battery charging must be enabled via the CFG_B-C_EN strap or OTP write in the default unflexed state.

7.0 ADDITIONAL HARDWARE CONSIDERATIONS

Schematics for FlexConnect applications are implementation specific and hence do not necessarily follow any common framework. The succeeding sections show few common considerations that must be made for each design.

7.1 Host VBUS Detection

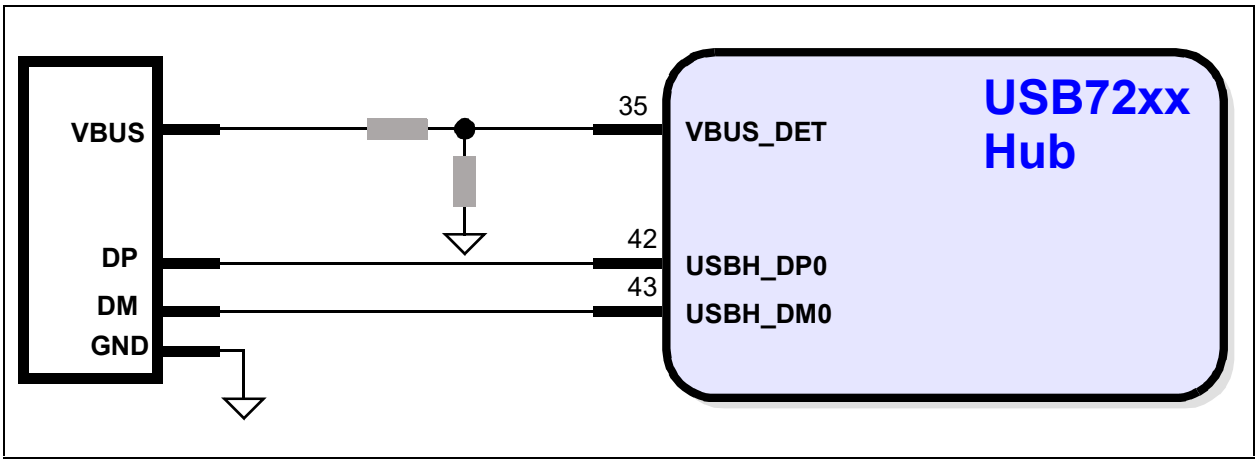
The upstream VBUS detection is a signal used by the hub to determine when a USB host is connected. When VBUS_MON_UP/VBUS_DET is not present, the hub enters a Low-Power state to conserve energy. This will cause the hub to disconnect when either is enumerated through the upstream port or the new flexed upstream port.

7.1.1 NO POWER ROLE SWAP VBUS_DET IMPLEMENTATION

If power roles do not change when initiating FlexConnect, it may simply connect VBUS_DET directly to the default USB host's VBUS pin through a resistor divider. As shown in Figure 13, this is a popular implementation in the automotive application space as the head unit will always be connected to the hub.

Note that you must ensure that the default USB host will not toggle its VBUS supply at any time when FlexConnect is initiated. Otherwise, the hub will be reset and will revert to its default state.

FIGURE 13: NO POWER ROLE SWAP VBUS_DET CONFIGURATION



7.1.2 CONNECT VBUS_DET DIRECTLY TO A FIXED 3.3V

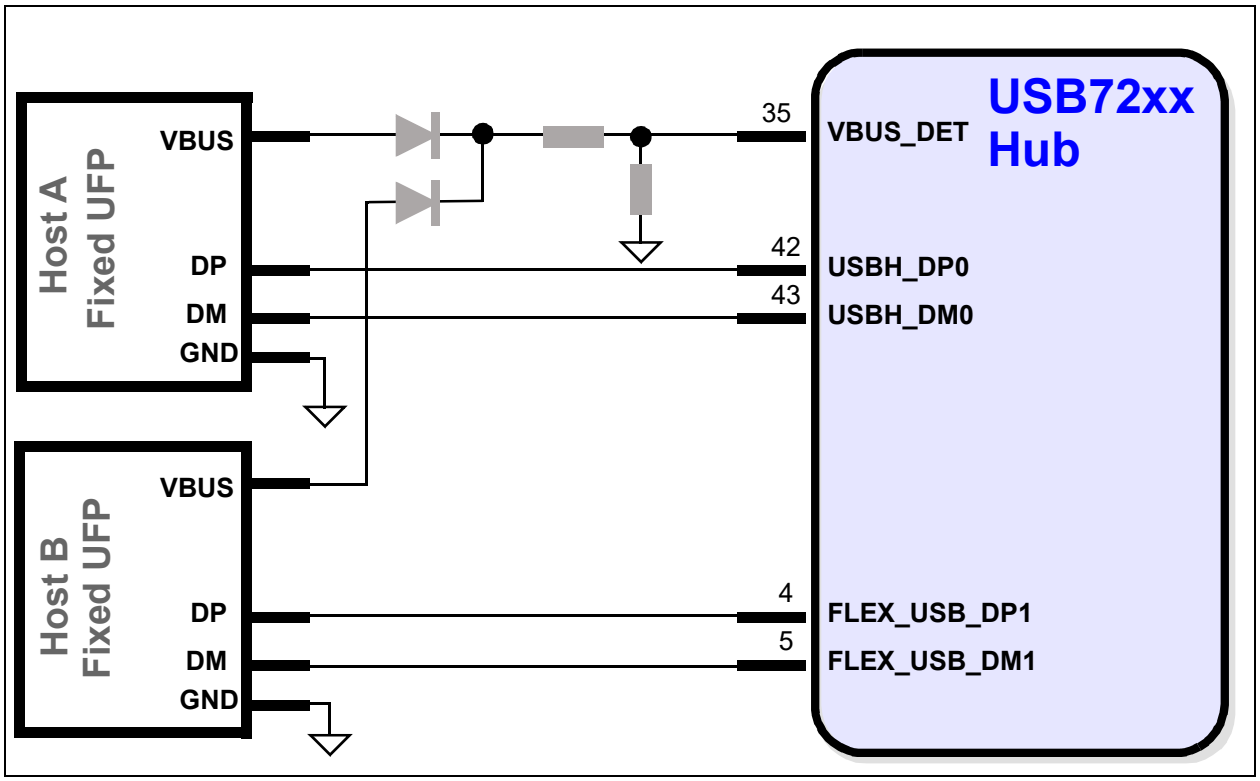
If Low-Power states are not required when no USB host is present, it is acceptable to connect VBUS_DET to a fixed 3.3V supply on the PCB. This method is only recommended for designs wherein the hub is connected to an embedded host.

Note that in some instances, a USB host may attempt to force a hard Reset on a device by toggling VBUS. In this instance, the hub will not reset.

7.1.3 'OR' ALL HOST VBUS CONNECTIONS TO VBUS_DET

In Host-Sharing-type systems, "OR"-ing all host VBUS connections would be an appropriate solution as shown in Figure 14. This can be used when the "one-host-at-a-time" implementation is used. The drawback with this type of solution is that there is no way to distinguish which host port is actually supplying VBUS.

FIGURE 14: DIODE-OR VBUS_DET SIGNALS

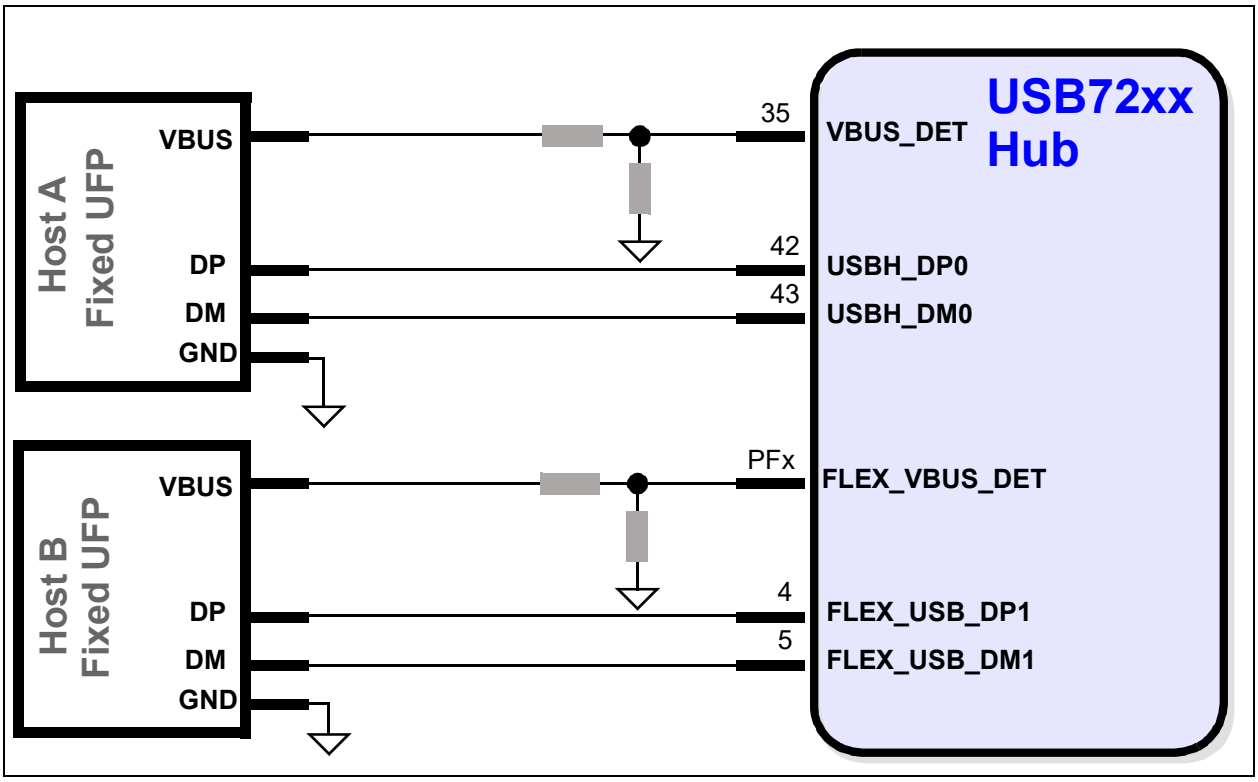


Note:	The resistor divider values will change depending on the characteristics of the diodes used.

7.1.4 ASSIGN A SPECIFIC FLEX_VBUS_DET PIN

An available PFx/GPIOx pin may be reassigned the role of FLEX_VBUS_DET either permanently via the hub OTP configuration or dynamically through the FLEX_CFG space. If using the FLEX_VBUS_DET option, the standard/default VBUS_DET pin is ignored while in the Flexed state. Likewise, the FLEX_VBUS_DET pin state is ignored while the hub is in default state. Note that when FLEX_VBUS_DET is enabled, the PIO24 and PIO32 options in VBUS Pass Through Register are selected automatically and the states of PIO24 and PIO32 will follow the FLEX_VBUS_DET pin.

FIGURE 15: DIODE-OR VBUS_DET SIGNALS



The register for controlling this feature is detailed in Table 31.

TABLE 31: FLEX_VBUS_DET CONFIGURATION REGISTER

FLEX_VBUSDET_REG (BFD2_3454h)			FlexConnect VBUS Detect Configuration Register
Bit	**Name**	**R/W**	**Description**
7	FLEX_VBUSDET_EN	R/W	1 = The specific GPIO is selected in bits [2:0] of this register is the VBUS detection pin while the hub is in the Flexed state. 0 = The standard/default VBUS detection pin is also used as the VBUS detection pin while in the Flexed state.
6	FLEX_OUT_ACTIVE_HIGH	R/W	1 = VBUS_DET is forced high internally such that VBUS is always detected by the hub regardless of the pin state. All other bits in this register is ignored. 0 = VBUS_DET to the hub is driven based on FLEX_VBUSDET_EN.
5:3	Reserved	R	Reserved

TABLE 31: FLEX_VBUS_DET CONFIGURATION REGISTER (CONTINUED)

FLEX_VBUSDET_REG (BFD2_3454h)			FlexConnect VBUS Detect Configuration Register
Bit	**Name**	**R/W**	**Description**
2:0	FLEX_OUT_IO	R/W	Selects the GPIO to be used as FLEX_VBUS_DET 000 = PF6/GPIO70 001 = PF7/GPIO71 010 = PF14/GPIO78 011 = PF19/GPIO83 100 = PF26/GPIO90 101 = PF27/GPIO91 110 = PF28/GPIO92 111 = PF29/GPIO93

7.2 Port 1 to 6 Port Power Control

The required behavior of the PRT_CTLx pins should be considered before and after the FlexConnect mode is initiated during the system architecture design phase of the application.

Additional configuration options exist which allow the end system integrator to change how PRT_CTLx works while in the Flexed state or assign a wholly new output signal to be activated while in the Flexed state. Table 32 describes the possible configuration options.

TABLE 32: PRT_CTLX BEHAVIORAL PPTIONS

FLEX_PRTCTL_EN	FLEX_PRTCTL_PIO_EN	Unflexed Port Control Output Behavior	Flexed Port Control Output Behavior
0 [default]	0 [default]	**PRT_CTLx:** Controlled from USB Host commands. The pin will enable an internal 50 kΩ pull-up resistor when the USB host issues to command to enable power to the port, and will drive low during hub initialization or when the USB host issues to command to disable power to the port. **FLEX_PRTCTL:** No action	**PRT_CTLx:** Set to Output and Drive High **FLEX_PRTCTL:** No action
0	1		**PRT_CTLx:** Set to Output and Drive High **FLEX_PRTCTL:** No action
1	0		**PRT_CTLx:** Set per PRTCTL_OUT[1:0] bit field **FLEX_PRTCTL:** No action
1	1		**PRT_CTLx:** Set to Output and Drive High **FLEX_PRTCTL:** Selected GPIO is set per PRTCTL_OUT[1:0] bit field.

Each physical port which utilizes the FlexConnect feature must be configured if settings which deviate from the default options are desired by the end system integrator.

TABLE 33: PHYSICAL PORT 1 FLEXCONNECT PORT POWER CONTROL REGISTER

FLEX_PRTCTL_PORT1 (BFD2_344Eh)			FlexConnect Port Power Control Register
Bit	**Name**	**R/W**	**Description**
7	FLEX_PRTCTL_EN	R/W	1 = Enables alternate port power control operation which functions per the control bits within this register. 0 = Default operation. The standard PRT_CTL1 is set as an output and driven high while in the flexed state.
6:5	PRTCTL_OUT[1:0]	R/W	00 = Tristated 01 = Drive high 10 = Drive low 11 = Internal Pull-up resistor
4	Reserved	R	Reserved
3	FLEX_PRTCTL_PIO_EN	R/W	1 = GPIO selected in FLEX_PRTCTL_PIO is set to the state selected in PRTCTL_OUT[1:0]. 0 = The standard PRT_CTL1 pin is set to the state selected in PRTCTL_OUT[1:0].
2:0	FLEX_PRTCTL_PIO	R/W	This bit selects the GPIO to be used for the Physical Port 1 FlexConnect port power control. 000 = PF6/GPIO70 001 = PF7/GPIO71 010 = PF14/GPIO78 011 = PF19/GPIO83 100 = PF26/GPIO90 101 = PF27/GPIO91 110 = PF28/GPIO92 111 = PF29/GPIO93

TABLE 34: PHYSICAL PORT 2 FLEXCONNECT PORT POWER CONTROL REGISTER

FLEX_PRTCTL_PORT2 (BFD2_344Fh)			FlexConnect Port Power Control Register
Bit	**Name**	**R/W**	**Description**
7	FLEX_PRTCTL_EN	R/W	1 = Enables alternate port power control operation which functions per the control bits within this register. 0 = Default operation. The standard PRT_CTL2 is set as an output and driven high while in the flexed state.
6:5	PRTCTL_OUT[1:0]	R/W	00 = Tristated 01 = Drive high 10 = Drive low 11 = Internal Pull-up resistor
4	Reserved	R	Reserved

TABLE 34: PHYSICAL PORT 2 FLEXCONNECT PORT POWER CONTROL REGISTER

FLEX_PRTCTL_PORT2 (BFD2_344Fh)			FlexConnect Port Power Control Register
Bit	**Name**	**R/W**	**Description**
3	FLEX_PRTCTL_PIO_EN	R/W	1 = GPIO selected in FLEX_PRTCTL_PIO is set to the state selected in PRTCTL_OUT[1:0]. 0 = The standard PRT_CTL2 pin is set to the state selected in PRTCTL_OUT[1:0].
2:0	FLEX_PRTCTL_PIO	R/W	This bit selects the GPIO to be used for the Physical Port 2 FlexConnect port power control. 000 = PF6/GPIO70 001 = PF7/GPIO71 010 = PF14/GPIO78 011 = PF19/GPIO83 100 = PF26/GPIO90 101 = PF27/GPIO91 110 = PF28/GPIO92 111 = PF29/GPIO93

TABLE 35: PHYSICAL PORT 3 FLEXCONNECT PORT POWER CONTROL REGISTER

FLEX_PRTCTL_PORT3 (BFD2_3450h)			FlexConnect Port Power Control Register
Bit	**Name**	**R/W**	**Description**
7	FLEX_PRTCTL_EN	R/W	1 = Enables alternate port power control operation which functions per the control bits within this register. 0 = Default operation. The standard PRT_CTL3 is set as an output and driven high while in the flexed state.
6:5	PRTCTL_OUT[1:0]	R/W	00 = Tristated 01 = Drive high 10 = Drive low 11 = Internal Pull-up resistor
4	Reserved	R	Reserved
3	FLEX_PRTCTL_PIO_EN	R/W	1 = GPIO selected in FLEX_PRTCTL_PIO is set to the state selected in PRTCTL_OUT[1:0]. 0 = The standard PRT_CTL3 pin is set to the state selected in PRTCTL_OUT[1:0].
2:0	FLEX_PRTCTL_PIO	R/W	This bit selects the GPIO to be used for the Physical Port 3 FlexConnect port power control. 000 = PF6/GPIO70 001 = PF7/GPIO71 010 = PF14/GPIO78 011 = PF19/GPIO83 100 = PF26/GPIO90 101 = PF27/GPIO91 110 = PF28/GPIO92 111 = PF29/GPIO93

TABLE 36: PHYSICAL PORT 4 FLEXCONNECT PORT POWER CONTROL REGISTER

FLEX_PRTCTL_PORT4 (BFD2_3451h)			FlexConnect Port Power Control Register
Bit	**Name**	**R/W**	**Description**
7	FLEX_PRTCTL_EN	R/W	1 = Enables alternate port power control operation which functions per the control bits within this register. 0 = Default operation. The standard PRT_CTL4 is set as an output and driven high while in the Flexed state.
6:5	PRTCTL_OUT[1:0]	R/W	00 = Tristated 01 = Drive high 10 = Drive low 11 = Internal Pull-up resistor
4	Reserved	R	Reserved
3	FLEX_PRTCTL_PIO_EN	R/W	1 = GPIO selected in FLEX_PRTCTL_PIO is set to the state selected in PRTCTL_OUT[1:0]. 0 = The standard PRT_CTL4 pin is set to the state selected in PRTCTL_OUT[1:0].
2:0	FLEX_PRTCTL_PIO	R/W	This bit selects the GPIO to be used for the Physical Port 4 FlexConnect port power control. 000 = PF6/GPIO70 001 = PF7/GPIO71 010 = PF14/GPIO78 011 = PF19/GPIO83 100 = PF26/GPIO90 101 = PF27/GPIO91 110 = PF28/GPIO92 111 = PF29/GPIO93

TABLE 37: PHYSICAL PORT 5 FLEXCONNECT PORT POWER CONTROL REGISTER

FLEX_PRTCTL_PORT5 (BFD2_3452h)			FlexConnect Port Power Control Register
Bit	**Name**	**R/W**	**Description**
7	FLEX_PRTCTL_EN	R/W	1 = Enables alternate port power control operation which functions per the control bits within this register. 0 = Default operation. The standard PRT_CTL5 is set as an output and driven high while in the flexed state.
6:5	PRTCTL_OUT[1:0]	R/W	00 = Tristated 01 = Drive high 10 = Drive low 11 = Internal Pull-up resistor
4	Reserved	R	Reserved
3	FLEX_PRTCTL_PIO_EN	R/W	1 = GPIO selected in FLEX_PRTCTL_PIO is set to the state selected in PRTCTL_OUT[1:0]. 0 = The standard PRT_CTL5 pin is set to the state selected in PRTCTL_OUT[1:0].

TABLE 37: PHYSICAL PORT 5 FLEXCONNECT PORT POWER CONTROL REGISTER

FLEX_PRTCTL_PORT5 (BFD2_3452h)			FlexConnect Port Power Control Register
Bit	**Name**	**R/W**	**Description**
2:0	FLEX_PRTCTL_PIO	R/W	This bit selects the GPIO to be used for the Physical Port 5 FlexConnect port power control. 000 = PF6/GPIO70 001 = PF7/GPIO71 010 = PF14/GPIO78 011 = PF19/GPIO83 100 = PF26/GPIO90 101 = PF27/GPIO91 110 = PF28/GPIO92 111 = PF29/GPIO93

TABLE 38: PHYSICAL PORT 6 FLEXCONNECT PORT POWER CONTROL REGISTER

FLEX_PRTCTL_PORT6 (BFD2_3453h)			FlexConnect Port Power Control Register
Bit	**Name**	**R/W**	**Description**
7	FLEX_PRTCTL_EN	R/W	1 = Enables alternate port power control operation which functions per the control bits within this register. 0 = Default operation. The standard PRT_CTL6 is set as an output and driven high while in the flexed state.
6:5	PRTCTL_OUT[1:0]	R/W	00 = Tristated 01 = Drive high 10 = Drive low 11 = Internal Pull-up resistor
4	Reserved	R	Reserved
3	FLEX_PRTCTL_PIO_EN	R/W	1 = GPIO selected in FLEX_PRTCTL_PIO is set to the state selected in PRTCTL_OUT[1:0]. 0 = The standard PRT_CTL6 pin is set to the state selected in PRTCTL_OUT[1:0].
2:0	FLEX_PRTCTL_PIO	R/W	This bit selects the GPIO to be used for the Physical Port 6 FlexConnect port power control. 000 = PF6/GPIO70 001= PF7/GPIO71 010 = PF14/GPIO78 011 = PF19/GPIO83 100 = PF26/GPIO90 101 = PF27/GPIO91 110 = PF28/GPIO92 111 = PF29/GPIO93

7.3 FlexConnect State Indicator Output

GPIOs may also be assigned the role of FlexConnect status indicator outputs. The use of these outputs is completely optional. These outputs can be connected to external LEDs or an embedded microcontroller to communicate the current FlexConnect state.

The GPIO can be configured as drive high/drive low or open drain, and the polarity can be configured. This mode should not be used in combination with the FlexConnect GPIO input mode.

Note:	These outputs operate with respect to the PHYSICAL port numbering (which is different than the FlexConnect input control operation)

TABLE 39: PHYSICAL PORT 1 FLEXCONNECT STATE INDICATOR GPIO CONFIGURATION REGISTER

FLEX_OUT_PORT1 (BFD2_3448h)			**FlexConnect State Indicator GPIO Configuration**
Bit	**Name**	**R/W**	**Description**
7	FLEX_OUT_EN	R/W	1 = Enables FlexConnect state indicator for Port 1 through GPIO. The specific GPIO is selected in bits [2:0] of this register. 0 = Disables FlexConnect state indicator for Port 1 through GPIO. All other bits in this register are ignored.
6	FLEX_OUT_ACTIVE_HIGH	R/W	1 = The selected GPIO is driven active-high while in FlexConnect state. Driven low otherwise. 0 = The selected GPIO is driven active-low while in FlexConnect state. Driven high otherwise.
5	FLEX_OUT_OD	R/W	1 = The selected GPIO is Open-drain Output mode. 0 = The selected GPIO is drive high/drive Low-output mode.
4:3	Reserved	R	Reserved
2:0	FLEX_OUT_IO	R/W	This bit selects the GPIO to be used for the Physical Port 1 FlexConnect state indicator. 000 = PF6/GPIO70 001 = PF7/GPIO71 010 = PF14/GPIO78 011 = PF19/GPIO83 100 = PF26/GPIO90 101 = PF27/GPIO91 110 = PF28/GPIO92 111 = PF29/GPIO93

TABLE 40: PHYSICAL PORT 2 FLEXCONNECT STATE INDICATOR GPIO CONFIGURATION REGISTER

FLEX_OUT_PORT2 (BFD2_3449h)			FlexConnect State Indicator GPIO Configuration
Bit	**Name**	**R/W**	**Description**
7	FLEX_OUT_EN	R/W	1 = Enables FlexConnect state indicator for Port 2 through GPIO. The specific GPIO is selected in bits [2:0] of this register. 0 = Disables FlexConnect state indicator for Port 2 through GPIO. All other bits in this register are ignored.
6	FLEX_OUT_ACTIVE_HIGH	R/W	1 = The selected GPIO is driven active-high while in FlexConnect state. Driven low otherwise. 0 =The selected GPIO is driven active-low while in FlexConnect state. Driven high otherwise.
5	FLEX_OUT_OD	R/W	1 = The selected GPIO is Open-drain Output mode. 0 = The selected GPIO is drive high/drive Low Output mode.
4:3	Reserved	R	Reserved
2:0	FLEX_OUT_IO	R/W	This bit selects the GPIO to be used for the Physical Port 2 FlexConnect state indicator. 000 = PF6/GPIO70 001 = PF7/GPIO71 010 = PF14/GPIO78 011 = PF19/GPIO83 100 = PF26/GPIO90 101 = PF27/GPIO91 110 = PF28/GPIO92 111 = PF29/GPIO93

FIGURE 16: PHYSICAL PORT 3 FLEXCONNECT STATE INDICATOR GPIO CONFIGURATION REGISTER

FLEX_OUT_PORT3 (BFD2_344Ah)			FlexConnect State Indicator GPIO Configuration
Bit	**Name**	**R/W**	**Description**
7	FLEX_OUT_EN	R/W	1 = Enables FlexConnect state indicator for Port 3 through GPIO. The specific GPIO is selected in bits [2:0] of this register. 0 = Disables FlexConnect state indicator for Port 3 through GPIO. All other bits in this register are ignored.
6	FLEX_OUT_ACTIVE_HIGH	R/W	1 = The selected GPIO is driven active-high while in FlexConnect state. Driven low otherwise. 0 =The selected GPIO is driven active-low while in FlexConnect state. Driven high otherwise.
5	FLEX_OUT_OD	R/W	1 = The selected GPIO is Open-drain Output mode. 0 = The selected GPIO is drive high/drive Low Output mode.

FIGURE 16: PHYSICAL PORT 3 FLEXCONNECT STATE INDICATOR GPIO CONFIGURATION REGISTER

FLEX_OUT_PORT3 (BFD2_344Ah)			FlexConnect State Indicator GPIO Configuration
Bit	**Name**	**R/W**	**Description**
4:3	Reserved	R	Reserved
2:0	FLEX_OUT_IO	R/W	This bit selects the GPIO to be used for the Physical Port 3 FlexConnect state indicator. 000 = PF6/GPIO70 001 = PF7/GPIO71 010 = PF14/GPIO78 011 = PF19/GPIO83 100 = PF26/GPIO90 101 = PF27/GPIO91 110 = PF28/GPIO92 111 = PF29/GPIO93

TABLE 41: PHYSICAL PORT 4 FLEXCONNECT STATE INDICATOR GPIO CONFIGURATION REGISTER

FLEX_OUT_PORT4 (BFD2_344Bh)			FlexConnect State Indicator GPIO Configuration
Bit	**Name**	**R/W**	**Description**
7	FLEX_OUT_EN	R/W	1 = Enables FlexConnect state indicator for Port 4 through GPIO. The specific GPIO is selected in bits [2:0] of this register. 0 = Disables FlexConnect state indicator for Port 4 through GPIO. All other bits in this register are ignored.
6	FLEX_OUT_ACTIVE_HIGH	R/W	1 = The selected GPIO is driven active-high while in FlexConnect state. Driven low otherwise. 0 = The selected GPIO is driven active-low while in FlexConnect state. Driven high otherwise.
5	FLEX_OUT_OD	R/W	1 = The selected GPIO is Open-drain Output mode. 0 = The selected GPIO is drive high/drive Low-output mode.
4:3	Reserved	R	Reserved
2:0	FLEX_OUT_IO	R/W	This bit selects the GPIO to be used for the Physical Port 4 FlexConnect state indicator. 000 = PF6/GPIO70 001 = PF7/GPIO71 010 = PF14/GPIO78 011 = PF19/GPIO83 100 = PF26/GPIO90 101 = PF27/GPIO91 110 = PF28/GPIO92 111 = PF29/GPIO93

TABLE 42: PHYSICAL PORT 5 FLEXCONNECT STATE INDICATOR GPIO CONFIGURATION REGISTER

FLEX_OUT_PORT5 (BFD2_344Ch)			FlexConnect State Indicator GPIO Configuration
Bit	**Name**	**R/W**	**Description**
7	FLEX_OUT_EN	R/W	1 = Enables FlexConnect state indicator for Port 5 through GPIO. The specific GPIO is selected in bits [2:0] of this register. 0 = Disables FlexConnect state indicator for Port 5 through GPIO. All other bits in this register are ignored.
6	FLEX_OUT_ACTIVE_HIGH	R/W	1 = The selected GPIO is driven active-high while in FlexConnect state. Driven low otherwise. 0 = The selected GPIO is driven active-low while in FlexConnect state. Driven high otherwise.
5	FLEX_OUT_OD	R/W	1 = The selected GPIO is Open-drain Output mode. 0 = The selected GPIO is drive high/drive Low-Output mode.
4:3	Reserved	R	Reserved
2:0	FLEX_OUT_IO	R/W	This bit selects the GPIO to be used for the Physical Port 5 FlexConnect state indicator. 000 = PF6/GPIO70 001 = PF7/GPIO71 010 = PF14/GPIO78 011 = PF19/GPIO83 100 = PF26/GPIO90 101 = PF27/GPIO91 110 = PF28/GPIO92 111 = PF29/GPIO93

TABLE 43: PHYSICAL PORT 6 FLEXCONNECT STATE INDICATOR GPIO CONFIGURATION REGISTER

FLEX_OUT_PORT6 (BFD2_344Dh)			FlexConnect State Indicator GPIO Configuration
Bit	**Name**	**R/W**	**Description**
7	FLEX_OUT_EN	R/W	1 = Enables FlexConnect state indicator for Port 6 through GPIO. The specific GPIO is selected in bits [2:0] of this register. 0 = Disables FlexConnect state indicator for Port 6 through GPIO. All other bits in this register are ignored.
6	FLEX_OUT_ACTIVE_HIGH	R/W	1 = The selected GPIO is driven active-high while in FlexConnect state. Driven low otherwise. 0 = The selected GPIO is driven active-low while in FlexConnect state. Driven high otherwise.
5	FLEX_OUT_OD	R/W	1 = The selected GPIO is Open-drain Output mode. 0 = The selected GPIO is drive high/drive Low Output mode.
4:3	Reserved	R	Reserved

TABLE 43: PHYSICAL PORT 6 FLEXCONNECT STATE INDICATOR GPIO CONFIGURATION REGISTER (CONTINUED)

FLEX_OUT_PORT6 (BFD2_344Dh)			FlexConnect State Indicator GPIO Configuration
Bit	**Name**	**R/W**	**Description**
2:0	FLEX_OUT_IO	R/W	This bit selects the GPIO to be used for the Physical Port 6 FlexConnect state indicator. 000 = PF6/GPIO70 001 = PF7/GPIO71 010 = PF14/GPIO78 011 = PF19/GPIO83 100 = PF26/GPIO90 101 = PF27/GPIO91 110 = PF28/GPIO92 111 = PF29/GPIO93

7.4 FlexConnect Hub Attach Delay

Certain systems may require a specific amount of debounce or delay between when the hub is issued the FlexConnect command when it attempts to reattach in the Flexed state. This feature may also be useful during debugging or troubleshooting systems. See Table 44 and Table 45.

TABLE 44: FLEXCONNECT HUB ATTACH DELAY REGISTER

FLEX_ATTACH_DELAY (BFD2_3455h)			FlexConnect Hub Attach Delay Register
Bit	**Name**	**R/W**	**Description**
7:0	FLEX_ATTACH_DELAY	R/W	This field may be used to add a delay between the moment when the FlexConnect command is issued and the hub detaches, and when the hub flexes and reattaches (enables the D+ pull-up of the upstream port) in the Flexed state. This delay is in increments of 10 ms. For example, a value of two provides 20 ms of delay before the USB hub reattaches in the Flexed state after the FlexConnect command is received. The default setting is 0x00.

TABLE 45: FLEXCONNECT ROLE SWITCH DELAY REGISTER

ROLE_SWITCH_DELAY (BFD2_3456h)			FlexConnect Role Switch Delay Register
Bit	**Name**	**R/W**	**Description**
7:0	ROLE_SWITCH_DELAY	R/W	This field refers to the amount of 10 ms by which role switch will be delayed once SET_ROLE_SWITCH command is initiated. This might be required with specific USB hosts where a debounce time is required between USB device detach and subsequent attach. For example, a value of 2 in this register provides 20 ms delay before role switch. The default setting is 0x00.

APPENDIX A: REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS00004550A (05-23-22)	Initial release.	

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