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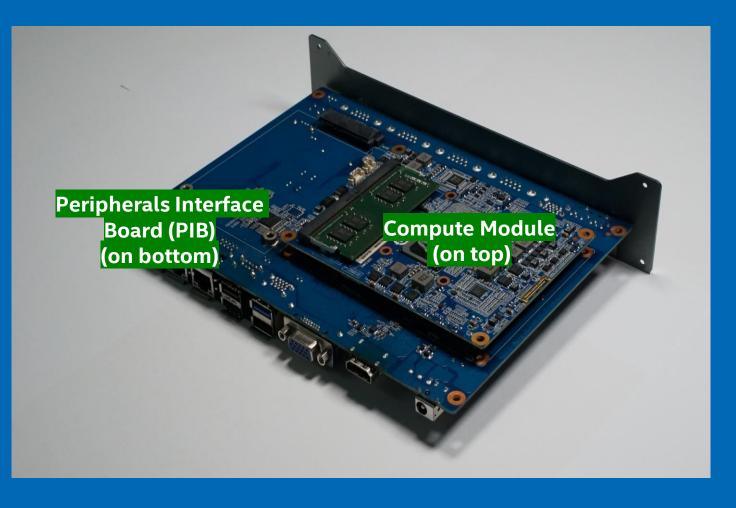
Agenda

- Intel Industrial Edge Module
- Peripherals interface board with FPGA
- Autonomous Mobile Robot application
 - Time synchronization



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Intel® Industrial Edge Module



Intel® Industrial Edge Module is a modular Hardware reference design based on Atom (Elkhart Lake) and Core (Whiskey Lake, Tiger Lake) platforms, optimized for Industrial applications such as control and vision.

Benefits:

- Modular Design: Cost & time saving on I/O customization, high-mix & low-volume SKUs
- Upgradable: Superior experience of newer CPU on legacy I/O
- Industrial Grade: Industrial I/Os, Industrial connectors & fanless robust design

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Peripherals Interface Board – Powered by FPGA

Cyclone VGT on board

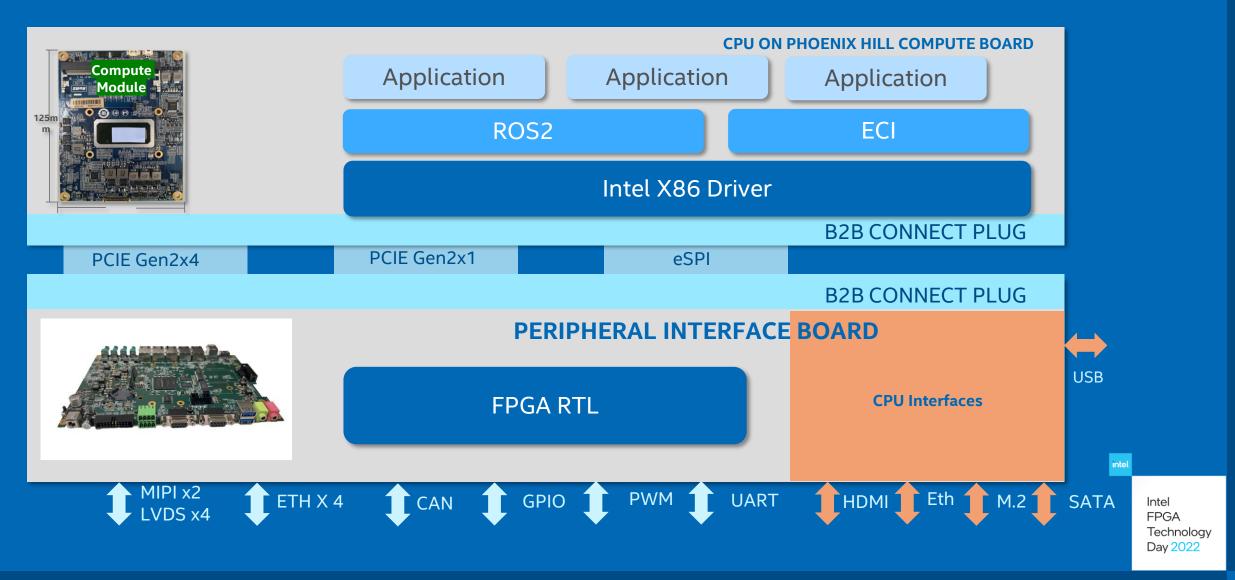


- Interface in Parallel
 - Senor Interfaces
 - Ethernet ports
 - Control Ports
- Deterministic Computation
 - PLC Control
 - Motion Control
- Workload offload
 - Imaging Signal Processing
 - Al inference



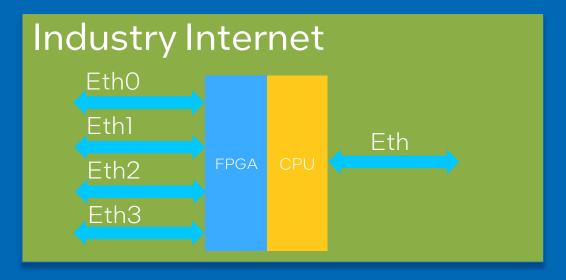


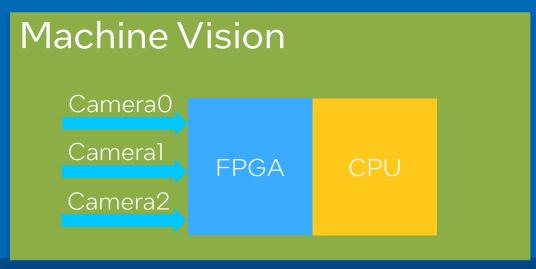
System Diagram

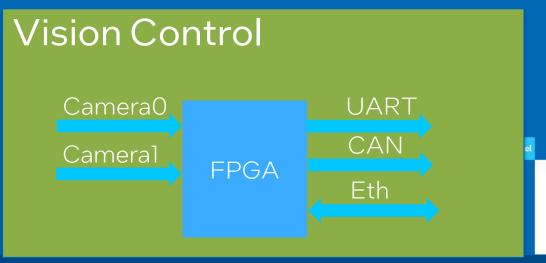


Target Area









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Sensor Fusion in AMR







Increased Demands

ncreased demands on AMR in various application scenarios



Complex Environment

ncreased complexity on the Moving environment



Multisensor Required

No single sensor could solve all the problems.

Requirement





Time Synchronization

- Need various sensors to assist on autonomous navigation accuracy and intelligent obstacle avoidance capability.
- Need time synchronization between sensor data to ensure the accuracy.

As-Is Solution

X86 CPU

- Connect to multi sensors and use soft time synchronization.
- × Number of sensor connected is limited.
- Cannot sure accurate time synchronization.
 MCU
- Connect to multi sensors
- X Cannot sure accurate time synchronization



——Our Proposed Solution



Extended Sensor Hub



Time Synchronization

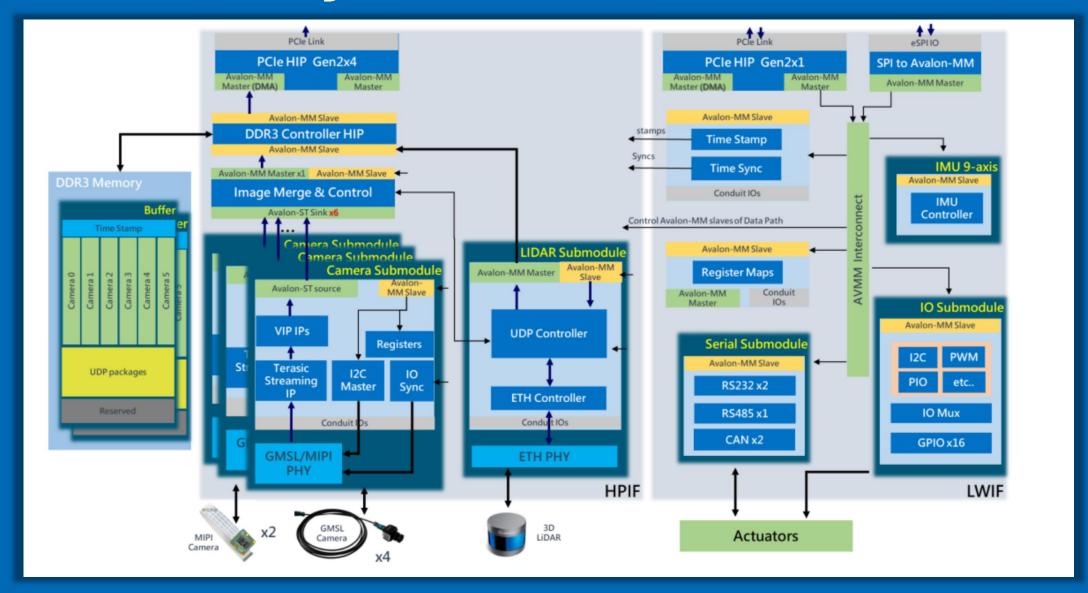
Trigger the sensor collection simultaneously to make sure the hard time synchronization between different sensors.



Image Preprocessing

Future use for image preprocessing, using ISP, before sending to CPU for further processing.

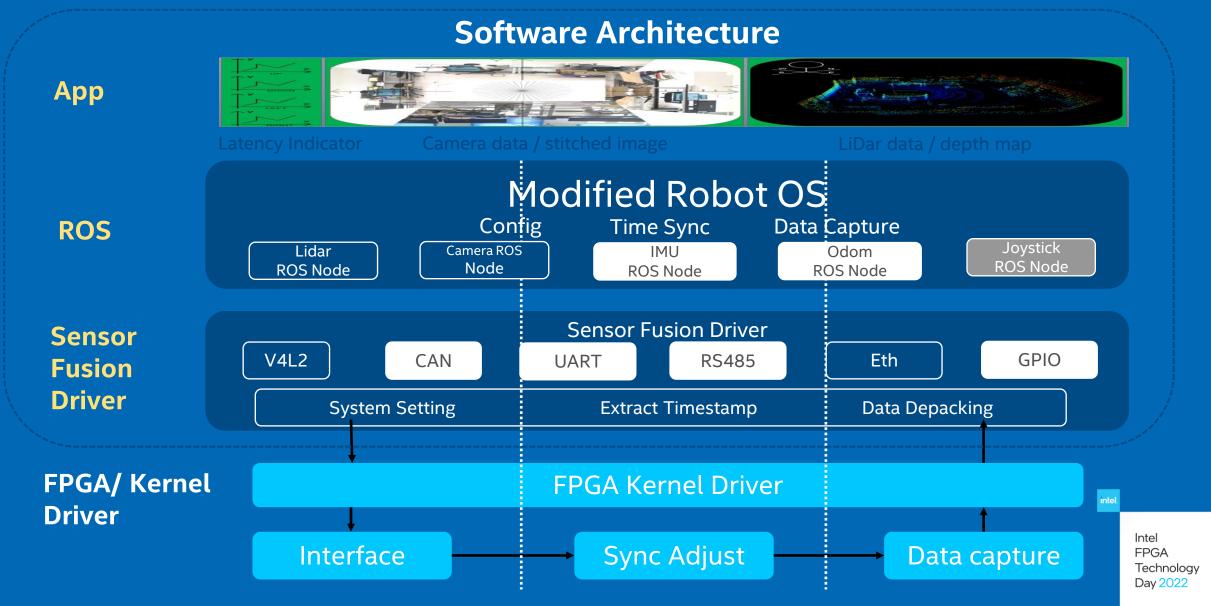
FPGA RTL Diagram



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Software Diagram



More are coming





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