

The above paper uses FPHA development version to implement the full homomorphic encryption processor. Craye Late is developed directly on a server with an FPGA? What are the terminal requirements?

The terminal requirements of FPGA are:

1. **Configurable logic block (CLB)** - An FPGA's essential component, allows it to support many hardware configurations since an FPGA is nothing more than a chip made up of CLBs.
2. **Digital signal processing slicing** - One of the specialized parts in an FPGA is known as a DSP slice, block, or cell. It is intended to do digital signal processing tasks far more effectively than if the same tasks were carried out using numerous CLBs, such as filtering or multiplying.
3. **Transceivers** - As they are designed to transmit and receive serial data (individual bits) to and from the FPGA at exceptionally rapid speeds, the name of this component is a mishmash of its capabilities. The configurable logic of the FPGA becomes more challenging to use as speeds increase, eventually reaching a speed cap, when converting information on the FPGA into serial data, as well as receiving serial data externally and converting it into useful information, while checking for errors in the data. With a specialized component readily available, users can easily implement high-speed data transfer without using up the FPGA's logic resources.
4. **Block Random Access Memory** - While there are other types of memory that can be found on an FPGA board, the specialized memory found on the actual chip is known as block RAM, or BRAM. Although each block has a fixed size (36K bits for Xilinx 7 series processors), these blocks can be separated or linked together to create BRAM in smaller or greater capacities. They can enable specialized functions like error correction and can operate in a range of operational conditions.
5. **Input/Output blocks** - They are the elements that allow data to enter and exit the FPGA. On the chip, input and output are handled by component groups called IO banks, which are made up of 50 distinct IO blocks. Depending on the kind of data the user anticipates sending or receiving, the IO blocks themselves can be configured in a variety of ways. These resemble transceivers but work more slowly and with greater functional flexibility. Even if the distance permitted it, transceivers have minimum operating speeds.