Design of 6-bit Fully Differential Current Steering DAC

A Report submitted in partial fulfillment of Mixed Signal Design (EC441) carried out at NITK Surathkal.

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Abstract:

The design and implementation of a 6-bit fully differential current-steering digital-to-analog converter (DAC) with stringent performance specifications is presented. The DAC is designed using a 180 nm CMOS process, targeting a full-scale output voltage range of 1.6 V (peak-to-peak) and operating within a 1.8 V supply voltage. The design aims to achieve an integral non-linearity (INL) and differential non-linearity (DNL) below 0.5 LSB while consuming less than 1 mW of static power. This report includes a step-by-step development process: starting with ideal current sources, integrating PMOS current sources with row-column decoding, and analyzing the effects of random mismatches in transistor widths. Simulations validate the design through transfer characteristics, INL, and DNL analysis.

Objective:

The objective of this project is to design, simulate, and analyze a 6-bit fully differential current-steering DAC that meets the following specifications:

- **Process**: 180 nm CMOS
- **Supply Voltage**: 1.8 V
- **Full-Scale Output Voltage**: 1.6 V (peak-to-peak)
- **INL/DNL**: < 0.5 LSB
- **Analog Input Range**: 0–1.6 V
- **Static Power Consumption**: < 1 mW

  => (1.8V)(63I)<(1 mW)

  => I<8.81 uA

The focus is on optimizing linearity and power efficiency and evaluating performance under random mismatches.

STEP 1: Design of 6-bit fully differential current steering DAC using Ideal Current Source.

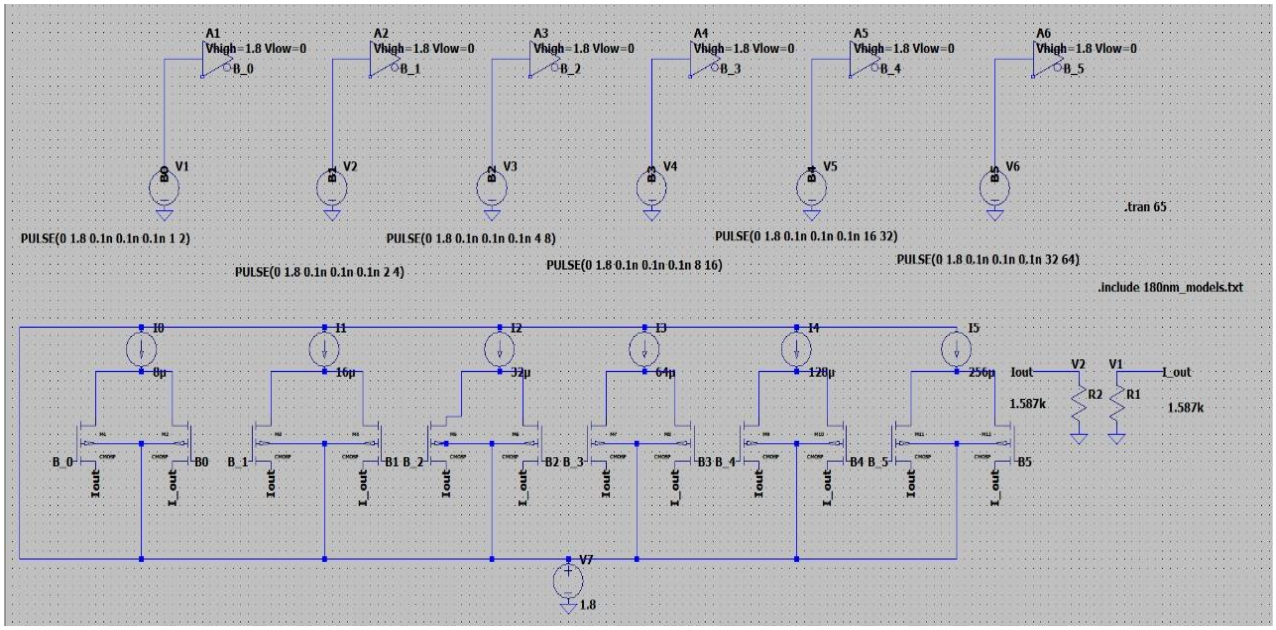

Fig.1.LTspice Schematic of 6-bit fully differential current steering DAC using Ideal Current Source.

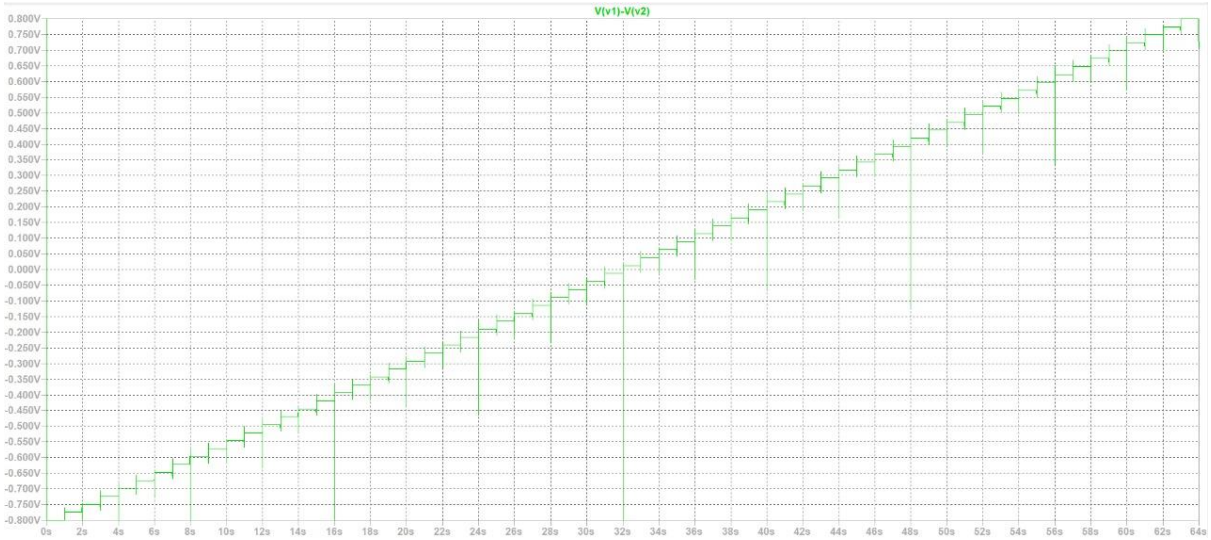

Fig.2. Differential Voltage Output waveform

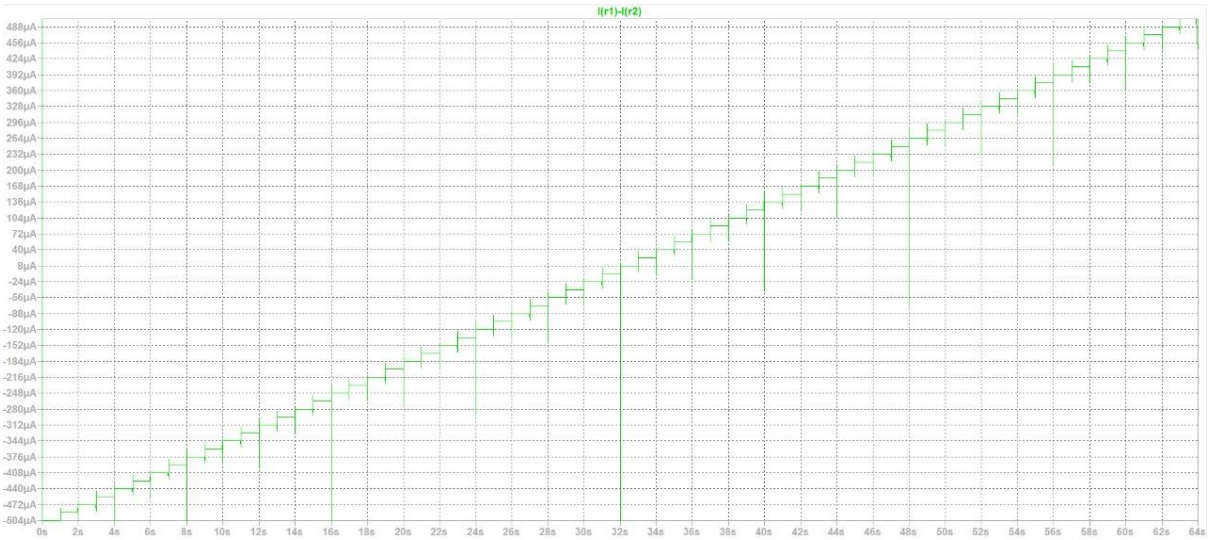

Fig.3.Differential Current output waveform

Explanation:

Fig.1 represents the schematic of a 6-bit binary weighted differential DAC using Ideal current and PMOS as switches. We chose 8,16,32,64,128,256 uA current sources because the value of I<8.81 uA was required due to static power constraints. The digital control signals (b0 to b5), generated by pulse sources, are used to drive the PMOS transistors, which steer the current from the current sources. This process facilitates the conversion of 6-bit digital input values into a corresponding analog output. The PMOS transistors are designed with a gate length of 180 nm and a gate width of 1 µm. The output current is subsequently transformed into a differential voltage using precisely matched resistors, each with a resistance value of 1.587 kΩ. The Transfer characteristics plots are shown in Fig.2 and Fig.3. for Voltage differential output and Current differential output, respectively.

STEP 2:

a)Design of 6 bit DAC using PMOS current sources along with the row-column decoder.

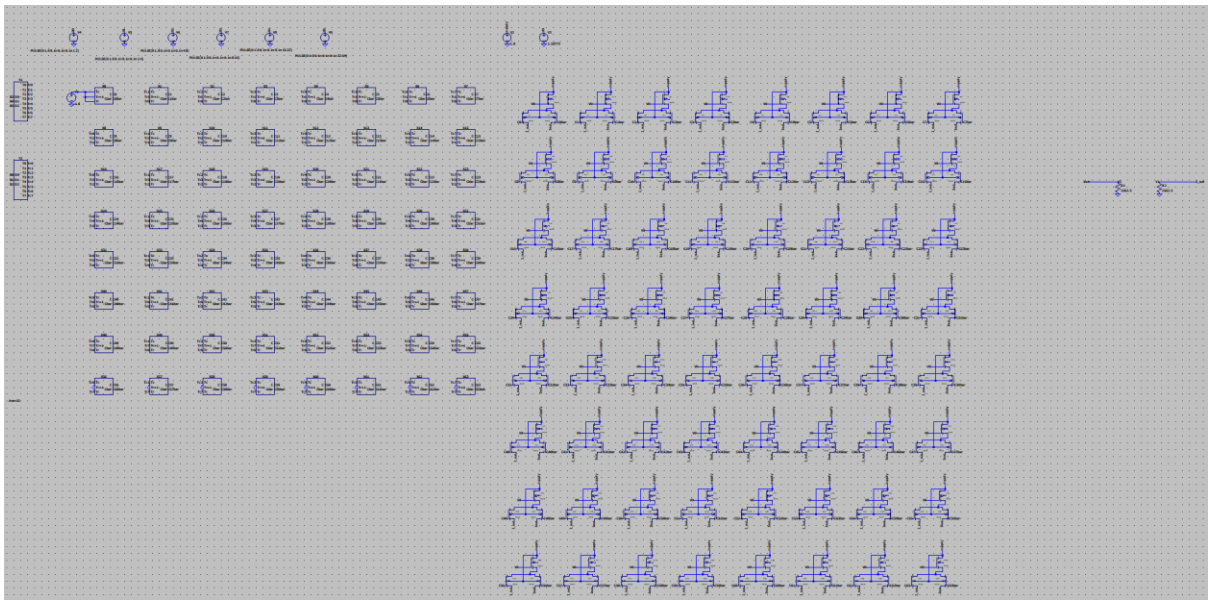

Fig.4.LTspice Schematic of 6-bit fully differential thermometer DAC using PMOS Current Source.

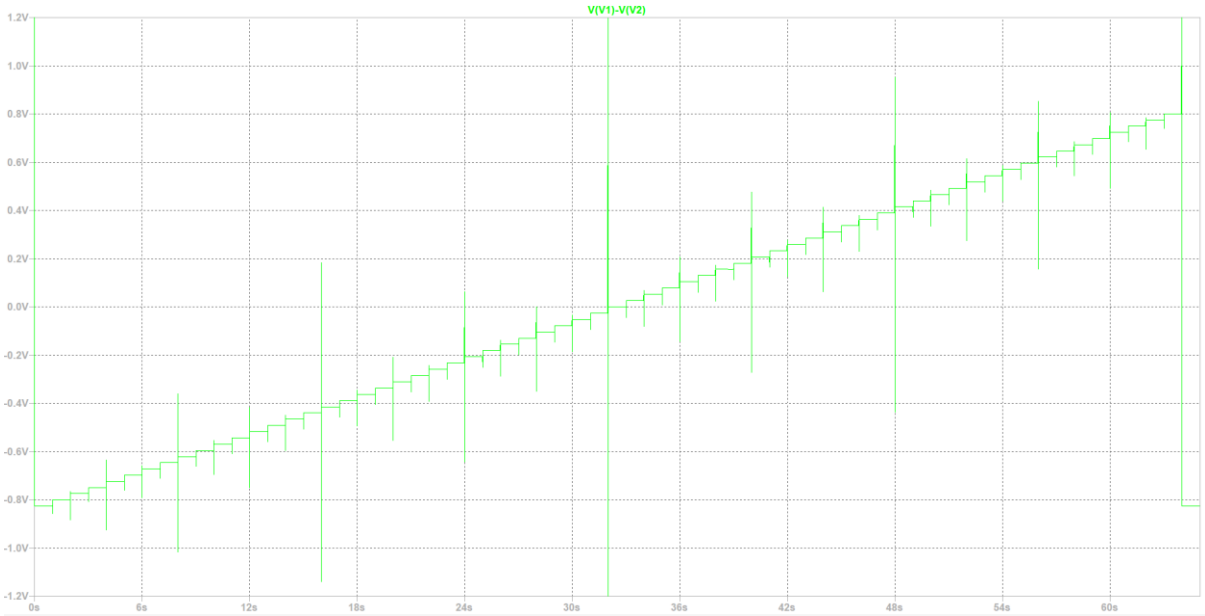

Fig.5 Differential Voltage Output waveform

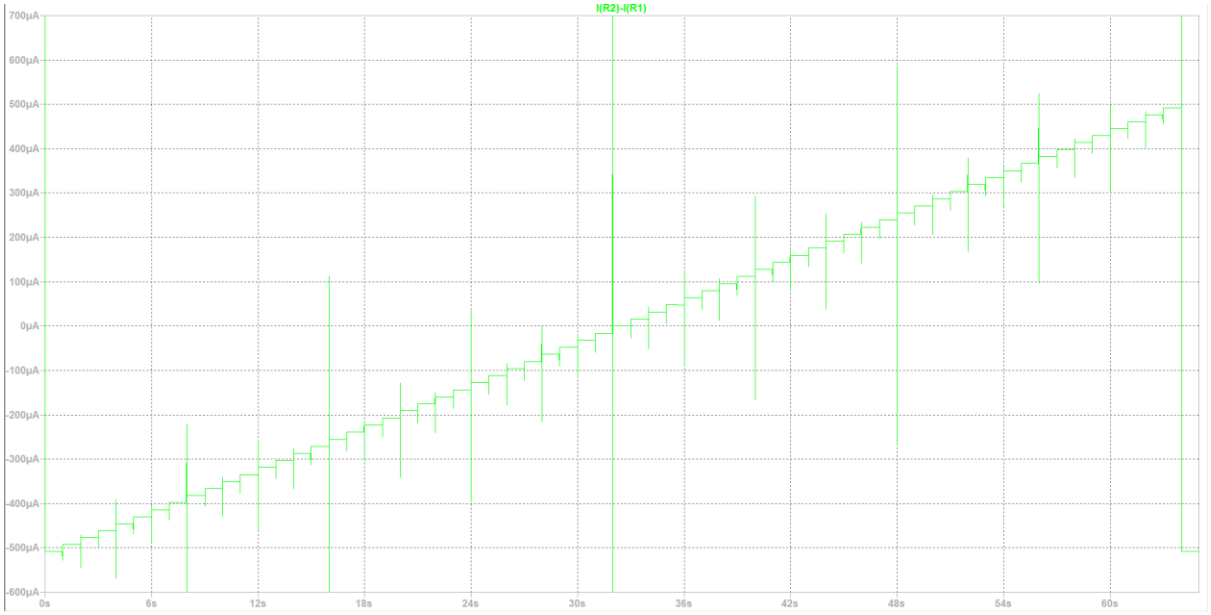

Fig.6 Differential Current output waveform

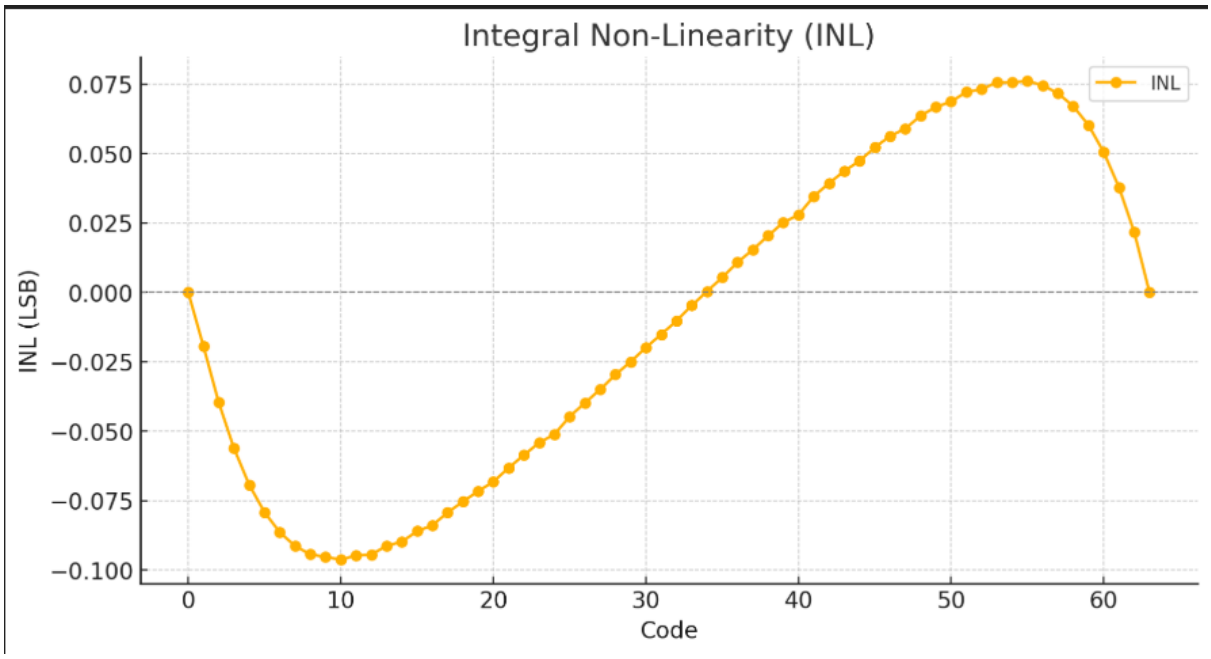

Fig.7 INL for point 0.1% random mismatch

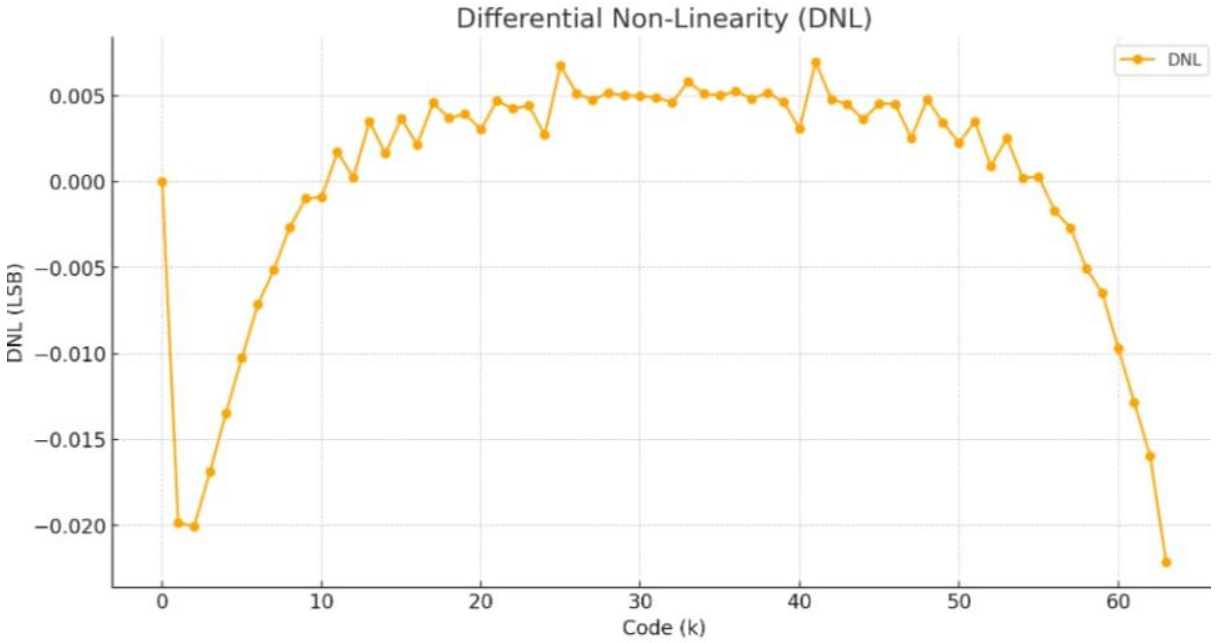

Fig.8 DNL for point 0.1% random mismatch

Explanation:

Fig.4 represents the schematic of a 6-bit thermometer differential DAC using current sources(made using pmos) and PMOS as switches. We chose 8 uA current sources because the value of I<8.81 uA was required due to static power constraints. The digital control signals (b0 to b5), generated by pulse sources, are used to drive the PMOS transistors, which steer the current from the current sources. This process facilitates the conversion of 6-bit digital input values into a corresponding analog output using a one-row decoder, a one-column decoder, and a local decoder corresponding to each cell. The PMOS transistors are designed with a gate length of 180 nm and a gate width of 1 µm. The output current is subsequently transformed into a differential voltage using precisely matched resistors, each with a resistance value of 1.6247 kΩ. The Transfer characteristics plots are shown in Fig.5 and Fig.6. for Voltage differential output and Current differential output, respectively. The INL and DNL of the output are shown in Fig. 7 and Fig. 8, respectively

b) Producing random mismatch in width of PMOS current sources with max deviation 0.1 percent.

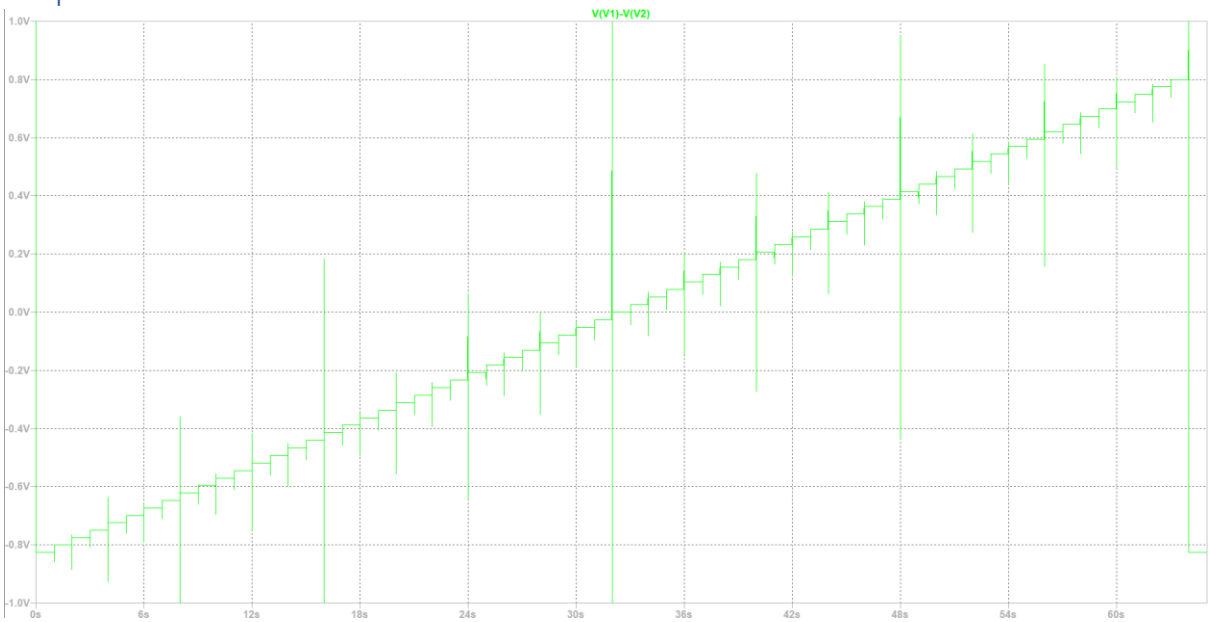

Fig.9 Differential Voltage Output waveform

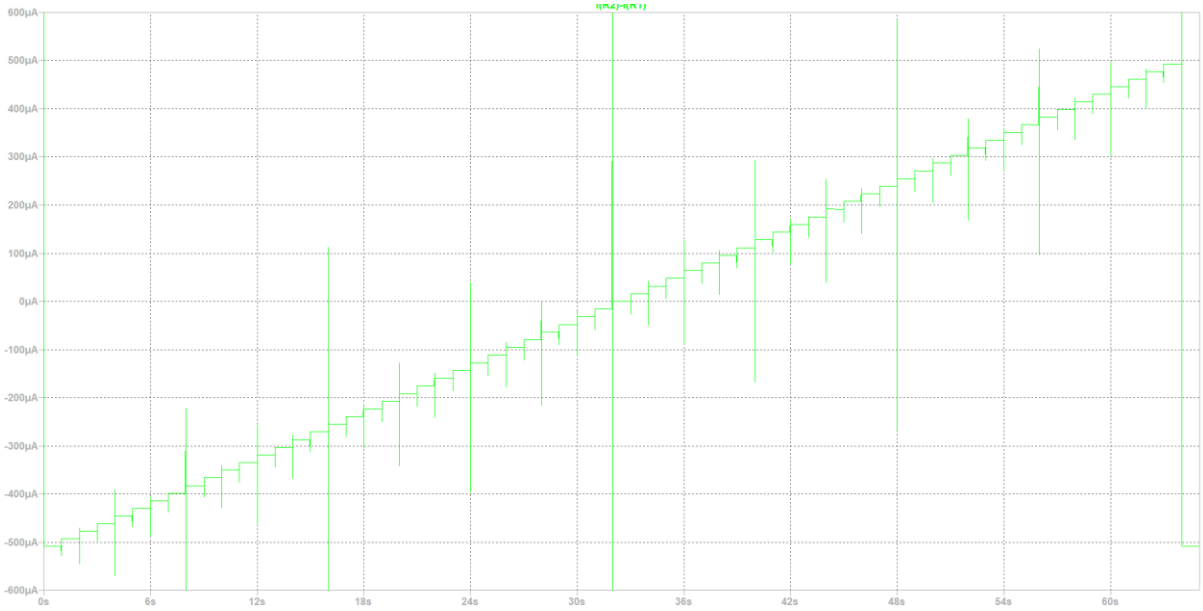

Fig.10 Differential Current output waveform

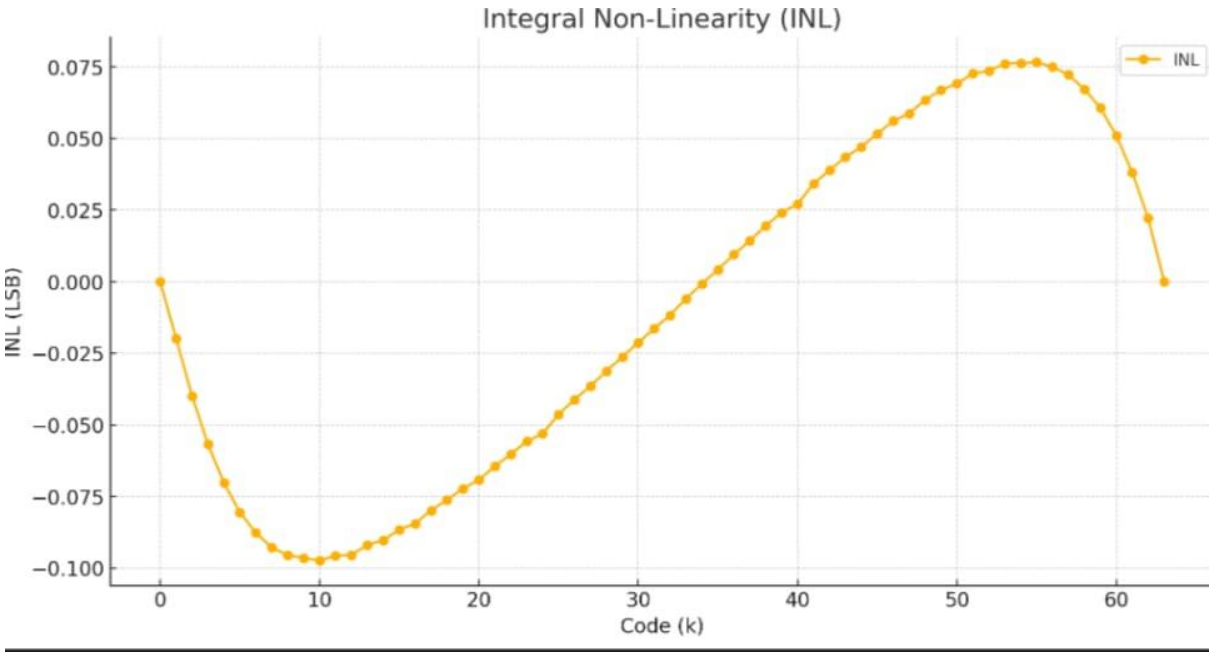

Fig.11 INL

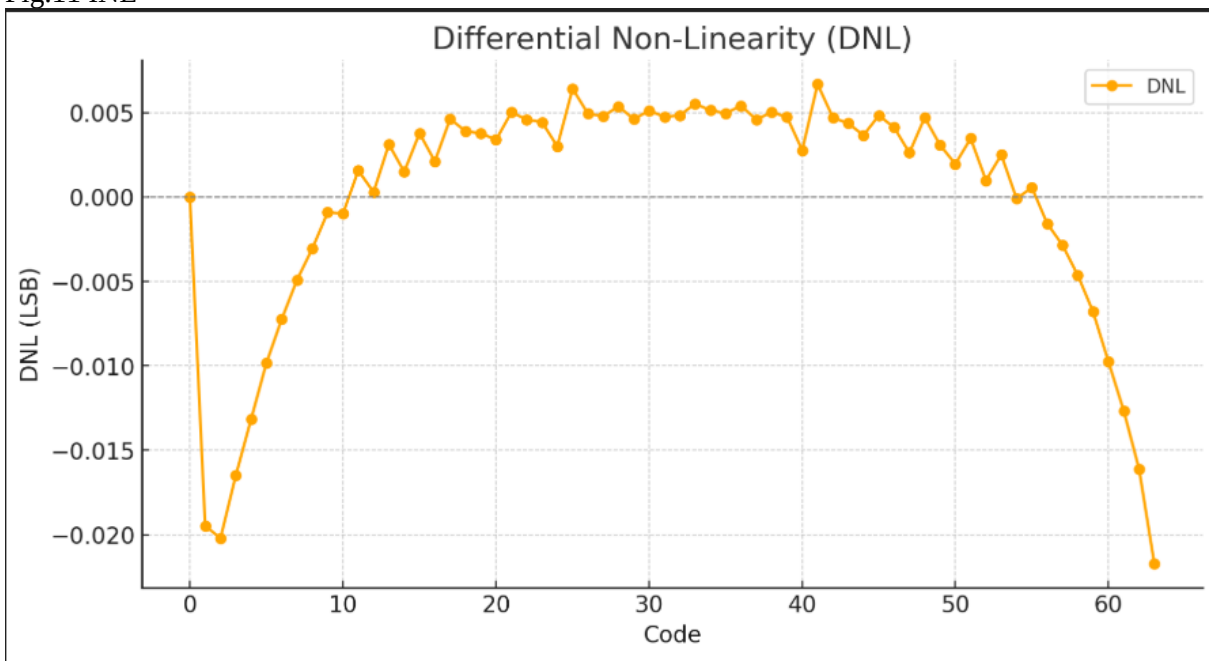

Fig.12 DNL

Explanation:

Fig.4 represents the schematic of a 6-bit thermometer differential DAC using current sources(made using pmos) with 0.1 percent random mismatch and PMOS as switches. We chose 8 uA current sources because the value of I<8.81 uA was required due to static power constraints. The digital control signals (b0 to b5), generated by pulse sources, are used to drive the PMOS transistors, which steer the current from the current sources. This process facilitates the conversion of 6-bit digital input values into a corresponding analog output using a one-row decoder, a one-column decoder, and a local decoder corresponding to each cell. The PMOS transistors are designed with a gate length of 180 nm and a gate width of 1 µm(with mismatches). The output current is subsequently transformed into a differential voltage using precisely matched resistors, each with a resistance value of 1.6247 kΩ. The Transfer characteristics plots are shown in Fig.9 and Fig.10. for Voltage differential output and Current differential output, respectively. The INL and DNL of the output are shown in Fig. 11 and Fig. 12, respectively.

c) Repeated (b) for maximum deviation of 1%

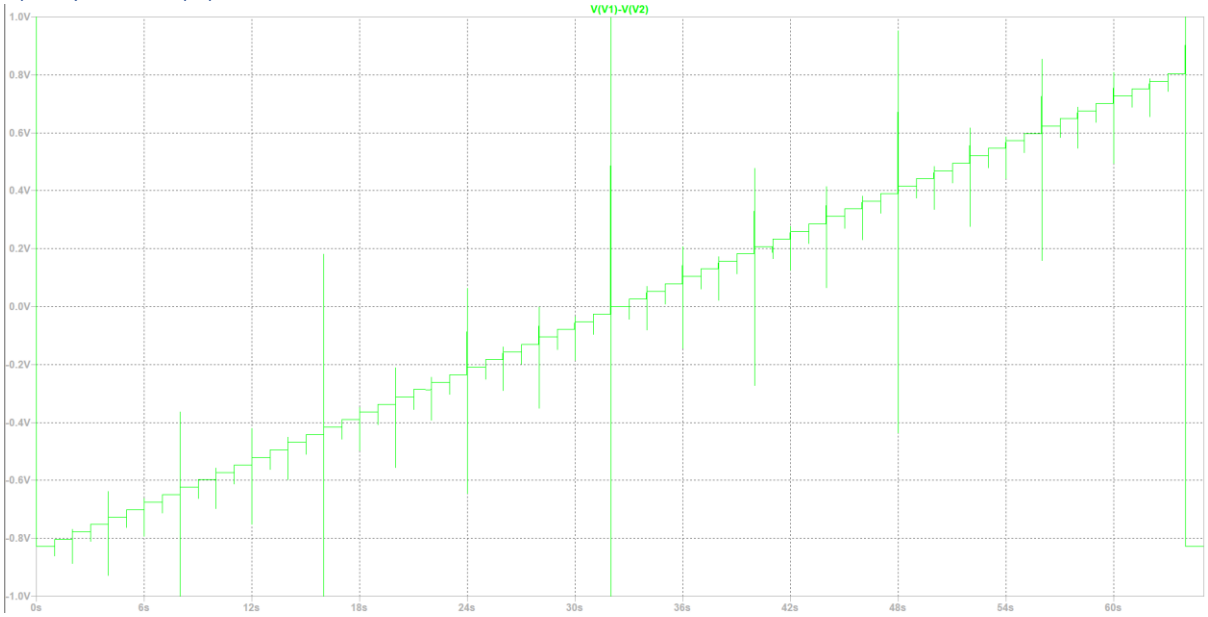

Fig.13 Differential Voltage Output waveform

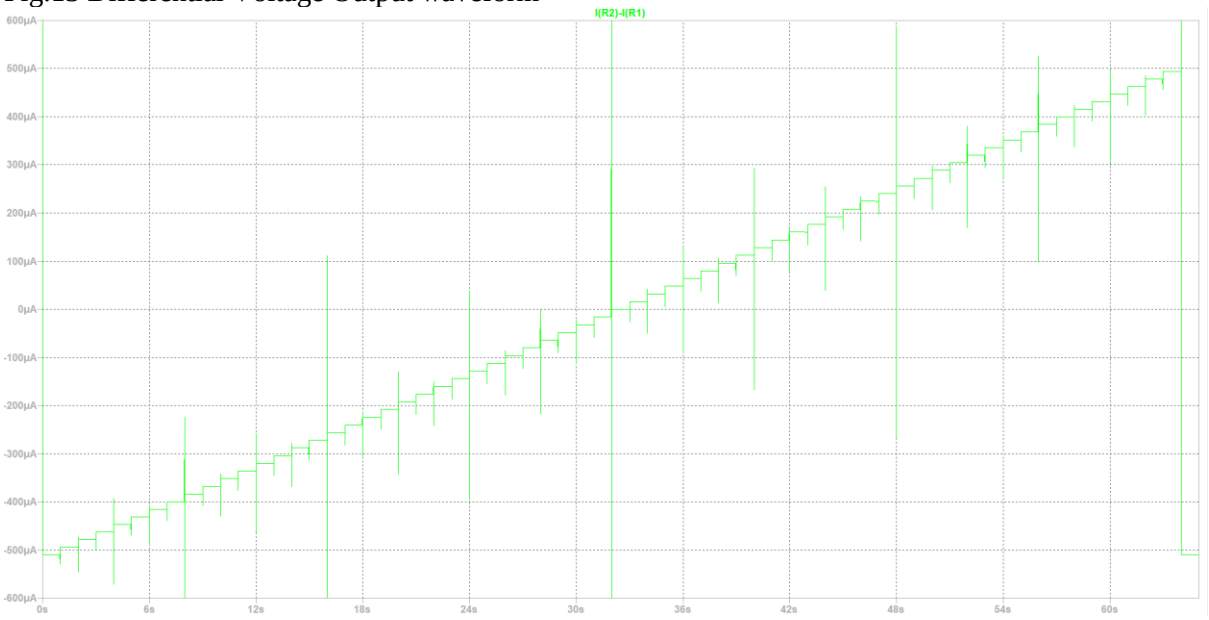

Fig.14 Differential Current output waveform

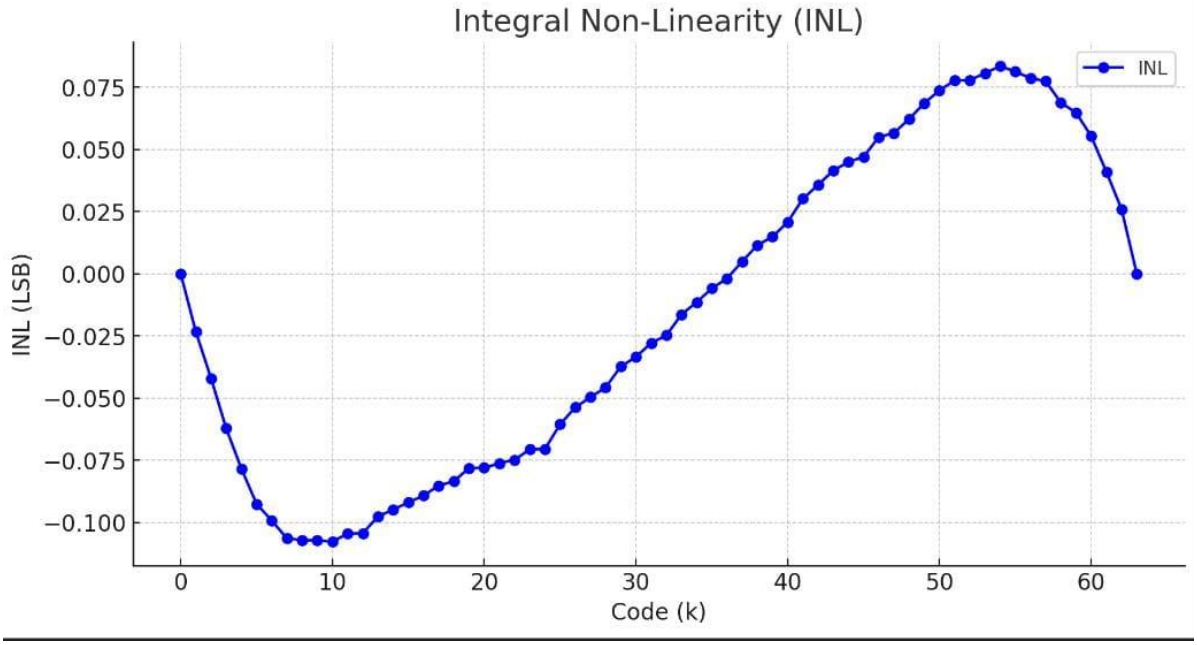

Fig.15 INL for point 1% random mismatch

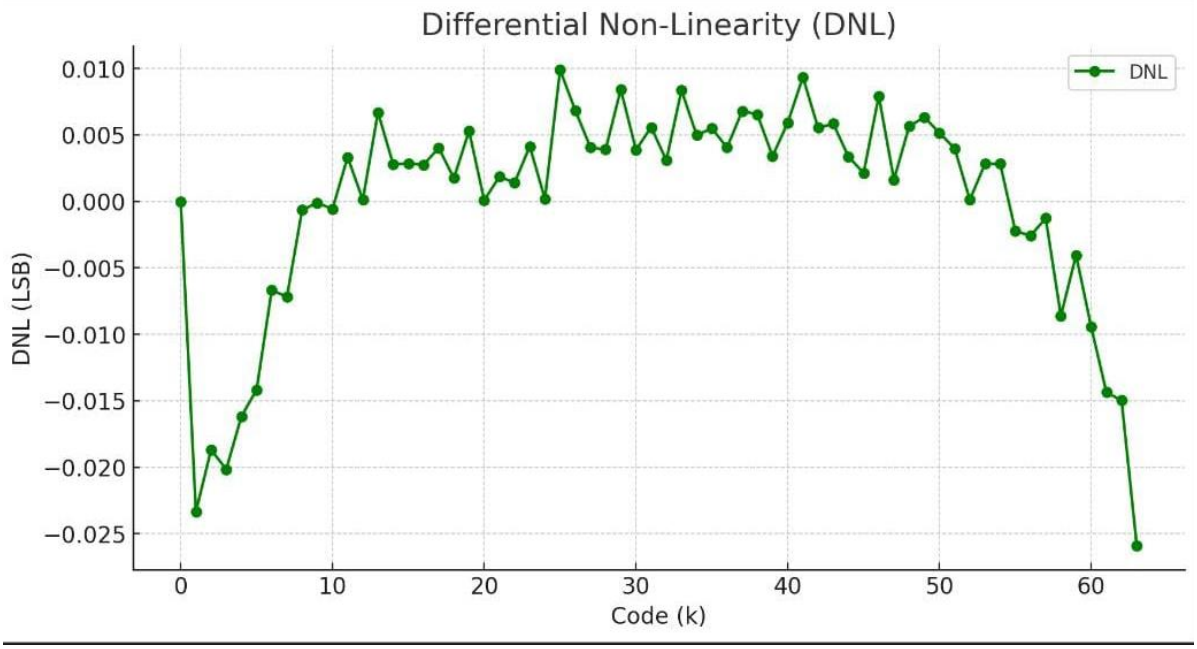

Fig.16 DNL for point 1% random mismatch

Explanation:

Fig.4 represents the schematic of a 6-bit thermometer differential DAC using current sources(made using pmos) with 1 percent random mismatch and PMOS as switches. We chose 8 uA current sources because the value of I<8.81 uA was required due to static power constraints. The digital control signals (b0 to b5), generated by pulse sources, are used to drive the PMOS transistors, which steer the current from the current sources. This process facilitates the conversion of 6-bit digital input values into a corresponding analog output using a one-row decoder, a one-column decoder, and a local decoder corresponding to each cell. The PMOS transistors are designed with a gate length of 180 nm and a gate width of 1 µm(with mismatches). The output current is subsequently transformed into a differential voltage using precisely matched resistors, each with a resistance value of 1.6247 kΩ. The Transfer characteristics plots are shown in Fig.13 and Fig.14. for Voltage differential output and Current differential output, respectively. The INL and DNL of the output are shown in Fig. 15 and Fig. 16, respectively.