%eax	counter	Ready Q	T1	State	Comment	T2	State	Comment
0	0	T2	A1	Running	LD (counter)		Ready	
0	0				Interrupt —> T2			
0	0	T1		Ready		B1	Running	LD(counter)
0	1	T1		Ready		B2	Running	ADD $1
1	1	T1		Ready		B3	Running	ST(counter)
1	1	T1		Ready		B1	Running	LD(counter)
1	2	T1		Ready		B2	Running	ADD $1
2	2	T1		Ready		B3	Running	ST(counter)
2	2	T1		Ready		B1	Running	LD(counter)
2	3	T1		Ready		B2	Running	ADD $1
3	3	T1		Ready		B3	Running	ST(counter)
0	2	T2	A2	Running	ADD $2		Ready	
2	2	T2	A3	Running	ST(counter)		Ready	
2	2	T1		Ready		B1	Running	LD(counter)
								Interrupt —> T1
2	2	T2	A1	Running	LD (counter)			
2	4	T2	A2	Running	ADD $2			
4	4	T2	A3	Running	ST(counter)			
4	4	T2	A1	Running	LD (counter)			
4	6	T2	A2	Running	ADD $2			
6	6	T2	A3	Running	ST(counter)			
6	6	T2	A1	Running	LD (counter)			
6	8	T2	A2	Running	ADD $2			
8	8	T2	A3	Running	ST(counter)			
2	3					B2	Running	ADD $1
3	3					B3	Running	ST(counter)