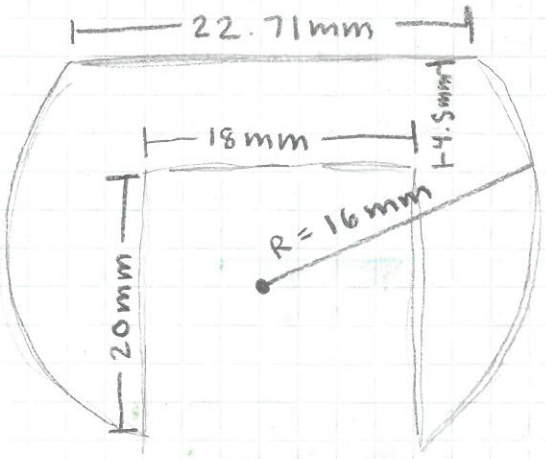
Cara Sears

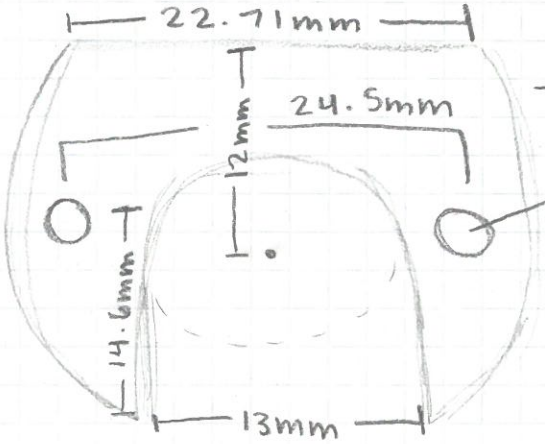
Nov 18/25

Sketch #1



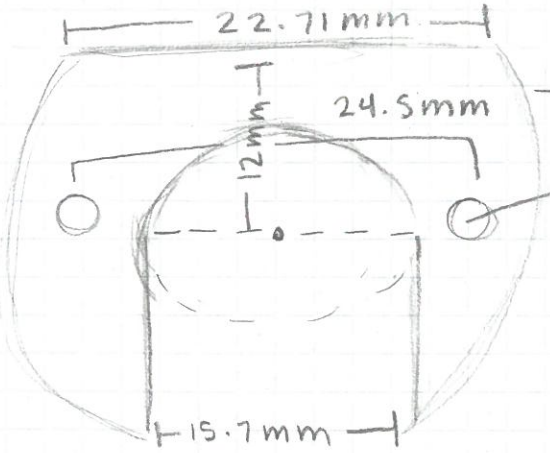
height = 40mm
position z = 0mm

Sketch #2a



height = 1.7mm
position z = -1.7mm

Sketch #3

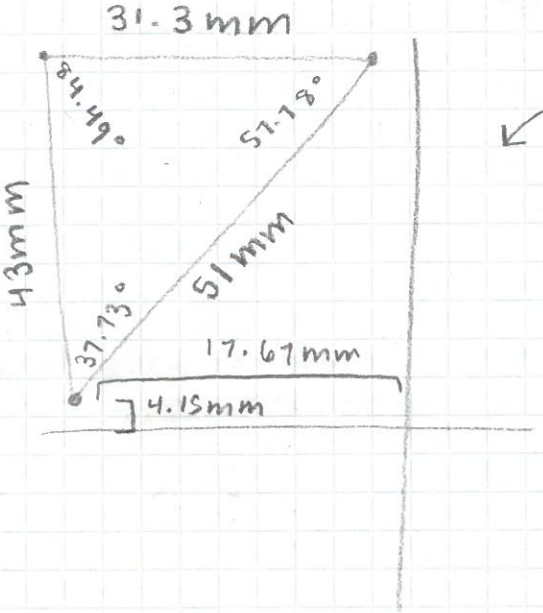


height = 1.7mm
position z = -3.5mm

★ repeat sketch 2a (name this 2b) where height = 1.7mm and position z = -5.2mm

and repeat sketch 2a again (name this 2c) where height = 4.8mm and position z = -10mm

After sketching and padding is complete, create a new sketch in the body 'Sketch #1'. Make this sketch a pocket to create the angled surface

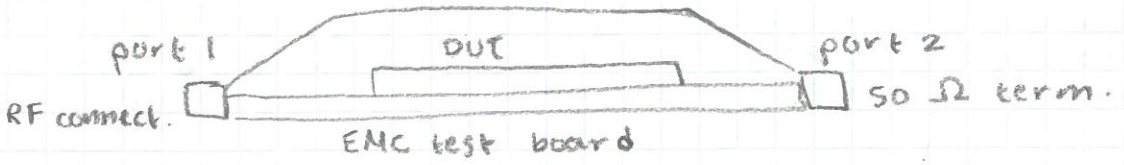


create sketch in zy plane with these dimensions

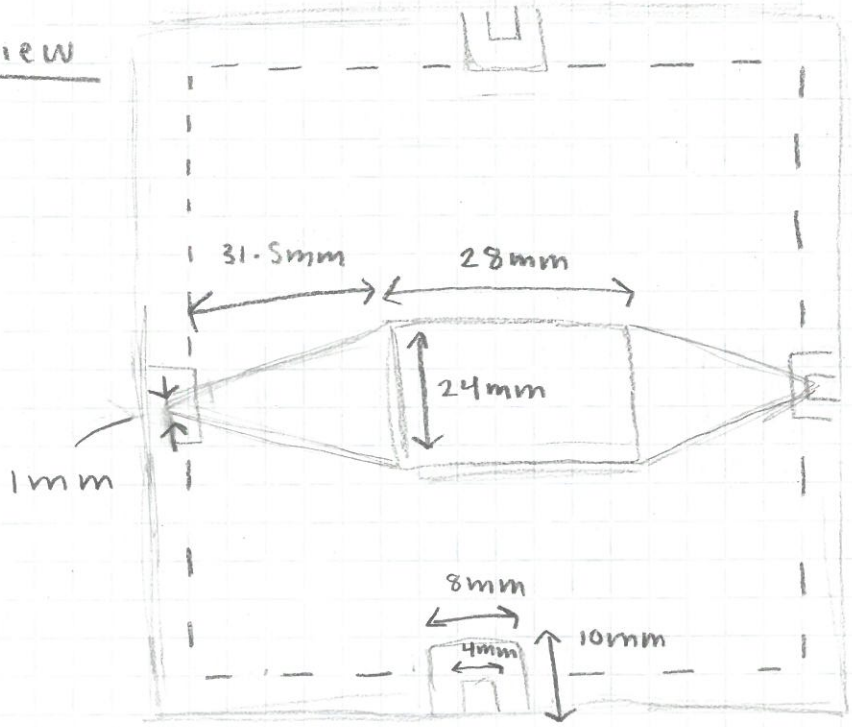
Finally, round all outward, forward facing edges by 1mm

IC - Stripline

side view



top view



Layers of test board

Layer	Descript.	Material	Thickness
1	signal	copper	0.071 mm
		prepreg	0.152 mm
2	gnd	copper	0.035 mm
		prepreg	1.028 mm
3	Vcc	copper	0.035mm
		prepreg	0.152 mm
4	signal	copper	0.071mm

Specifications

Frequency range - 150kHz to 3 GHz
VSWR - < 1.25
Stripline height - the height of the DUT must be less than 50% of the conductors height
Stripline width - the width of the device under test must be less than 110% of the conductor width