Portable NMR Spectroscopy with Direct Sampling

Interim Report

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1. Introduction

Nuclear Magnetic Resonance (NMR) Spectroscopy is a chemical analysis tool that is used ubiquitously in many fields such as chemistry, biomedicine [1], and food safety [2]. Despite its utility, traditional NMR machines are bulky and require high maintenance which limits its use to large facilities [3]. Hence there has been an emerging body of work related to the study of portable NMR spectrometers for use in cases such as in-vivo biomedical studies [4] or on-field autonomous monitoring systems [5].

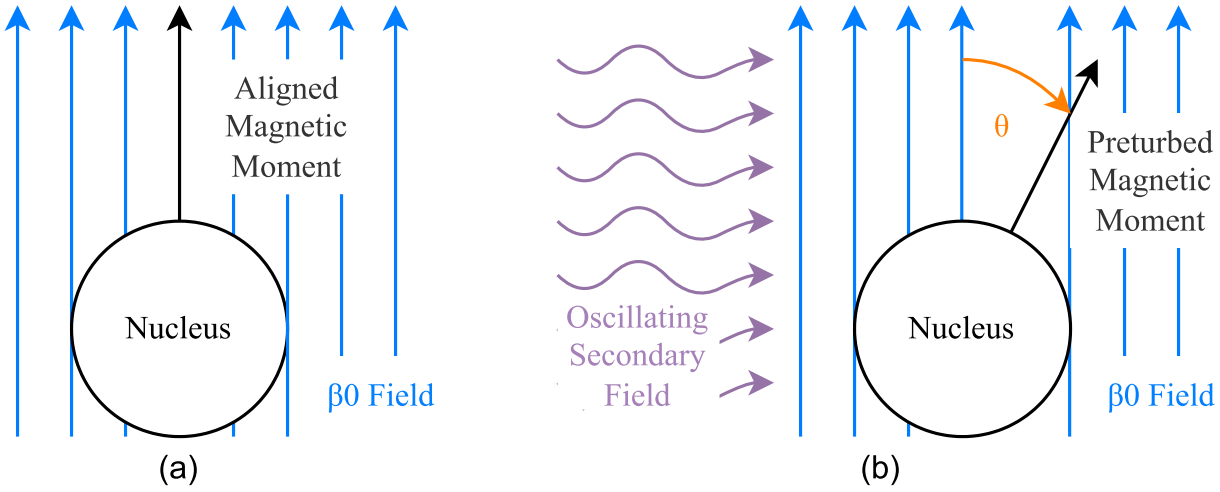


Figure 1. (a): Nucleus under a β_0 field. Magnetic moment is aligned with β_0 field. (b): Nucleus influenced by β_0 and a second field. Magnetic moment is perturbed from the β_0 by θ [6].

NMR spectroscopy is performed by first applying a strong static magnetic field β_0 to a given sample. This field aligns the spin of nuclei as shown in Figure 1a such that their magnetic moments are orientated parallel to the applied field. Then, as shown in Figure 1b, a secondary oscillating field is established perpendicularly to β_0 that perturb the magnetic moment away from β_0, increasing the potential energy of the nuclei. When this secondary field is removed, the nuclei undergo a 'relaxation' in which it realigns with β_0 and releases the potential energy as a signal according to the relation:

$$|E| = hf = \mu\beta_0 Cos(\theta) \qquad (1)$$

E: energy released, h: Plank's constant, f: frequency of released signal, μ: magnetic moment, θ: angle of perturbation [6].

This released NMR signal is highly characteristic and can be used to determine the nature of the bonds that exist in the sample. In a frequency spectrogram, they appear as 'peaks' that are 'shifted' from the spectrometer's Larmor frequency f_L, a reference frequency that is a function of the strength of β_0 and the geomagnetic ratio of the nucleus. These shifts are referred to as 'chemical shifts' and are commonly represented in units of parts-per-million (ppm) [6].

The relationship between f_L, β_0, and chemical shift constrains existing NMR designs. Using a stronger β_0 magnetic field leads to larger shifts in the NMR frequency as described by the relation in Equation (1), allowing for a more detailed distinction of molecules as the peaks will have more distance from each other in the frequency domain. However, it equally increases f_L, increasing demands on the receiver to process high-frequency signals.

Existing portable systems thereby compromise by sacrificing accuracy of analysis. They can use a weaker β_0 to capture the signal at a lower f_L and sacrificing detail in the frequency domain, or more commonly, increase the complexity of the Receiver (Rx) using methods such as I-Q demodulation to allow sampling of the signal at lower frequencies. But increasing Rx complexity will inevitably introduce noise and distortion that would limit the accuracy of the analysis.

This project proposes to gain the benefits from both a stronger β_0 as well as a simplified Rx by leveraging advances in modern high frequency analog-to-digital converters (ADC). The goal of such a system would be to maximize resolution in the frequency spectrum, using powerful β_0 fields to get a high frequency resolution, and maintaining the integrity of the signal through direct sampling of the high frequency NMR signal, minimizing the introduction of noise and distortion from alternative complex analog processing techniques. The signal will then be analyzed in the digital domain with a deep Fast Fourier Transform (FFT) for a high-resolution analysis of the sample range of hundreds of ppm or better (e.g., 10-15ppm).

2. Background and Motivation

Existing portable NMR Systems [3] [5] [7] [8] all broadly share four defined components: Tx – Transmitter of the oscillating field, Rx – Receiver that captures the signal, a timing controller for synchronizing the Rx and Tx, and a form of digital signal processing (DSP) unit responsible for data analysis. For this proposal, the focus is on the Rx and the digital DSP.

D.Ha et.al. [3] is a significant paper in the scalable NMR body of work with over 80 citations. They aimed to create a scalable NMR system on a single Integrated Chip (IC). They utilized a field with β_0 = 0.51T and the corresponding f_L = 21.8MHz. The receiver consists of a low noise amplifier (LNA) followed by an I-Q demodulator (IQD), which allowed them to use a low frequency 14-bit 20kHz ADC. As their work's focus was mainly concerned with the transceiver and pulse sequencer, the ADC was not present on the IC but was connected externally.

D.Ariando et.al. [5] is the only existing implementation that did not utilize an I-Q demodulation technique for the analog receiver. They have utilized a common-gate low noise preamplifier followed by a second stage 4th order tunable gain amplifier. A common-gate band pass preamplifier was opted as the first stage over a narrow band pass filter (NBPF) for simplicity, as they found in their previous work that the NBPF was difficult to tune in practice. Both the center frequency and the gain of this receiver can be controlled by the FPGA with the gain having a range of 40-66dB. After the two-stage pre-amplifier the signal is directly sampled via 14-bit 25MHz ADC (LTC1746 Analog Devices). This was possible as this system has a relatively weak β_0 of only 0.101T and hence an f_L of 3 to 5MHz. As a result, the ADC was able to satisfy the Nyquist criteria. Finally, in terms of the digital processing, Ariando et.al. utilizes an Intel Cyclone V FPGA programmed via HDL for control of the analog components such as the receiver and the transmitter. It has the capability to temporarily store 1.28s of the measured data at 25MHz but does not process the data on the FPGA. Instead, it then transfers the data to a dual-core ARM Cortex-A9 running Ubuntu which performs digital post-processing via high level languages like python.

H.Burkle et.al. [7] focused on attempting to increase the voltage compliance of the NMR coil such that it can be enlarged to accommodate larger samples with the goal of benefiting from the improved concentration and volume of the sample. The IC design focused mostly on the high-voltage transmitter and thereby does not have an ADC included in the IC. The receiver is composed of an LNA, followed by an IQD. It has a significantly larger β_0 of 1.1T with f_L of 48MHz.

S.Hong et.al. [8] in their paper aimed to target the problems with timing issues occurring between Tx and Rx, their synchronization and Rx settling times. Their β_0 and f_L was similar to that of [3] at 0.5T and 21.07MHz respectively. The receiver consisted of a LNA, followed by an IQ demodulator, a second order low pass filter (LPF) tunable to 150-650kHz, then a variable gain

amplifier (VGA) tunable to 0-60dB. The ADC utilized is a 11-bit 2MHz ADC communicating with an FPGA.

Table 1: State-of-Art comparison of NMR receiver systems and the proposed system

Reference	**[3]**	**[5]**	**[7]**	**[8]**	**Proposed System**
Published Year	2014	2018	2021	2021	-
β_0	0.5T	0.101T	1.1T	0.5T	-
f_L	21.8MHz	3-5MHz	48MHz	21.07MHz	500MHz
Receiver Type	I-Q demodulation	Direct sampling	I-Q demodulation	I-Q demodulation	Direct sampling
Receiver Config	LNA→IPQ	LNA→Gain Amp	LNF → IQD	IQD→LPF→VGA	NBPF → Gain Amp
ADC Type	• 14-bit 20kHz • LT1407A	• 14-bit 25MHz • LTC1746 Analog Devices	-	• 11-bit 2MHz	• 12-bit 4GHz • Included on Xilinx FPGA
Digital Hardware	-	• Intel Cyclone V FPGA for analog control and measurement • Storage of 1.28s of data at 25MHz • ARM Cortex-A9 for higher level post-processing	-	Digilent FPGA	Xilinx RFSoC 2x2 FPGA Board [9]

Table 1 summarizes the state-of-art systems under study. None of the state-of-art portable NMR systems operate at f_L close to this thesis's target of 500MHz. D.Ariando et.al [5] reports the only system which has utilized direct sampling to simplify Rx, but the target f_L is a very low 3-5MHz making it only fit for macro level analysis. All other examined systems target f_L=20-50MHz and use IQ Demodulation to reduce the sampling frequency significantly.

In contrast, this paper's proposed system will utilize modern 12bit 4GHz ADCs on the Xilinx RFSoC 2x2 FPGA [9] which exceeds the Nyquist criteria for the target f_L of 500MHz by 4x. To avoid intermodulation and distortion that can occur when transmitting high frequency signals, a

pre-ADC Filter is proposed as the analog front-end between the NMR Rx Coil and the ADCs of the FPGA as seen in Figure 2.

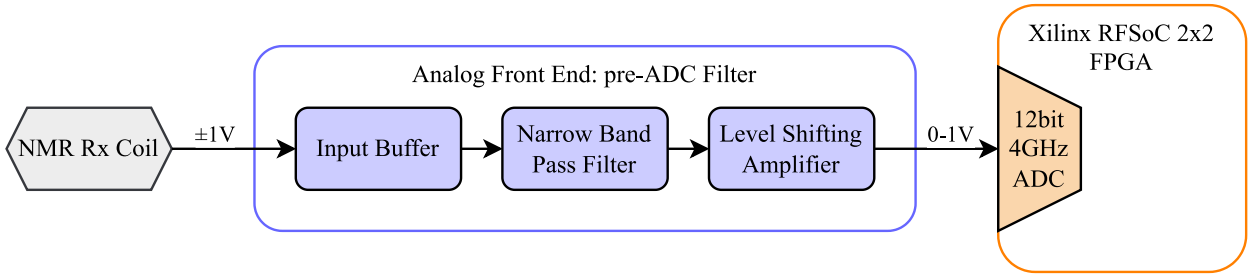


Figure 2: Block diagram of proposed system. Front end provides band-passing and ADC input voltage matching.

This front-end's goal would be to provide a simple layer of band-pass filtering to attenuate from irrelevant frequencies to reduce intermodulation, in addition to providing gain and adjusting the DC level of the signal to match the input voltages of the Xilinx RFSoC 2x2 Board.

3. Analog Front End Design

3a. Input Buffer

To protect the integrity of the output of the NMR coil, an input buffer is required as the first stage of the analog front-end. Without this buffer, the coil would effectively become a part of the front-end circuit, and its output behavior may distort significantly due to interactions with other components of the circuit. Hence, a common method of preserving the output of the coil is by a buffer like a unity gain amplifier.

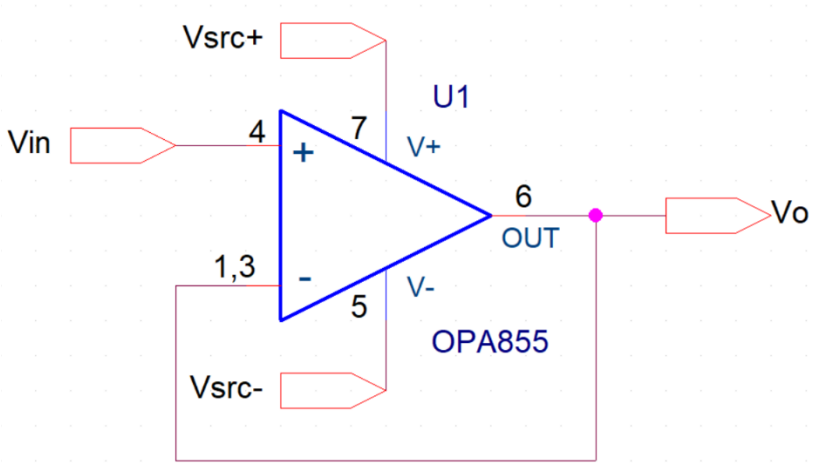


Figure 3: Circuit diagram of the unity gain amplifier.

The output of this amplifier follows the input while providing a very high impedance to the NMR coils, conveying the signal while isolating the coil from the rest of the circuit. This will ensure that later stages of the front-end does not overload the signal from the NMR coil.

The Texas Instruments OPA855 transimpedance amplifier [10] was chosen for all stages of this front-end. With an 8 GHz gain bandwidth (GBW) product, which is 16x greater than the target f_L=500MHz, it sufficient to meet the requirements of this research.

3b. NBPF Filter

One of the key considerations in designing a band pass filter is the Q factor that describes how narrow the bandwidth is where higher numbers indicate a narrower width. To completely reduce noise outside of the desired range, a greedy solution to this problem would be to design a very narrow band to completely attenuate any irrelevant frequencies. For the target range of 10-15ppm with f_L of 500MHz, the Q factor of the filter, which describes how narrow the bandwidth is, would need to be extremely high:

$$15\ ppm = \frac{\Delta f}{f_L} * 10^6 \rightarrow \Delta f = 7.5kHz \quad (2)$$

$$Q = \frac{f_c}{BW} = \frac{500MHz}{2*7.5kHz} = 33.3k \quad (3)$$

Where Δf is the shift in frequency from f_L at a given ppm, f_c and BW is the desired center frequency and bandwidth of the desired band pass filter respectively.

This greedy approach is unrealistic in implementation, involving NBPF of extremely high orders which would introduce significant complexity to the circuit. Hence, a heuristic approach was taken. The pre-ADC filter would aim for a much lower and realistic Q factor, not aiming to eliminate all noise outside of relevant frequencies but aiming to reduce intermodulation and distortion from the non-relevant components into the ADC. The required narrower band widths will then be processed in the digital domain, leveraging the direct-sample approach of this thesis.

A Deliyannis Filter (DF) was ultimately chosen as the NBPF of choice due to the ease of its implementation with only resistive and capacitive elements that are less sensitive in high-frequency environments compared to LC circuits. Its downside is the relatively low Q factor, which would have to be compensated by increasing the order of the filter.

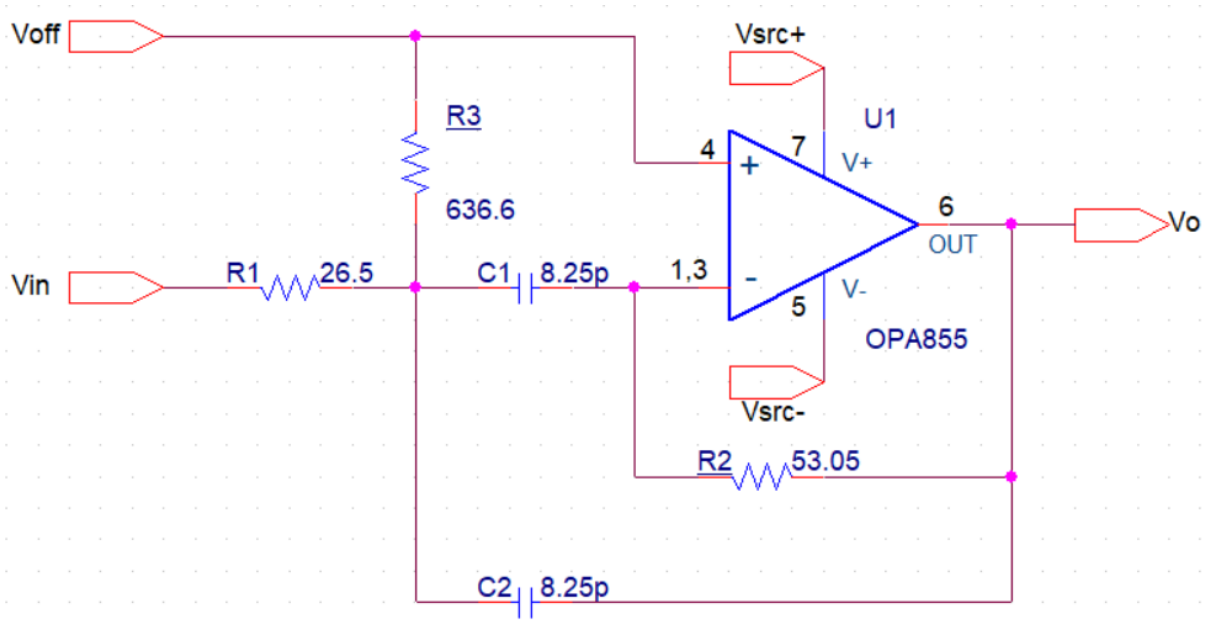


Figure 4: Circuit diagram of the Deliyannis filter.

The equations for the Deliyannis Filters were taken from [11]:

$$R_1 = \frac{Q}{G*2\pi f*C}, R_2 = \frac{Q}{(2Q^2-G)*2\pi f*C}, R_3 = \frac{Q}{\pi f*C} \quad (4)$$

The following target parameters were used to obtain initial values for the components: Q = 3, f_c = 500MHz, $C = 3pF$, gain (G) = 12. There was a significant iterative process involved in the computation of these values. The equations are empirical and may not accurately model the filters at high frequencies and with the chosen high-frequency OPA855 op-amps. Hence, C had to be chosen through simulations as 8.25pF to attain the desired f_c.

Due to inaccuracy, the simulated Q and G values were 0.71 and 0.46dB respectively despite the target Q and G above as shown in Figure 5. The simulated f_c was 517.6MHz.

To compensate for the low-Q, the filters were the repeated 3 times as to increase Q to1.53 and G to 2.02dB, with f_c=511.7MHz as shown in Figure 6. Further orders of the filter were not added to reduce complexity in the system.

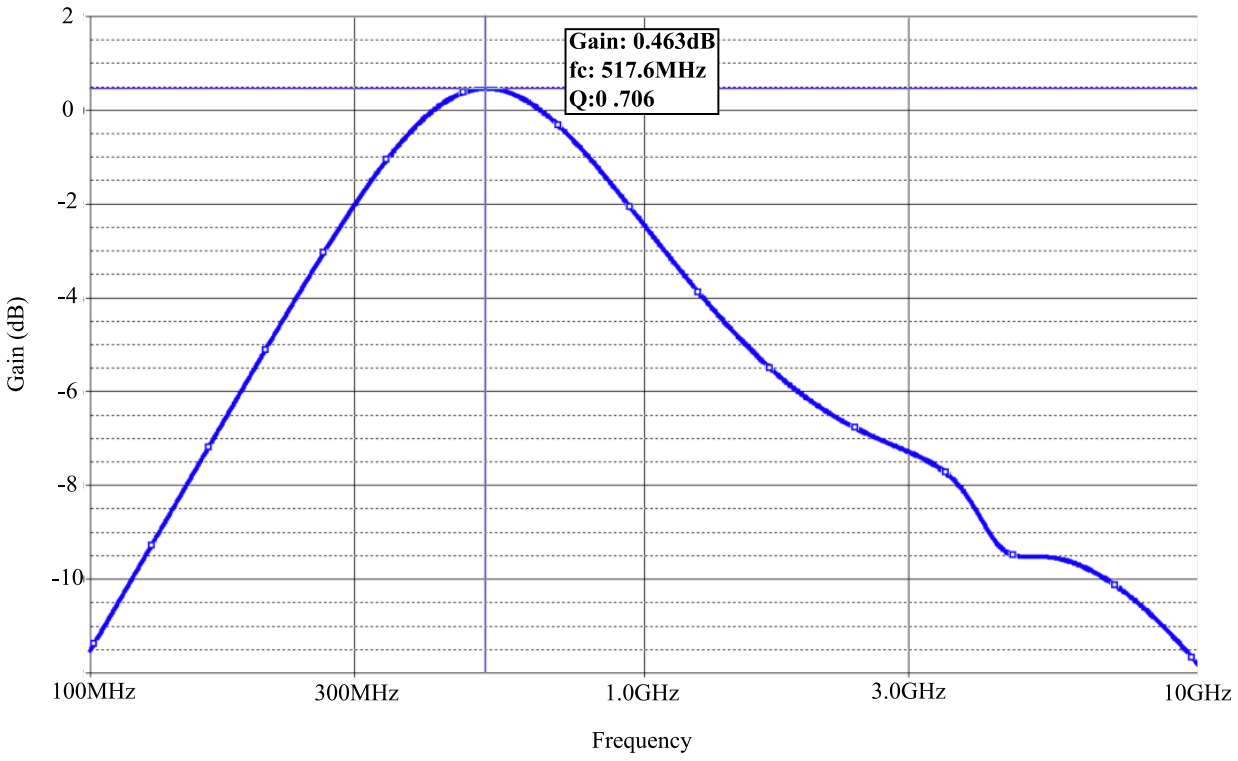


Figure 5: AC analysis of a single stage Deliyannis filter. G=0.463dB, f_c=517MHz, Q=0.706.

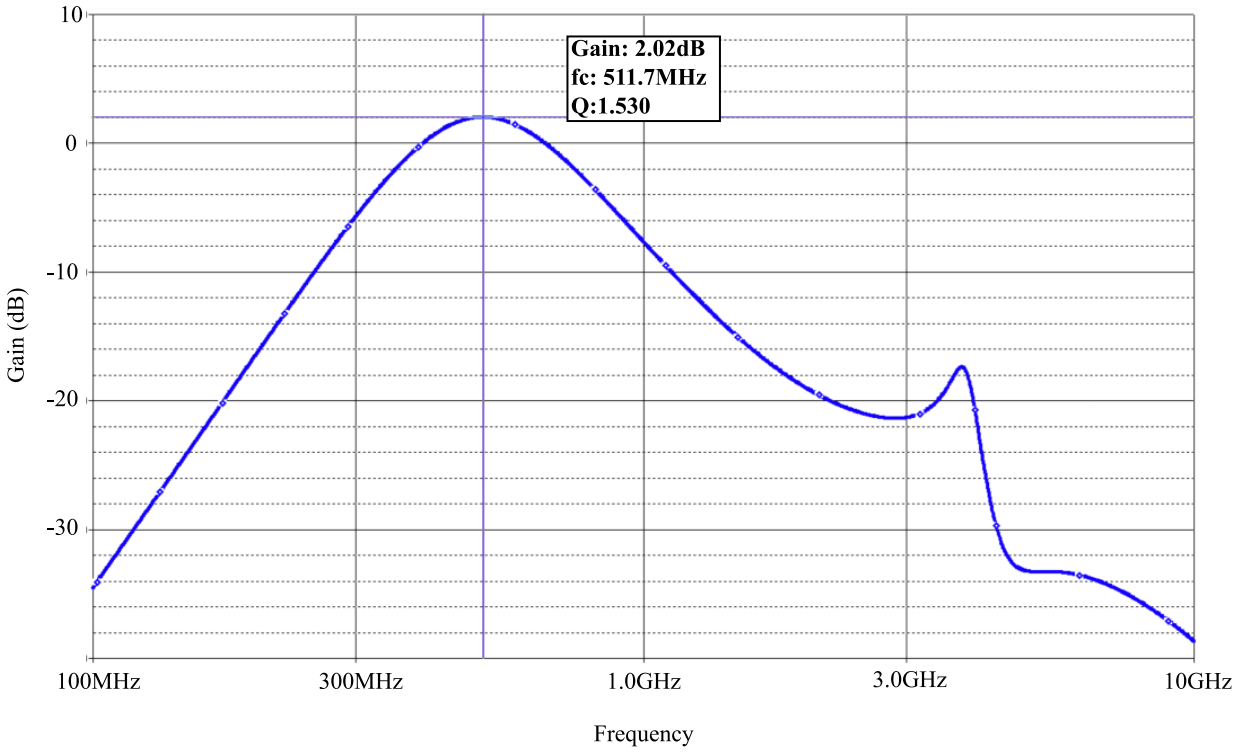


Figure 6: AC analysis of a three stage Deliyannis filter. G=2.02dB, f_c=511.7MHz, Q=1.530.

3c. Level Shifting Amplifier

The NBPFs were followed by a final layer of amplification to shift the DC level of the signal and amplify the signal to match the 0 to 1V input range for compatibility with the ADCs on the Xilinx RFSoC 2x2 board to minimize any quantization noise.

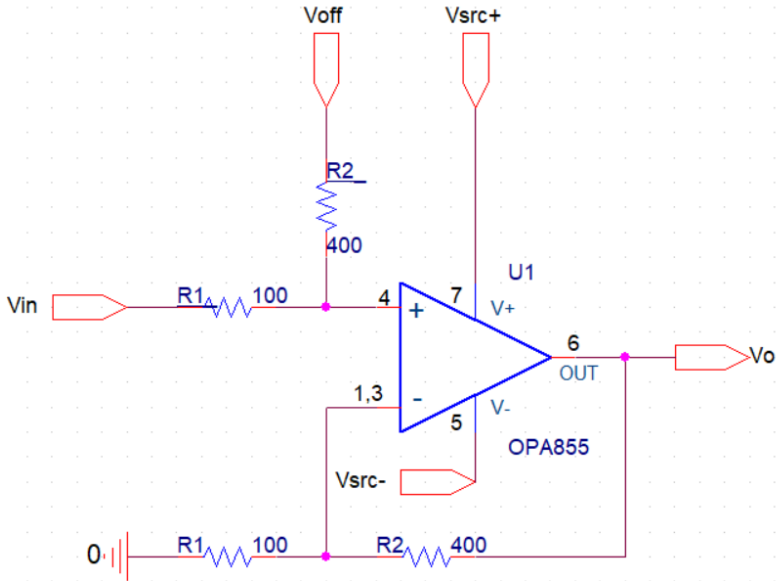


Figure 7: Circuit diagram of the level shifting amplifier.

3d. Front-End System Overview

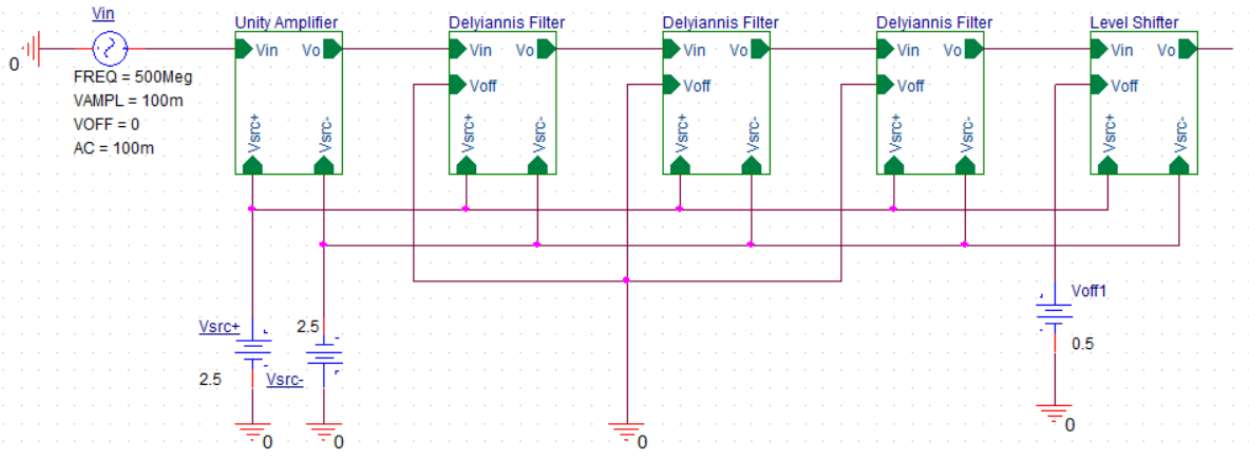


Figure 8: Final block level diagram of the pre-ADC filter driver circuit.

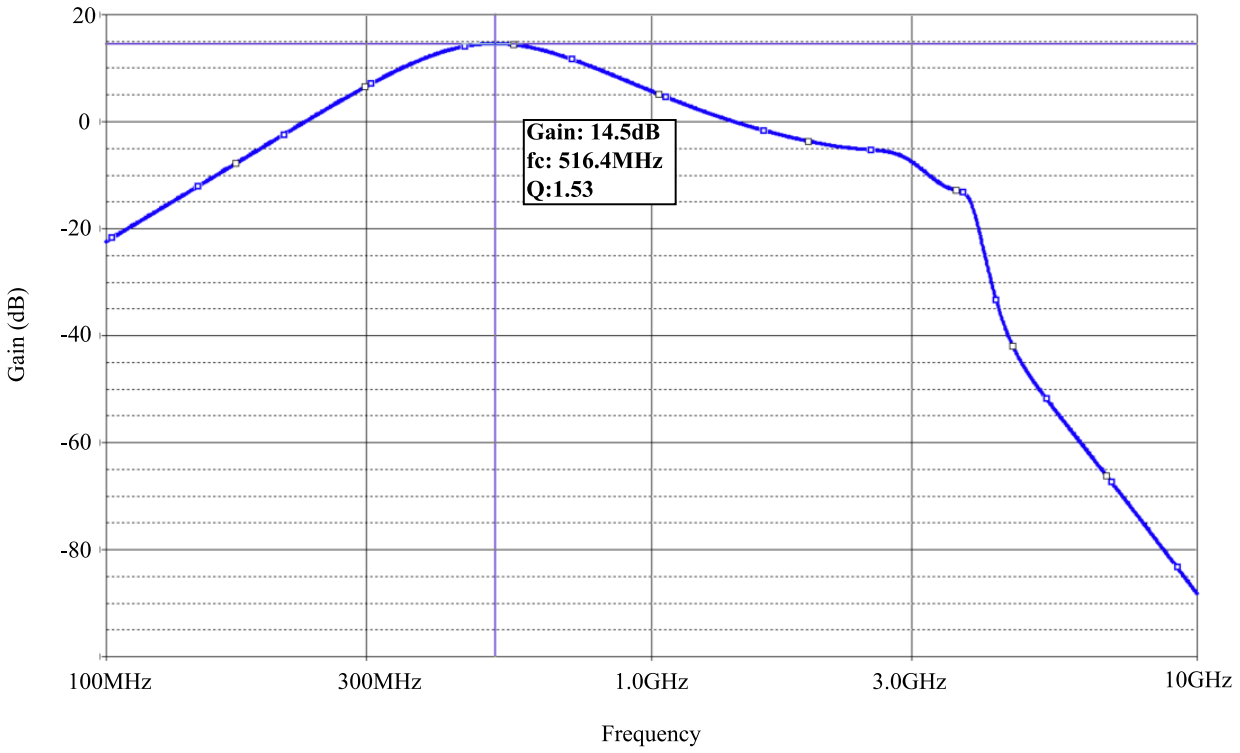


Figure 9: AC analysis simulation of final output of the pre-ADC driver circuit. G=14.5dB, f_c=516.4MHz, Q=1.53.

The above figures Figure 8 and Figure 9 show the final block diagrams and AC analysis simulation of the pre-ADC circuit. The final parameters achieved were $f_c = 516.4\text{MHz}$, $G = 14.5dB$, $Q = 1.53$.

4. Experimentation Setup and Results

4a. Front-End Layout

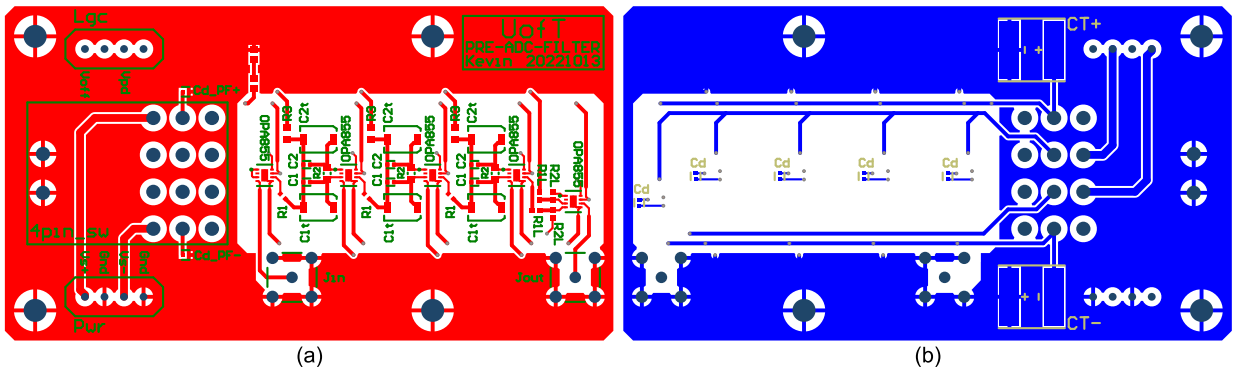


Figure 10. (a): Top layer PCB layout diagram of the pre-ADC filter circuit. (b): Bottom layer PCB layout diagram of the pre-ADC filter circuit.

The pre-ADC front-end was implemented into PCB layout. Special care was taken in layout to minimize the introduction of noise. Components of size standard 0603 or smaller were used exclusively in any high-frequency paths of the circuit to reduce parasitic capacitances. Decoupling capacitors C_d were used at the power inputs of all opamp chips. Special care was taken to ensure symmetry in trace lengths in the signal inputs to the op-amps. Finally, a ground pour was applied in all non-high-frequency regions of the board to further reduce parasitic capacitances.

4b. Front-End Assembly

The assembly of the pre-ADC filter was done stage-by-stage, fully assembling one stage of the circuit, validating the functionality, then moving on after validation. As seen in Figure 11, the assembly is still in progress, with the level shifting amplifier yet to be soldered.

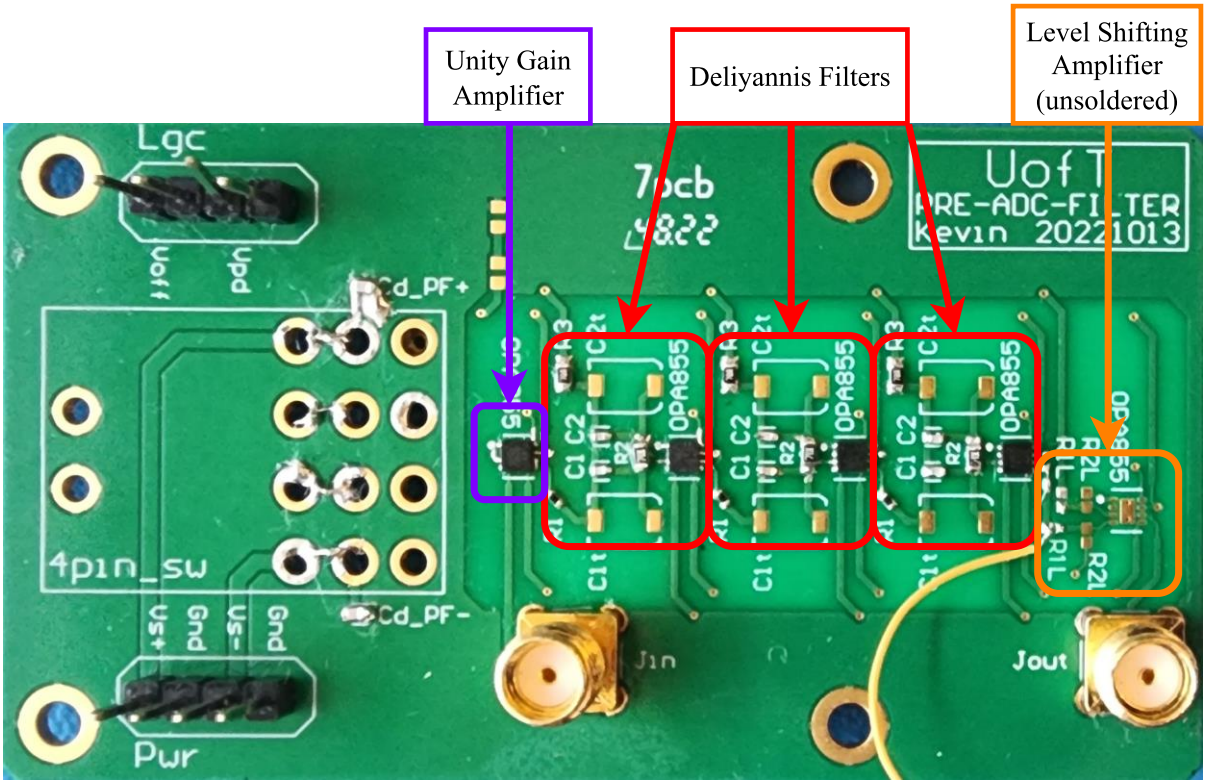


Figure 11: Image of the partially assembled pre-ADC filter. The level shifting amplifier has not been soldered.

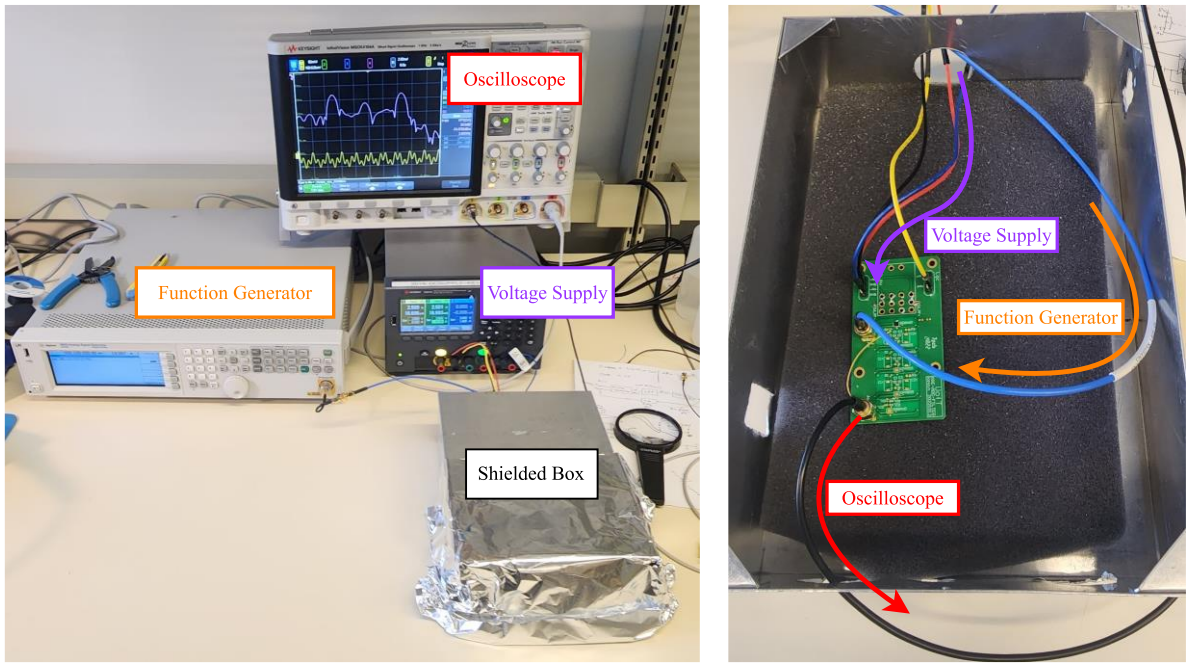
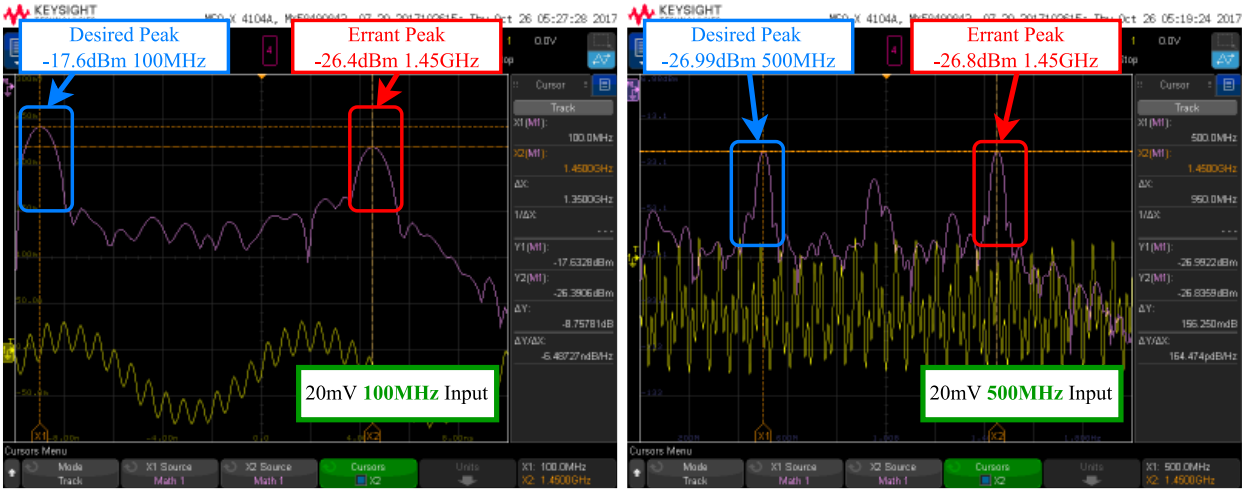


Figure 12.
(a): Overview image of validation setup. (b): Image of the circuit-under-test inside the metal shielded box.

The validation of a block was performed with a high-frequency function generator and oscilloscope as shown on Figure 12. The function generator would be used to create a sinusoidal input at a target frequency. The output of a block was then analyzed via an oscilloscope with the desired output being a clean sinusoidal of the same input frequency albeit with the same gain as in simulation. A metal box was utilized as a shield to minimize noise from external sources such as radio stations.

4c. Input Buffer Validation

The unity gain amplifier exhibited an unexpected behavior during validation. While the input of the system was a sinusoidal, the time domain output was clearly a modulation of multiple frequencies as can be seen in Figure 13. Under frequency domain, there was a peak present with an amplitude of -26dBm at 1.45GHz. This peak was present with or without the presence of the metal shield and was static in magnitude and frequency when the input frequency was modified from 500MHz to100MHz.

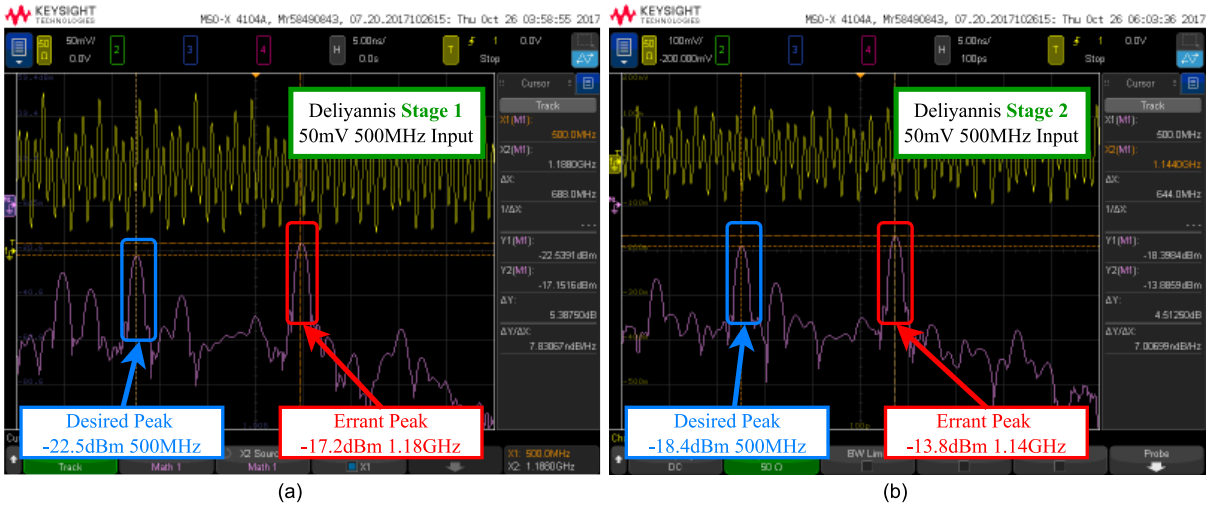


(a) (b)

Figure 13.
(a): Output of unity gain amplifier at 100MHz input. (b): Output of unity gain amplifier at 500MHz input.

4d. Deliyannis Stage Validation

The errant peak observed in the input buffer was also observed in the Deliyannis stages. As seen in Figure 14, at the first Deliyannis stage it was present with an amplitude of -17.2dBm at 1.18GHz and at the second Deliyannis stage it was present with an amplitude of -13.8dBm at 1.14GHz. This suggests that the noise is increasing with subsequent stages and getting closer to the target f_L. Furthermore, with an input amplitude of 50mV, even at the first Deliyannis stage its amplitude was greater than the desired peak at -22.5dBm.



(a) (b)

Figure 14. (a): Output of Delyiannis Stage 1 at 500MHz. (b): Output of Delyiannis Stage 2 at 500MHz.

There is also significant intermodulation occurring between this distortion and the desired signal as shown in Figure 15. As the input frequency changed from 500MHz to 540MHz, intermodulation could be seen in the frequency domain as intermodulation peaks appeared and disappeared around the two peaks.

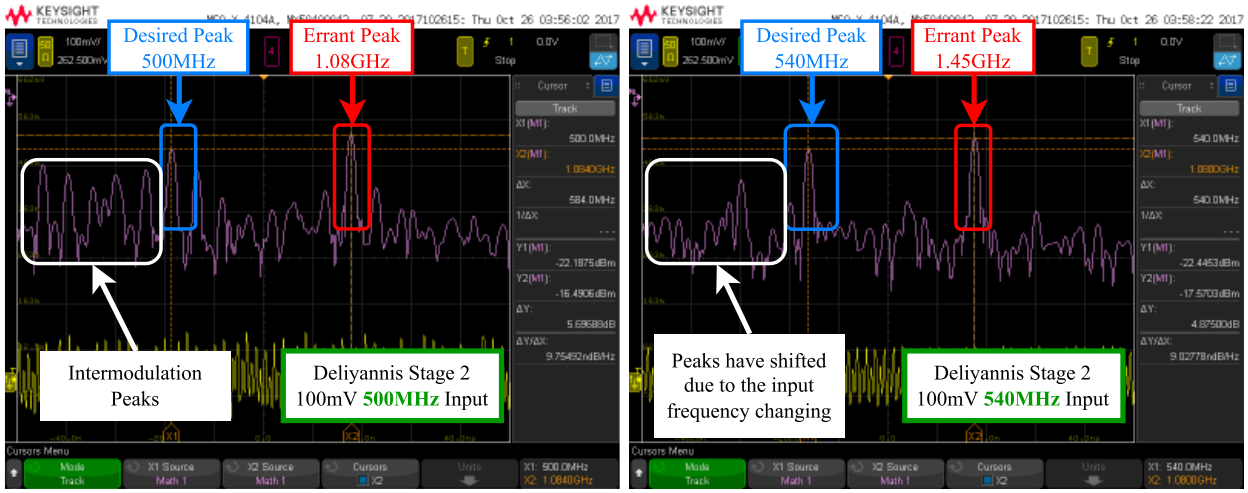


Figure 15. (a): Output of Delyiannis Stage 2 at 500MHz. (b): Output of Delyiannis Stage 2 at 540MHz.

4e. Discussion

The source and nature of this errant peak is yet undetermined. It is unlikely to be external noise as the noise is not attenuated by the presence of the metal shielding. Its static nature with respect to the input frequency suggests that it is also not a harmonic of the input, as a harmonic, being a multiple of the fundamental frequency, would surely change with the change in the input. It also cannot be an intermodulation with another higher-order frequency as intermodulation would imply that it be a function of the input frequency and hence would be subject to change with the input frequency. It could be some sort of distortion in the system but confirming this would be difficult. Regardless of its nature, its increase in amplitude at higher stages to the point of overshadowing the 50mV amplitude input and the intermodulation with the fundamental frequency are will need to be addressed before proceeding to further steps.

5. Summary

This thesis aimed to simplify the Rx of portable NMR spectrometers with the goal of increasing the discrimination of frequency peaks during analysis. To achieve such detail, a strong β_0 is required but existing works are constrained by low-frequency ADCs that are not able to directly capture the resulting high frequency f_L. This thesis aims to leverage modern advances in high frequency ADCs to direct sample the NMR signals with high f_L, increasing the detail of analysis by reducing noise and more distinguished peaks.

A pre-ADC filter was designed to act as an analog-front end. The goal of this filter would be to attenuate non-relevant frequencies enough to minimize intermodulation and distortion being transferred into the digital domain, where further analysis of the signal would occur.

The implementation of this circuit has encountered difficulties due to a distortion of unknown nature at around 1 GHz. The amplitude of this distortion is significant compared to the input, and further work needs to be done to address it.

6. Future Work

The immediate next step should be the completion of the pre-ADC filter such that experimental data can be acquired on the FPGA. Given the distortion that is observed in the circuit, there is still significant amount of work required in this part. At best, components of the pre-ADC filter could be substituted with different values to achieve better results. At worst it may require a redesign of the circuit using a different filter such as an LC filter that can achieve higher Q values in lower orders. The downside of the LC filters are that they are difficult to tune as they are highly sensitive to parasitic capacitances.

After the completion of the pre-ADC filter would be implementation of the FPGA. A digital filter and FFT should be implemented on the Xilinx board to post-process the data in the digital domain. Higher level computation may be required externally to the Xilinx board if there is a processing bottleneck.

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