**CPEN 211 Introduction to Microcomputers, 2023**
**Lab Proficiency Test #3**

**Question 1 [2.5 marks, part marks possible]:** In a file "**q1.sv**" write **synthesizable** Verilog implementing the datapath in the figure below. Your top-level module *must* be declared as:

```
module datapath(clk,in,rsel,Rw,w,Rr,loadA,aluop,loadN,N,out);
  input clk, rsel, w, loadA, loadN;
  input [1:0] Rw, Rr, aluop;
  input [15:0] in;
  output [15:0] out;
  output reg N;
```

Use the signal names as shown in the figure. ALU is combinational logic defined as follows:

| aluop | ALU Operation |
|---|---|
| 2'b00 | aout = rout << 1 |
| 2'b01 | aout = (rout << 1) + 1 |
| 2'b10 | aout = {A[7:0],rout[7:0]} |
| 2'b11 | aout = {8'b0,A[15:8]} - rout |

The output `aN` of the ALU is a 1-bit signal that is 1 when 2's complement ALU output `aout` is negative and 0 otherwise. The datapath contains five 16-bit registers with load enable and clock input `clk`, connected to 16-bit signals `R0`, `R1`, `R2`, `R3`, and `A`. Datapath output `out` is connected to `R1`. The block "Loader" is combinational logic that enables loading of `R0` only when `w` is 1 and `Rw` is `2'b00`, `R1` only when `w` is 1 and `Rw` is `2'b01`, `R2` only when `w` is 1 and `Rw` is `2'b10`, and `R3` only when `w` is 1 and `Rw` is `2'b11`. The input "`Rr`" is 2-bit binary select, input "`loadA`" and "`loadN`" are load enables. You can include testbenches in q1.sv. The testbench `tb_check_q1` in `tb.sv` inside https://cpen211.ece.ubc.ca/2023/lpt3-Check-Dz7-e9V.zip should print "`INTERFACE OK`" **and generate no ModelSim warnings** if your interface is compatible with the autograder (cut and paste link if clicking does not work). Your q1.sv **must** include definitions for any modules instantiated. *Hint:* Tor's solution for q1.sv is 31 lines. **Upload your Verilog file named "q1.sv" for Question 1 on "Lab Proficiency Test #3" on Canvas before 5:45 pm.**