**CPEN 211 Introduction to Microcomputers, 2021**
**Lab Proficiency Test #3**

**Question 1 [2.5 marks, part marks possible]:** In a file "**q1.v**" write **synthesizable** Verilog implementing the datapath in the figure below. Your top-level module must be declared as:

```
module datapath(clk,in,sr,Rn,w,aluop,lt,tsel,bsel,out);
  input clk, w, lt;
  input [7:0] in;
  input [1:0] sr, Rn, aluop;
  input [2:0] bsel, tsel;
  output [7:0] out;
```

Use the signal names as shown in the figure. ALU is combinational logic defined as follows:

| aluop | ALU Operation |
|---|---|
| 2'b00 | alu_out = tmp ^ Bin |
| 2'b01 | alu_out = tmp & Bin |
| 2'b10 | alu_out = tmp << 1 |
| 2'b11 | alu_out = Bin |

The datapath contains five 8-bit registers with load enable and clock input `clk`, connected to 8-bit signals `R0`, `R1`, `R2`, `R3`, and `tmp`. The block "Loader" is combinational logic that enables loading of `R0` only when `w` is 1 and `Rn` is `2'b00`, `R1` only when `w` is 1 and `Rn` is `2'b01`, `R2` only when `w` is 1 and `Rn` is `2'b10`, and `R3` only when `w` is 1 and Rn is `2'b11`. The input "`sr`" is 2-bit binary select, 3-bit inputs "`tsel`" and "`bsel`" are one-hot select, and input "`lt`" is a load enable. Your q1.v **must** include definitions for any modules instantiated. You can include testbenches in q1.v. The testbench `tb_check_q1` in tb.v inside https://cpen211.ece.ubc.ca/2021/lpt-3-checker-G3iW.zip should print "`INTERFACE OK`" and generate no ModelSim warnings if your interface is compatible with the autograder (cut and paste link if clicking does not work). **Upload your Verilog file named "q1.v" for Question 1 on "Lab Proficiency Test #3" on Canvas before 6:45 pm.**