ISLAMIC UNIVERSITY OF TECHNOLOGY (IUT)

ORGANISATION OF ISLAMIC COOPERATION (OIC)

Department of Computer Science and Engineering (CSE)

SEMESTER FINAL EXAMINATION SUMMER SEMESTER, 2021-2022

DURATION: 3 HOURS FULL MARKS: 150

CSE 4205: Digital Logic Design

Programmable calculators are not allowed. Do not write anything on the question paper.

Answer **all 6 (six)** questions. Figures in the right margin indicate full marks of questions whereas corresponding CO and PO are written within parentheses.

Necessary intermediate steps, examples, and figures must be provided if required.

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1. a) i. Design a combinational circuit which will either subtract X from Y or Y from X, depending on the value of A. Here, Both X and Y are 4-bit in length. If $A = 1$, the output should be $X - Y$, and if $A = 0$, the output should be $Y - X$. Use the block diagrams of 4-bit adder ICs (IC 74283) and 2-to-1 multiplexer to design this circuit. — 10 (CO1) (PO1)

ii. Implement the same circuit as described in Question 1.a)i. with the required number of tri-state buffers. — 10 (CO1) (PO1)

b) The Code Converter is used to convert one type of binary code to another. Implement a BCD to 2421 Code Converter using an appropriate decoder with active low outputs and minimum number of gates. — 5 (CO2) (PO1)

2. a) *A full subtractor is a combinational circuit that performs subtraction of two bits: one is minuend and other is subtrahend, considering borrow of the previous adjacent lower minuend bit. Implement a full subtractor using the following LSIs:* — 7+8 (CO1) (PO1)

i. *8-to-1 MUX*

ii. *4-to-1 MUX*

b) A characteristic equation gives the next state in terms of the current state and input. Derive the characteristic equations for the following flip-flops in product-of-sums form. — 2.5×4 (CO5) (PO1)

i. S-R flip-flop

ii. D flip-flop

iii. J-K flip-flop

iv. T flip-flop

3. a) How can a universal shift register be developed from a bidirectional shift register? Draw a figure of a 4 bits universal shift register where register operation can be categorized as shown in Table 1. — 10 (CO3) (PO1)

Table 1: Choices for Register's operation for question 3.a)

Operation Order	Register Operation
1	Parallel Loading
2	Shift Left
3	Shift Right
4	No Change
5	Complement

b) i. Implement the following equations using the PLA shown in Figure 1:

$$X = AB'D + A'C' + BC + C'D'$$
$$Y = A'C' + AC + C'D'$$
$$Z = CD + A'C' + AB'D$$

Redraw this PLD notation (from Figure 1) showing the proper connections that will be made to implement these equations and develop its corresponding program table. The horizontal lines in Figure 1 represent the required number of AND arrays.

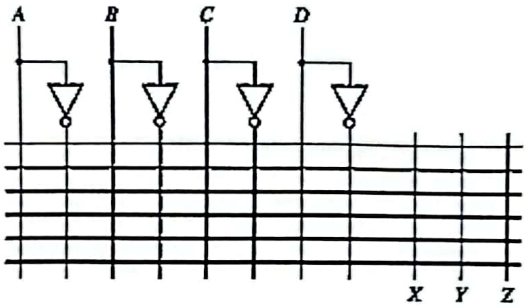

Figure 1: PLD notation for PLA for Question 3.b)

ii. Implement the equations mentioned above with an appropriate ROM using PLD notation and program table. 7 (CO4) (PO2)

4. a) *Sequential circuits are digital circuits that store and use the previous state information to determine their next state. The state diagram of a sequential circuit is shown in* Figure 2. 10+5 (CO4) (PO2)

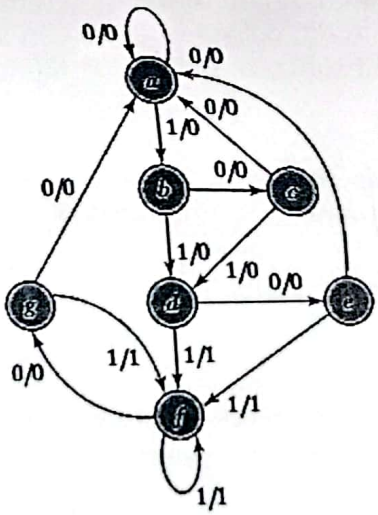

Figure 2: State diagram of a sequential circuit for Question 4.a)

i. Draw the reduced state diagram of Figure 2 showing the intermediate steps.

ii. Starting from state *a* and the input sequence 01110010011, determine the output sequence for the state diagram in Figure 2 and its reduced state diagram. Show that the same output sequence is obtained for both.

...the sequential logic circuit in Figure 3 and explain its operation following a ...ward procedure: 15 (CO3) (PO2)

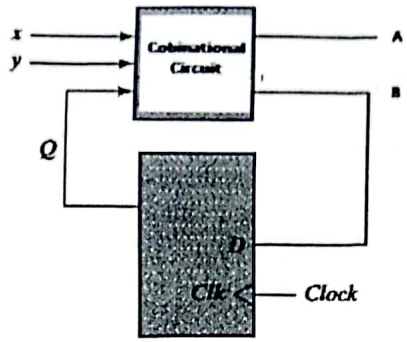

Figure 3: A sequential logic circuit for Question 4.b)

5. a) Design a counter with JK flip-flops that goes through the following binary repeated sequence: 0, 1, 3, 7, 6, 4. Show that when binary states 010 and 101 are considered as don't care conditions, the counter may not operate properly. Find a way to correct the design 15 (CO5) (PO2)

   b) What are D/A converters and A/D converters and what are their uses? Explain how sampling, quantization and resolution are important to design them. 5 (CO5) (PO1)

6. Design a sequential circuit as shown in Figure 4 which investigates an input sequence X and will produce an output, **Z** = 1 for any input sequence ending in 0010 or 100. 25 (CO2) (PO2)

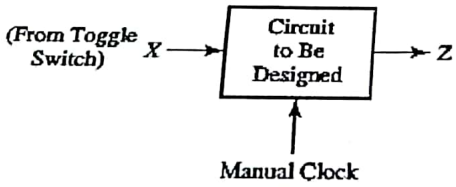

Figure 4: A sequential circuit to be designed.

Sample Input and Output:

$X = 1\,1\,0\,0\,1\,0\,0\,1\,0\,1\,0\,0\,1\,0\,1$

$Z = 0\,0\,0\,1\,0\,1\,1\,0\,1\,0\,0\,1\,0\,1\,0$

i. Your circuit should have a start state and should be provided with a method for manually resetting the flip-flops to the start state. A minimum solution requires six states.
Design your circuit using universal gates, and D flip-flops. Any solution which is minimal for your state assignment and uses 10 or fewer gates and inverters is acceptable. You should assign 000 to the start state.

ii. Starting in the proper initial state, determine the output sequence for each of the following input sequences:
(1) $X1 = 0\,0\,1\,1\,0\,1\,0\,0\,1\,0\,1\,0\,1\,0\,0\,0\,1\,0\,0\,1\,0\,0\,1\,0$
(2) $X2 = 1\,1\,0\,0\,1\,1\,0\,0\,1\,0\,1\,0\,1\,0\,0\,1\,0\,1\,0\,1\,0\,0\,1\,0$