CSE 4205
Digital Logic Design

Analysis and Design Procedure of Sequential Circuits

Course Teacher: Md. Hamjajul Ashmafee

Lecturer, CSE, IUT

Email: ashmafee@iut-dhaka.edu

Remaining to Add

- For Design and Analysis Procedure
  - Review other books and internet resources
  - Give 2 hours to make it complete and beautiful
- For Pattern/Sequence detector:
  - Review other books and internet resources
  - Draw the figure with Wacom (slide 11)

Analysis Procedure

From book [Page 250]

- **Starting with a sequential Circuit**
- **Deriving its state table**
  - **2 variants to represent**
- **Deriving its state diagram** from the state table
- **Deriving its state equation** from the state table
  - ***Final outcome***
  - ***Also, need to describe the behavior of the circuit [Preferred]***
- **Summarize all *generalized steps***

Design Procedure

From book [Page 254]

- Mention all ***Generalized Steps***
- ***Example*** following those steps

Example of Design Procedure

Sequence/Pattern Detector

Sequence/Pattern Detector

- A **sequential circuit** that takes the **input** of **binary bit streams** and generate **an output true** (e.g. logic 1) when the **target sequence** is detected
  - Bit stream (1s and 0s) will be fed/inserted as input to check for particular pattern or sequence
    - As soon as, the target pattern is detected, it will make the output high
- As the output depends on the current state as well as the external input (x), a **Mealy FSM** is considered

Sequence/Pattern Detector: Types

- Types:
  - **Overlapping**
    - The last bit of one sequence becomes the intermediate bit of the next sequence
  - **Non-overlapping**
    - The last bit of one sequence doesn't become the intermediate bit of the next sequence
- They will be clear from the examples

Design A Sequence Detector

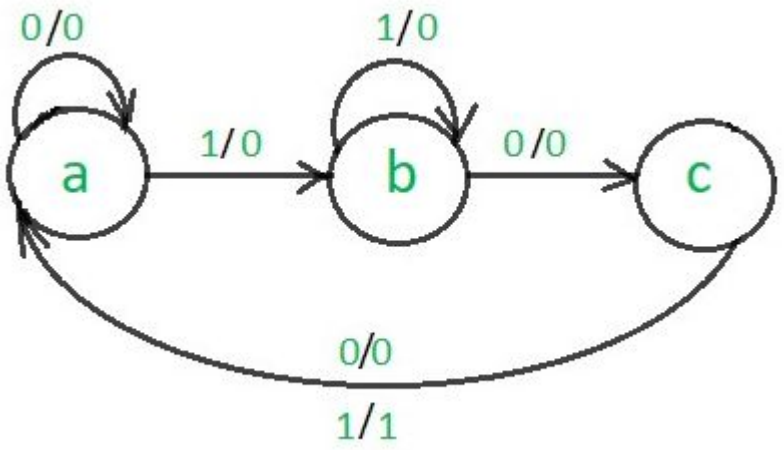
- **Steps:**
  - Step 1: Develop the state diagram
  - Step 2: Perform the state assignment and state reduction
  - Step 3: Select the number and type of the flip flop
  - Step 4: Derive Circuit Excitation Table
  - Step 5: Derive the expressions for input of the flip flops and output(s)
  - Step 6: Develop the circuit

Non-overlapping '101' Mealy Sequence Detector

- **Example:**

Input :	0	1	1	0	1	0	1	0	1	1	0	0	1
Output:	0	0	0	0	1	0	0	0	1	0	0	0	0

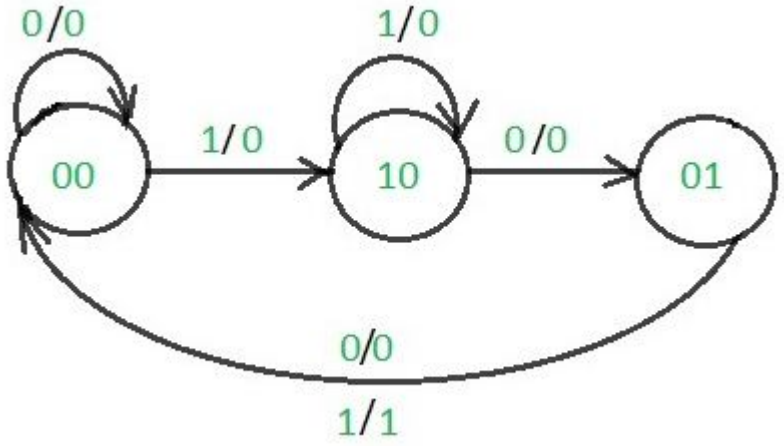
- **State Diagram:**



Non-overlapping '101' Mealy SD…

- **State Assignment:**

a	00	Nothing detected
b	10	'1' detected
c	01	'10' detected



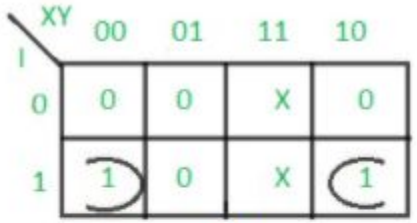
Non-overlapping '101' Mealy SD…

- **Type and number of flip flops:**
  - Two D flip flops
- **Circuit Excitation Table:**

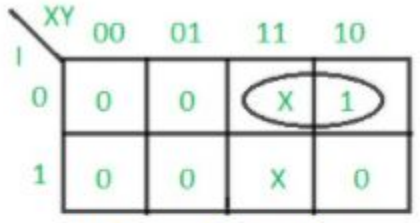
Present States		i/p	Next States		Flip Flop Excitations		O/P
Qa	Qb	x	Qa+	Qb+	Da	Db	y
0	0	0	0	0	0	0	0
0	0	1	1	0	1	0	0
0	1	0	0	0	0	0	0
0	1	1	0	0	0	0	1
1	0	0	0	1	0	1	0
1	0	1	1	0	1	0	0
1	1	0	X	X	X	X	X
1	1	1	X	X	X	X	X

Non-overlapping '101' Mealy SD…

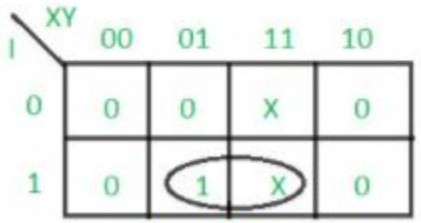
- **Expression Derivation:**



Da = Qb' . x



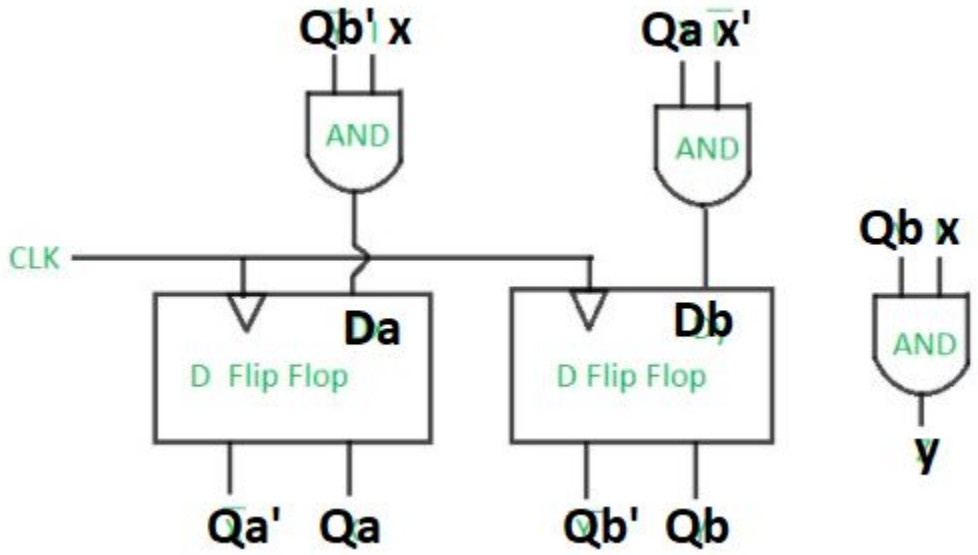
Db = Qa . x'



y = Qb . x

Non-overlapping '101' Mealy SD…

- **Circuit Implementation:**

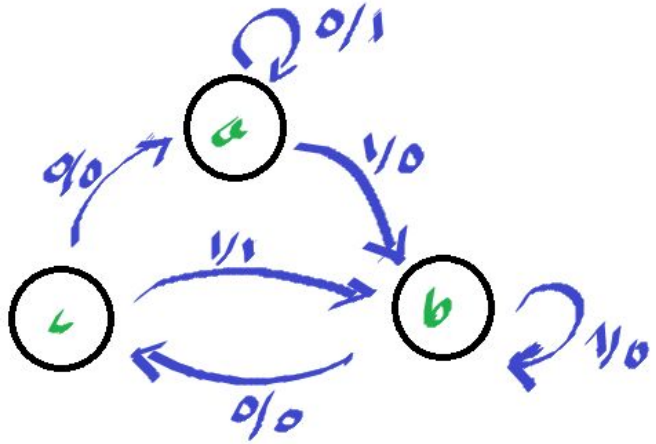


Overlapping 101 Mealy Sequence Detector

- Example:

Input :	0	1	1	0	1	0	1	0	1	1	0	0	1
Output:	0	0	0	0	1	0	1	0	1	0	0	0	0

- State Diagram:



Overlapping 101 Mealy SD…

- Others steps would be same as before.

Administration

- abc

Administration

- abc

Administration

- abc

Administration

- abc

Administration

- abc

Administration

- abc

Administration

- **abc**

Motivation

- abc