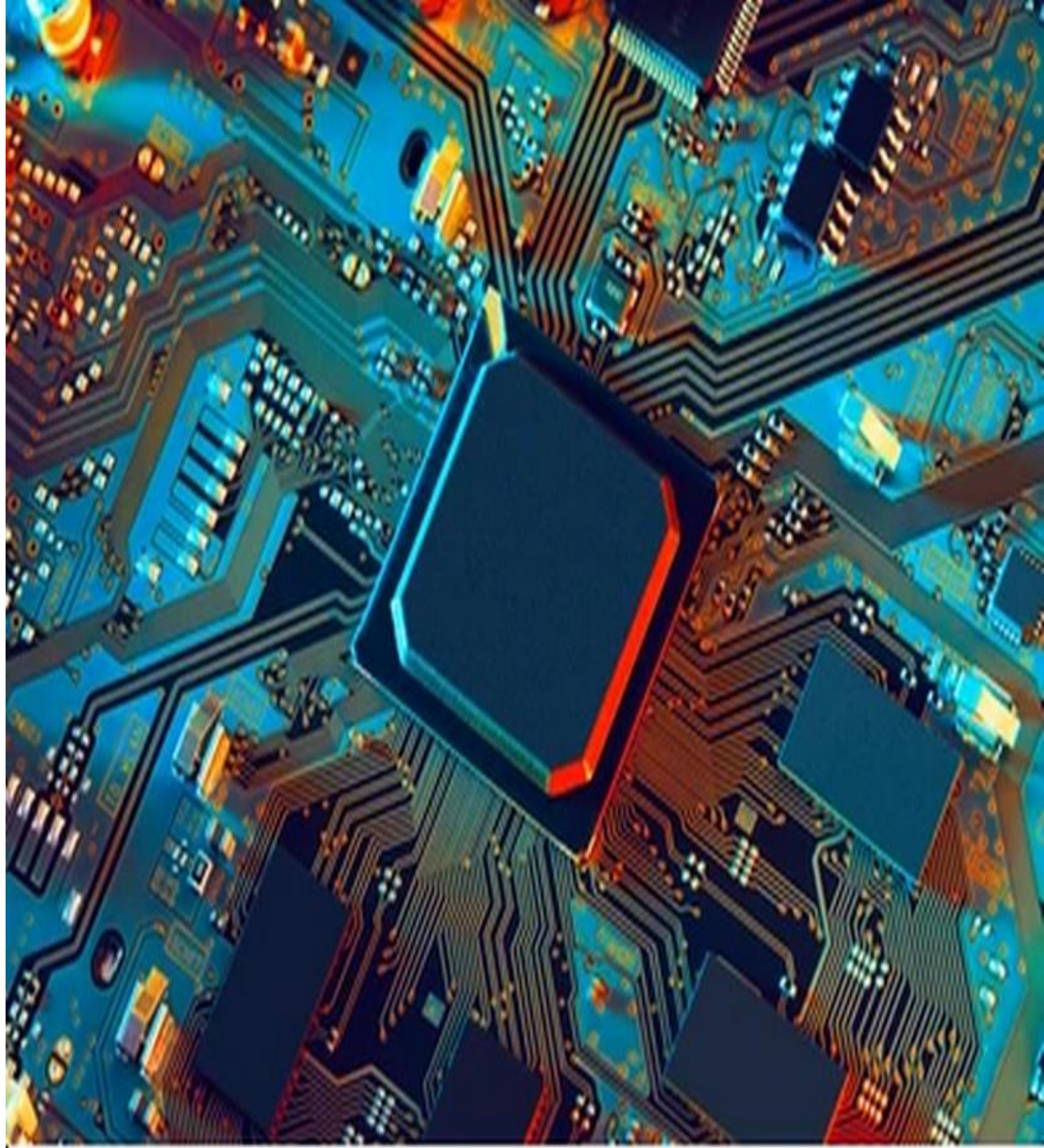
P-N JUNCTION DIODE



Types of Materials in terms of Conduction

- Insulators
- Conductors
- Semiconductors **

Unique Qualities of Semiconductor:

✓ Impurities can be mixed to change semiconductors characteristics.

What is Doping?

- Addition of impurities into a semiconductor crystal for modification of conductivity.
- Impurities are atoms that are not semiconductors, and donates electrons or holes (void of electrons) to semiconductor crystal.

To demonstrate the effect of adding impurities, let us use Silicon as semiconductor crystal that will be doped using two different impurities.

The three semiconductors used most frequently in the construction of electronic devices are Ge, Si, and GaAs.

A semiconductor material that has been subjected to the doping process is called an extrinsic material

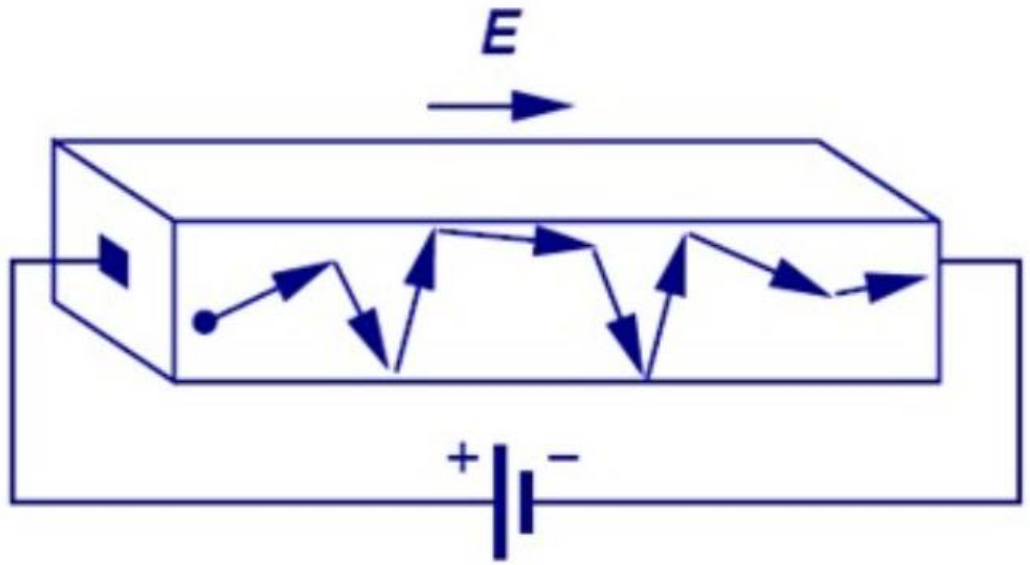
There are two extrinsic materials of immeasurable importance to semiconductor device fabrication:
1. *n* -type and
2. *p* -type materials

Drift and Diffusion

(and the battle between the two!)

The two basic processes which cause electrons and holes to move in a semiconductor are:

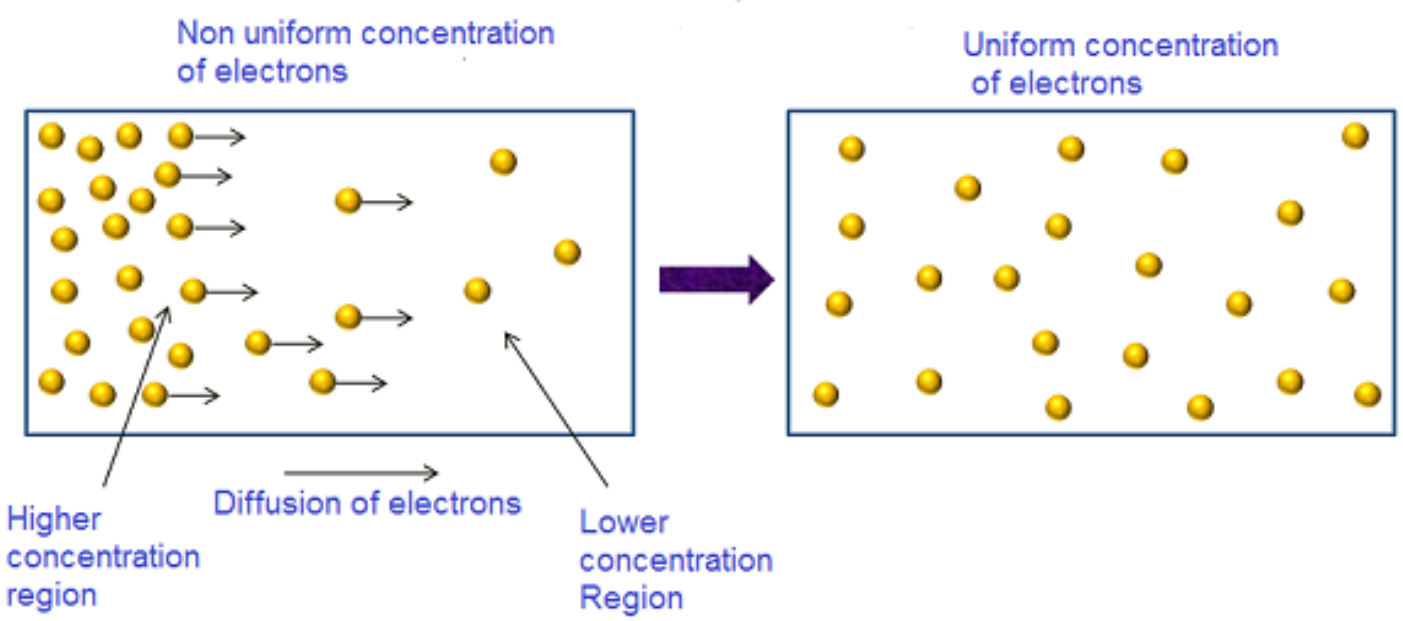
- Drift
- Diffusion



Drift Process

Drift is the movement caused by electric fields

(Example: Voltage)



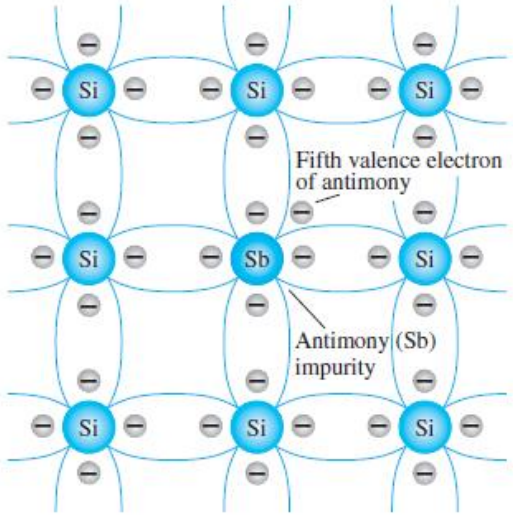
Diffusion Process

Diffusion is the flow caused by variations in the concentration of charge carriers

(electrons and holes)

n -Type Material

An *n* -type material is created by introducing impurity elements that have *five* valence electrons (*pentavalent*), such as *antimony* , *arsenic* , and *phosphorus*
the four covalent bonds are still present. There is, however, an additional fifth electron due to the impurity atom, which is *unassociated* with any particular covalent bond. This remaining electron, loosely bound to its parent (antimony) atom, is relatively free to move within the newly formed *n* -type material.



In an n-type material the electron is called the majority carrier and the hole the minority carrier

p -Type Material

The *p* -type material is formed by doping a pure germanium or silicon crystal with impurity atoms having *three* valence electrons. The elements most frequently used for this purpose are *boron* , *gallium* , and *indium.*

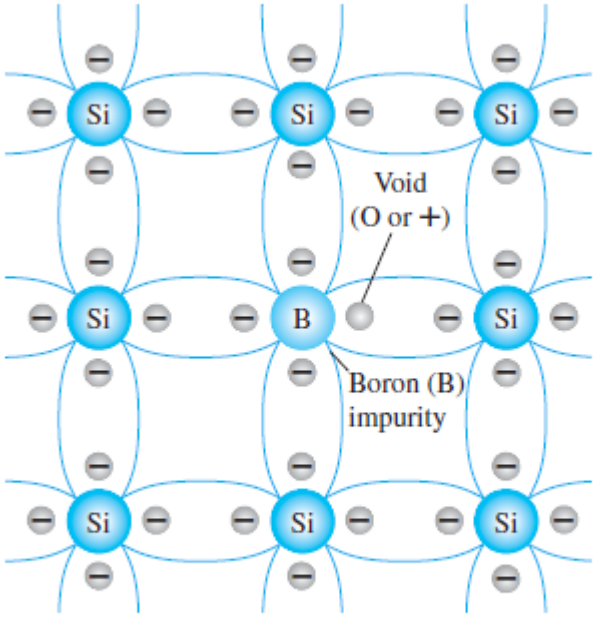
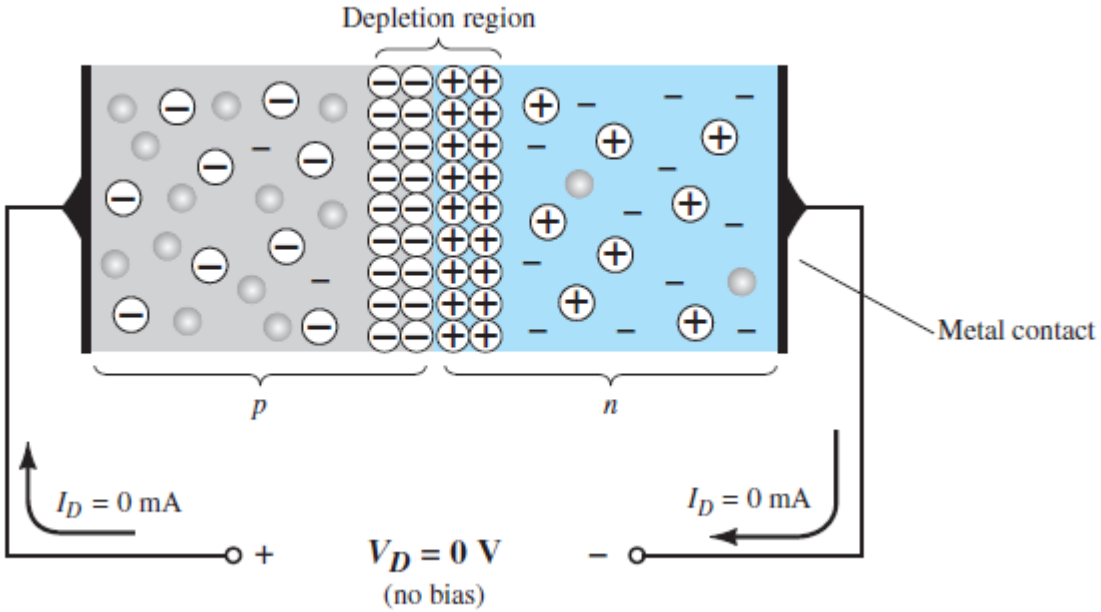


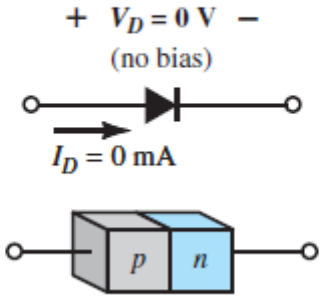
FIG. 1.9
Boron impurity in p-type material.

In a p-type material the hole is the majority carrier and the electron is the minority carrier.

SEMICONDUCTOR DIODE

The *semiconductor diode* , is created by simply joining an *n* -type and a *p* -type material together,



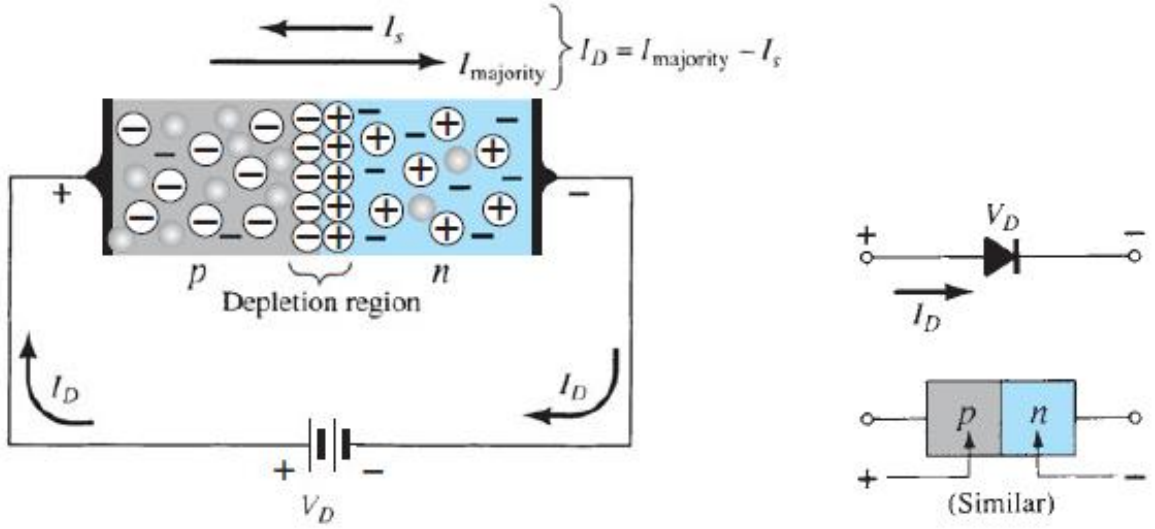


Under no-bias conditions, any minority carriers (holes) in the *n* -type material that find themselves within the depletion region for any reason whatsoever will pass quickly into the *p* -type material. The closer the minority carrier is to the junction, the greater is the attraction for the layer of negative ions and the less is the opposition offered by the positive ions in the depletion region of the *n* -type material.

This region of uncovered positive and negative ions is called the depletion region due to the “depletion” of free carriers in the region.

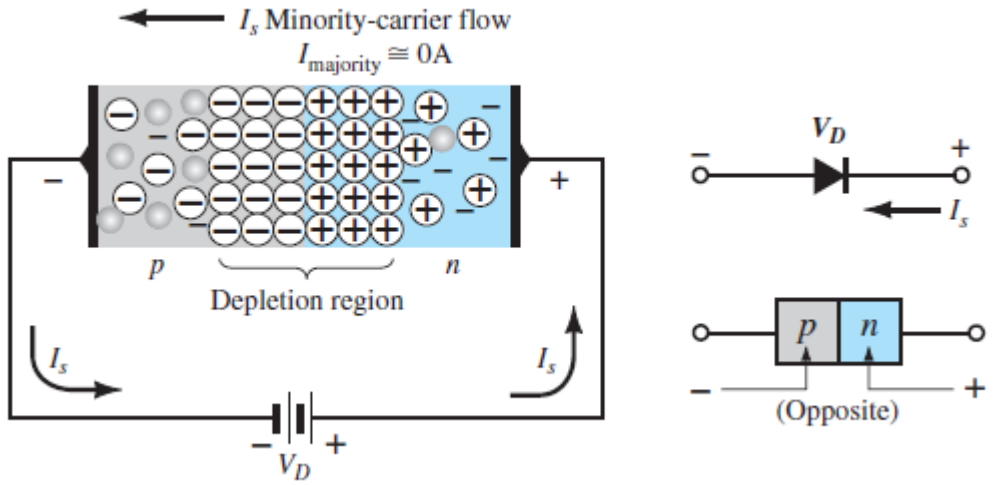
Forward-Bias Condition

A *forward-bias* or “on” condition is established by applying the positive potential to the *p* -type material and the negative potential to the *n* -type material as shown in Fig



Reverse-Bias Condition

the positive terminal is connected to the *n* -type material and the negative terminal is connected to the *p* -type material



This widening of the depletion region will establish too great a barrier for the majority carriers to overcome, effectively reducing the majority carrier flow to zero

The current that exists under reverse-bias conditions is called the reverse saturation current and is represented by I s .

The general characteristics of a semiconductor diode can be defined by the following equation, referred to as Shockley's equation, for the forward- and reverse-bias regions

$$I_D = I_s(e^{V_D/nV_T} - 1) \quad \text{(A)} \tag{1.2}$$

where I_s is the reverse saturation current
V_D is the applied forward-bias voltage across the diode
n is an ideality factor, which is a function of the operating conditions and physical construction; it has a range between 1 and 2 depending on a wide variety of factors ($n = 1$ will be assumed throughout this text unless otherwise noted).

The voltage V_T in Eq. (1.1) is called the *thermal voltage* and is determined by

$$V_T = \frac{kT_K}{q} \quad \text{(V)} \tag{1.3}$$

where k is Boltzmann's constant $= 1.38 \times 10^{-23}$ J/K
T_K is the absolute temperature in kelvins = 273 + the temperature in °C
q is the magnitude of electronic charge $= 1.6 \times 10^{-19}$ C

A silicon diode said to be a 1-mA device displays a forward voltage of 0.7 V at a current of 1 mA. Evaluate the junction scaling constant I_S. What scaling constants would apply for a 1-A diode of the same manufacture that conducts 1 A at 0.7 V?

Solution

Since

$$i = I_S e^{v/V_T}$$

then

$$I_S = ie^{-v/V_T}$$

For the 1-mA diode:

$$I_S = 10^{-3} e^{-700/25} = 6.9 \times 10^{-16} \text{ A}$$

The diode conducting 1 A at 0.7 V corresponds to one-thousand 1-mA diodes in parallel with a total junction area 1000 times greater. Thus I_S is also 1000 times greater,

$$I_S = 6.9 \times 10^{-13} \text{ A}$$

Terminal Characteristics of Junction Diodes

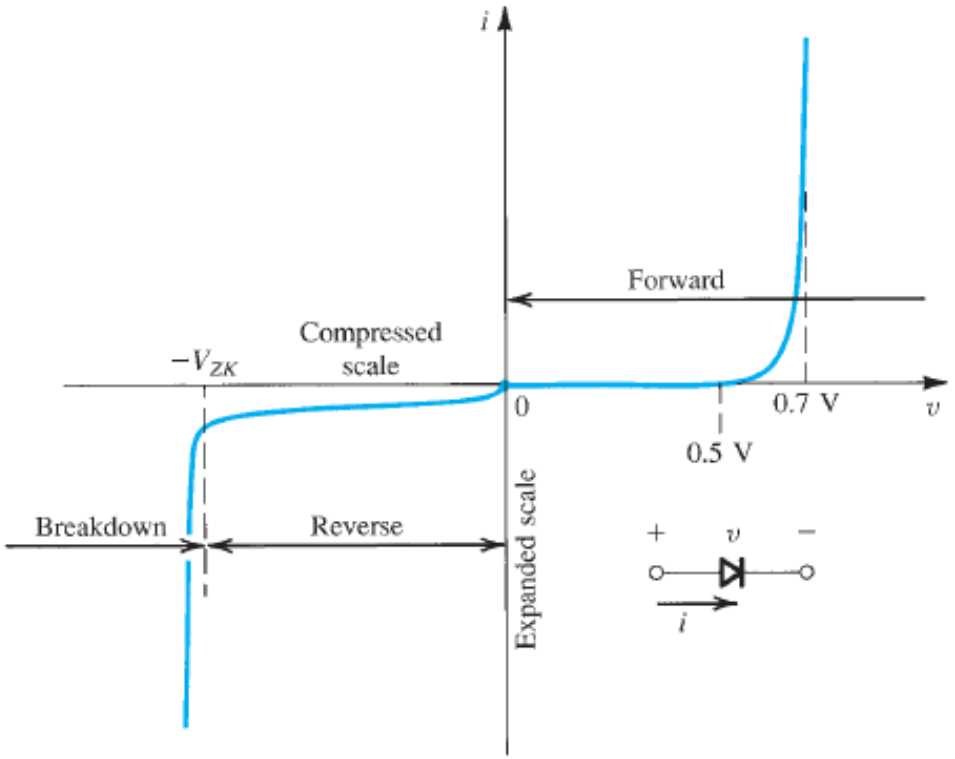


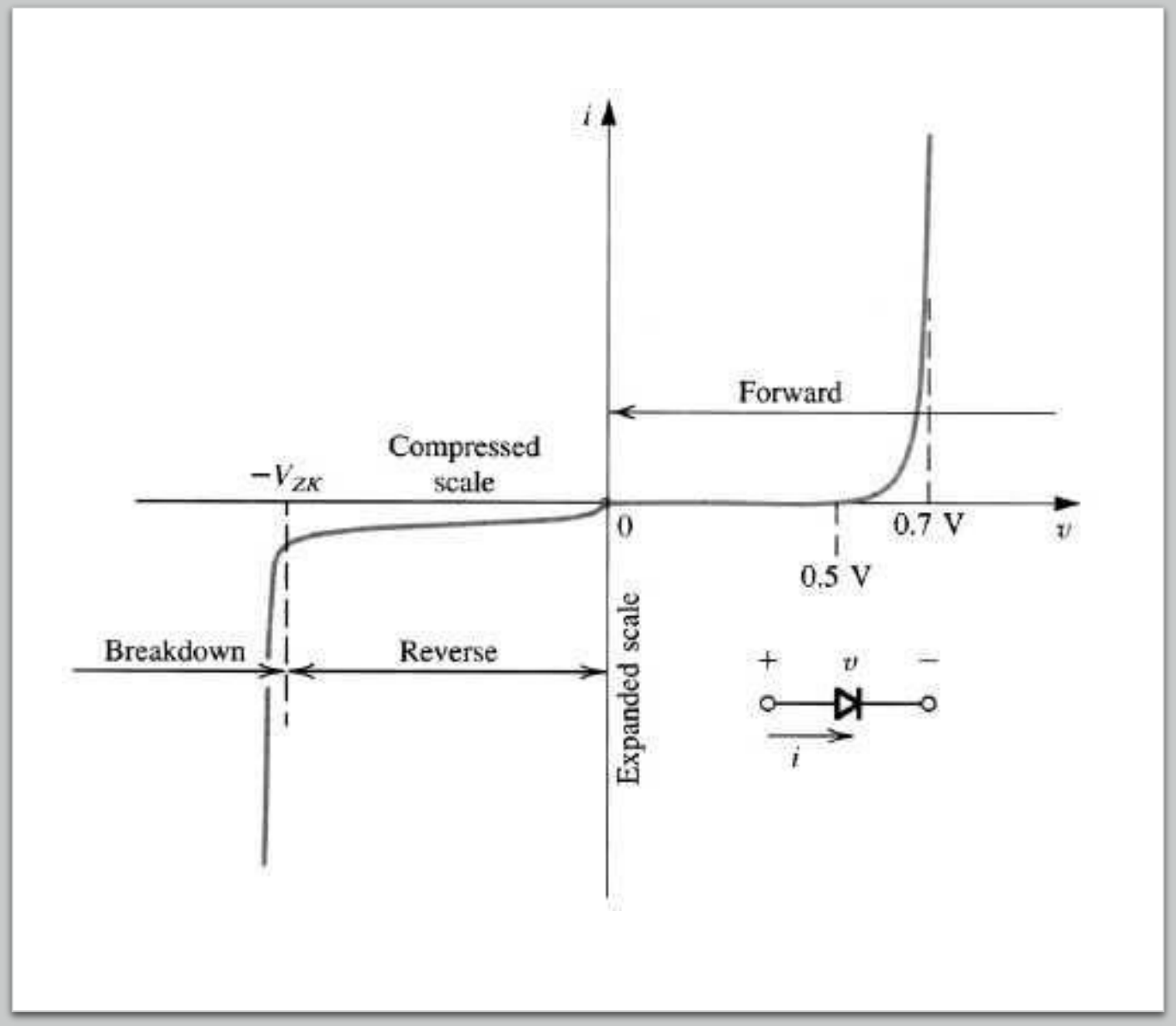
Figure 4.8 The diode I–v relationship with some scales expanded and others compressed in order to reveal details.

VI Characteristics of a Diode

When Forward biased:

- No Current until a threshold is exceeded (0.5v in picture)
- Diode starts fully conducting after 0.7v
- After 0.7v, slight change in voltage can increase current level significantly

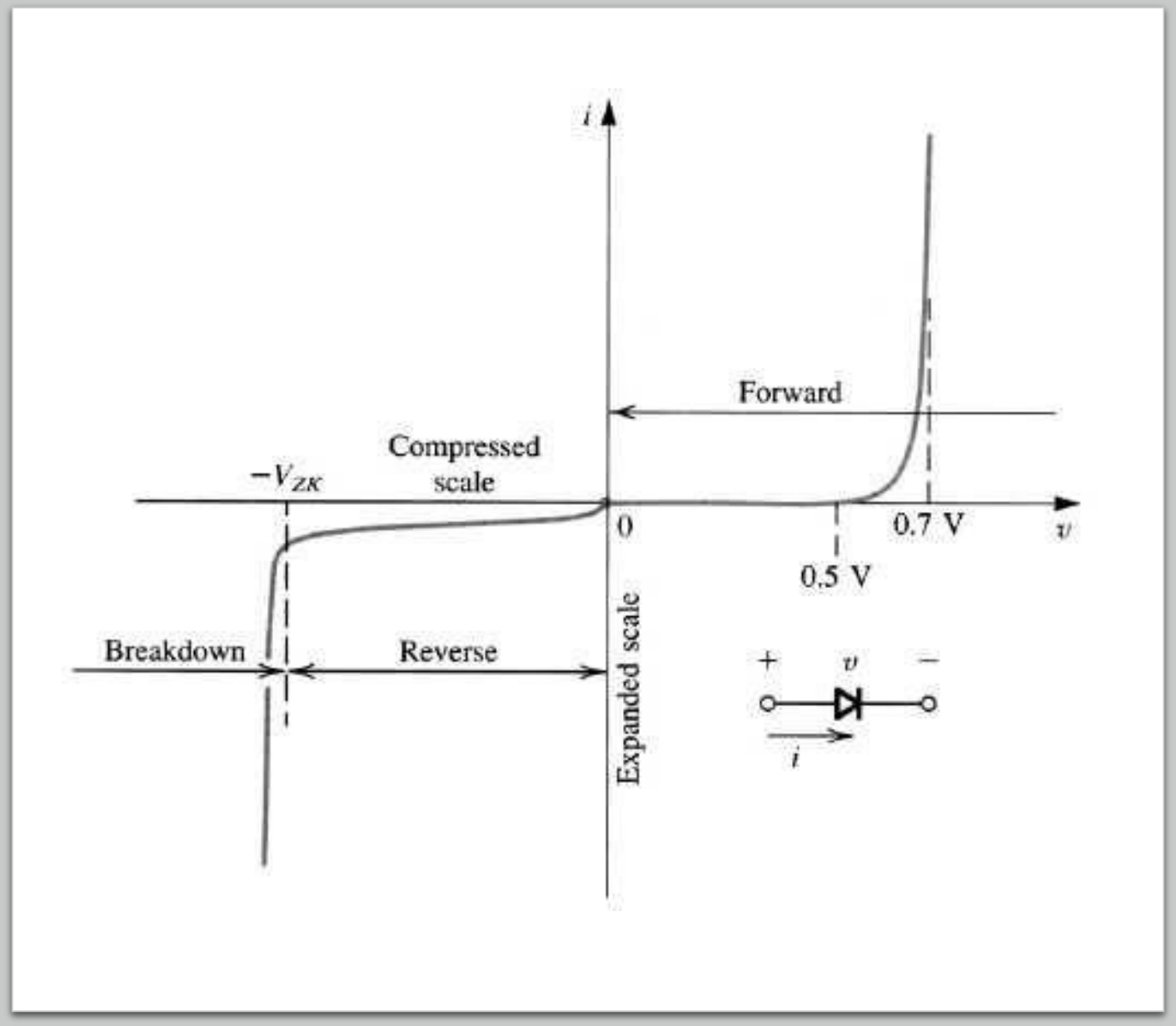
(This voltage values are different for different diodes)



VI Characteristics of a Diode

When Reverse biased:

- A very small amount of current is seen (reverse saturation current/ leakage current)
- Diode depletion region breaks down with a high voltage called breakdown voltage (Vzk)
- Breakdown voltage cause high current to flow in reverse direction and can damage device

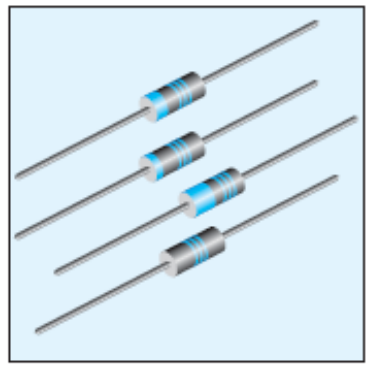


In the Forward Biasing Mode, when the voltage is increased initially we see very minimal increase in current. At a certain voltage, current increases abruptly and massively. This voltage is known as knee voltage and this point on graph is **knee point.**

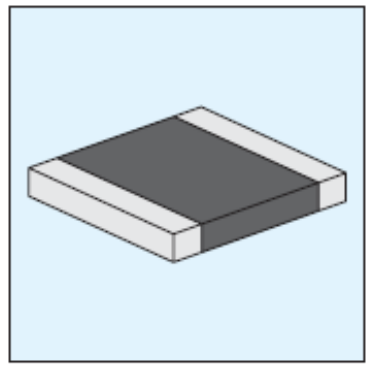
A P-N junction diode acts as a resistor for very low voltages but later acts as a conductor.

The breakdown region is entered when the magnitude of the reverse voltage exceeds a threshold value that is specific to the particular diode, called the **breakdown voltage.** This is the voltage at the “knee” of the *i*–*v* curve in Fig. and is denoted *VZK*

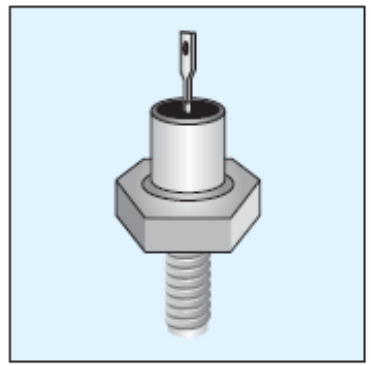
The maximum reverse-bias potential that can be applied before entering the breakdown region is called the **peak inverse voltage** (referred to simply as the PIV rating) or the peak reverse voltage



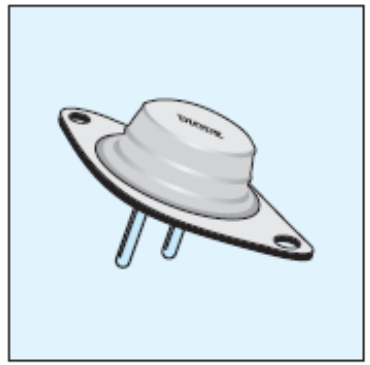
General purpose diode



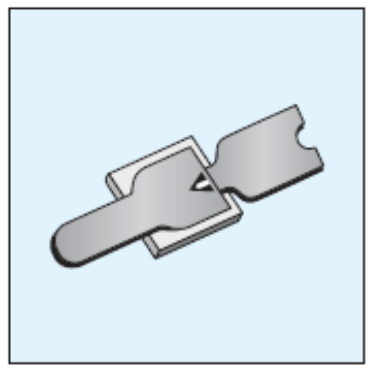
Surface mount high-power PIN diode



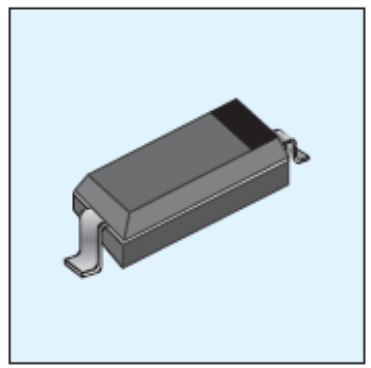
Power (stud) diode



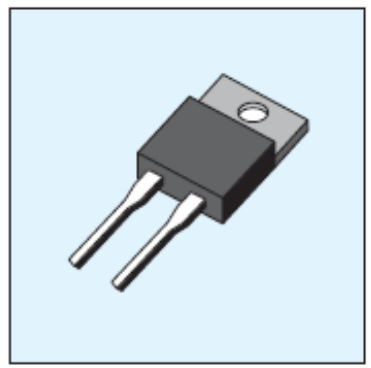
Power (planar) diode



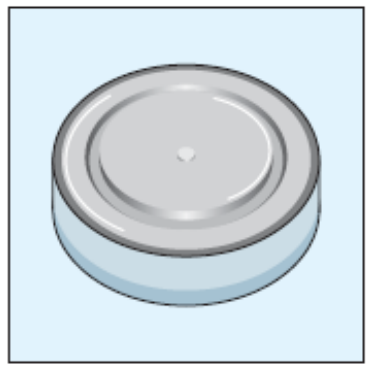
Beam lead pin diode



Flat chip surface mount diode



Power diode



Power (disc, puck) diode

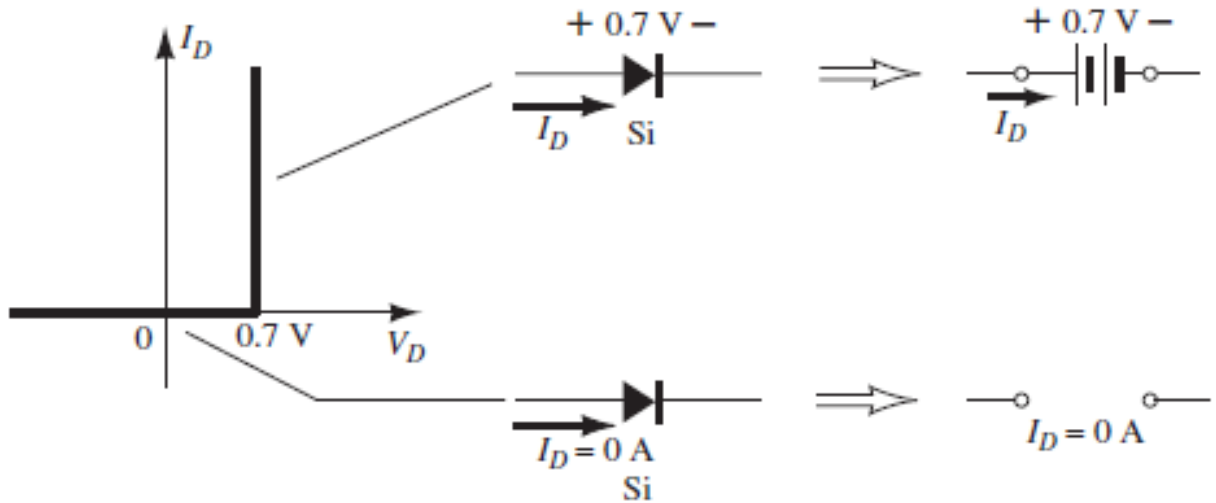
FIG. 1.39

Various types of junction diodes.

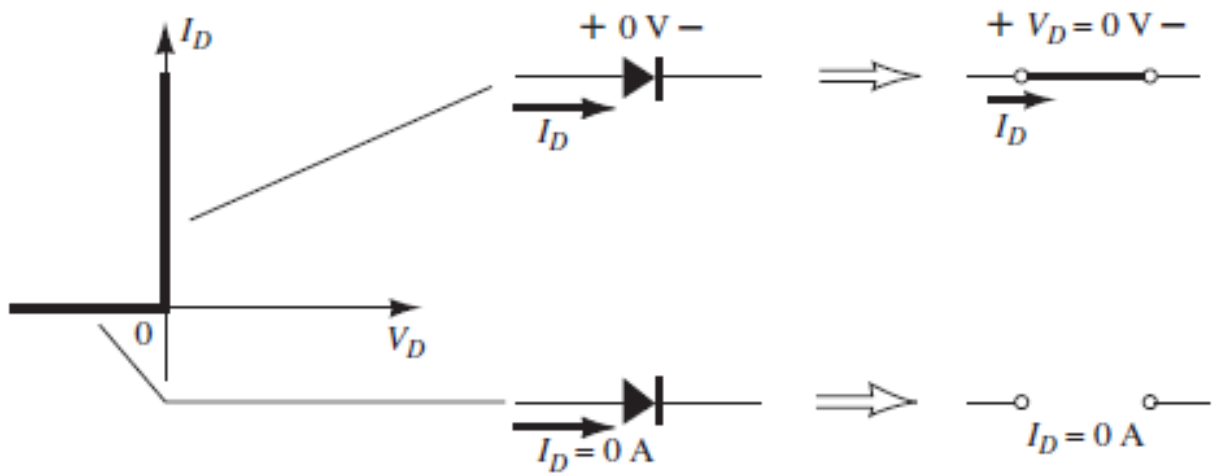
TABLE 2.1

Approximate and Ideal Semiconductor Diode Models.

Silicon:



Ideal:



DIODE EQUIVALENT CIRCUITS

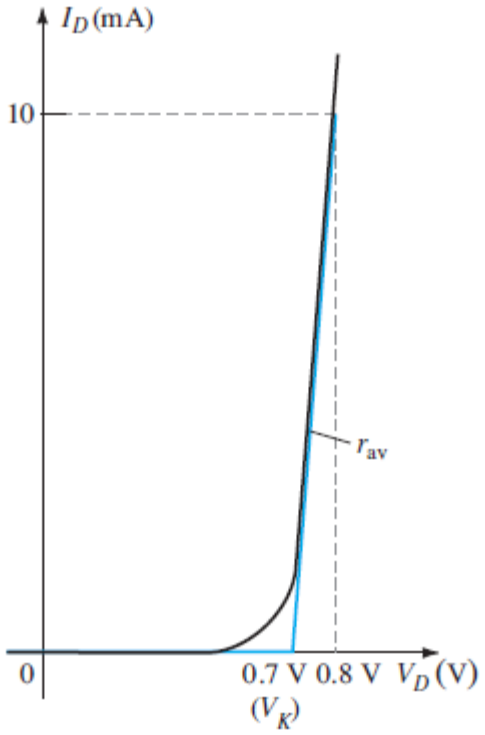
An equivalent circuit is a combination of elements properly chosen to best represent the actual terminal characteristics of a device or system in a particular operating region.

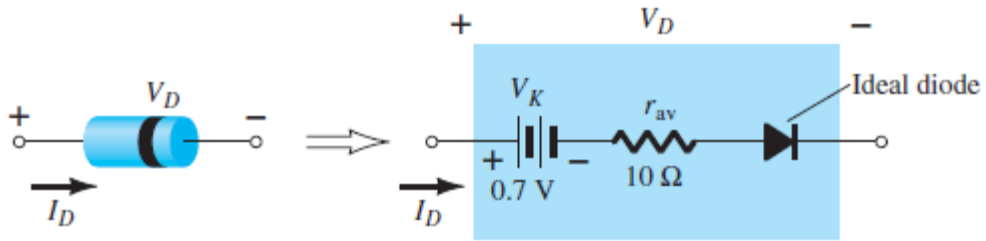
1. Piecewise-Linear Equivalent Circuit
2. Ideal Equivalent Circuit
3. Simplified Equivalent Circuit

Piecewise-Linear Equivalent Circuit

The resulting segments are sufficiently close to the actual curve to establish an equivalent circuit that will provide an excellent first approximation to the actual behavior of the device.

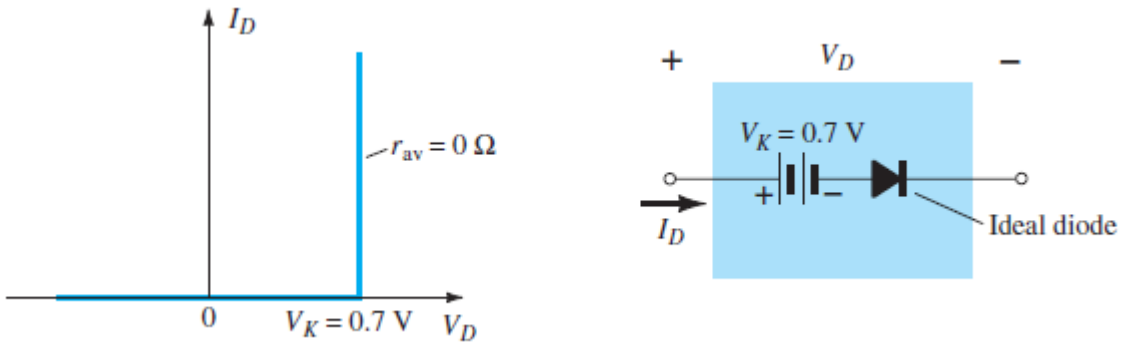
When conduction is established the resistance of the diode will be the specified value of r_{av}





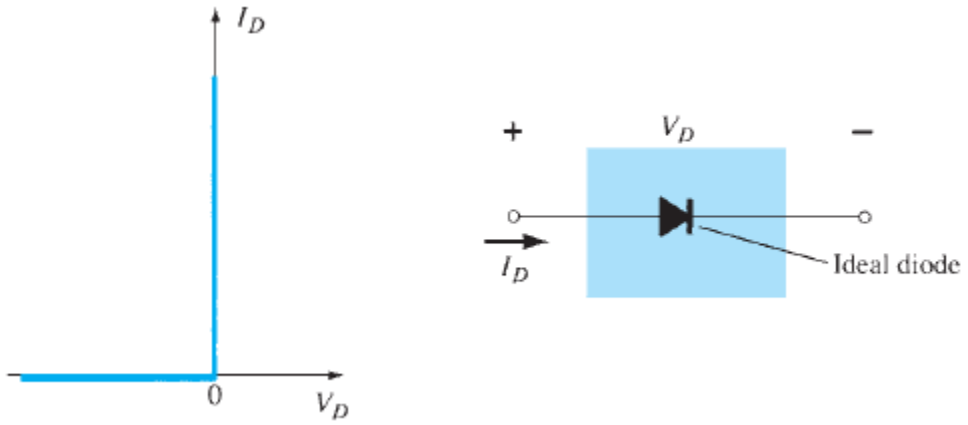
Simplified Equivalent Circuit

The resistance *r* av is sufficiently small to be ignored in comparison to the other elements of the network. It states that a forward biased silicon diode in an electronic system under dc conditions has a drop of 0.7 V across it in the conduction state at any level of diode current



Ideal Equivalent Circuit

Now that *r* av has been removed from the equivalent circuit, let us take the analysis a step further and establish that a 0.7-V level can often be ignored in comparison to the applied voltage level.



SERIES DIODE CONFIGURATIONS

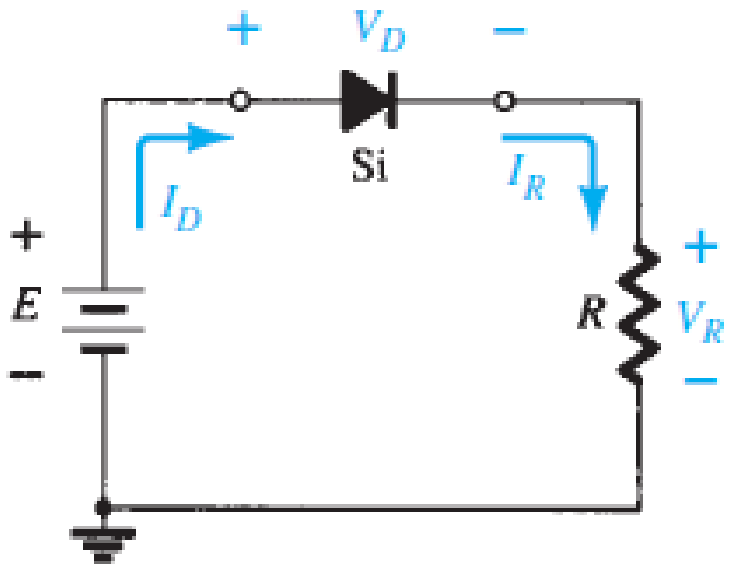
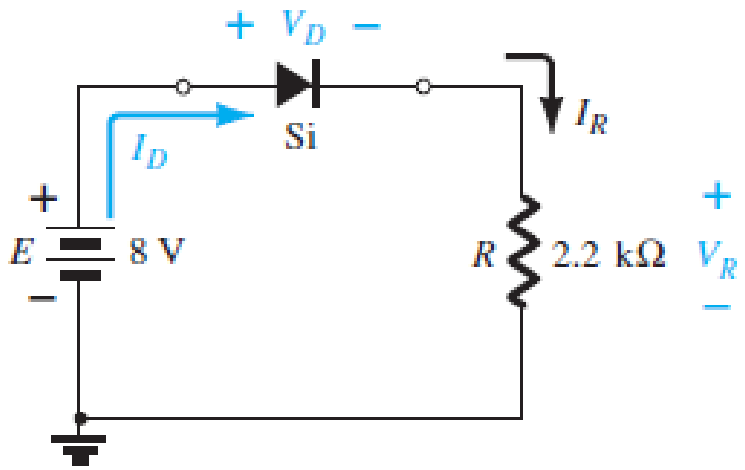


FIG. 2.8

Series diode configuration.

EXAMPLE 2.4 For the series diode configuration of Fig. 2.13, determine V_D, V_R, and I_D.



Solution: Since the applied voltage establishes a current in the clockwise direction to match the arrow of the symbol and the diode is in the "on" state,

$$V_D = \mathbf{0.7\ V}$$

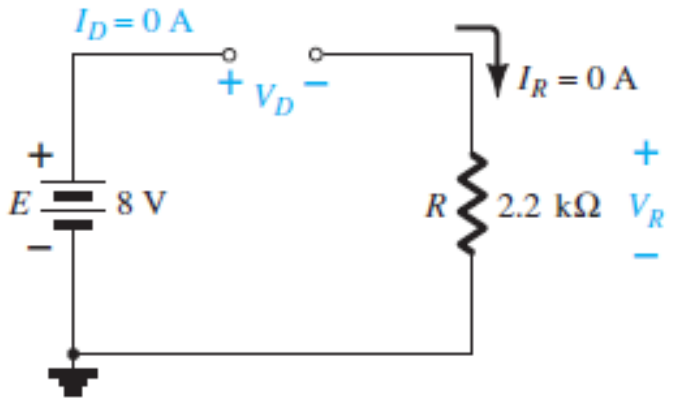
$$V_R = E - V_D = 8\ \text{V} - 0.7\ \text{V} = \mathbf{7.3\ V}$$

$$I_D = I_R = \frac{V_R}{R} = \frac{7.3\ \text{V}}{2.2\ \text{k}\Omega} \cong \mathbf{3.32\ mA}$$

EXAMPLE 2.5 Repeat Example 2.4 with the diode reversed.

Solution: Removing the diode, we find that the direction of I is opposite to the arrow in the diode symbol and the diode equivalent is the open circuit no matter which model is employed. The result is the network of Fig. 2.14, where $I_D = \mathbf{0\ A}$ due to the open circuit. Since $V_R = I_R R$, we have $V_R = (0)R = \mathbf{0\ V}$. Applying Kirchhoff's voltage law around the closed loop yields

$$E - V_D - V_R = 0$$
$$V_D = E - V_R = E - 0 = E = 8\ \text{V}$$



EXAMPLE 2.6 For the series diode configuration of Fig. 2.16, determine V_D, V_R, and I_D.

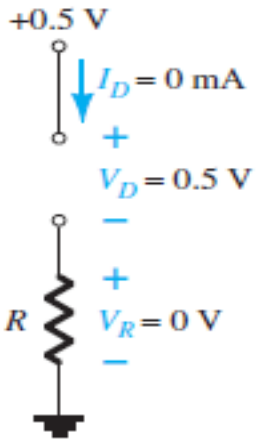
Solution: Although the "pressure" establishes a current with the same direction as the arrow symbol, the level of applied voltage is insufficient to turn the silicon diode "on." The point of operation on the characteristics is shown in Fig. 2.17, establishing the open-circuit equivalent as the appropriate approximation, as shown in Fig. 2.18. The resulting voltage and current levels are therefore the following:

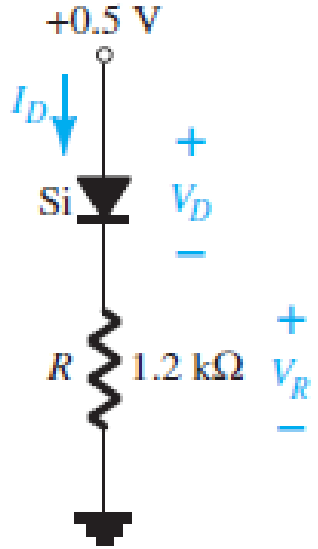
$$I_D = \mathbf{0\ A}$$

$$V_R = I_R R = I_D R = (0\ \text{A})\,1.2\ \text{k}\Omega = \mathbf{0\ V}$$

and

$$V_D = E = \mathbf{0.5\ V}$$





EXAMPLE 2.9 Determine I, V_1, V_2, and V_o for the series dc configuration of Fig. 2.25.

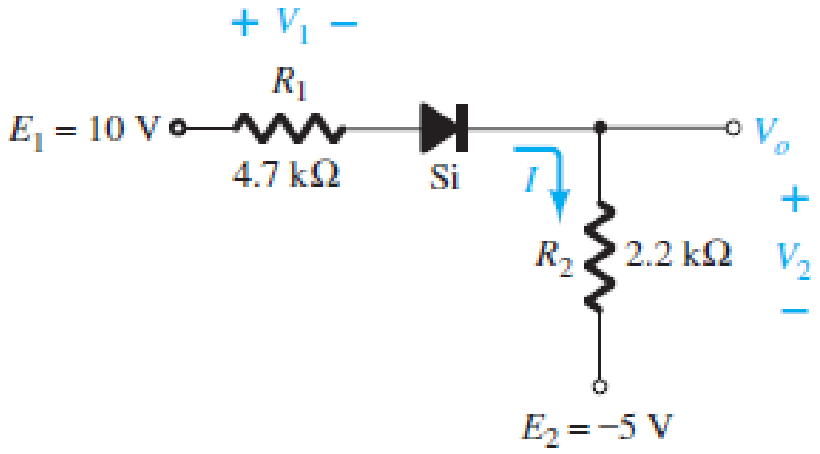
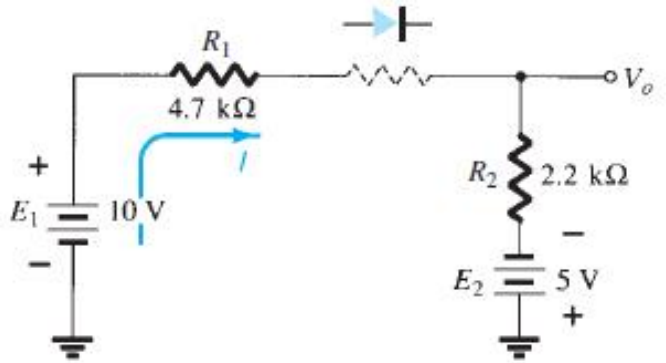
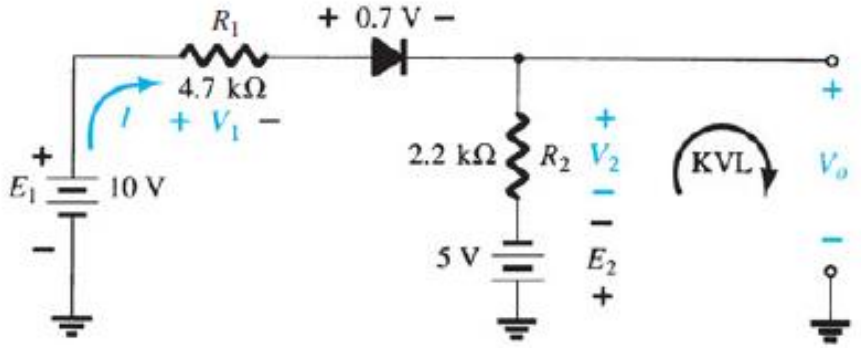


FIG. 2.25

Solve?





PARALLEL AND SERIES–PARALLEL CONFIGURATIONS

EXAMPLE 2.10 Determine V_o, I_1, I_{D_1}, and I_{D_2} for the parallel diode configuration of Fig. 2.28.

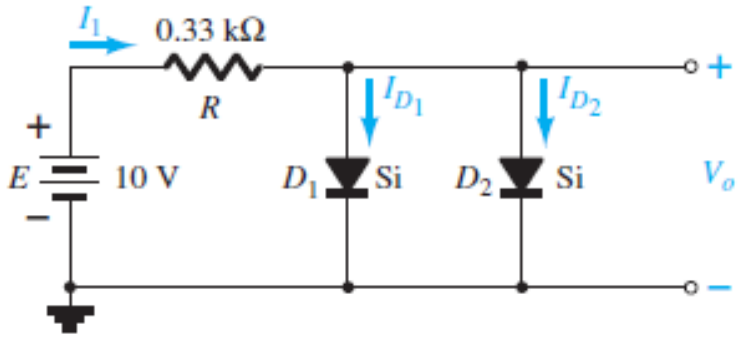


FIG. 2.28

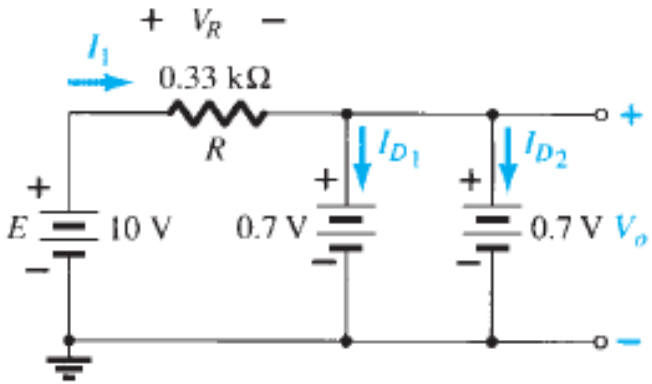


FIG. 2.29

$$V_o = \mathbf{0.7\ V}$$

The current is

$$I_1 = \frac{V_R}{R} = \frac{E - V_D}{R} = \frac{10\ \text{V} - 0.7\ \text{V}}{0.33\ \text{k}\Omega} = \mathbf{28.18\ mA}$$

Assuming diodes of similar characteristics, we have

$$I_{D_1} = I_{D_2} = \frac{I_1}{2} = \frac{28.18\ \text{mA}}{2} = \mathbf{14.09\ mA}$$

Diode Logic Gates

A positive-logic system in which voltage values close to 0 V correspond to logic 0 (or low) and voltage values close to +5 V correspond to logic 1 (or high). Thus *the output will be high if one or more of the inputs are high*. The circuit therefore implements the **logic OR function**, which in Boolean notation is expressed as

$$Y = A + B + C$$

Similarly, the reader is encouraged to show that using the same logic system mentioned above, the circuit of Fig. 4.5(b) implements the **logic AND function**,

$$Y = A \cdot B \cdot C$$

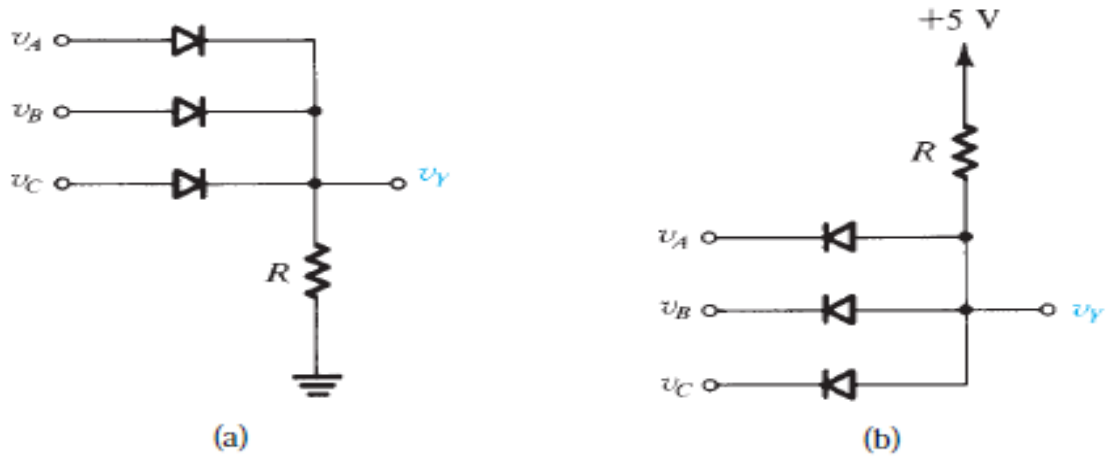
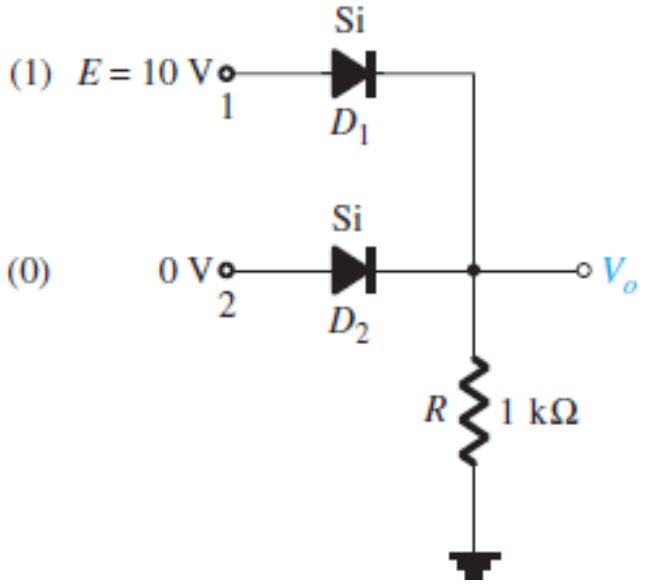
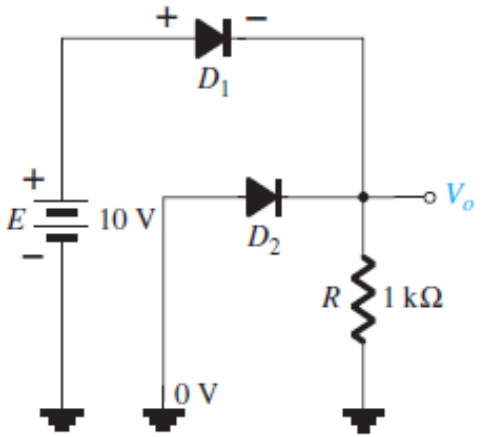


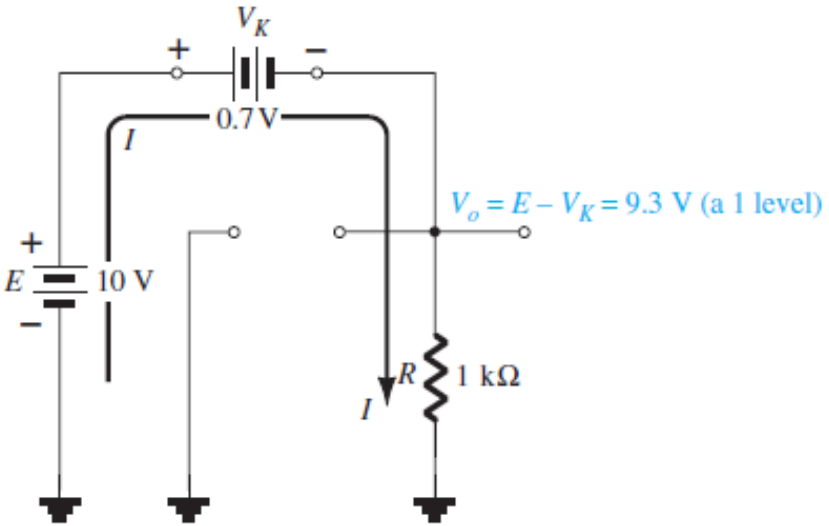
Figure 4.5 Diode logic gates: **(a)** OR gate; **(b)** AND gate (in a positive-logic system).

EXAMPLE 2.14 Determine V_o for the network

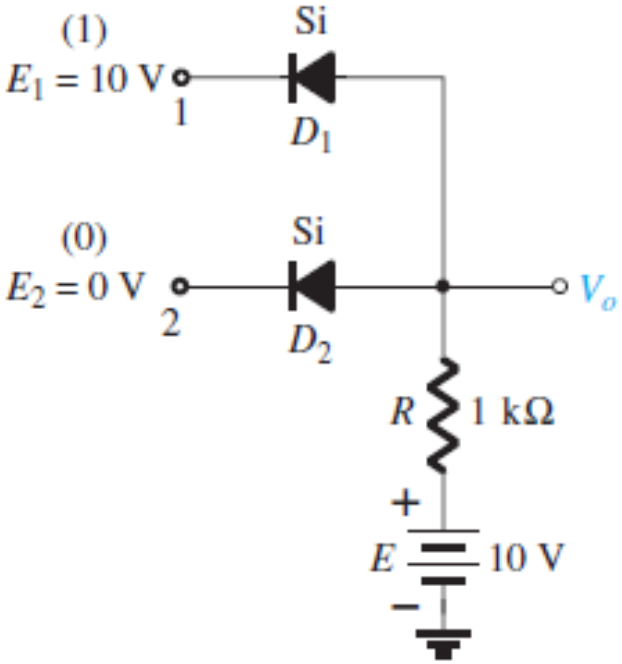


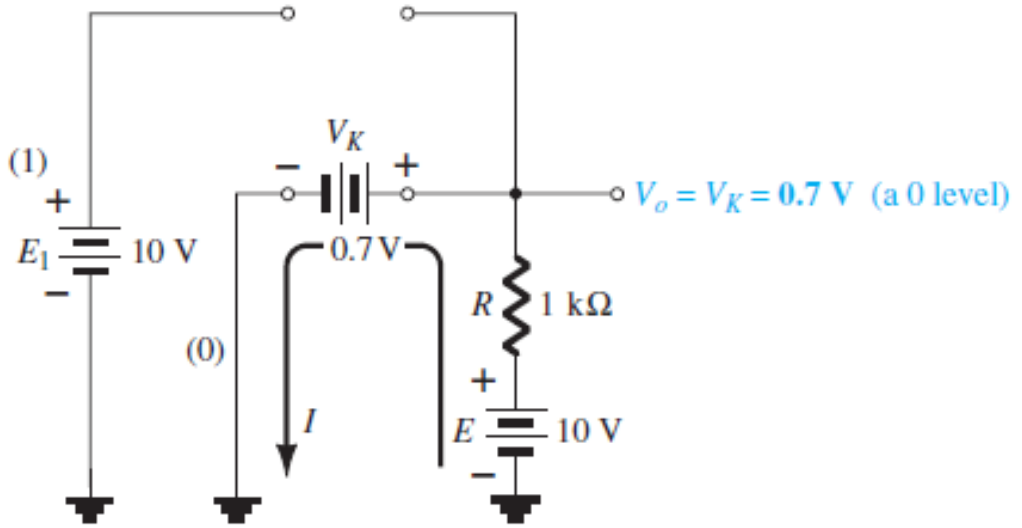
$$I = \frac{E - V_D}{R} = \frac{10\text{ V} - 0.7\text{ V}}{1\text{ k}\Omega} = \mathbf{9.3\text{ mA}}$$





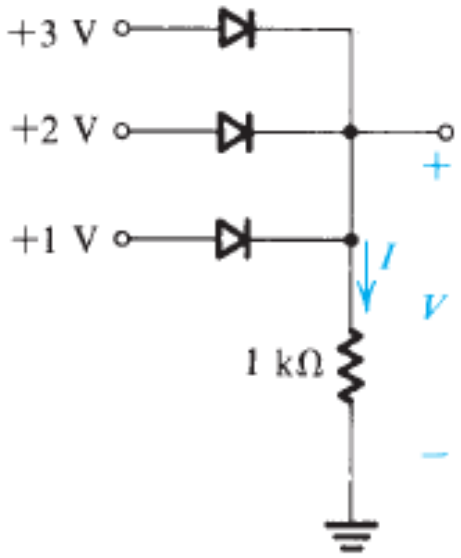
EXAMPLE 2.15 Determine V_o for the network



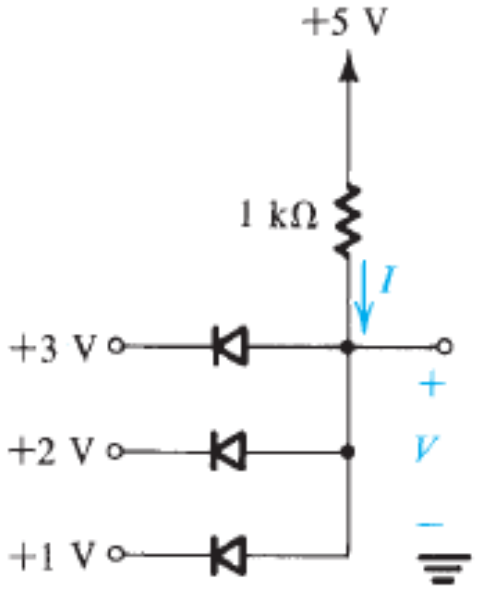


$$I = \frac{E - V_K}{R} = \frac{10\text{ V} - 0.7\text{ V}}{1\text{ k}\Omega} = \mathbf{9.3\text{ mA}}$$

Find the values of I and V in the circuits shown



(e)

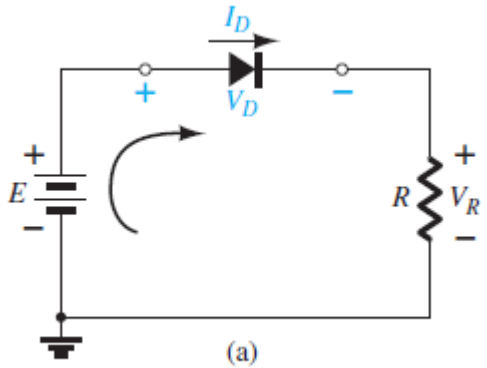


(f)

Solve ?

LOAD-LINE ANALYSIS

It will be used to describe the analysis of a diode circuit using its actual characteristics



(a)

The intersections of the load line on the characteristics of Fig. 2.2 can be determined by first applying Kirchhoff's voltage law in the clockwise direction, which results in

$$+E - V_D - V_R = 0$$

or

$$\boxed{E = V_D + I_D R} \tag{2.1}$$

The two variables of Eq. (2.1), V_D and I_D, are the same as the diode axis variables of Fig. 2.2. This similarity permits plotting Eq. (2.1) on the same characteristics of Fig. 2.2.

The intersections of the load line on the characteristics can easily be determined if one simply employs the fact that anywhere on the horizontal axis $I_D = 0$ A and anywhere on the vertical axis $V_D = 0$ V.

If we *set* $V_D = 0$ V in Eq. (2.1) and solve for I_D, we have the magnitude of I_D *on* the vertical axis. Therefore, with $V_D = 0$ V, Eq. (2.1) becomes

$$\begin{aligned} E &= V_D + I_D R \\ &= 0\,\text{V} + I_D R \end{aligned}$$

and

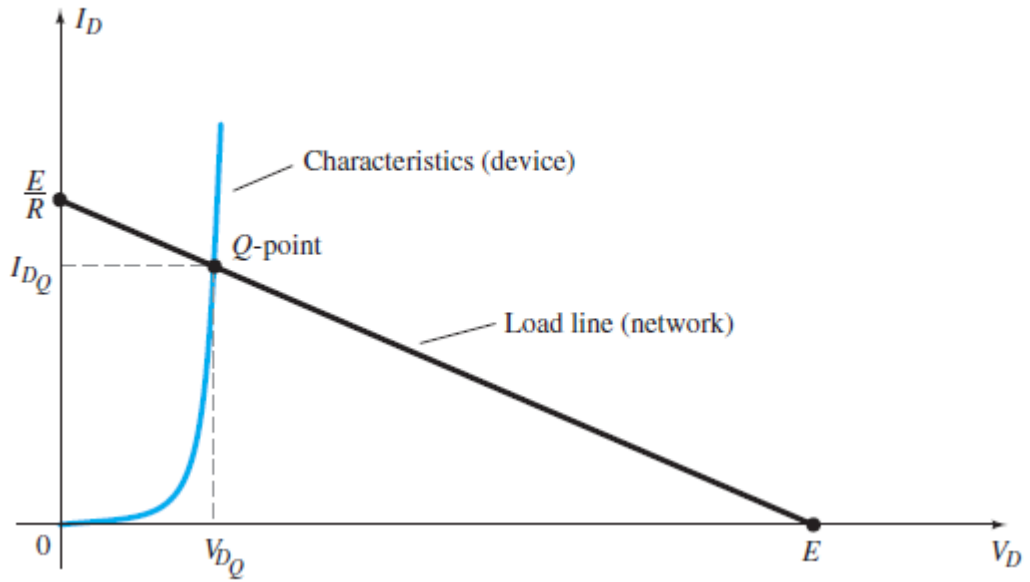
$$\boxed{I_D = \left.\frac{E}{R}\right|_{V_D = 0\,\text{V}}} \tag{2.2}$$

as shown in Fig. 2.2. If we *set* $I_D = 0$ A in Eq. (2.1) and solve for V_D, we have the magnitude of V_D *on* the horizontal axis. Therefore, with $I_D = 0$ A, Eq. (2.1) becomes

$$\begin{aligned} E &= V_D + I_D R \\ &= V_D + (0\,\text{A})R \end{aligned}$$

and

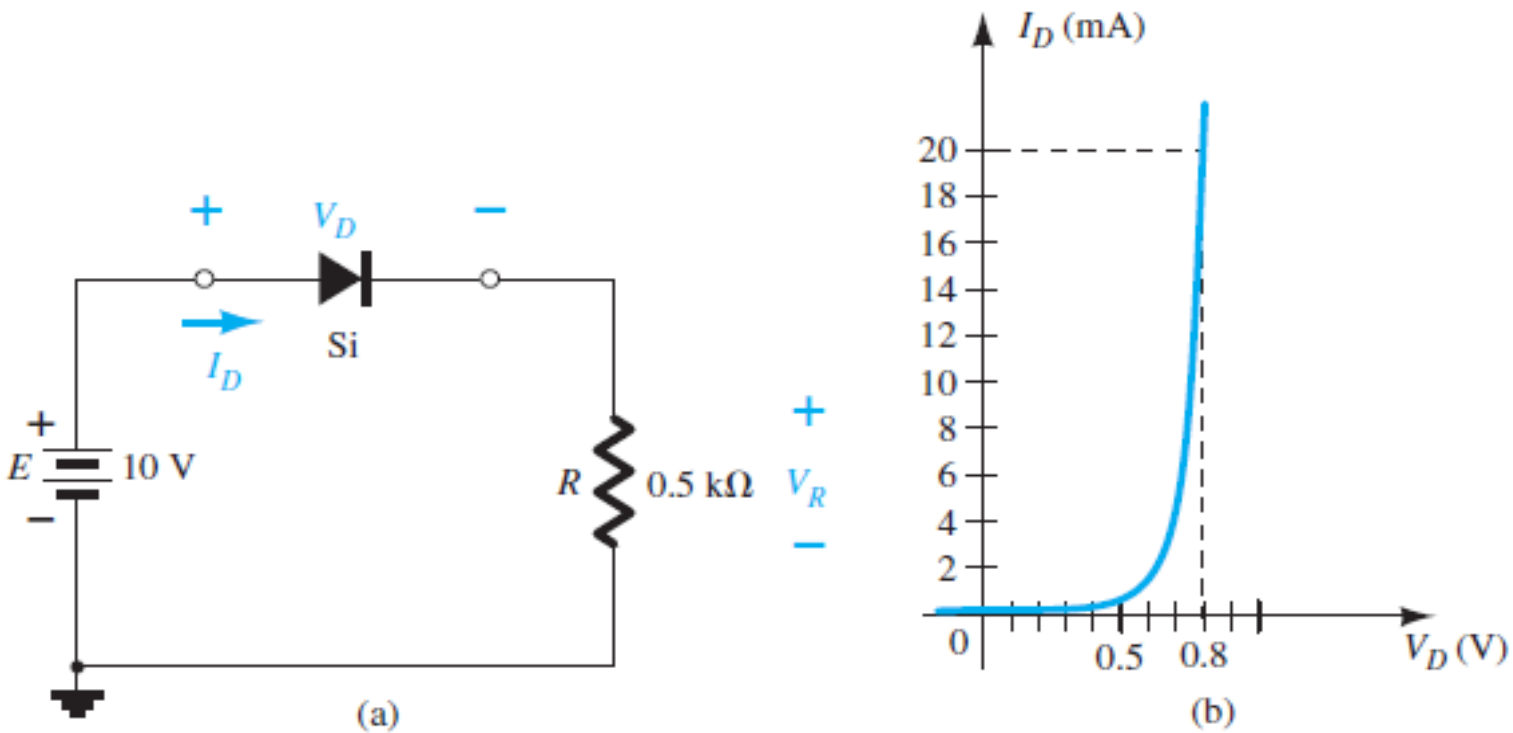
$$\boxed{V_D = E|_{I_D = 0\,\text{A}}} \tag{2.3}$$



Drawing the load line and finding the point of operation.

EXAMPLE 2.1 For the series diode configuration of Fig. 2.3a, employing the diode characteristics of Fig. 2.3b, determine:

a. V_{D_Q} and I_{D_Q}.
b. V_R.



Solution:

a. Eq. (2.2): $$I_D = \frac{E}{R}\Big|_{V_D=0\text{ V}} = \frac{10\text{ V}}{0.5\text{ k}\Omega} = 20\text{ mA}$$

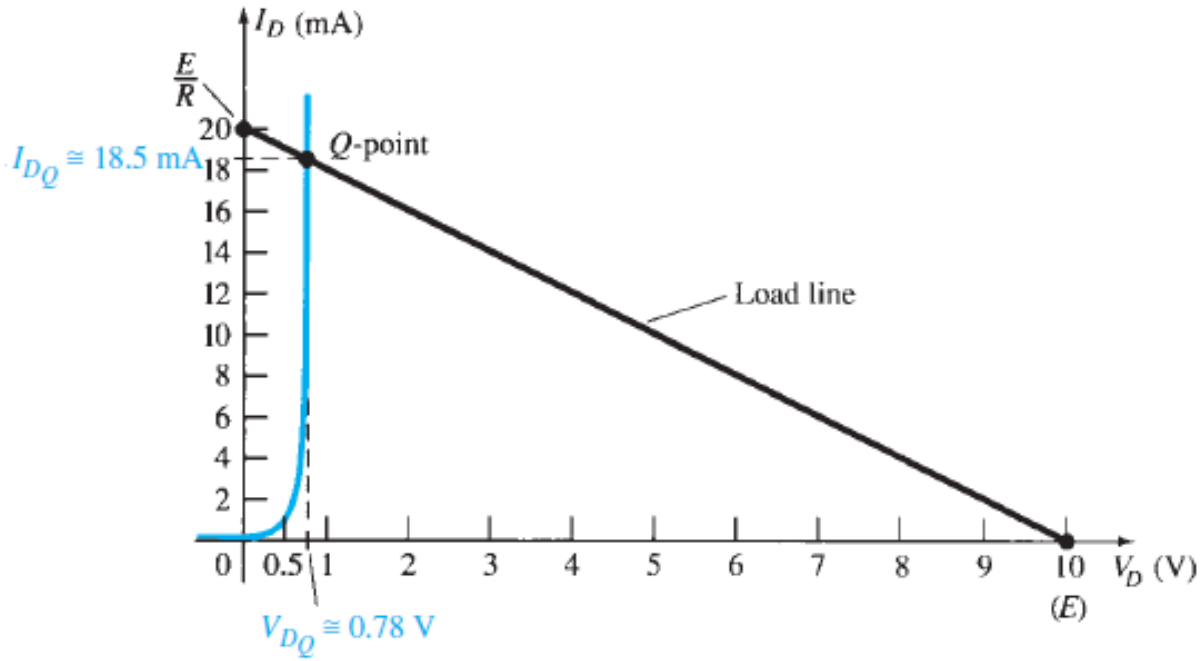
Eq. (2.3): $$V_D = E|_{I_D=0\text{ A}} = 10\text{ V}$$

The resulting load line appears in Fig. 2.4. The intersection between the load line and the characteristic curve defines the Q-point as

$$V_{D_Q} \cong \mathbf{0.78\text{ V}}$$
$$I_{D_Q} \cong \mathbf{18.5\text{ mA}}$$

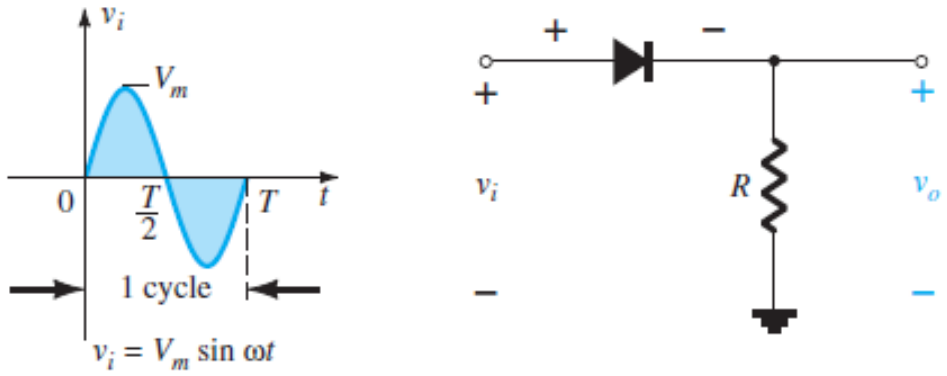
The level of V_D is certainly an estimate, and the accuracy of I_D is limited by the chosen scale. A higher degree of accuracy would require a plot that would be much larger and perhaps unwieldy.

b. $V_R = E - V_D = 10\text{ V} - 0.78\text{ V} = \mathbf{9.22\text{ V}}$

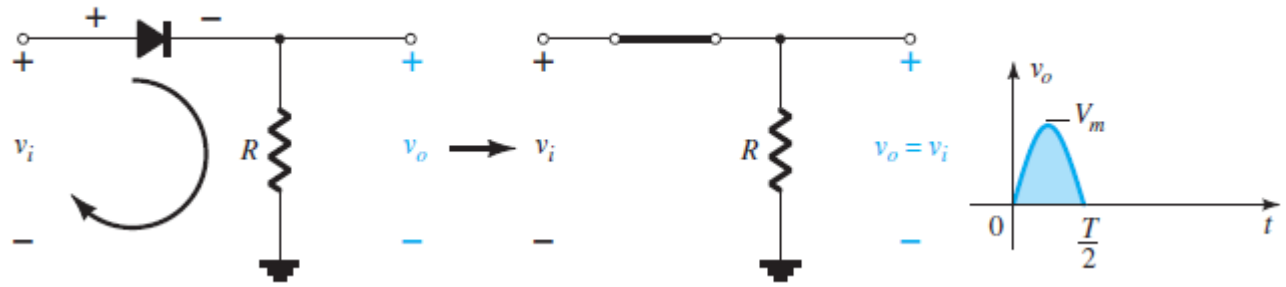


HALF-WAVE RECTIFICATION

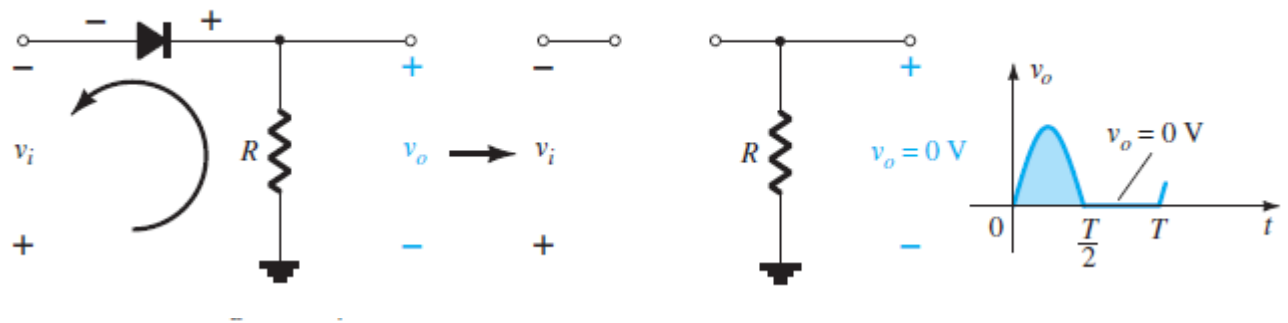
The process of removing one-half the input signal to establish a dc level is called *halfwave rectification*

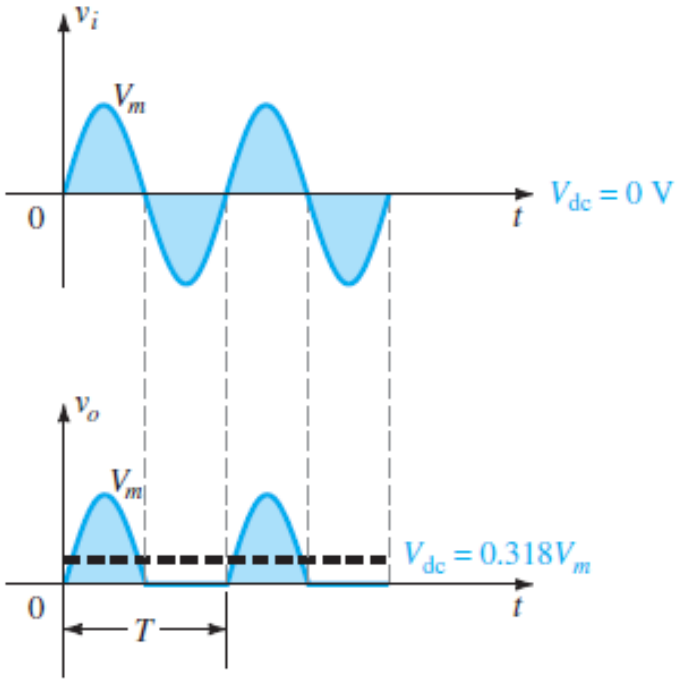


Conduction region (0 to *T/2).*



Conduction region (T/2 to T).





a full period and an average value determined by

$$V_{dc} = 0.318\,V_m$$

half-wave

Self Task

a. Sketch the output v_o and determine the dc level of the output for the network of Fig. 2.49.
b. Repeat part (a) if the ideal diode is replaced by a silicon diode.
c. Repeat parts (a) and (b) if V_m is increased to 200 V, and compare solutions using Eqs. (2.7) and (2.8).

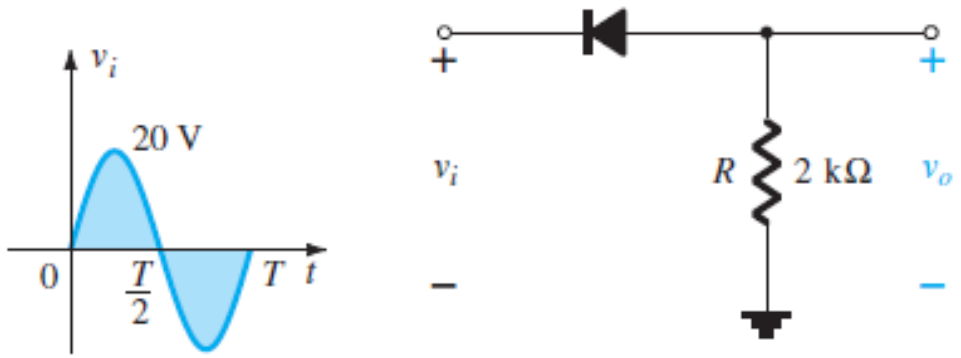


FIG. 2.49

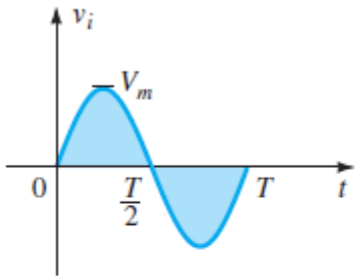
FULL-WAVE RECTIFICATION

The dc level obtained from a sinusoidal input can be improved 100% using a process called *full-wave rectification*

1.Bridge Network
2.Center-Tapped Transformer

Bridge Network

.



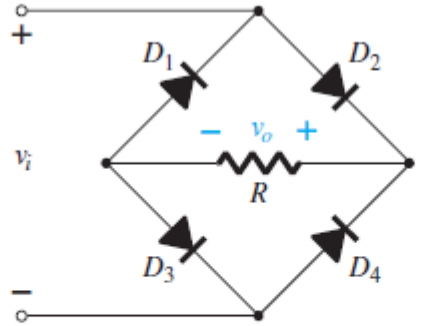


FIG. 2.53
Full-wave bridge rectifier.

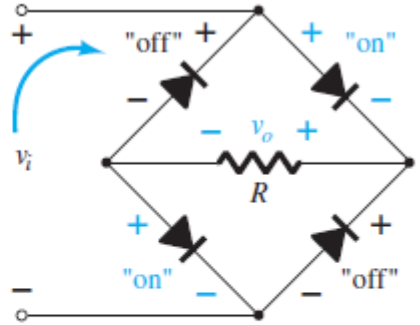
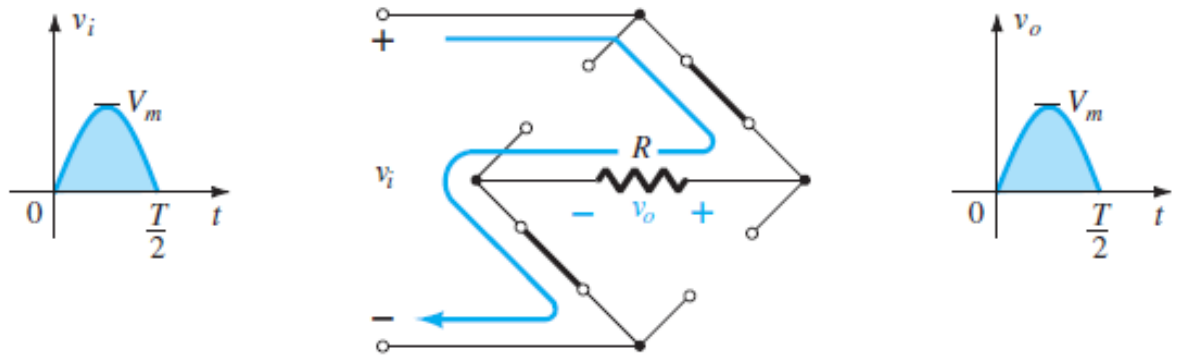
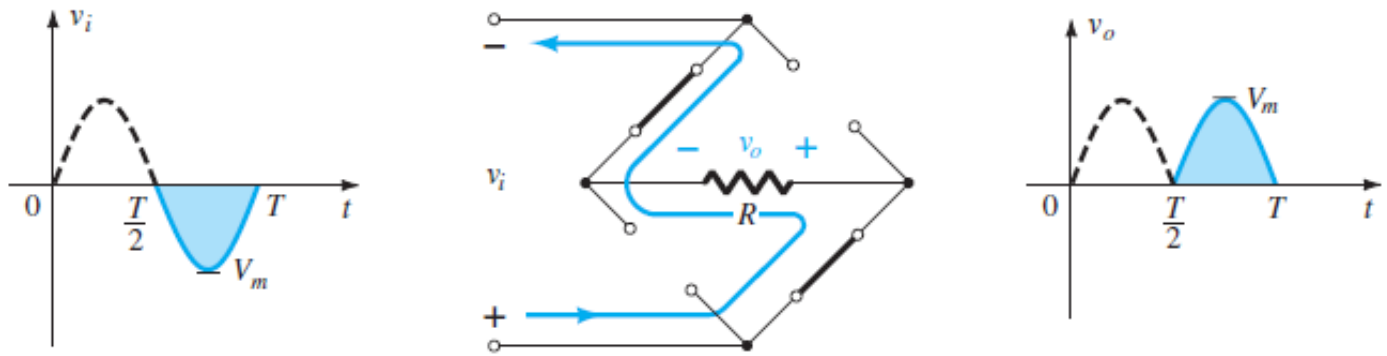


FIG. 2.54
Network of Fig. 2.53 for the period $0 \rightarrow T/2$ of the input voltage v_i.

D_2 and D_3 are conducting, whereas D_1 and D_4 are in the “off” state.



For the negative region of the input the conducting diodes are D_1 and D_4



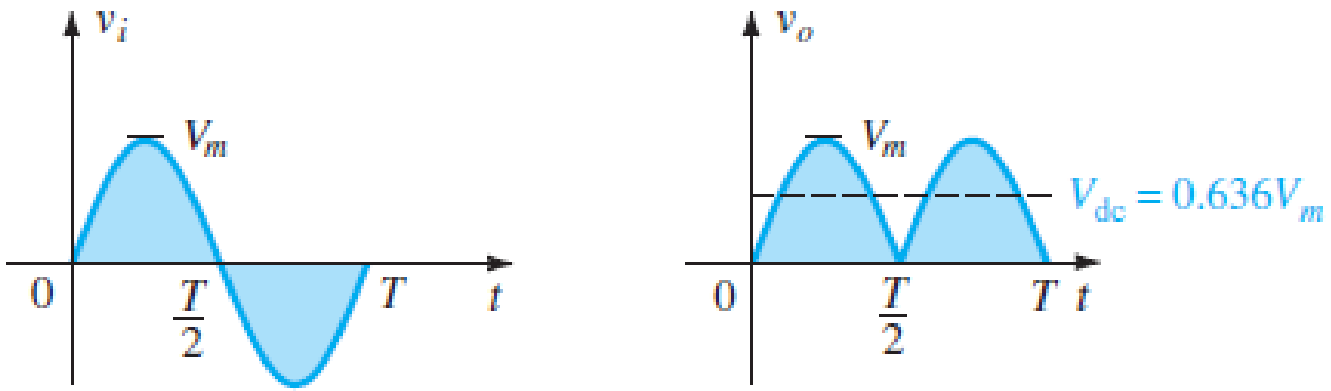


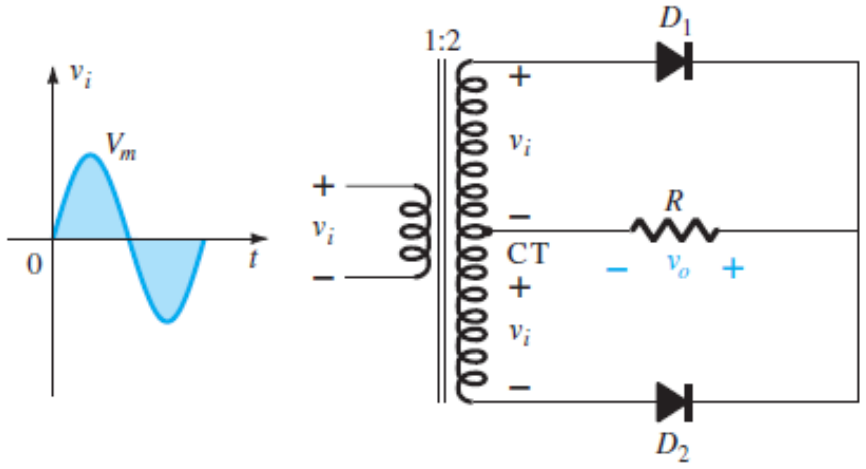
FIG. 2.57

Input and output waveforms for a full-wave rectifier.

$$V_{dc} = 0.636\,V_m$$ full-wave

Center-Tapped Transformer

A second popular full-wave rectifier appears in Fig. 2.60 with only two diodes but requiring a center-tapped (CT) transformer to establish the input signal across each section of the secondary of the transformer.



with a positive pulse across each section of the secondary coil. D_1 assumes the short-circuit equivalent and D_2 the open-circuit equivalent

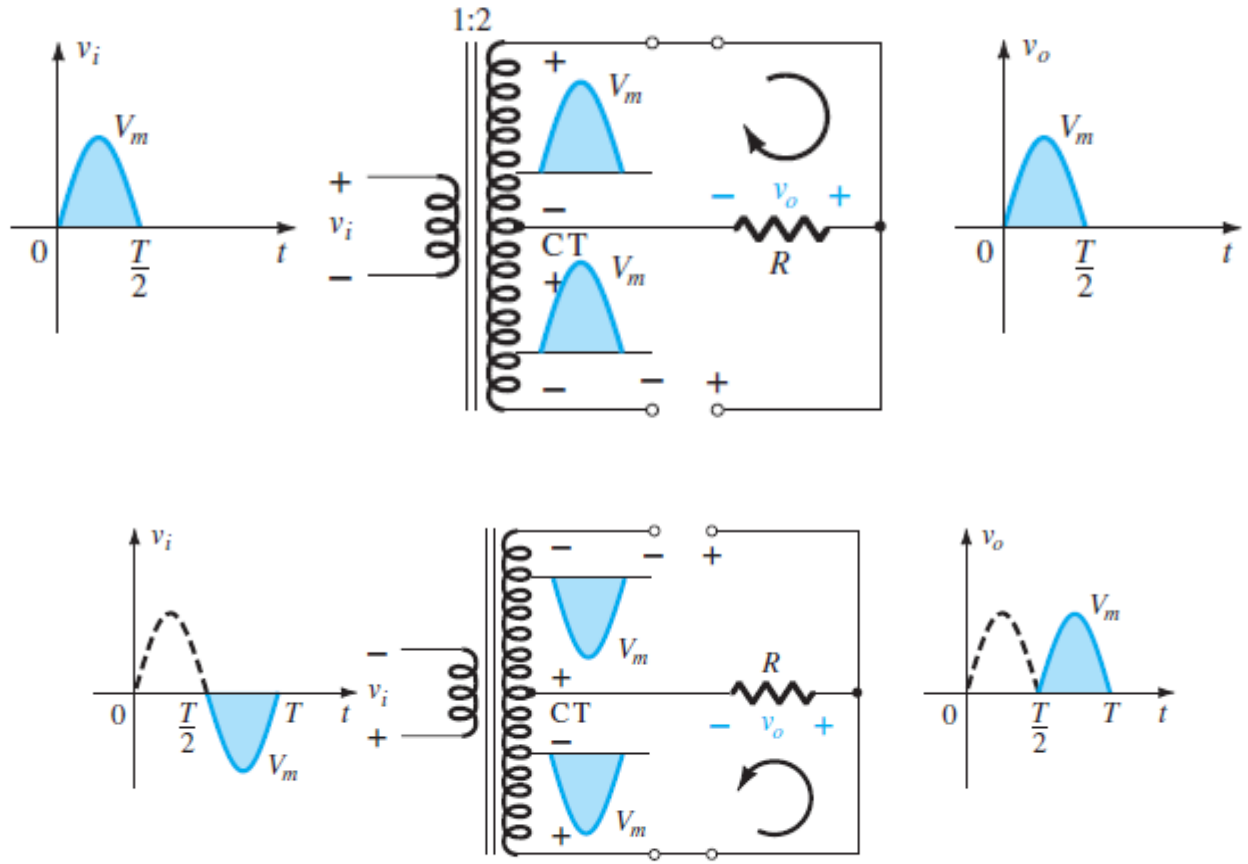


FIG. 2.62
Network conditions for the negative region of v_i.

EXAMPLE 2.17 Determine the output waveform for the network of Fig. 2.64 and calculate the output dc level and the required PIV of each diode.

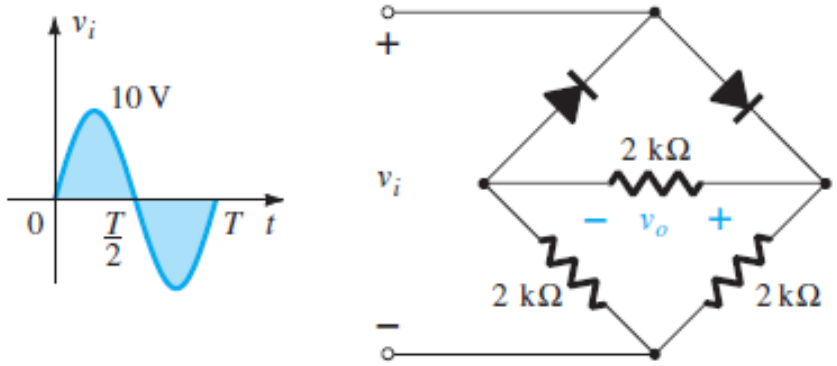


FIG. 2.64
Bridge network for Example 2.17.

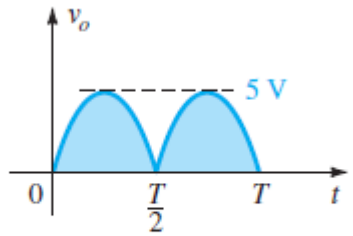
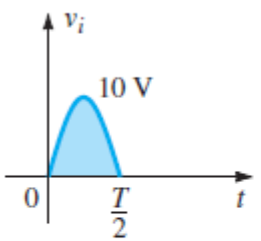


FIG. 2.67
Resulting output for Example 2.17.



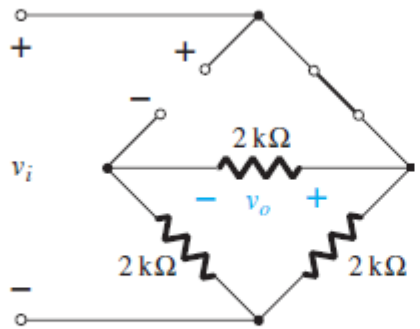


FIG. 2.65
Network of Fig. 2.64 for the positive region of v_i.

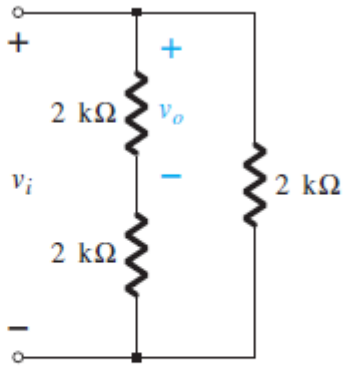
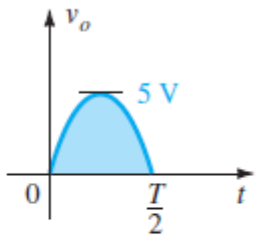


FIG. 2.66
Redrawn network of Fig. 2.65.



$V_{dc} = 0.636(5\text{ V}) = \mathbf{3.18\text{ V}}$

CLAMPERS

A clamper is a network constructed of a diode, a resistor, and a capacitor that shifts a waveform to a different dc level without changing the appearance of the applied signal.

Clamping networks have a capacitor connected directly from input to output with a resistive element in parallel with the output signal. The diode is also in parallel with the output signal but may or may not have a series dc supply as an added element.

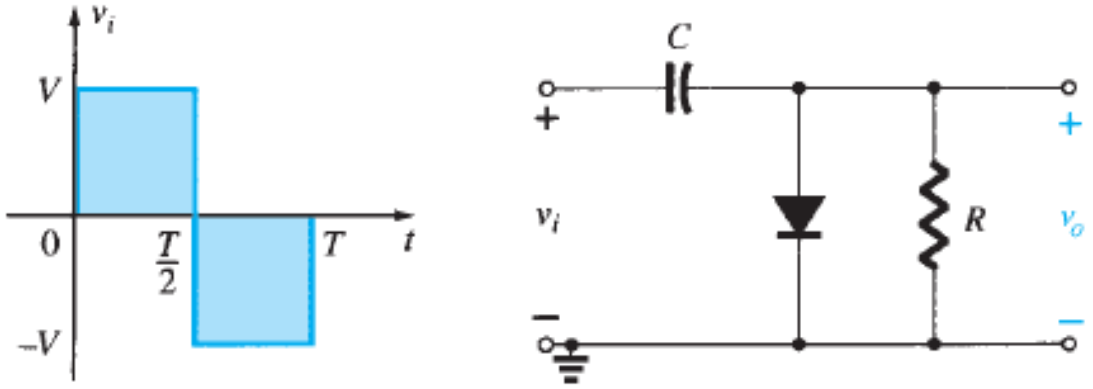


FIG. 2.89
Clamper.

Mainly 2 types :-

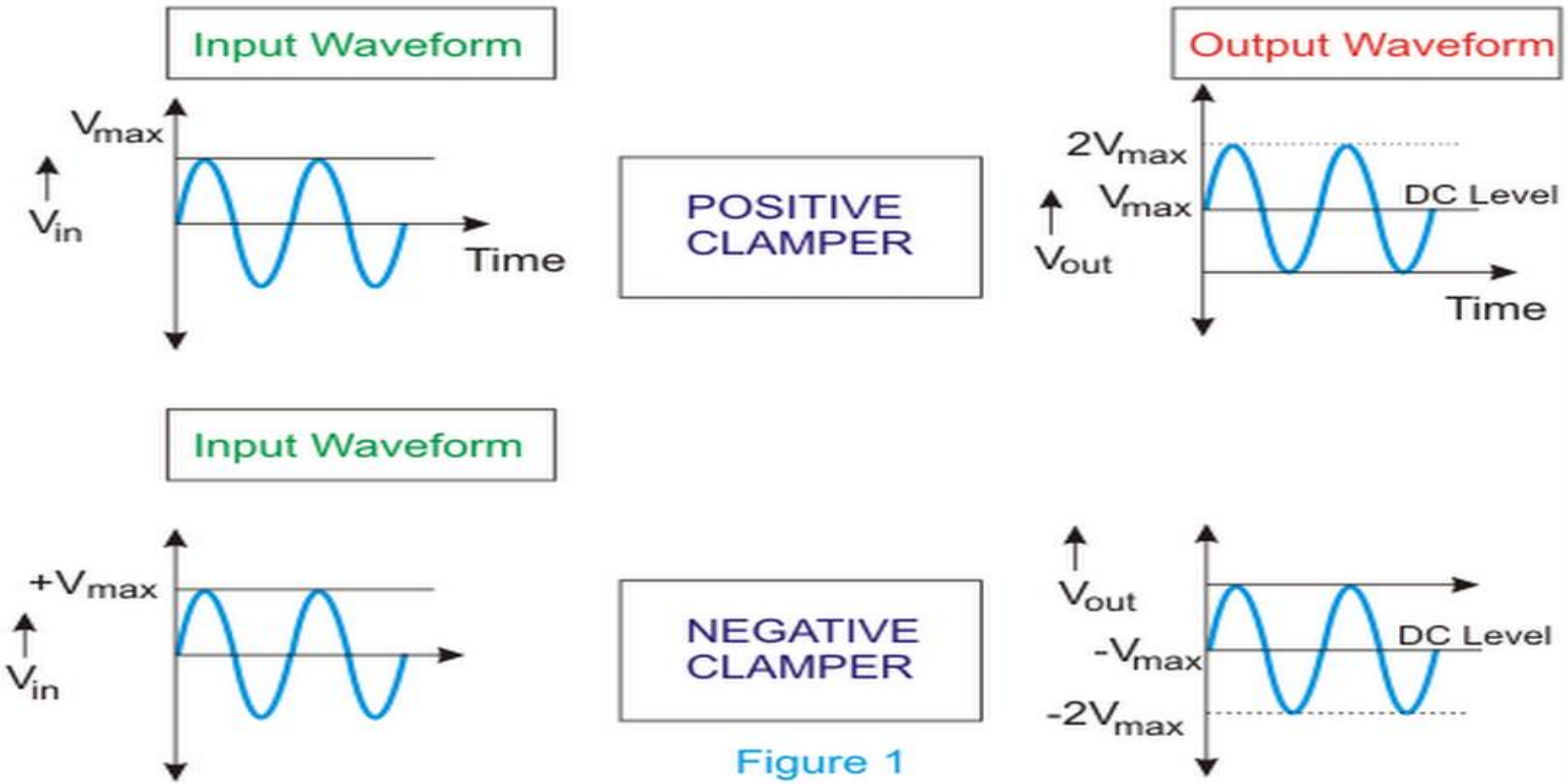


Figure 1

EXAMPLE 2.22 Determine v_o for the network of Fig. 2.93 for the input indicated.

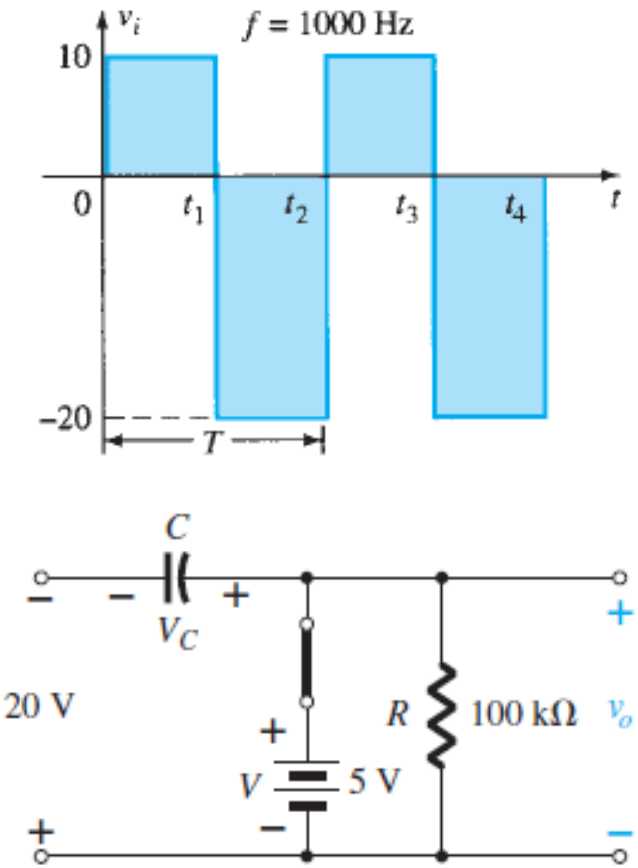
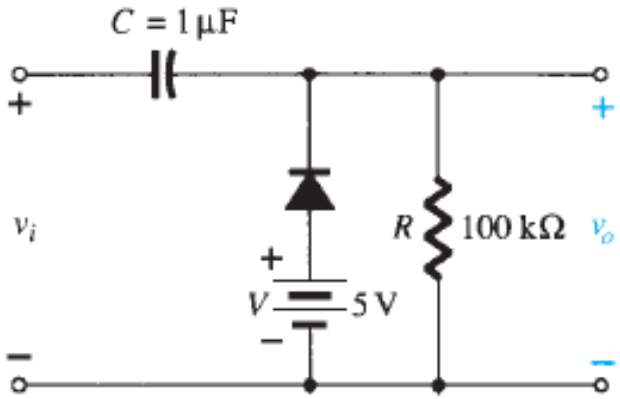


FIG. 2.94
Determining v_o and V_C with the diode in the "on" state.



$$v_o = 5 \text{ V}$$

$$-20 \text{ V} + V_C - 5 \text{ V} = 0$$

$$V_C = 25 \text{ V}$$

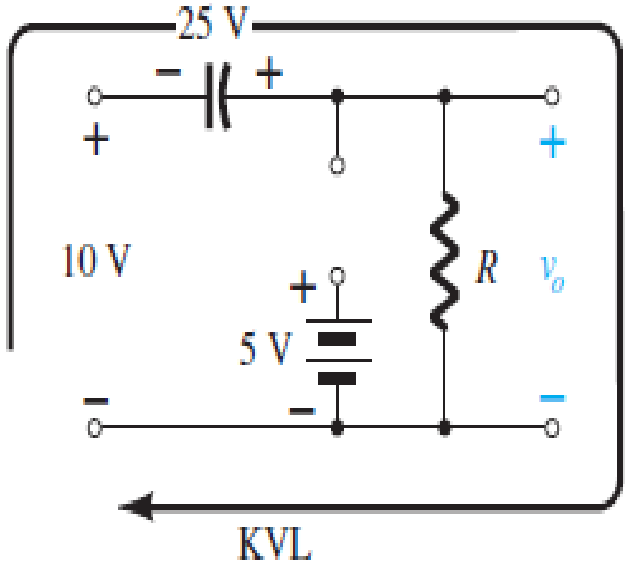
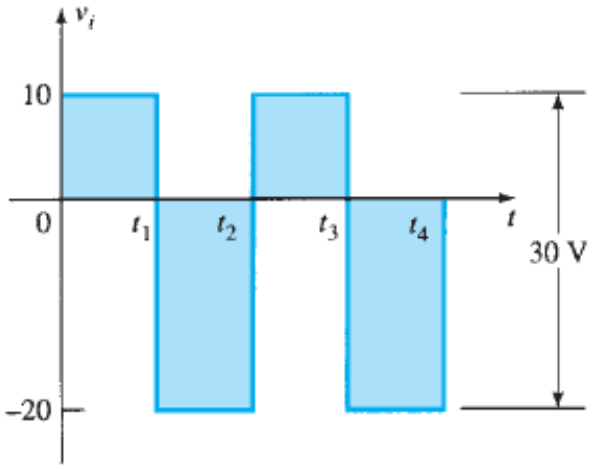


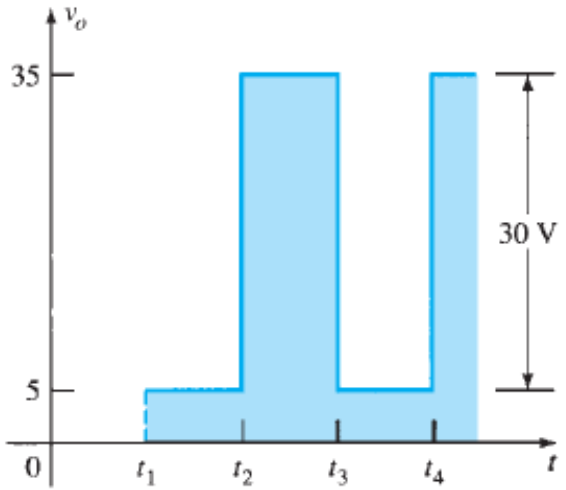
FIG. 2.95

Determining v_o with the diode in the "off" state.

$$+10\text{ V} + 25\text{ V} - v_o = 0$$

$$v_o = 35\text{ V}$$





EXAMPLE 2.23 Repeat Example 2.22 using a silicon diode with $V_K = 0.7$ V.

Solution: For the short-circuit state the network now takes on the appearance of Fig. 2.97, and v_o can be determined by Kirchhoff's voltage law in the output section:

$$+5\text{ V} - 0.7\text{ V} - v_o = 0$$

and

$$v_o = 5\text{ V} - 0.7\text{ V} = 4.3\text{ V}$$

For the input section Kirchhoff's voltage law results in

$$-20\text{ V} + V_C + 0.7\text{ V} - 5\text{ V} = 0$$

and

$$V_C = 25\text{ V} - 0.7\text{ V} = 24.3\text{ V}$$

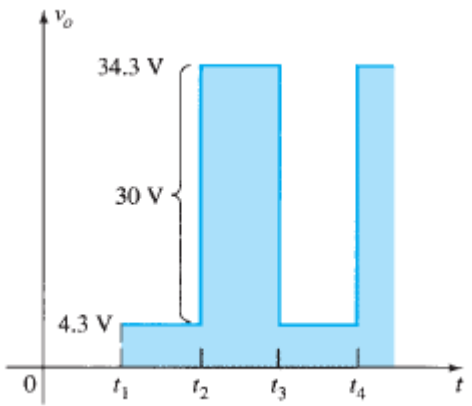
For the period $t_2 \rightarrow t_3$ the network will now appear as in Fig. 2.98, with the only change being the voltage across the capacitor. Applying Kirchhoff's voltage law yields

$$+10\text{ V} + 24.3\text{ V} - v_o = 0$$

and

$$v_o = 34.3\text{ V}$$

The resulting output appears in Fig. 2.99, verifying the statement that the input and output swings are the same.



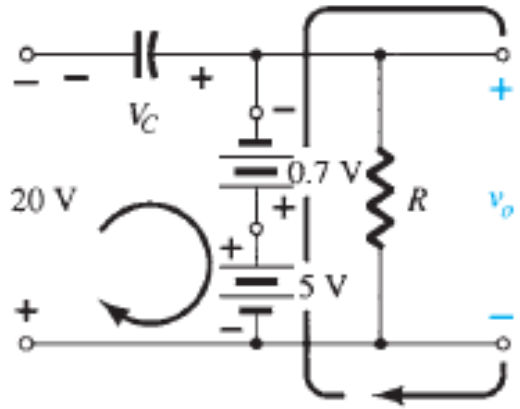


FIG. 2.97
Determining v_o and V_C with the diode in the "on" state.

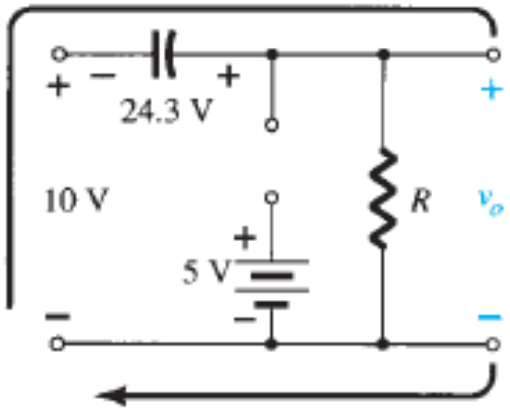
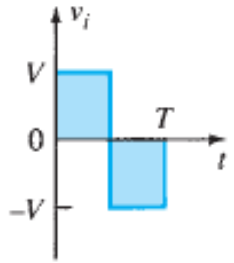
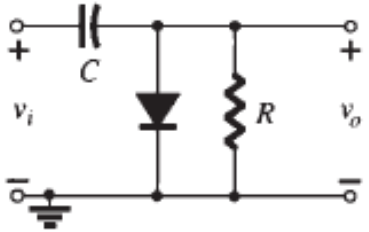
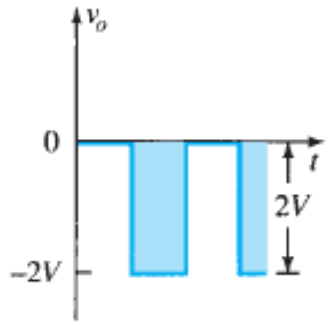


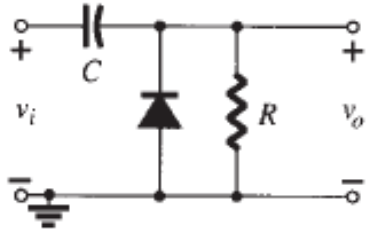
FIG. 2.98
Determining v_o with the diode in the open state.

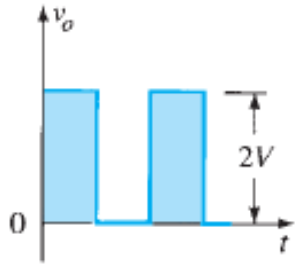
Clamping Networks

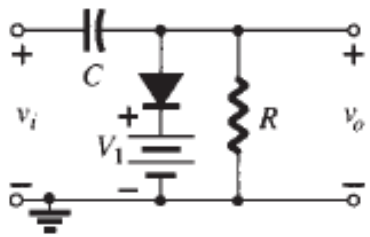


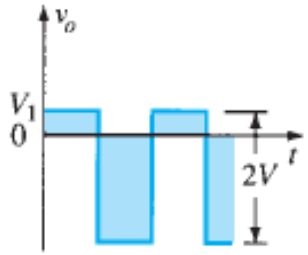


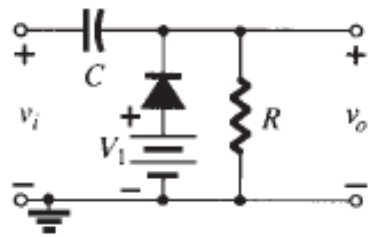


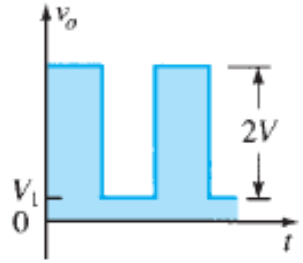


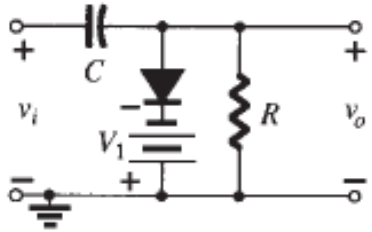


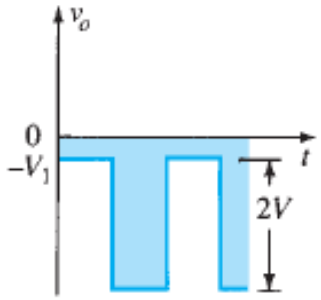


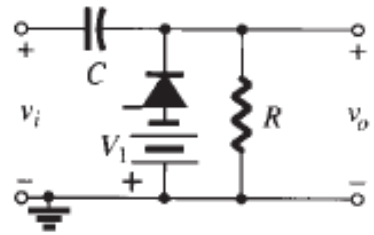


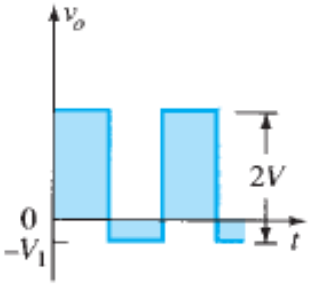












CLIPPERS

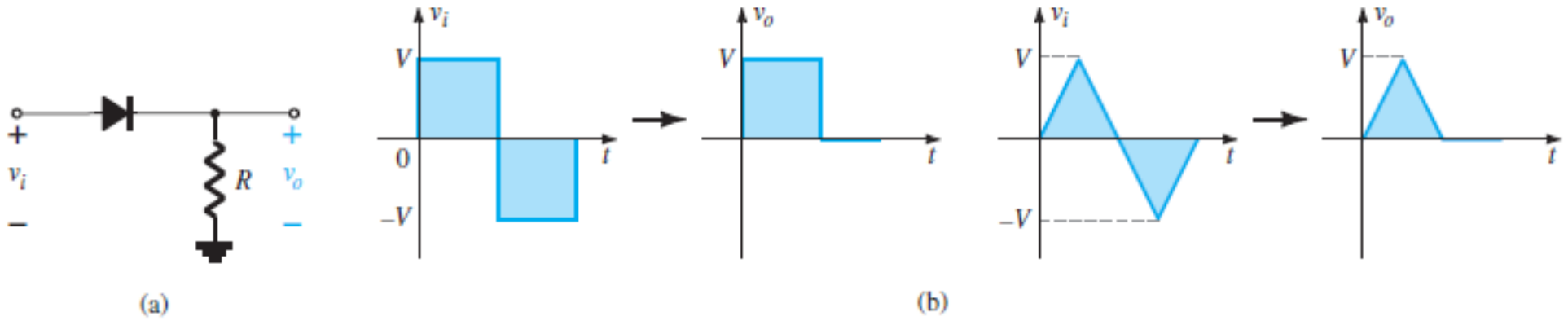
Clippers are networks that employ diodes to “clip” away a portion of an input signal without distorting the remaining part of the applied waveform.

There are two general categories of clippers:

1.*series*

2. *parallel.*

Series clipper.



Parallel clipper

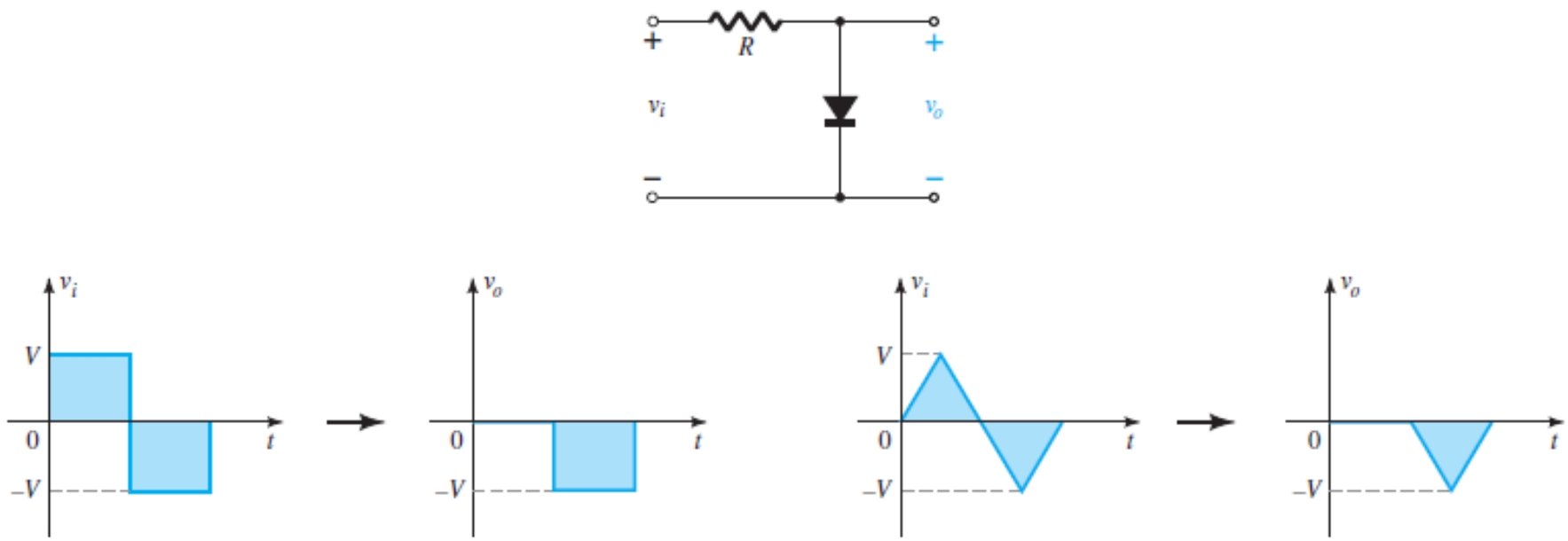
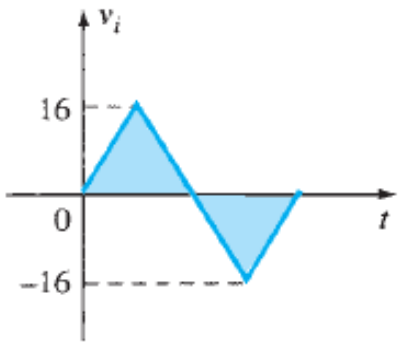


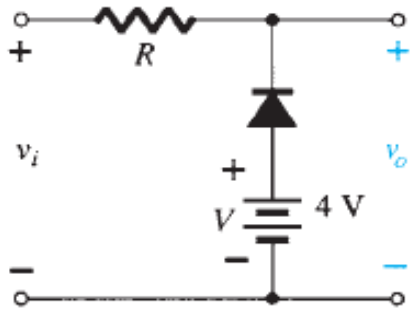
FIG. 2.81
Response to a parallel clipper.

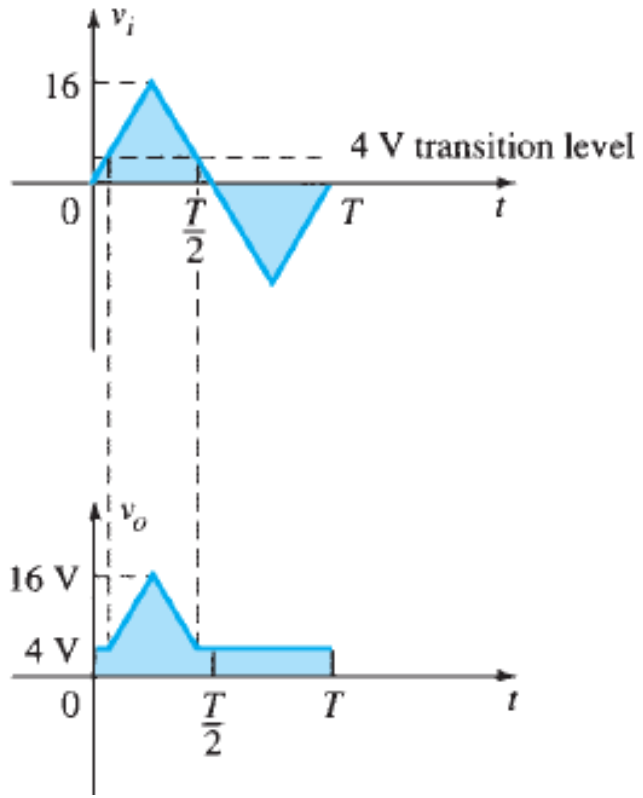
EXAMPLE 2.20 Determine v_o for the network of Fig. 2.82.

Solution:

Step 1: In this example the output is defined across the series combination of the 4-V supply and the diode, not across the resistor R.

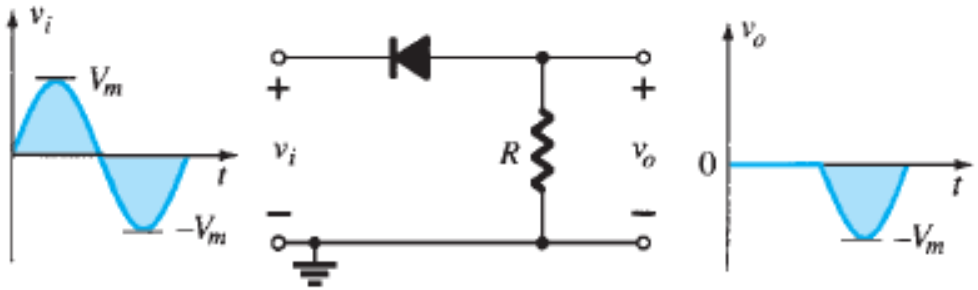




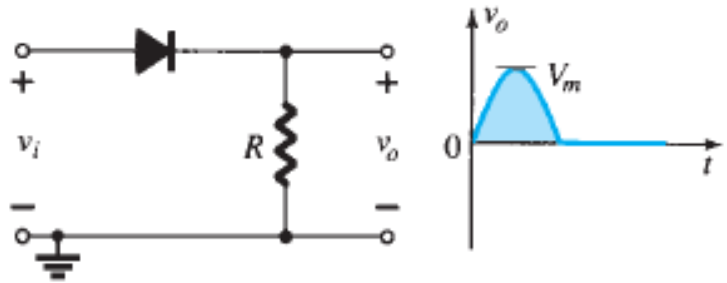


Simple Series Clippers (Ideal Diodes)

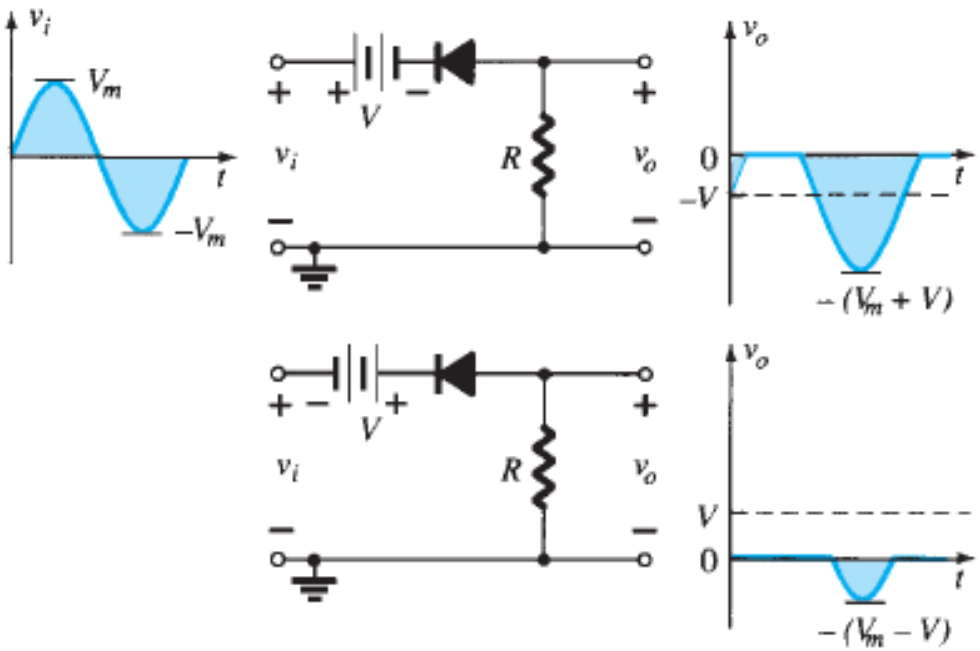
POSITIVE

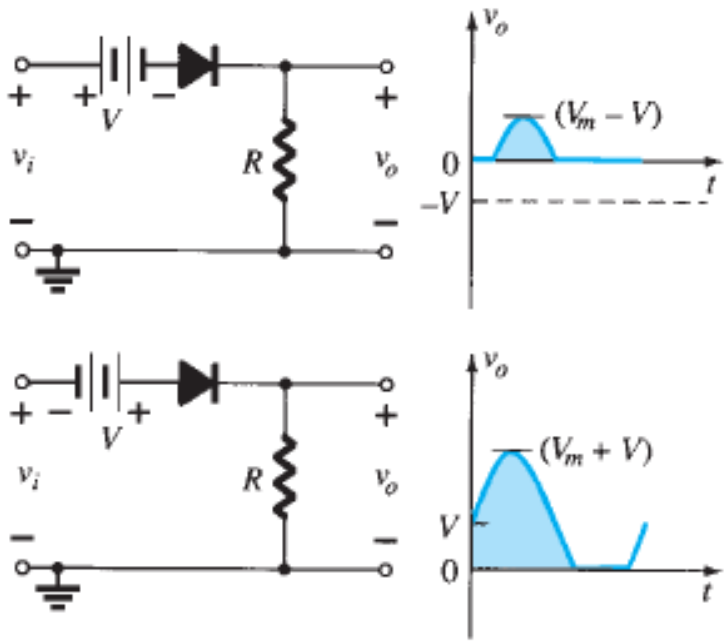


NEGATIVE



Biased Series Clippers (Ideal Diodes)





Biased Parallel Clippers (Ideal Diodes)