



CSE 4205

Digital Logic Design

Counter

Course Teacher: Md. Hamjajul Ashmafee

AP, CSE, IUT

Email: ashmafee@iut-dhaka.edu



Introduction

- The simplest type of MSI sequential circuit
 - Made of one or more flip flops (building block of sequential circuit)
- Definition: Basically, a counter changes its state in a prescribed sequence when input pulses are received
 - Driven by a clock signal (common input pulse)
- Application: count number of pulses/cycles (Hz), to measure time (T) and frequency (f)
- Basically, we use T flip flop which has the toggling feature (input, $T = 1$) best suited for counting operation



Types

- Broadly categorized in different ways:
 1. Asynchronous and synchronous counter
 2. Single and multimode counter
 3. Modulus counter

All of them has further classifications



Asynchronous and Synchronous Counter

- Asynchronous Counter
 - Simple and straightforward in operation and construction
 - Each flip flop is triggered by the previous flip flop
 - Also known as ripple or serial counter
- Synchronous Counter
 - Clock pulses are simultaneously applied to all flip flops
 - To increase the speed of the counter, more sophisticated hardware is required
 - Also known as parallel counter



Single and Multimode Counter

- Modes of counting
 - Count-Up
 - Count-Down
- Single-mode Counter
 - Either count-up mode or count-down mode is in operation
- Multimode Counter
 - Both modes are in operation



Modulus Counter

- It is defined by the number of states it is capable of counting.
 - To define all states, if n bits are required to represent each state, in total $2^n (=N)$ states are possible (maximum count)
- Types:
 - Mod- N or Mod- 2^n
 - Mod “ $<N$ ”

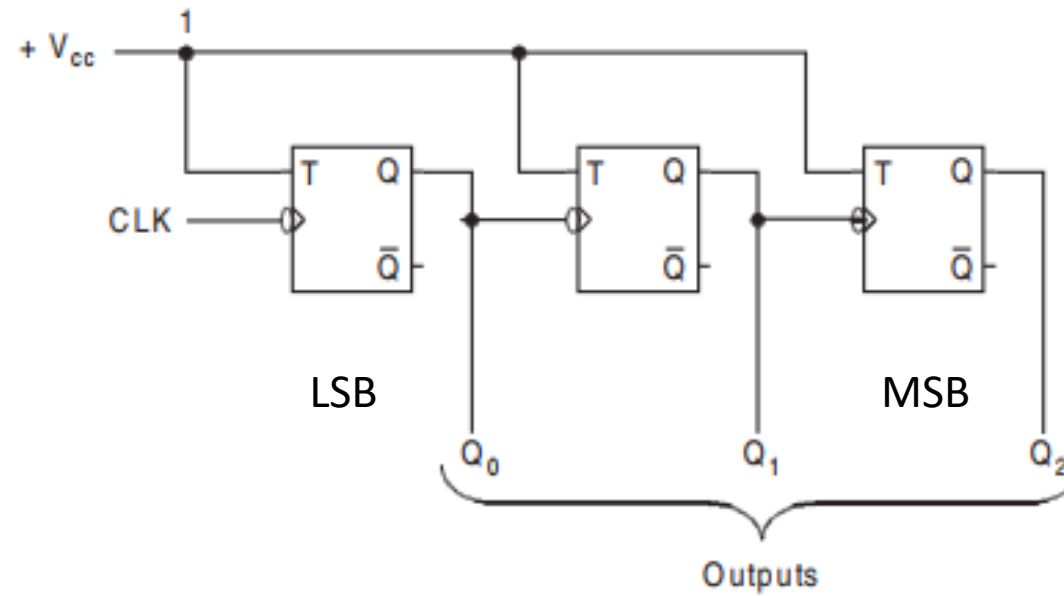


Asynchronous Counter

- All the flip flops are not driven by same clock pulse
- It has cumulative settling time of all flip flops
- It causes the ripple through the changes of the states of the flip flops successively

3 Bit Asynchronous Up Counter

Logic Diagram



3 Bit Asynchronous Up Counter

Count Sequence

| Counter State | Q_2 | Q_1 | Q_0 |
|---------------|-------|-------|-------|
| 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 |
| 2 | 0 | 1 | 0 |
| 3 | 0 | 1 | 1 |
| 4 | 1 | 0 | 0 |
| 5 | 1 | 0 | 1 |
| 6 | 1 | 1 | 0 |
| 7 | 1 | 1 | 1 |

Asynchronous Down Counter

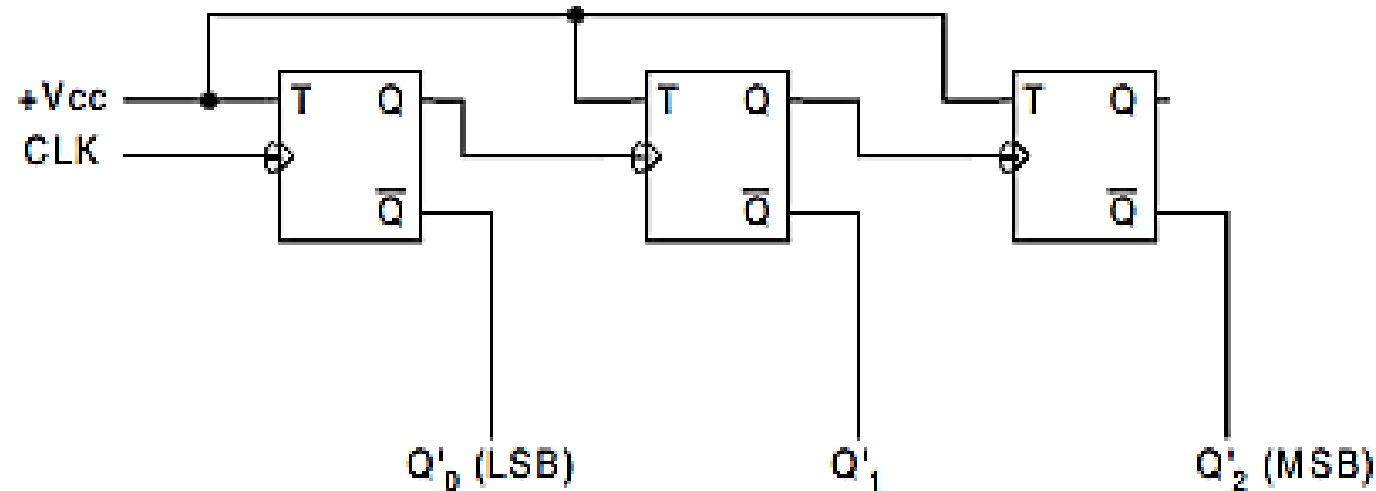
- Counts downward starting from a maximum count of (2^n-1) to 0

| Counter State | Q_2 | Q_1 | Q_0 |
|---------------|-------|-------|-------|
| 7 | 1 | 1 | 1 |
| 6 | 1 | 1 | 0 |
| 5 | 1 | 0 | 1 |
| 4 | 1 | 0 | 0 |
| 3 | 0 | 1 | 1 |
| 2 | 0 | 1 | 0 |
| 1 | 0 | 0 | 1 |
| 0 | 0 | 0 | 0 |

- Application: Count-down timer
- There are three different ways to implement...

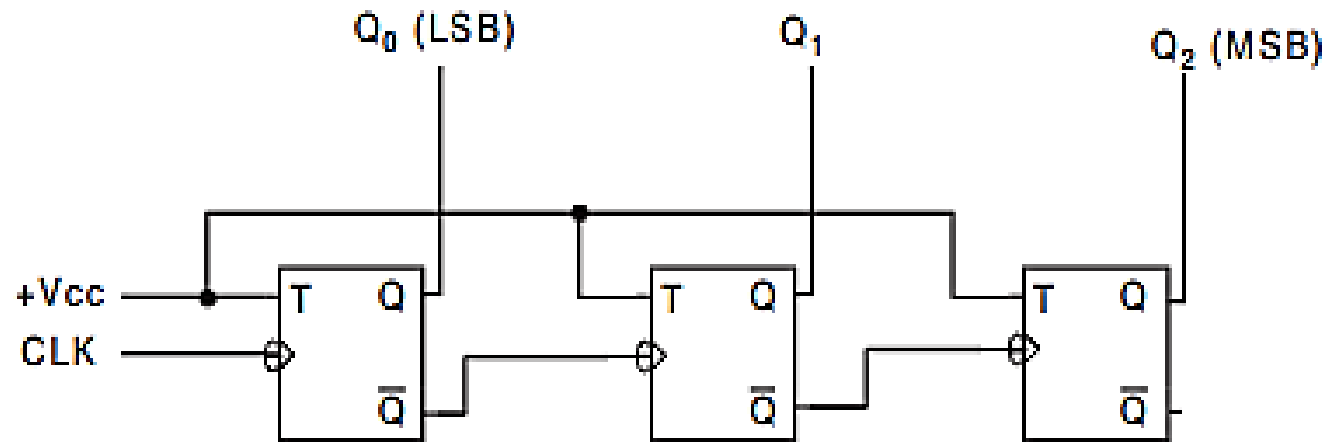
Asynchronous Down Counter: Way 1

- With same circuit as previous, only outputs of the counter may be taken from the complement outputs (Q') of the flip-flops



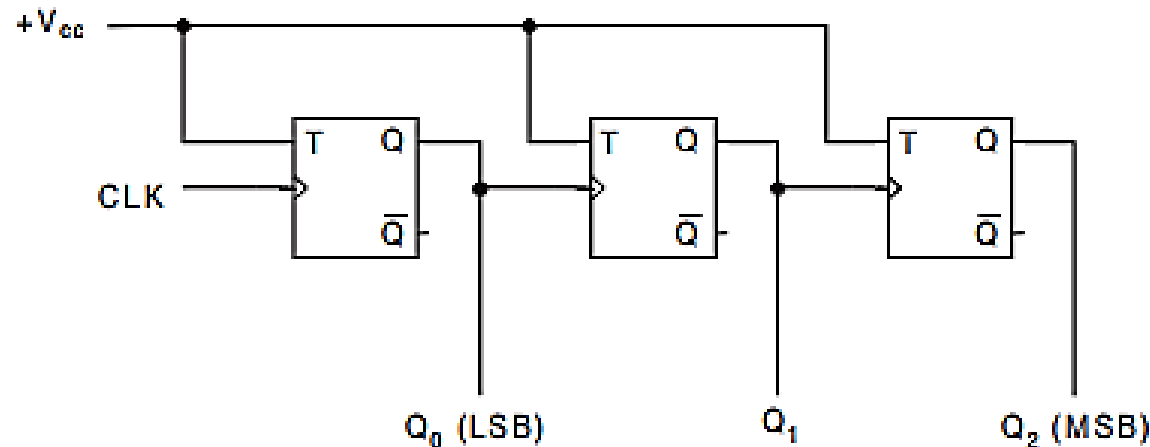
Asynchronous Down Counter: Way 2

- The circuit will be slightly modified so that the clock inputs of successive flip-flops will be driven by the Q' output of preceding stages (flip-flops)



Asynchronous Down Counter: Way 3

- The circuit will be similar to the up-counter circuit replacing the negative edge triggering flip-flops to the positive edge triggering flip-flops



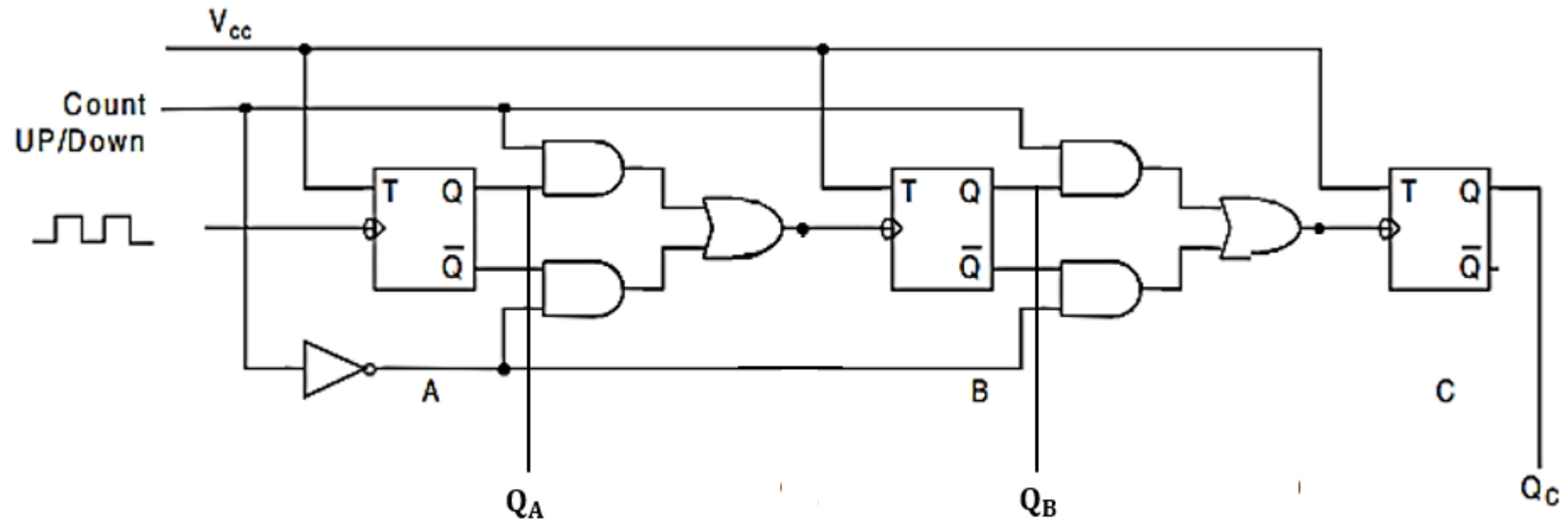


Asynchronous Up-Down Counter

- We combine the up and down modes in a single up-down counter
 - Count both upward as well as downward
 - It is also called the “multimode” counter
- The operation of such counter is controlled by up-down controller
 - To select the mode – up or down

Asynchronous Up-Down Counter

Circuit Diagram





Propagation Delay of Asynchronous Counter

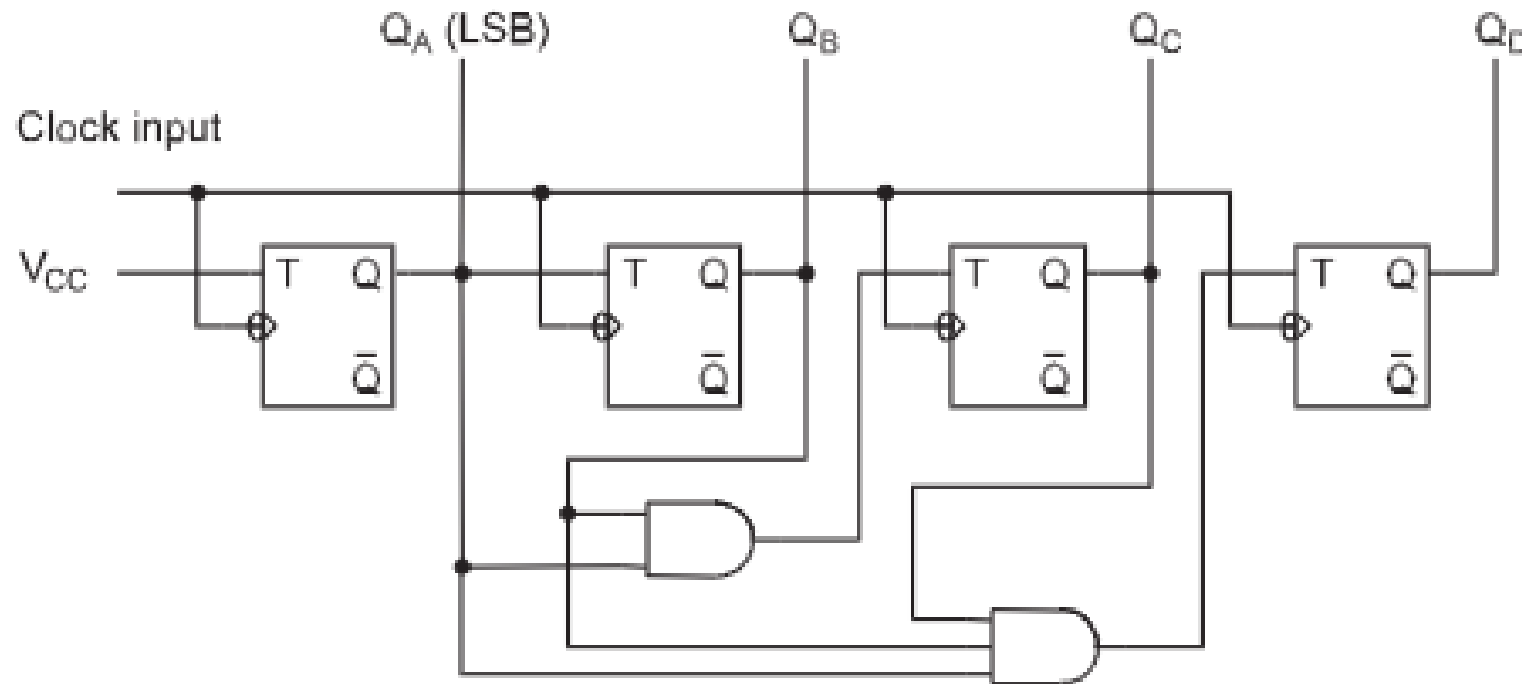
- Self Study



Synchronous Counter

- All flip-flops are clocked synchronously
- But T inputs of different flip-flops could be varied based on necessity

Synchronous *Up Counter* with Parallel Carry

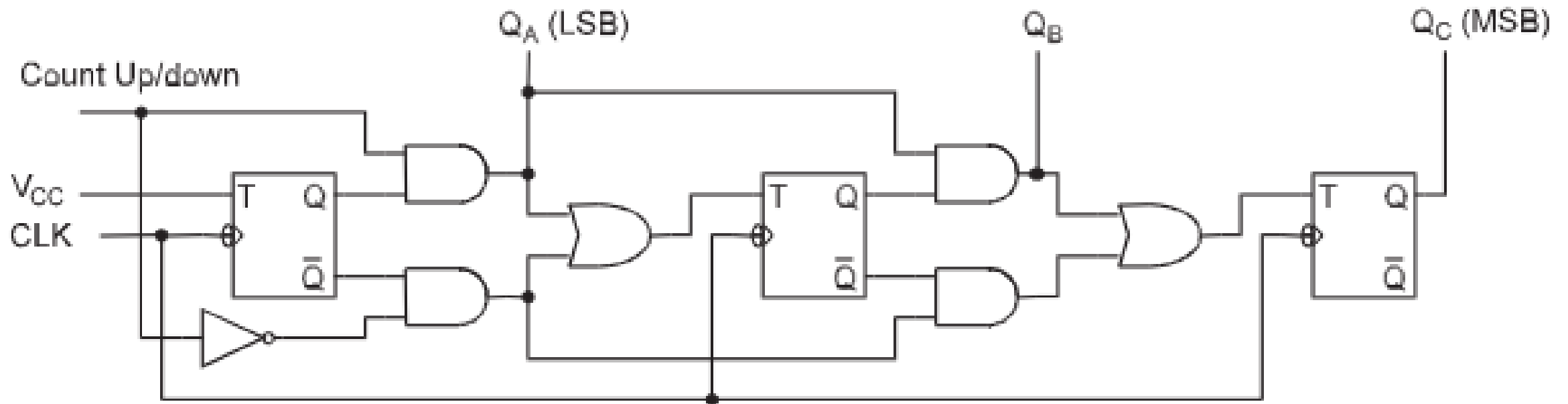


For the first FF (LSB), $T=1$. It changes the output constantly.





Synchronous Up-Down Counter





Other Synchronous Counter

- Same as **design procedure** of Sequential circuit to design any synchronous counter
 - **Example:**
 - Modulus $< N$ (2^n) counter
 - BCD Counter
 - Gray code counter
 - Irregular counter
 - Sequence Generator



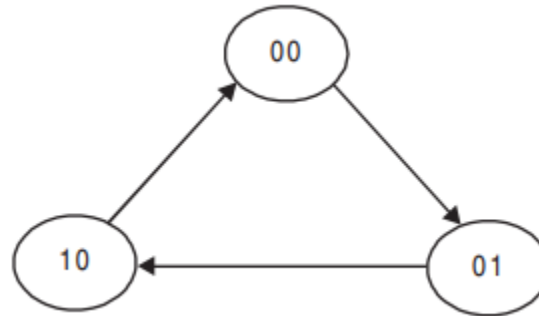
Synchronous Counter: Design Procedure

- From the problem statement, draw the **state diagram** that describes the operation of a counter
- Derive the **state table** and **circuit excitation table** from the state diagram maintaining the count sequence
- Find the **number** of the flip-flops
- Determine the flip-flop **type** and its inputs
- Prepare the **K-maps to get the simplified expressions** for each inputs in term of the outputs and external inputs of flip-flops
- Connect the circuit using the flip-flops and other gates corresponding to the simplified expressions

SC: Design Procedure – Example

Design of a MOD-3 counter

- State Diagram:



- State Table and Circuit Excitation Table:

| <i>Present state</i> | <i>Next state</i> |
|----------------------|-------------------|
| 00 | 01 |
| 01 | 10 |
| 10 | 00 |

| <i>Count Sequence</i> | | <i>Flip-flop inputs</i> | |
|-----------------------|-------|-------------------------|--------|
| A_1 | A_0 | TA_1 | TA_0 |
| 0 | 0 | 0 | 1 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 1 | 0 |

SC: Design Procedure – Example...

Design of a MOD-3 counter

- K-map for simplification:

- Logic Diagram:

| A ₁ \ A ₀ | 0 | 1 |
|---------------------------------|---|---|
| 0 | 0 | 1 |
| 1 | 1 | X |

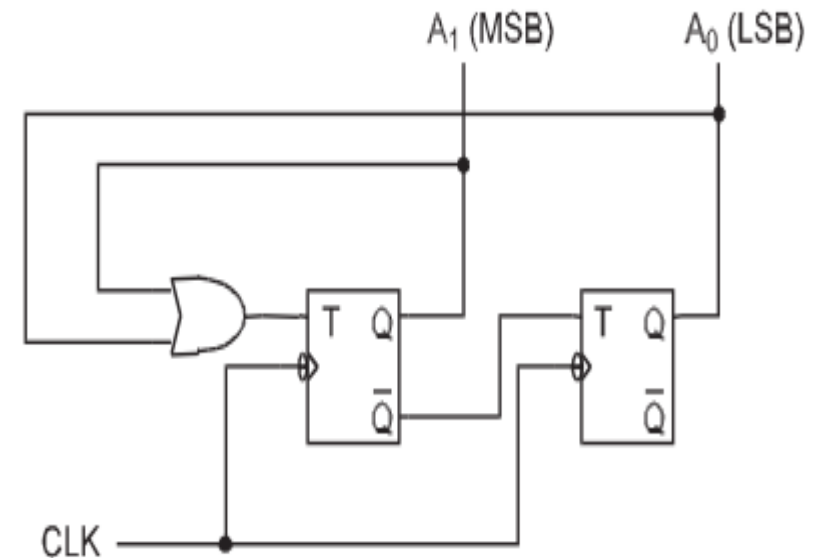
(a) For TA_1

$$TA_1 = A_1 + A_0$$

| A ₁ \ A ₀ | 0 | 1 |
|---------------------------------|---|---|
| 0 | 1 | 1 |
| 1 | 0 | X |

(b) For TA_0

$$TA_0 = A'_1$$





Propagation Delay of Synchronous Counter

- Self Study



Synchronous-Asynchronous Counter

- Some hybrid counters combines the good feature of these both
 - Simplicity of the asynchronous counter and speed of the synchronous counter
 - **Example:** BCD synchronous-asynchronous counter
 - **Explanation:** Self-study



Comparison between Synchronous and Asynchronous Counter

- Self Study



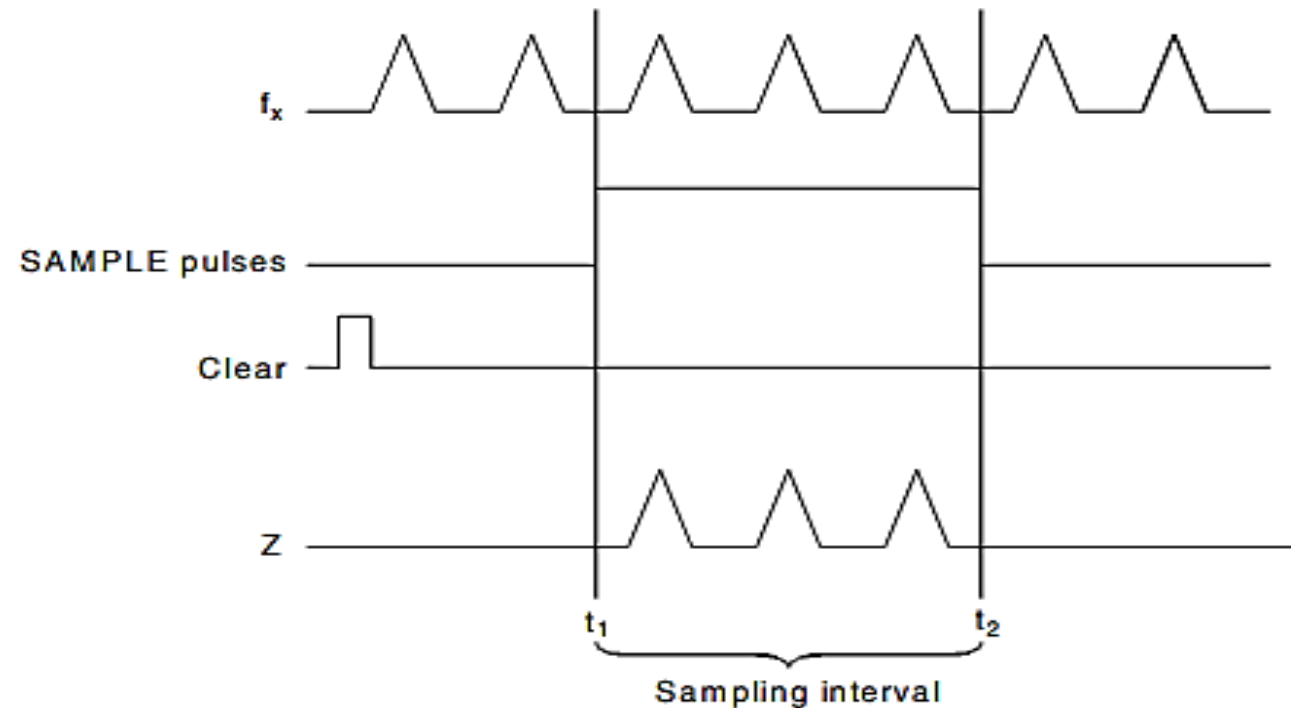
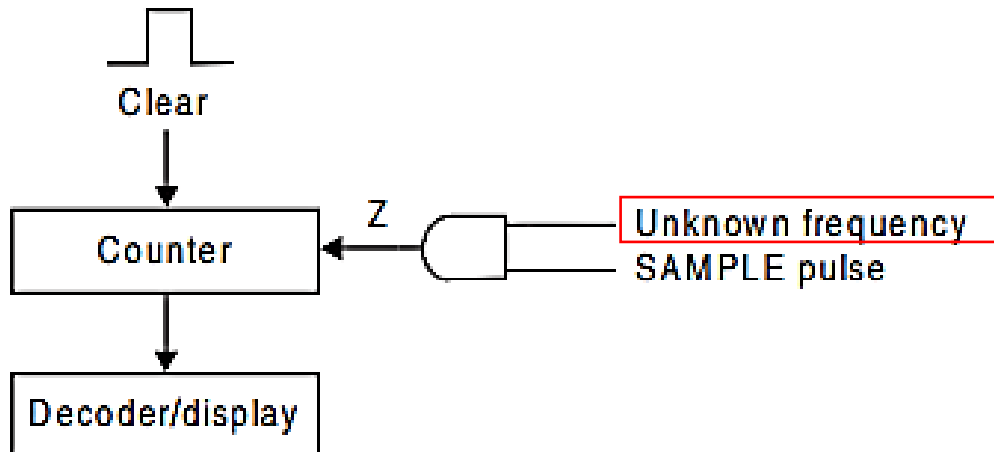
Some Other Terms

- Lock out states/conditions:
 - Some unused states may not have the known next state. A counter with such unused states may suffer from lock out problem.
- Presetable/programmable counter:
 - A counter that has the capability to start counting from any desired state maintaining an appropriate logic circuit.

Application of Counter

- **Frequency Counter**

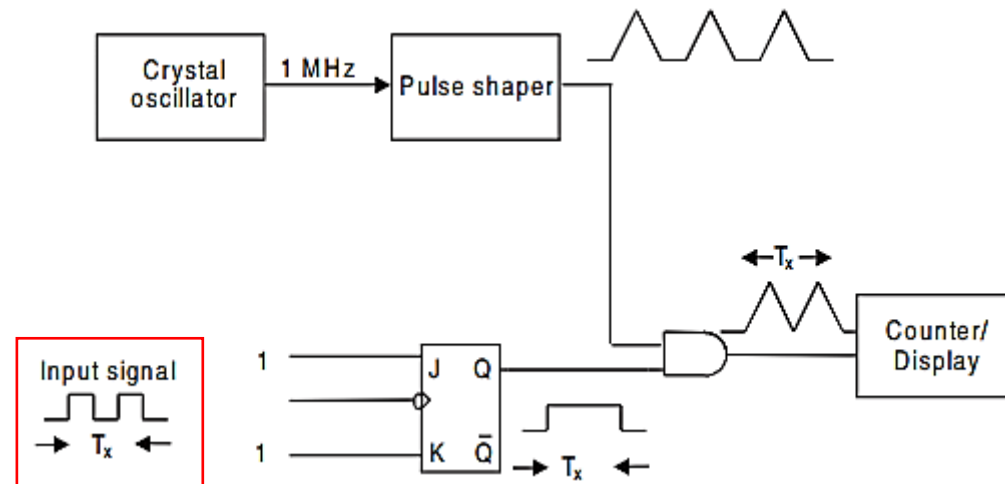
- Measure and display the frequency of a signal
- It will measure the unknown frequency (f_x) against a known SAMPLE pulse



Application of Counter...

• Measurement of Period

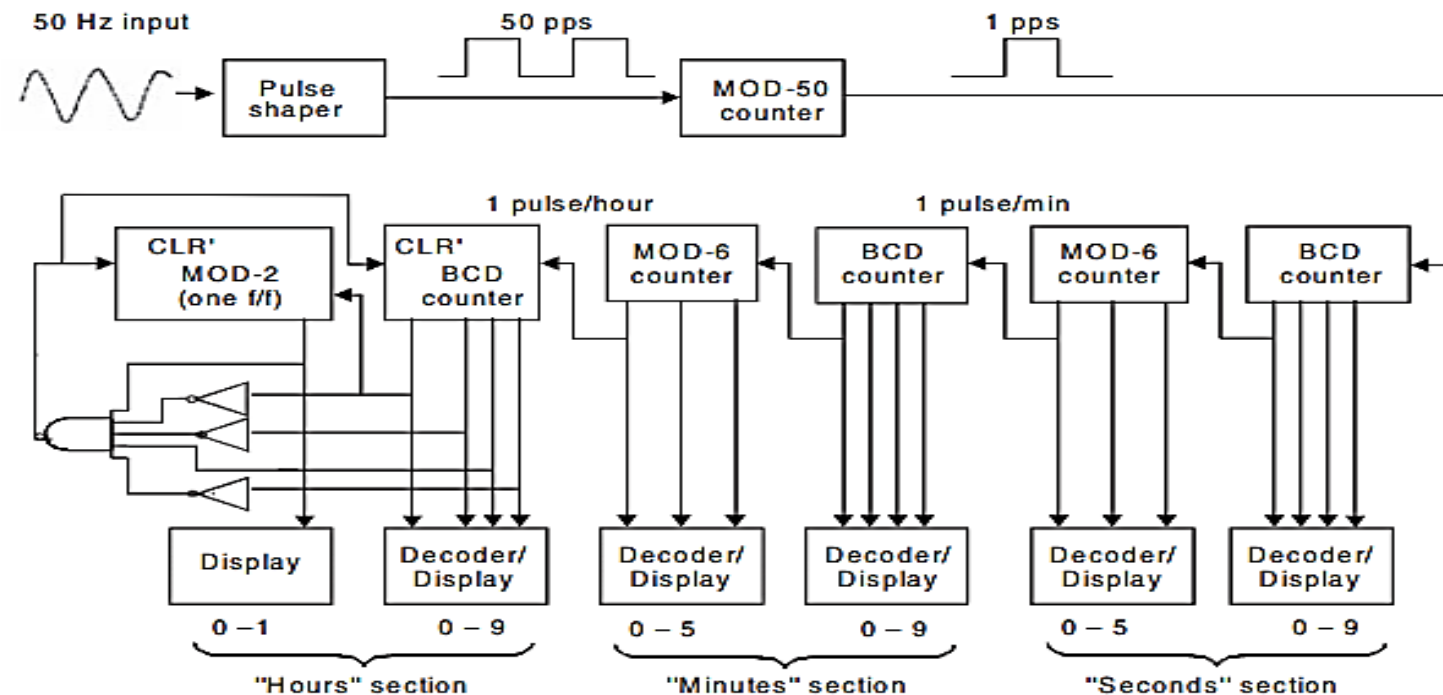
- An accurate 1 MHz reference frequency is gated into the counter for any time duration T_x
 - The counter counts and displays the values of T_x in units of micro-seconds
 - **Example:** for 1.17 milli-second, the gate will allow 1170 pulses into the counter



Application of Counter...

- **Digital Clock**

- Displays time of day in hours, minutes and seconds
- To get accurate clock, a very highly controlled basic clock frequency is required





Self Study

- **Hazards in digital circuits**
 - Due to some undesirable glitches and propagation delay
 - Static hazard
 - Dynamic hazard
 - Essential hazard



Self Study...

- **Frequency Division:**

- If the clock is not the same for all flip flops, frequency for n^{th} flip-flop (stages) will be $f_{CLK}/2^n$