ISLAMIC UNIVERSITY OF TECHNOLOGY (IUT)
ORGANISATION OF ISLAMIC COOPERATION (OIC)
Department of Computer Science and Engineering (CSE)

SEMESTER FINAL EXAMINATION   **SUMMER SEMESTER, 2019-2020**
DURATION: 1 Hour 30 Minutes   **FULL MARKS: 75**

CSE 4205: Digital Logic Design

Figures in the right margin indicate marks. **Answer all three questions.**
Write examination information on the **first page** and write **studentID and page number** in every page of
the answer script. Submission pdf should be named as **studentID_CourseCode_Final.pdf**
The use of pencil is recommended to discourage any writing from being crossed

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1   a)   What are D/A converters and A/D converters and what are their uses? Explain a real-life   7
         application for an example of all this. To illustrate it better, you might use a block diagram.

    b)   For the function (**Y**) executed by the circuit below (figure 1), write the minimized Boolean   8
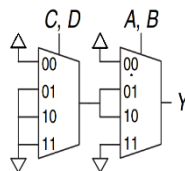   equation with its corresponding truth table:

Figure 1: A combinational circuit

Note: Here A, B, C and D denote the input variables of the function

    c)   Design a MOD-11 ripple multimode counter that can be manually RESET by an external push   10
         button.

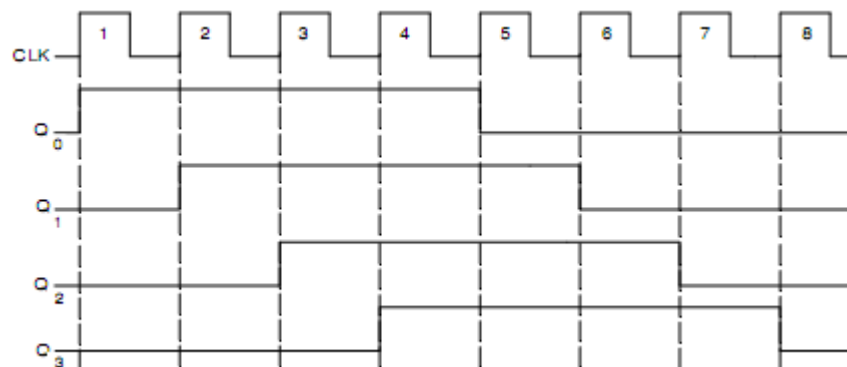2   a)   Draw a sequential circuit for the output sequence given below (figure 2):   7

Figure 2: A timing diagram

What's the best flip-flop to use here, rather than others? Justify the explanation.

    b)   How does a programmable logic device (PLD) differ from a fixed logic device? What are the   8
         primary advantages of using PLDs? Differentiate, based on basic points, among various types of
         PLDs.

c) Design a left-shift register which is operated by two distinct control inputs: **S** and **L**. It should shift left if S=1, load if S=0 and L=1, and hold its state if S=L=0. For the implementation of the circuit, the RS flip flop is preferred. 10

3 a) A pet robotic snail with an FSM brain is operated by Zunaira. The snail crawls over a paper tape 25
containing a series of 1's and 0's, from left to right. The snail crawls up to the next bit on each clock cycle. When the last two pieces that it has crawled over are, from left to right, 01, the snail smiles. The A input is the bit under the antennae of the snail. When the snail smiles, the Y output is TRUE.
   i.   Design the both Mealy and Moore FSM to compute when the snail should smile. Compare them briefly.
   ii. Sketch a timing diagram for each machine showing the input, states, and output as Zunaira's snail crawls along the sequence 0100110111.
   iii. Zunaira's snail has a daughter with the FSM brain of a Mealy machine. Whenever she slides over the pattern 1101 or the pattern 1110, the daughter snail laughs. Sketch the state transition diagram for this happy snail using as few states as possible.
   iv. From the question (iii), perform the state assignment and derive the state table. Is it possible to perform the state reduction? Justify your answer in short.
   v.   From the question (iii), write the next state and output equations