Page 2

LPC3154 Powering and Unused parts

Page 3

LPC3154 Digital I/O

Page 4

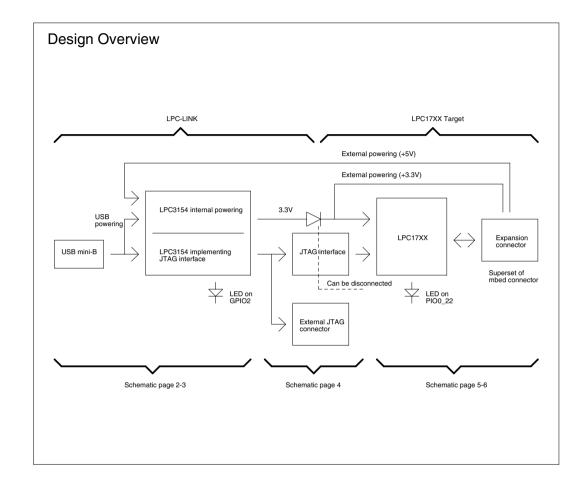
JTAG Interface

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LPC17XX with Expansion connector

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LPC17XX



UL = UnLoaded = normally not mounted component.

Default jumper settings are indicated in the schematic. However, always check jumper positions on actual boards since there is no guarantee that all jumpers are in default place.

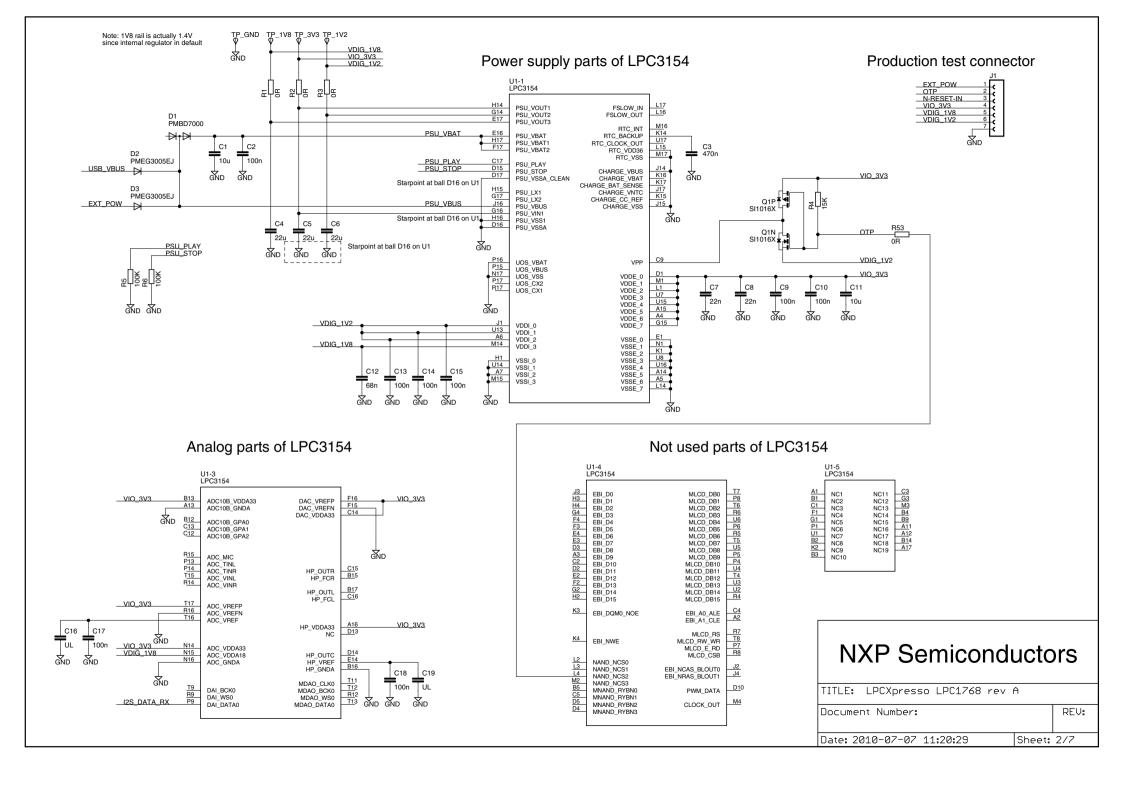
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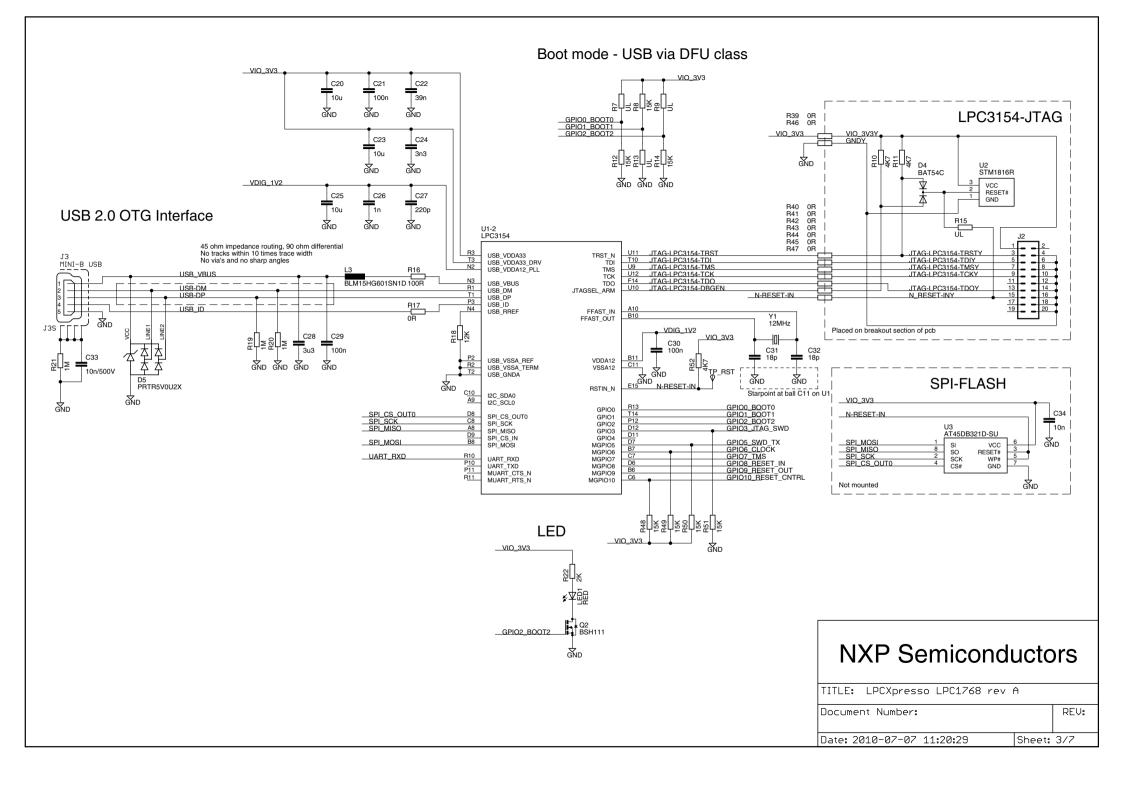
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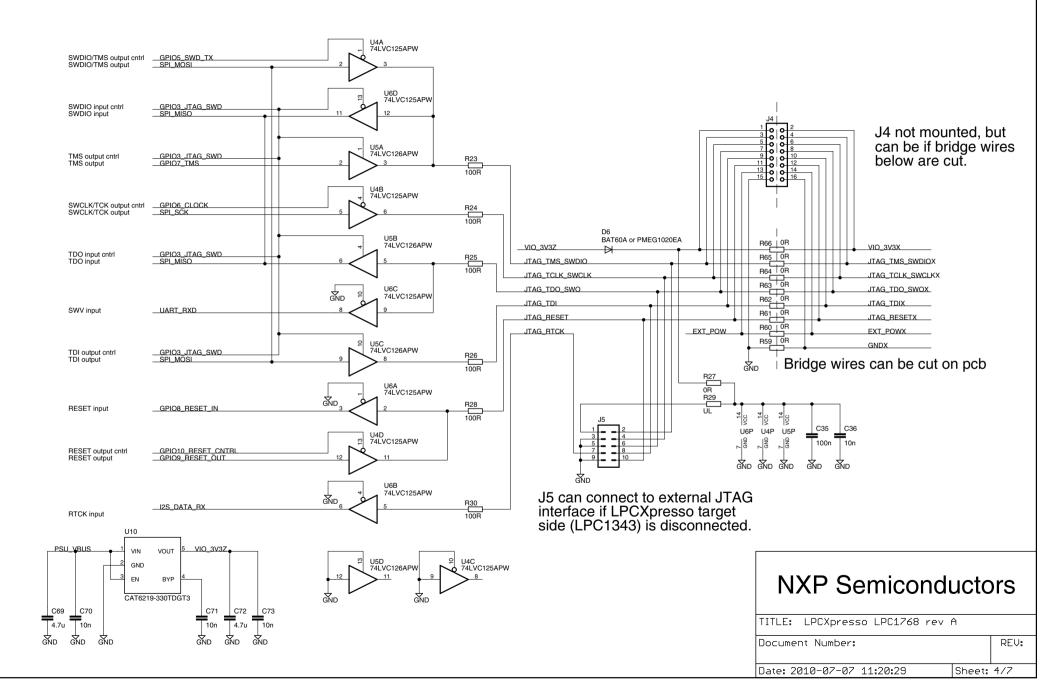
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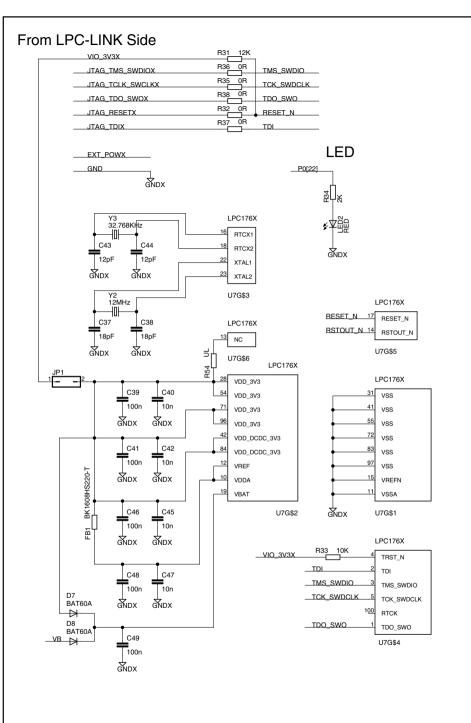
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JTAG Interface





LPC1XXX Target Side

Expansion Connector (superset of mbed pinning)

mbed	LPCXpresso		Dual row holes (2x27), 100 mil spacing			LPCXpresso		mbed	
GND	GND		GNDX	(J6-1	VIO_3V3	X (J6-28	VOUT (+3.3'	V out) if self se +3.3V input	VOUT (3.3V out)
VIN (4.5-14V)	VIN (4.5-5.5V)		EXT_POV	VX_ ∢ J6-2		-∢ J6-29	not used	io rolov input	VU (5.0V USB out)
VB (battery supply)	VB (battery supply)		VB	—(J6-3		-∢ J6-30	not used		IF+
nR (reset)	RESET_N		RESET_N (J6-4			─¢ J6-31			IF-
SPI1-MOSI	P0.9	MOSI1	P0[9]	(J6-5	RD-	(J6-32	RD-		RD- (Ethernet)
SPI1-MISO	P0.8	MISO1	P0[8]	─€ J6-6	RD+	─ J6-33	RD+		RD+ (Ethernet)
SPI1-SCK	P0.7	SCK1	_P0[7]	──€ J6-7	TD	 J6-34	TD-		TD- (Ethernet)
GPIO	P0.6	SSEL1	P0[6]	─€ J6-8	TD+	 J6-35	TD+		TD+ (Ethernet)
UART1-TX / I2C1-SDA	P0.0	TXD3/SDA1	P0[0]	─€ J6-9	USB-D	 J6-36	USB-D-		D- (USB)
UART1-RX / I2C1-SCL	P0.1	RXD3/SCL1	_P0[1]	─€ J6-10	USB-D+_	──€ J6-37	USB-D+		D+ (USB)
SPI2-MOSI	P0.18	MOSI0	P0[18]	─€ J6-11	P0[4]	 J6-38	P0.4	CAN_RX2	CAN-RD
SPI2-MISO	P0.17	MISO0	_P0[17]	─(J6-12	P0[5]	 J6-39	P0.5	CAN_TX2	CAN-TD
SPI2-SCL / UART2-TX	P0.15	TXD1/SCK0	_P0[15]	─€ J6-13	P0[10]	 J6-40	P0.10	TXD2/SDA2	UART3-TX / I2C2-SDA
UART2-RX	P0.16	RXD1/SSEL0	_P0[16]	─€ J6-14	P0[11]	 J6-41	P0.11	RXD2/SCL2	UART3-RX / I2C2-SCL
AIN0	P0.23	AD0.0	_P0[23]	─€ J6-15	P2[0]	 J6-42	P2.0	PWM1.1	PWMOUT0
AIN1	P0.24	AD0.1	P0[24]	─€ J6-16	P2[1]	 J6-43	P2.1	PWM1.2	PWMOUT1
AIN2	P0.25	AD0.2	P0[25]	─€ J6-17	P2[2]	 J6-44	P2.2	PWM1.3	PWMOUT2
AIN3 / AOUT	P0.26	AD0.3/AOUT	_P0[26]	─€ J6-18	P2[3]	 J6-45	P2.3	PWM1.4	PWMOUT3
AIN4	P1.30	AD0.4	P1[30]	—(J6-19	P2[4]	(J6-46	P2.4	PWM1.5	PWMOUT4
AIN5	P1.31	AD0.5	P1[31]	—(J6-20	P2[5]	 J6-47	P2.5	PWM1.6	PWMOUT5
	P0.2		P0[2]	 J6-21	P2[6]	(J6-48	P2.6		
	P0.3		_P0[3]	—(J6-22	P2[7]	(J6-49	P2.7		
	P0.21		_P0[21]	—(J6-23	P2[8]	(J6-50	P2.8		
	P0.22		_P0[22]	(J6-24	P2[10]	 J6-51	P2.10		
	P0.27		_P0[27]	(J6-25	P2[11]	(J6-52	P2.11		
	P0.28		_P0[28]	(J6-26	P2[12]	(J6-53	P2.12		
	P2.13		P2[13]	──(J6-27	GNDX	 J6-54	GND		

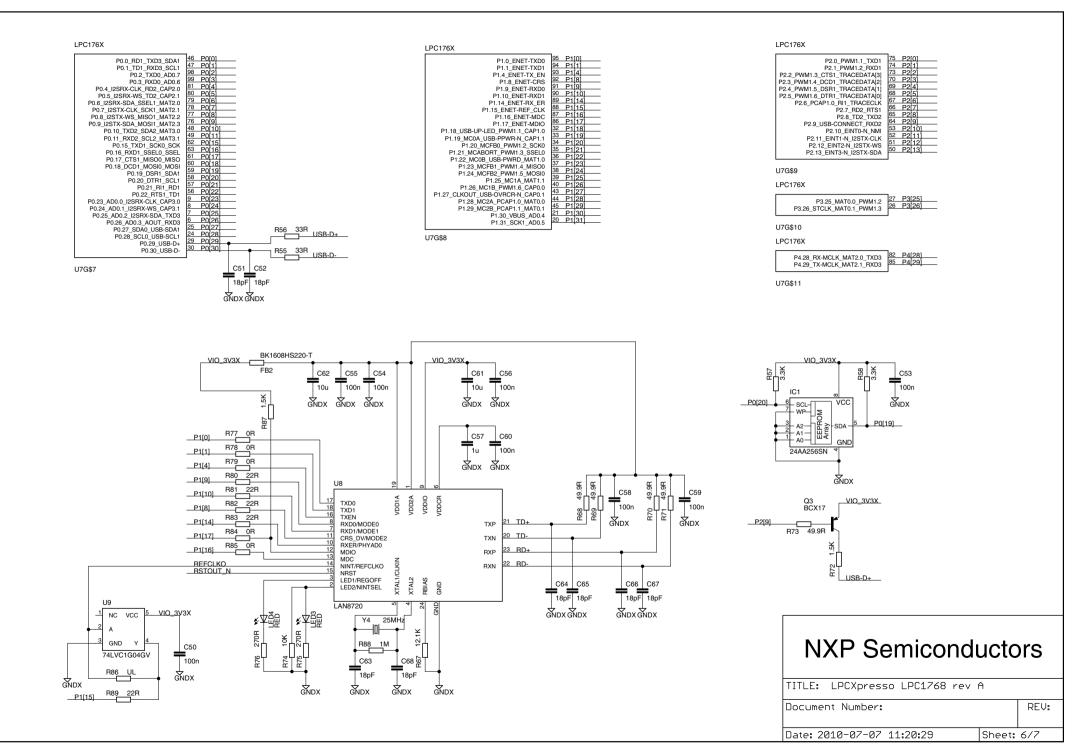
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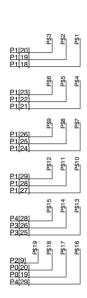
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