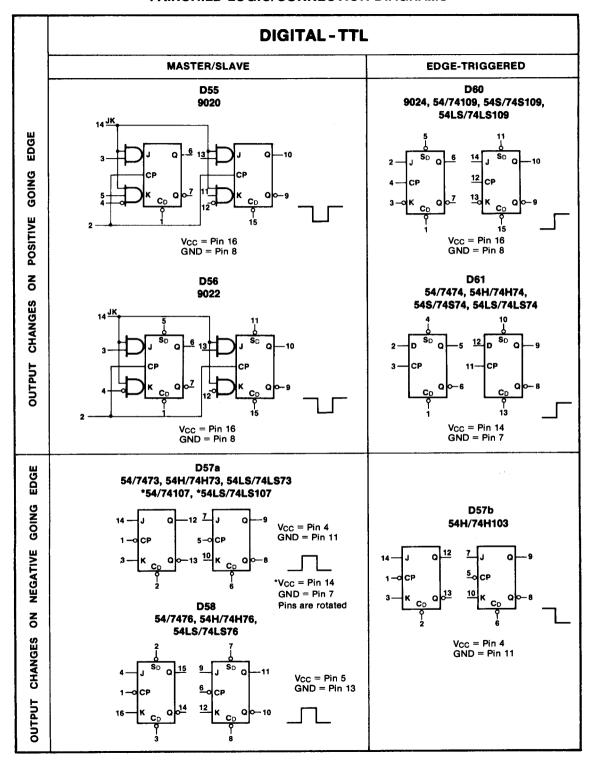
13

FAIRCHILD LOGIC/CONNECTION DIAGRAMS



FAIRCHILD DIGITAL

TTL

TTL SINGLE AND DUAL FLIP-FLOPS

Item	Function	DEVICE NO.	Inputs	Clock Edge	Direct Set	Direct Clear	Clock Frequency MHz (Typ)	Clock to Output Delay-ns (Typ)	Power Dissipation mW (Typ)	Logic/Connection Diagram	Package(s)
1	Single JK	9000	3J, 3K, JK	7	Х	Х	20	16	100	D50	3I, 6A
2	Single JK	9001	2J, 2K, J, K, JK	۲	х	х	50	16	115	D51	3I, 6A
3	Single JK	54H/74H71	(AOI) (2+2)J,(2+2)K	7	х	_	30	22	95	D52a	31, 6A, 9A
4	Single JK	54H/74H101	(AOI) (2+2)J, (2+2)K		х		50	16	100	D52b	31, 6A, 9A
5	Single JK	54/7472	3J, 3K	7	Х	X	20	25	50	D53a	3I, 6A, 9A
6	Single JK	54H/74H72	3J, 3K	7	X	X	30	22	80	D53a	3I, 6A, 9A
7	Single JK	54H/74H102	3J, 3K	l	Х	X	50	16	100	D53b	3I, 6A, 9A
8	Single JK	54/7470	2J, 2K, J, K	_ ح	Х	Х	35	27	65	D54	31, 6A, 9A
9	Dual D	54/7474	D	-1	Х	Х	25	20	85	D61	3I, 6A, 9A
_10	Dual D	54H/74H74	D	工	Х	Х	43	13	150	D61	31, 6A, 9A
11	Dual D	548/74874	D	7	Х	X	100	7.0	150	D61	31, 6A, 9A
12	Dual D	54LS/74LS74	D	7	Х	Х	50	15	20	D61	31, 6A, 9A
13	Dual JK	9020	$J, K, \overline{J}, \overline{K}, JK$	ᇺ	_	Х	50	16	210	D55	4L, 6B
14	Dual JK	9022	J, K, JK	٦٢	Х	x	15	16	210	D56	4L, 6B
15	Dual JK	54/7473	J, K	工	_	х	20	25	100	D57a	3I, 6A, 9A
16	Dual JK	54/74107	J, K	工	_	X	20	25	100	D57a	3I, 6A, 9A
_ 17	Dual JK	54H/74H73	J, K	工	_	Х	30	22	160	D57a	31, 6A, 9A
18	Dual JK	54H/74H103	J, K	٦	_	Х	50	16	200	D57b	31, 6A, 9A
19	Dual JK	54S/74S113	J, K	Z.	Х	_	125	5.0	150	D63	31, 6A, 9A
20	Dual JK	54LS/74LS113	J, K	2	X	_	60	12	20	D63	31, 6A, 9A
21	Dual JK	54/7476	J, K	几	Х	х	20	25	100	D58	4L, 6B, 9B
22	Dual JK	54H/74H76	J, K	7_	Х	x	30	22	150	D58	4L, 6B, 9B
23	Dual JK	54H/74H106	J, K	Z	х	х	50	16	200	D58	4L, 6B, 9B
24	Dual JK	54\$/74\$112	J, K	ı	Х	х	125	5.0	150	D62	4L,6B,9B
25	Dual JK	54LS/74LS112	J, K	ı	Х	X	60	12	20	D62	4L,6B,9B
26	Dual JK	54H/74H78	J, K	77	х	X	30	22	160	D59a	31,6A,9A
27	Dual JK	54H/74H108	J, K	l	Х	Х	50	16	200	D59b	31,6A,9A