

# SN54192, SN54193, SN54LS192, SN54LS193, SN74192, SN74193, SN74LS192, SN74LS193 SYNCHRONOUS 4-BIT UP/DOWN COUNTERS (DUAL CLOCK WITH CLEAR)

SDLS074 - DECEMBER 1972 - REVISED MARCH 1988

- Cascading Circuitry Provided Internally
- Synchronous Operation
- Individual Preset to Each Flip-Flop
- Fully Independent Clear Input

TYPES	TYPICAL MAXIMUM COUNT FREQUENCY	TYPICAL POWER DISSIPATION
'192, '193	32 MHz	325 mW
'LS192, 'LS193	32 MHz	95 mW

## description

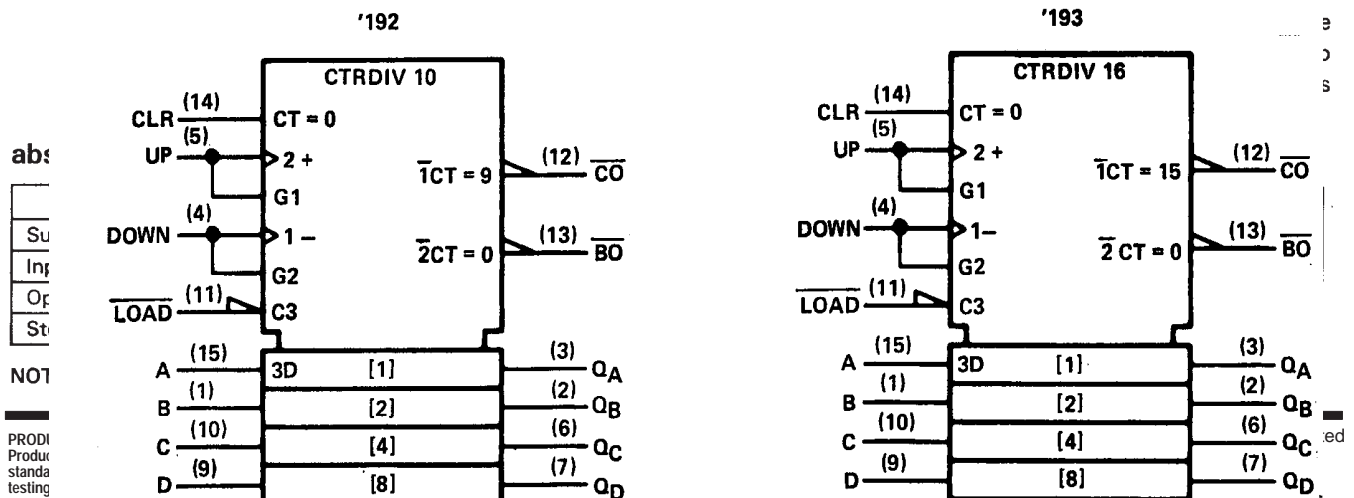
These monolithic circuits are synchronous reversible (up/down) counters having a complexity of 55 equivalent gates. The '192 and 'LS192 circuits are BCD counters and the '193 and 'LS193 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidentally with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple-clock) counters.

The outputs of the four master-slave flip-flops are triggered by a low-to-high-level transition of either count (clock) input. The direction of counting is determined by which count input is pulsed while the other count input is high.

All four counters are fully programmable; that is, each output may be preset to either level by entering the desired data at the data inputs while the load input is low. The output will change to agree with the data inputs independently of the count pulses. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

A clear input has been provided which forces all outputs to the low level when a high level is applied. The clear function is independent of the count and load inputs. The clear, count, and load inputs are buffered to lower the drive requirements. This reduces the number of clock drivers, etc., required for long words.

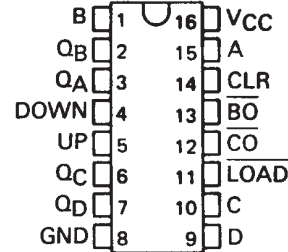
## logic symbols†



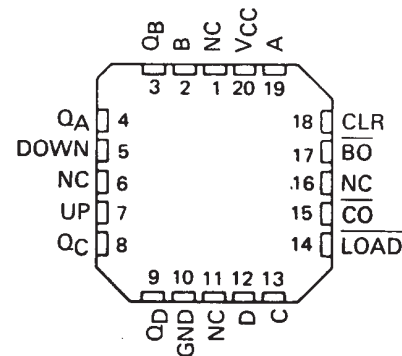
## schematics of inputs and outputs

SN54192, SN54193, SN54LS192,  
SN54LS193 . . . J OR W PACKAGE  
SN74192, SN74193 . . . N PACKAGE  
SN74LS192, SN74LS193 . . . D OR N PACKAGE

(TOP VIEW)



SN54LS192, SN54LS193 . . . FK PACKAGE  
(TOP VIEW)



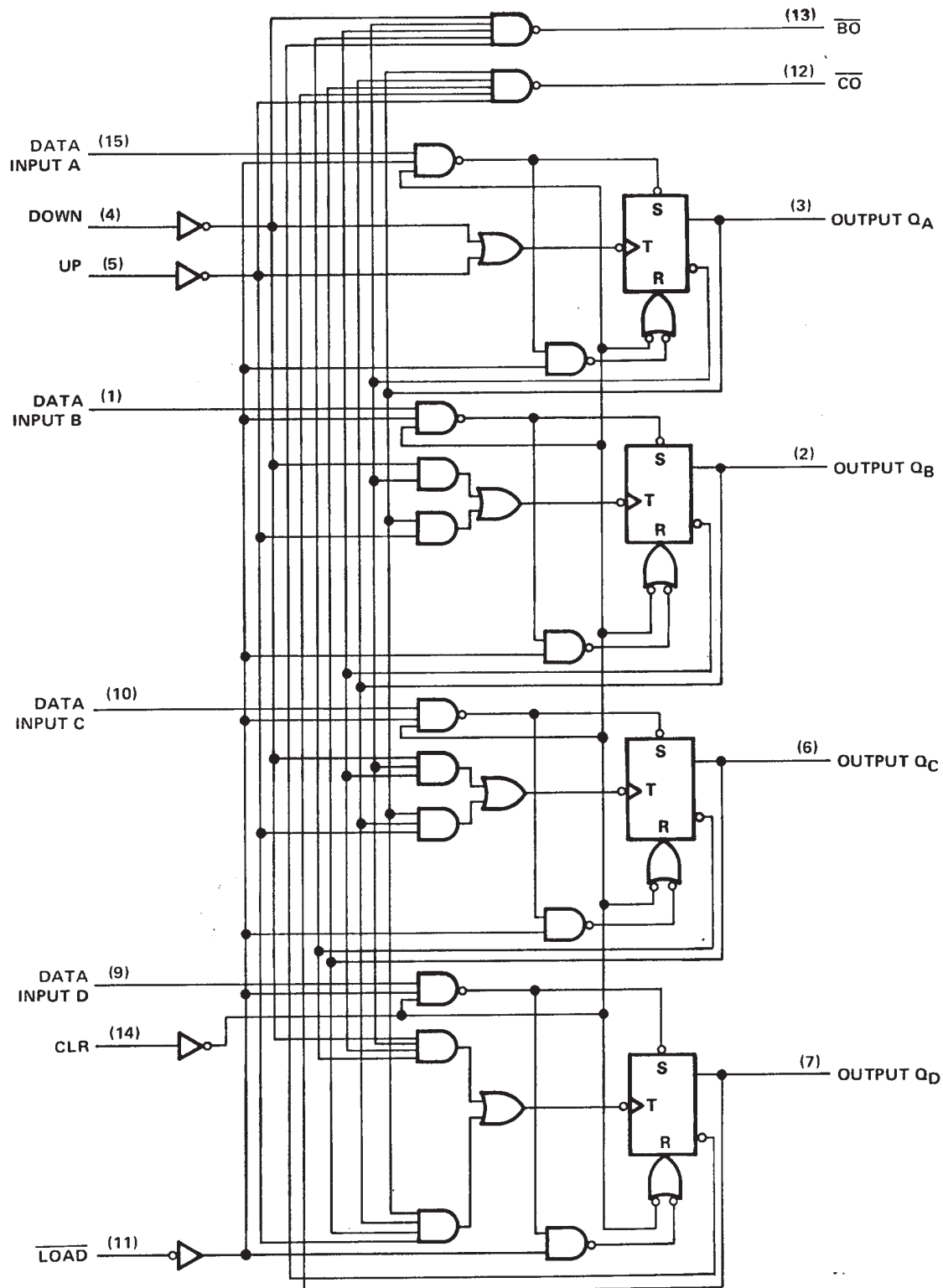
NC - No internal connection

# SN54193, SN54LS193, SN74193, SN74LS193

## SYNCHRONOUS 4-BIT UP/DOWN COUNTERS (DUAL CLOCK WITH CLEAR)

SDLS074 - DECMEBER 1972 - REVISED MARCH 1988

logic diagram (positive logic)



Pin numbers shown are for D, J, N, and W packages.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

# SN54193, SN54LS193, SN74193, SN74LS193 SYNCHRONOUS 4-BIT UP/DOWN COUNTERS (DUAL CLOCK WITH CLEAR)

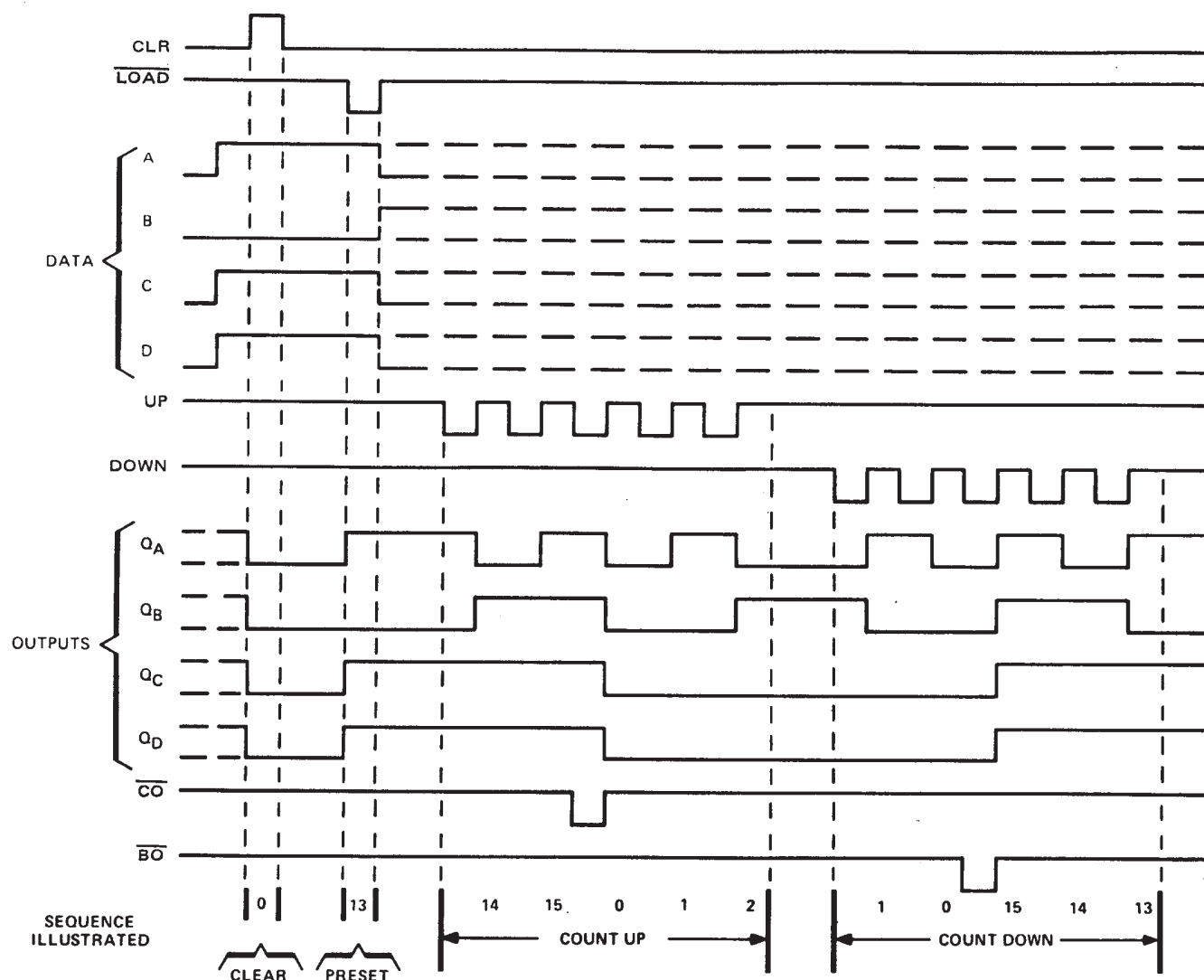
SDLS074 – DECEMBER 1972 – REVISED MARCH 1988

## '193, 'LS193 BINARY COUNTERS

### typical clear, load, and count sequences

Illustrated below is the following sequence:

1. Clear outputs to zero.
2. Load (preset) to binary thirteen.
3. Count up to fourteen, fifteen, carry, zero, one, and two.
4. Count down to one, zero, borrow, fifteen, fourteen, and thirteen.



NOTES: A. Clear overrides load, data, and count inputs.

B. When counting up, count-down input must be high; when counting down, count-up input must be high.

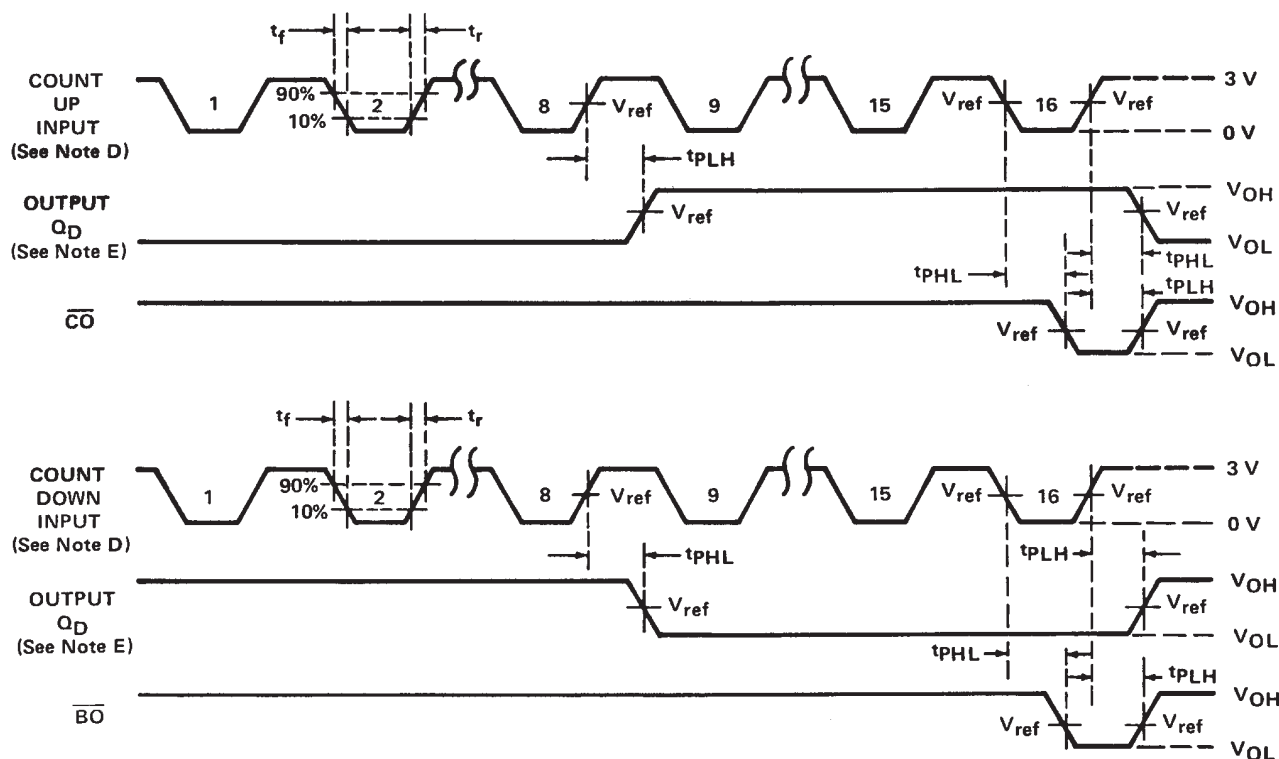


POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

SN54192, SN54193, SN54LS192, SN54LS193,  
 SN74192, SN74193, SN74LS192, SN74LS193  
 SYNCHRONOUS 4-BIT UP/DOWN COUNTERS (DUAL CLOCK WITH CLEAR)

SDLS074 – DECMEBER 1972 – REVISED MARCH 1988

PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS

- NOTES: A. The pulse generators have the following characteristics: PRR  $\approx$  1 MHz,  $Z_{out} \approx 50 \Omega$ , duty cycle = 50%.  
 B.  $C_L$  includes probe and jig capacitance.  
 C. Diodes are 1N3064 or equivalent.  
 D. Count-up and count-down pulse shown are for the '193 and 'LS193 binary counters. Count cycle for '192 and 'LS192 decade counters is 1 through 10.  
 E. Waveforms for outputs  $Q_A$ ,  $Q_B$ , and  $Q_C$  are omitted to simplify the drawing.  
 F.  $t_r$  and  $t_f \leq 7$  ns.  
 G.  $V_{ref}$  is 1.5 V for '192 and '193, 1.3 V for 'LS192 and 'LS193.

FIGURE 2B – PROPAGATION DELAY TIMES