

# CD54/74HC30, CD54/74HCT30

Data sheet acquired from Harris Semiconductor SCHS121D

August 1997 - Revised September 2003

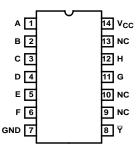
# High Speed CMOS Logic 8-Input NAND Gate

### **Features**

- · Buffered Inputs
- Typical Propagation Delay: 10ns at V<sub>CC</sub> = 5V, C<sub>L</sub> = 15pF, T<sub>A</sub> = 25°C
- Fanout (Over Temperature Range)
- Wide Operating Temperature Range . . . -55°C to 125°C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
  - 2V to 6V Operation
  - High Noise Immunity:  $N_{IL}$  = 30%,  $N_{IH}$  = 30% of  $V_{CC}$  at  $V_{CC}$  = 5V
- HCT Types
  - 4.5V to 5.5V Operation
  - Direct LSTTL Input Logic Compatibility,
    V<sub>IL</sub>= 0.8V (Max), V<sub>IH</sub> = 2V (Min)
  - CMOS Input Compatibility,  $I_I \le 1\mu A$  at  $V_{OL}$ ,  $V_{OH}$

#### **Pinout**

CD54HC30, CD54HCT30 (CERDIP) CD74HC30 (PDIP, SOIC, SOP, TSSOP) CD74HCT30 (PDIP, SOIC) TOP VIEW



## Description

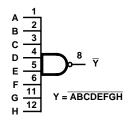
The 'HC30 and 'HCT30 each contain an 8-input NAND gate in one package. They provide the system designer with the direct implementation of the positive logic 8-input NAND function. Logic gates utilize silicon gate CMOS technology to achieve operating speeds similar to LSTTL gates with the low power consumption of standard CMOS integrated circuits. All devices have the ability to drive 10 LSTTL loads. The HCT logic family is functionally pin compatible with the standard LS logic family.

### Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE
CD54HC30F3A	-55 to 125	14 Ld CERDIP
CD54HCT30F3A	-55 to 125	14 Ld CERDIP
CD74HC30E	-55 to 125	14 Ld PDIP
CD74HC30M	-55 to 125	14 Ld SOIC
CD74HC30MT	-55 to 125	14 Ld SOIC
CD74HC30M96	-55 to 125	14 Ld SOIC
CD74HC30NSR	-55 to 125	14 Ld SOP
CD74HC30PW	-55 to 125	14 Ld TSSOP
CD74HC30PWR	-55 to 125	14 Ld TSSOP
CD74HC30PWT	-55 to 125	14 Ld TSSOP
CD74HCT30E	-55 to 125	14 Ld PDIP
CD74HCT30M	-55 to 125	14 Ld SOIC
CD74HCT30MT	-55 to 125	14 Ld SOIC
CD74HCT30M96	-55 to 125	14 Ld SOIC

NOTE: When ordering, use the entire part number. The suffixes 96 and R denote tape and reel. The suffix T denotes a small-quantity reel of 250.

# Functional Diagram

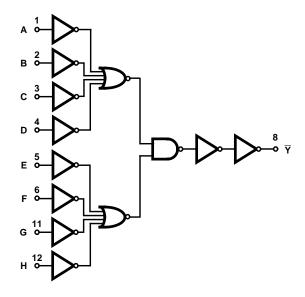


TRUTH TABLE

Α	В	С	D	E	F	G	Н	OUTPUT
L	Х	Х	Х	Х	Х	Х	Х	Н
Х	L	Х	Х	Х	Х	Х	Х	Н
Х	Х	L	Х	Х	Х	Х	Х	Н
Х	Х	Х	L	Х	Х	Х	Х	Н
Х	Х	Х	Х	L	Х	Х	Х	Н
Х	Х	Х	Х	Х	L	Х	Х	Н
Х	Х	Х	Х	Х	Х	L	Х	Н
Х	Х	Х	Х	Х	Х	Х	L	Н
Н	Н	Н	Н	Н	Н	Н	Н	L

NOTE: H = HIGH Voltage Level, L = LOW Voltage Level, X = Irrelevant

# Logic Symbol



# CD54/74HC30, CD54/74HCT30

# **Absolute Maximum Ratings**

DC Supply Voltage, V <sub>CC</sub>	-0.5V to 7V
DC Input Diode Current, I <sub>IK</sub>	
For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$	±20mA
DC Output Diode Current, I <sub>OK</sub>	
For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$	±20mA
DC Output Source or Sink Current per Output Pin, IO	
For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$	±25mA
DC V <sub>CC</sub> or Ground Current, I <sub>CC or</sub> I <sub>GND</sub>	±50mA

## **Operating Conditions**

Temperature Range (T <sub>A</sub> )55°C to 125°C
Supply Voltage Range, V <sub>CC</sub>
HC Types2V to 6V
HCT Types
DC Input or Output Voltage, V <sub>I</sub> , V <sub>O</sub> 0V to V <sub>CC</sub>
Input Rise and Fall Time
2V
4.5V 500ns (Max)
6V

#### **Thermal Information**

Package Thermal Impedance, $\theta_{JA}$ (see Note 1)
E (PDIP) Package80°C/W
M (SOIC) Package86°C/W
NS (SOP) Package76°C/W
PW (TSSOP) Package113°C/W
Maximum Junction Temperature (Hermetic Package or Die) 175°C
Maximum Junction Temperature (Plastic Package) 150°C
Maximum Storage Temperature Range65°C to 150°C
Maximum Lead Temperature (Soldering 10s)300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

#### NOTE:

1. The package thermal impedance is calculated in accordance with JESD 51-7.

### **DC Electrical Specifications**

			ST ITIONS			25°C		-40°C TO +85°C		-55°C T	O 125 <sup>0</sup> C	
PARAMETER	SYMBOL	V <sub>I</sub> (V)	I <sub>O</sub> (mA)	V <sub>CC</sub> (V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNITS
HC TYPES		-	-	-				-				
High Level Input V <sub>IH</sub> Voltage	V <sub>IH</sub>	-	-	2	1.5	-	-	1.5	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	3.15	-	\ \
				6	4.2	-	-	4.2	-	4.2	-	٧
Low Level Input	V <sub>IL</sub>	-	-	2	-	-	0.5	-	0.5	-	0.5	V
Voltage				4.5	-	-	1.35	-	1.35	-	1.35	٧
				6	-	-	1.8	-	1.8	-	1.8	٧
High Level Output	V <sub>OH</sub>	V <sub>IH</sub> or	-0.02	2	1.9	-	-	1.9	-	1.9	-	٧
Voltage CMOS Loads		V <sub>IL</sub>	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	٧
			-0.02	6	5.9	-	-	5.9	-	5.9	-	V
High Level Output			-	-	-	-	-	-	-	-	-	٧
Voltage TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	٧
			-5.2	6	5.48	-	-	5.34	-	5.2	-	٧
Low Level Output	V <sub>OL</sub>	V <sub>IH</sub> or	0.02	2	-	-	0.1	-	0.1	-	0.1	٧
Voltage CMOS Loads		V <sub>IL</sub>	0.02	4.5	-	-	0.1	-	0.1	-	0.1	٧
			0.02	6	-	-	0.1	-	0.1	-	0.1	٧
Low Level Output			-	-	-	-	-	-	-	-	-	٧
Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V
			5.2	6	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	lı	V <sub>CC</sub> or GND	-	6	-	-	±0.1	-	±1	-	±1	μА

# CD54/74HC30, CD54/74HCT30

## DC Electrical Specifications (Continued)

			ST ITIONS		25°C -40°C TO +85°C		O +85°C	-55°C T	O 125 <sup>0</sup> C			
PARAMETER	SYMBOL	V <sub>I</sub> (V)	I <sub>O</sub> (mA)	V <sub>CC</sub> (V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNITS
Quiescent Device Current	Icc	V <sub>CC</sub> or GND	0	6	-	-	2	-	20	-	40	μА
HCT TYPES												
High Level Input Voltage	V <sub>IH</sub>	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	V <sub>IL</sub>	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage CMOS Loads	V <sub>OH</sub>	V <sub>IH</sub> or V <sub>IL</sub>	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
High Level Output Voltage TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
Low Level Output Voltage CMOS Loads	V <sub>OL</sub>	V <sub>IH</sub> or	-0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	II	V <sub>CC</sub> and GND	-	5.5	-		±0.1	-	±1	-	±1	μА
Quiescent Device Current	Icc	V <sub>CC</sub> or GND	0	5.5	-	-	2	-	20	-	40	μА
Additional Quiescent Device Current Per Input Pin: 1 Unit Load (Note 2)	Δl <sub>CC</sub>	V <sub>CC</sub> -2.1	-	4.5 to 5.5	-	100	360	-	450	-	490	μΑ

#### NOTE:

## **HCT Input Loading Table**

INPUT	UNIT LOADS					
All	0.6					

NOTE: Unit Load is  $\Delta I_{CC}$  limit specified in DC Electrical Specifications table, e.g.  $360\mu A$  max at  $25^{\circ}C$ .

## Switching Specifications Input $t_r$ , $t_f$ = 6ns

		TEST	TEST V <sub>CC</sub> CONDITIONS (V)		25°C			-40°C TO 85°C		-55°C TO 125°C	
PARAMETER	SYMBOL	CONDITIONS			TYP	MAX	MIN	MAX	MIN	MAX	UNITS
HC TYPES									-		
Propagation Delay, Input to	t <sub>PLH</sub> , t <sub>PHL</sub>	C <sub>L</sub> = 50pF	2	-	-	130	-	165	-	195	ns
Output (Figure 1)			4.5 26 -	-	33	-	39	ns			
			6	-	-	22	-	28	-	33	ns
Propagation Delay, Data Input to Output Y	t <sub>PLH</sub> , t <sub>PHL</sub>	C <sub>L</sub> = 15pF	5	-	10	-	-	-	-	-	ns

<sup>2.</sup> For dual-supply systems theoretical worst case ( $V_I = 2.4V$ ,  $V_{CC} = 5.5V$ ) specification is 1.8mA.

## CD54/74HC30, CD54/74HCT30

# Switching Specifications Input $t_r$ , $t_f = 6ns$ (Continued)

		TEST	v <sub>cc</sub>		25°C			O 85°C	-55°C TO 125°C		
PARAMETER	SYMBOL	CONDITIONS	(V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNITS
Transition Times (Figure 1)	t <sub>TLH</sub> , t <sub>THL</sub>	C <sub>L</sub> = 50pF	2	-	-	75	-	95	-	110	ns
			4.5	-	-	15	-	19	-	22	ns
			6	-	-	13	-	16	-	19	ns
Input Capacitance	CI	-	-	-	-	10	-	10	-	10	pF
Power Dissipation Capacitance (Notes 3, 4)	C <sub>PD</sub>	-	5	-	25	-	-	-	-	-	pF
HCT TYPES											
Propagation Delay, Input to Output (Figure 2)	t <sub>RHL</sub> , t <sub>PHL</sub>	C <sub>L</sub> = 50pF	4.5	-	-	28	-	35	-	42	ns
Propagation Delay, Data Input to Output Y	t <sub>PLH</sub> , t <sub>PHL</sub>	C <sub>L</sub> = 15pF	5	-	11	-	-	-	-	-	ns
Transition Times (Figure 2)	t <sub>TLH</sub> , t <sub>THL</sub>	C <sub>L</sub> = 50pF	4.5	-	-	15	-	19	-	22	ns
Input Capacitance	C <sub>I</sub>	-	-	-	-	10	-	10	-	10	pF
Power Dissipation Capacitance (Notes 3, 4)	C <sub>PD</sub>	-	5	-	26	-	-	-	-	-	pF

#### NOTES:

- 3.  $C_{\mbox{\scriptsize PD}}$  is used to determine the dynamic power consumption, per gate.
- 4.  $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$  where  $f_i$  = Input Frequency,  $C_L$  = Output Load Capacitance,  $V_{CC}$  = Supply Voltage.

# Test Circuits and Waveforms

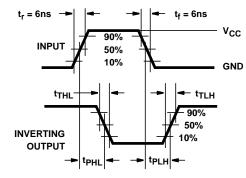


FIGURE 1. HC AND HCU TRANSITION TIMES AND PROPAGA-TION DELAY TIMES, COMBINATION LOGIC

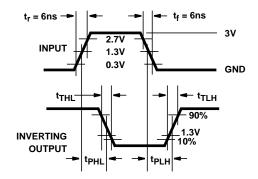


FIGURE 2. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC



## **PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp (3)
5962-8974601CA	ACTIVE	CDIP	J	14	1	TBD	Call TI	N / A for Pkg Type
8404001CA	ACTIVE	CDIP	J	14	1	TBD	Call TI	N / A for Pkg Type
CD54HC30F	ACTIVE	CDIP	J	14	1	TBD	Call TI	N / A for Pkg Type
CD54HC30F3A	ACTIVE	CDIP	J	14	1	TBD	Call TI	N / A for Pkg Type
CD54HCT30F3A	ACTIVE	CDIP	J	14	1	TBD	Call TI	N / A for Pkg Type
CD74HC30E	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD74HC30EE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD74HC30M	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC30M96	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC30M96E4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC30ME4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC30MT	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC30MTE4	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC30NSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC30NSRE4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC30PW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC30PWE4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC30PWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC30PWRE4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC30PWT	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC30PWTE4	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT30E	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD74HCT30EE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD74HCT30M	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT30M96	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT30M96E4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT30ME4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM



### PACKAGE OPTION ADDENDUM

12-Jan-2006

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins P	Package Qty	e Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
CD74HCT30MT	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT30MTE4	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

**Pb-Free** (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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#### 14 LEADS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

# N (R-PDIP-T\*\*)

# PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



# D (R-PDSO-G14)

# PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-012 variation AB.



## **MECHANICAL DATA**

# NS (R-PDSO-G\*\*)

# 14-PINS SHOWN

### PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



## PW (R-PDSO-G\*\*)

#### 14 PINS SHOWN

## PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.

D. Falls within JEDEC MO-153

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