54/7472 01/509
54H/74H72 01/510

JK MASTER/SLAVE FLIP-FLOP
(With AND Inputs)

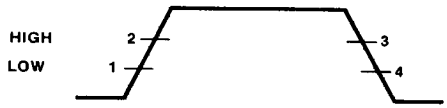
DESCRIPTION — The '72 is a high speed JK master/slave flip-flop with AND gate inputs. The AND gate inputs for entry into the master section are controlled by the clock pulse. The clock pulse also regulates the circuitry which connects the master and slave sections. The sequence of operation is as follows: 1) isolate slave from master; 2) enter information from AND gate inputs to master; 3) disable AND gate inputs; 4) transfer information from master to slave. The logic state of J and K inputs must not be allowed to change when the clock pulse is in a HIGH state.

TRUTH TABLE

INPUTS		OUTPUT
@ t_n		@ t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	Q_n

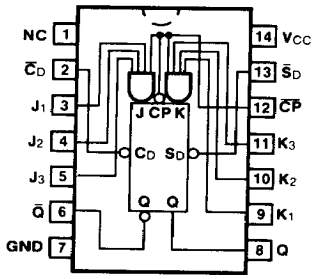
$J = (J_{1A} \bullet J_{1B}) + (J_{2A} \bullet J_{2B})$
$K = (K_{1A} \bullet K_{1B}) + (K_{2A} \bullet K_{2B})$
t_n = Bit time before clock pulse.
t_{n+1} = Bit time after clock pulse.
H = HIGH Voltage Level
L = LOW Voltage Level

CLOCK WAVEFORM

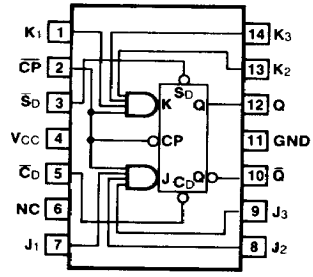


Asynchronous Inputs:
LOW input to $\overline{S}_D$ sets Q to HIGH level
LOW input to $\overline{C}_D$ sets Q to LOW level
Clear and Set are independent of clock
Simultaneous LOW on $\overline{C}_D$ and $\overline{S}_D$ is indeterminate

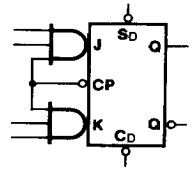
CONNECTION DIAGRAMS
PINOUT A



PINOUT B



LOGIC SYMBOL



VCC = Pin 14 (4)
GND = Pin 7 (11)
NC = Pin 1 (6)

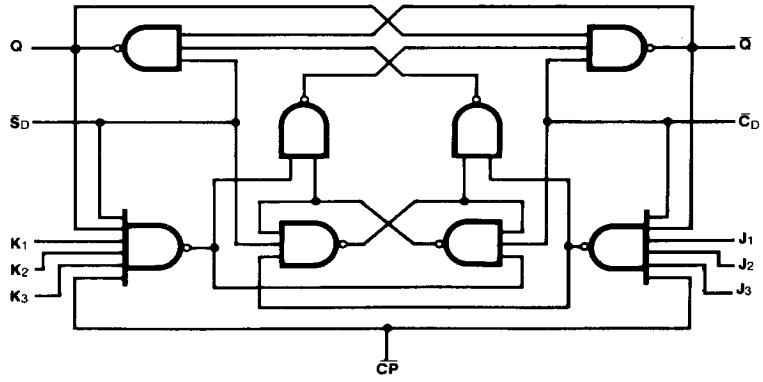
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE: VCC = +5.0 V ±5%, TA = 0°C to +70°C	MILITARY GRADE: VCC = +5.0 V ±10%, TA = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	7472PC, 74H72PC		9A
Ceramic DIP (D)	A	7472DC, 74H72DC	5472DM, 54H72DM	6A
Flatpak (F)	B	7472FC, 74H72FC	5472FM, 54H72FM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW	54/74H (U.L.) HIGH/LOW
$J_1 - J_3$, $K_1 - K_3$	Data Inputs	1.0/1.0	1.25/1.25
$\overline{CP}$	Clock Pulse Input (Active Falling Edge)	2.0/2.0	2.5/2.5
$\overline{C}_D$	Direct Clear Input (Active LOW)	2.0/2.0	2.5/2.5
$\overline{S}_D$	Direct Set Input (Active LOW)	2.0/2.0	2.5/2.5
Q, $\overline{Q}$	Outputs	20/10	12.5/12.5

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74		54/74H		UNITS	CONDITIONS
		Min	Max	Min	Max		
I_{CC}	Power Supply Current		20		25	mA	V_{CC} = Max, V_{CP} = 0 V

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74 C_L = 15 pF, R_L = 400 Ω		54/74H C_L = 25 pF, R_L = 280 Ω		UNITS	CONDITIONS
		Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	15		25		MHz	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}$ to Q or $\overline{Q}$		25 40		21 27	ns	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay $\overline{S}_D$ or $\overline{C}_D$ to Q or $\overline{Q}$		25 40		13 24	ns	Figs. 3-1, 3-10

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25° C

SYMBOL	PARAMETER	54/74		54/74H		UNITS	CONDITIONS
		Min	Max	Min	Max		
t_s (H) t_s (L)	Setup Time J_n or K_n to $\overline{CP}$	0		0		ns	Fig. 3-18
t_h (H) t_h (L)	Hold Time J_n or K_n to $\overline{CP}$	0		0		ns	Fig. 3-18
t_w (H) t_w (L)	$\overline{CP}$ Pulse Width	20 47		12 28		ns	Fig. 3-9
t_w (L)	$\overline{S}_D$ or $\overline{C}_D$ Pulse Width LOW	25		16		ns	Fig. 3-10