

Proiect CID

| PROIECT CID | Popa Carina

(10)

(11)

λ	clk	ld	en	Action
0	x	x	x	reset
1	\downarrow	1	x	load
1	\downarrow	0	1	count
otherwise				wait

MULTIPLEXOR 11: MUX 2:1 3: poti logica

$Q_D Q_C Q_B Q_A$	Cl	Ld	Em	Action	DCBA
0000	x	x	x	—	xxxx
0001	1	1	x	\uparrow	0100
0010	1	1	x	\uparrow	0111
0011	1	1	x	\uparrow	0001
0100	1	1	x	\uparrow	0010
0101	1	0	1	MA	xxxx
0110	1	1	x	\uparrow	0011
0111	1	1	x	\uparrow	0101

Cl = 1
Em = 1

$Q_D Q_C$

Q_A	00	01	11	10
0	1	1		
1	1		1	1

$$C = \overline{Q_C} \cdot \overline{Q_A} + \overline{Q_C} \cdot \overline{Q_B} + Q_C \cdot Q_A$$

$Q_D Q_C$

Q_A	00	01	11	10
0	1	1	1	1
1				1

$$B = \overline{Q_A}$$

$Q_D Q_C$

Q_A	00	01	11	10
0	1	1	1	1
1	1	1		1

$$A = Q_B$$

①

Pentru C

$Q_C Q_B Q_A$	C
000	x
001	1
010	1
011	0
100	0
101	x
110	0
111	1

Q_B/Q_A	0	1
0	0	1
1	1	1

Q_B/Q_A	0	1
0	0	1
1	1	1

$$J_0 = \overline{Q_B} + \overline{Q_A}$$

$$J_1 = Q_A$$

C

Pentru B

$Q_C Q_B Q_A$	B
000	x
001	0
010	1
011	0
100	1
101	x
110	1
111	0

Q_B/Q_A	0	1
0	0	1
1	1	1

Q_B/Q_A	0	1
0	0	1
1	1	1

$$J_0 = \overline{Q_A}$$

$$J_1 = \overline{Q_A}$$

B

Pentru A

$Q_C Q_B Q_A$	A
000	x
001	0
010	1
011	1
100	0
101	x
110	1
111	1

Q_B/Q_A	0	1
0	0	1
1	1	1

Q_B/Q_A	0	1
0	0	1
1	1	1

$$J_0 = Q_B$$

$$J_1 = Q_B$$

A

Pentru Ld

$Q_C Q_B Q_A$	Ld
000	x
001	1
010	1
011	1
100	1
101	0
110	1
111	1

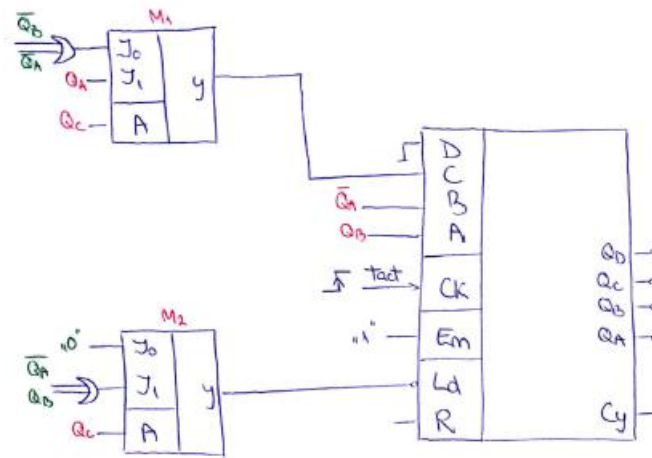
$$J_0 = '0'$$

Q_B/Q_A	0	1
0	1	1
1	1	1

$$J_1 = \overline{Q_A} + Q_B$$

2

Popa Carina-Ariana
Grupa 2123, semigrupa 2
Proiect CID



Popa Carina-Ariana
Grupa 2123, semigrupa 2
Proiect CID

➤ Simulare

project_CID_Carina_POPA - [C:/Users/Carina/Desktop/project_CID_Carina_Popa/project_CID_Carina_POPA/project_CID_Carina_POPA.xpr] - Vivado 2021.2

File Edit Flow Tools Reports Window Layout View Run Help Q: Quick Access Ready

Flow Navigator SIMULATION - Behavioral Simulation - Functional - sim_1 - simulare_Carina_POPA

PROJECT MANAGER

- Settings
- Add Sources
- Language Templates
- IP Catalog
- IP INTEGRATOR
 - Create Block Design
 - Open Block Design
 - Generate Block Design
- SIMULATION**
 - Run Simulation
- RTL ANALYSIS
 - Open Elaborated Design
- SYNTHESIS
 - Run Synthesis
 - Open Synthesized Design
- IMPLEMENTATION
 - Run Implementation
 - Open Implemented Design
- PROGRAM AND DEBUG

Scope Sources Objects Protocol Instance

Name Design... Block T...
sim simulare_1 VHDL Ent
automat1 VHDL Ent

Name Value Data T...
clk 1 Logic
clk 0 Logic
q[3: 5 Array

automat.vhd counter.vhd mux2.vhd simulare_Carina_POPA.vhd Untitled 1

Name Value
clk 0
clk 0
q[3:0] 1

120.000 ns 140.000 ns 160.000 ns 180.000 ns 200.000 ns 220.000 ns 240.000 ns

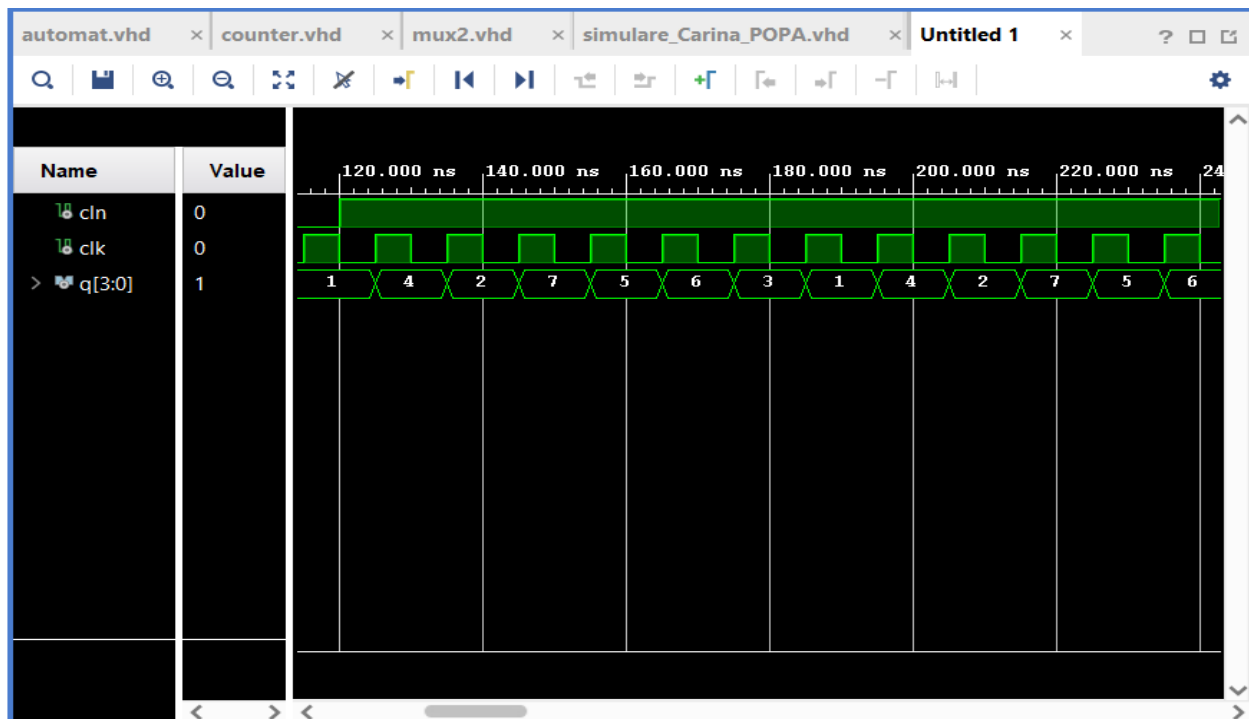
1 4 2 7 5 6 3 1 4 2 7 5 6

Tcl Console Messages Log

```
# run 1000ns  
INFO: [USF-XSim-96] XSim completed. Design snapshot 'simulare_Carina_POPA_behav' loaded.  
INFO: [USF-XSim-97] XSim simulation ran for 1000ns  
launch_simulation: Time (s): cpu = 00:00:07 ; elapsed = 00:00:11 . Memory (MB): peak = 1594.047 ; gain = 0.000
```

Activate Windows
Go to Settings to activate Windows.

Sim Time: 1 us



➤ Sursă counter

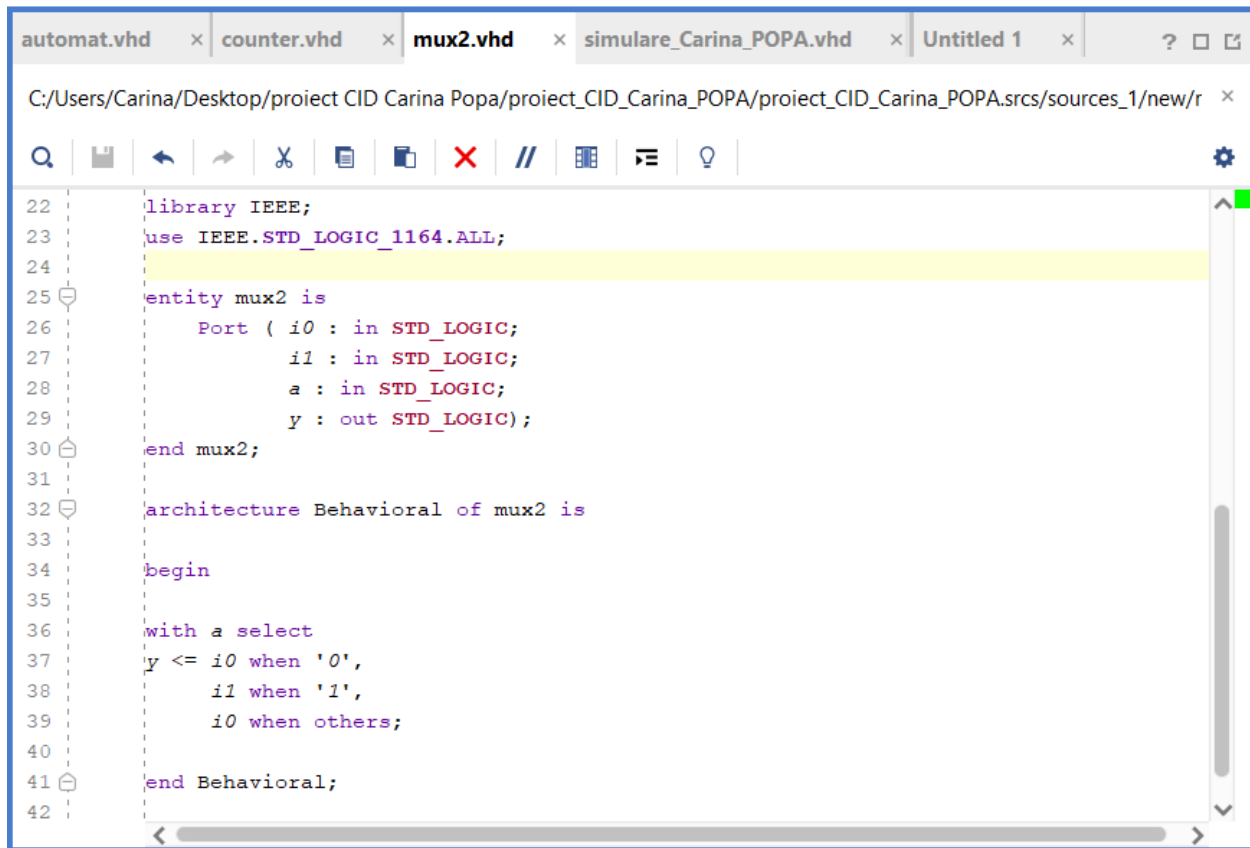
```
automat.vhd x counter.vhd x mux2.vhd x simulare_Carina_POPA.vhd x Untitled 1 x
C:/Users/Carina/Desktop/proiect CID Carina Popa/proiect_CID_Carina_POPA/proiect_CID_Carina_POPA.srcs/sources_1/new/c

22 library IEEE;
23 use IEEE.STD_LOGIC_1164.ALL;
24 use ieee.std_logic_arith.all;
25 use ieee.std_logic_unsigned.all;
26
27 entity counter is
28     Port ( d : in STD_LOGIC_VECTOR (3 downto 0);
29           clk : in STD_LOGIC;
30           pt : in STD_LOGIC;
31           ldn : in STD_LOGIC;
32           oln : in STD_LOGIC;
33           q : out STD_LOGIC_VECTOR (3 downto 0);
34           cy : out STD_LOGIC);
35 end counter;
36
37 architecture Behavioral of counter is
38
39     signal qint: std_logic_vector(3 downto 0);
40
41 begin
42
```

```
automat.vhd x counter.vhd x mux2.vhd x simulare_Carina_POPA.vhd x Untitled 1 x
C:/Users/Carina/Desktop/proiect CID Carina Popa/proiect_CID_Carina_POPA/proiect_CID_Carina_POPA.srcs/sources_1/new/c

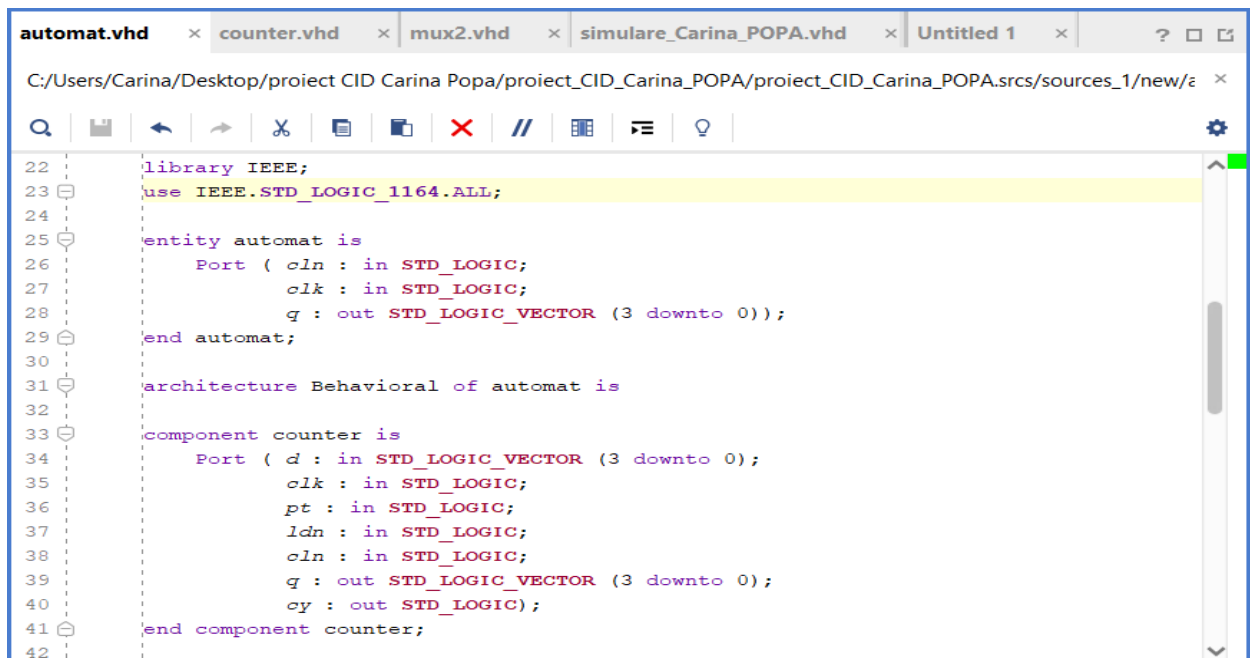
39     signal qint: std_logic_vector(3 downto 0);
40
41     begin
42
43     process (clk, oln)
44     begin
45         if oln='0' then qint<="0001";
46         elsif rising_edge(clk) then
47             if ldn='1' then qint<=d;
48             elsif pt='1' then qint<=qint+1;
49             else qint<=qint;
50             end if;
51         end if;
52     end process;
53
54     q<=qint;
55     cy<='1' when (qint="1111" and pt='1') else '0';
56
57 end Behavioral;
58
```

➤ Sursă MUX



```
22 library IEEE;
23 use IEEE.STD_LOGIC_1164.ALL;
24
25 entity mux2 is
26     Port ( i0 : in STD_LOGIC;
27           i1 : in STD_LOGIC;
28           a : in STD_LOGIC;
29           y : out STD_LOGIC);
30 end mux2;
31
32 architecture Behavioral of mux2 is
33
34 begin
35
36     with a select
37     y <= i0 when '0',
38         i1 when '1',
39         i0 when others;
40
41 end Behavioral;
42
```

➤ Sursă automat



```
22 library IEEE;
23 use IEEE.STD_LOGIC_1164.ALL;
24
25 entity automat is
26     Port ( cln : in STD_LOGIC;
27           clk : in STD_LOGIC;
28           q : out STD_LOGIC_VECTOR (3 downto 0));
29 end automat;
30
31 architecture Behavioral of automat is
32
33 component counter is
34     Port ( d : in STD_LOGIC_VECTOR (3 downto 0);
35           clk : in STD_LOGIC;
36           pt : in STD_LOGIC;
37           ldn : in STD_LOGIC;
38           cln : in STD_LOGIC;
39           q : out STD_LOGIC_VECTOR (3 downto 0);
40           cy : out STD_LOGIC);
41 end component counter;
42
```

Popa Carina-Ariana
Grupa 2123, semigrupa 2
Project CID

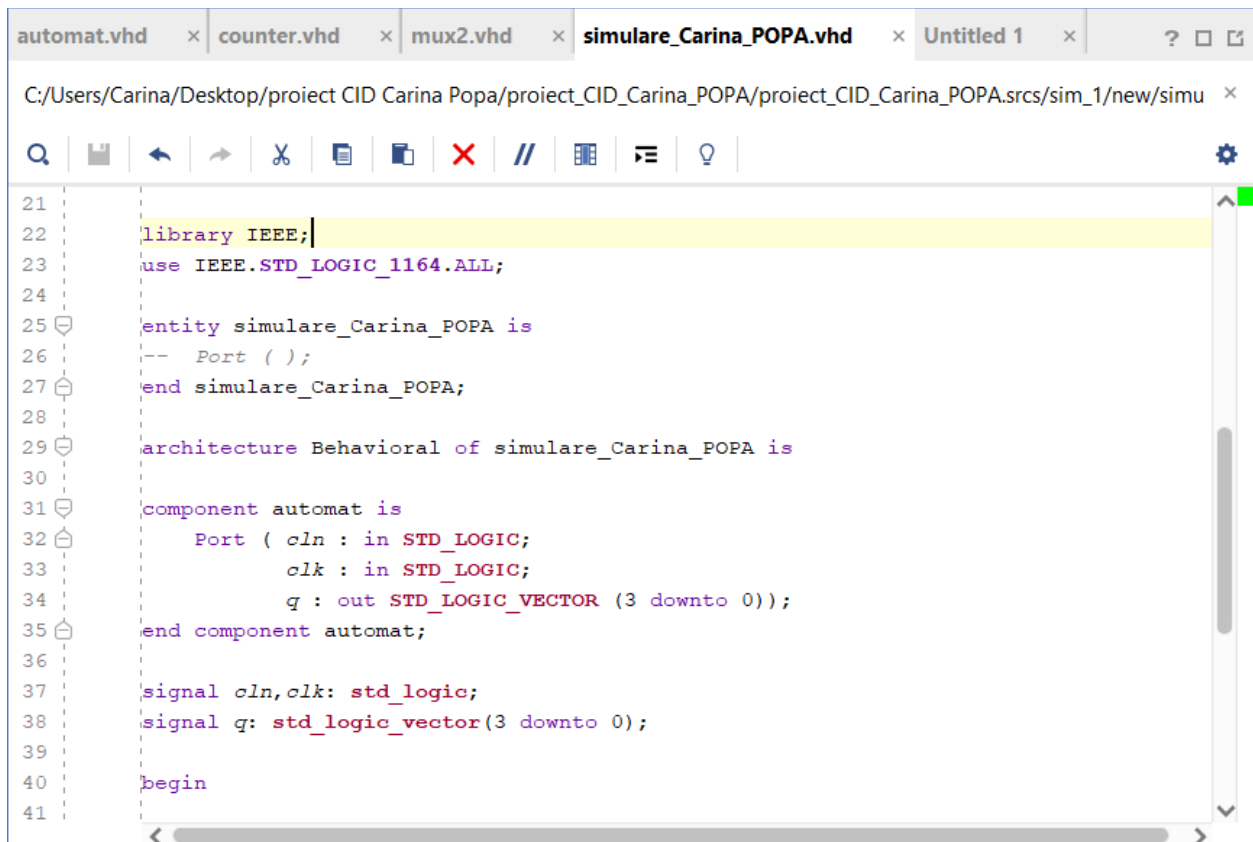
```
automat.vhd x counter.vhd x mux2.vhd x simulare_Carina_POPA.vhd x Untitled 1 x ? □ ↗
C:/Users/Carina/Desktop/proiect CID Carina Popa/proiect_CID_Carina_POPA/proiect_CID_Carina_POPA.srscs/sources_1/new/ε x

41 end component counter;
42
43 component mux2 is
44     Port ( i0 : in STD_LOGIC;
45           i1 : in STD_LOGIC;
46           a : in STD_LOGIC;
47           y : out STD_LOGIC);
48 end component mux2;
49
50 signal qint: std_logic_vector(3 downto 0);
51 signal pt, ldn: std_logic;
52 signal d: std_logic_vector(3 downto 0);
53
54 begin
55     u: counter port map(d=>d,
56                        clk=>clk,
57                        pt=>pt,
58                        cln=>cln,
59                        ldn=>ldn,
60                        q=>qint);
61     q <= qint;
```

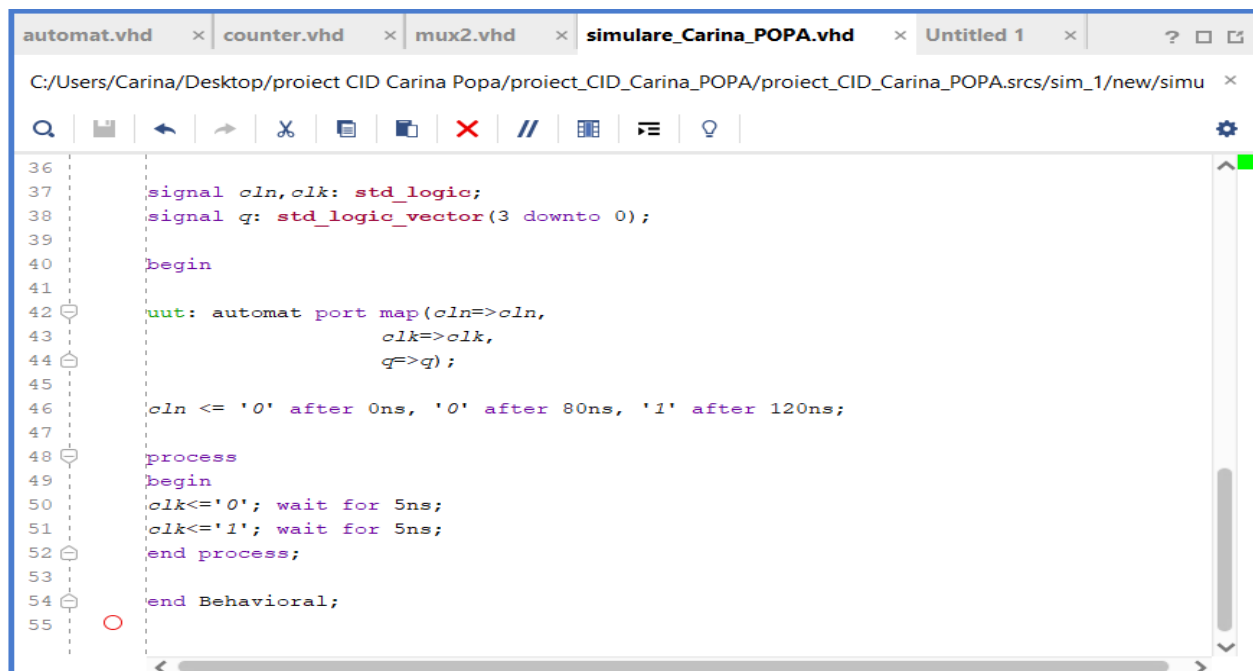
```
automat.vhd x counter.vhd x mux2.vhd x simulare_Carina_POPA.vhd x Untitled 1 x ? □ ↗
C:/Users/Carina/Desktop/proiect CID Carina Popa/proiect_CID_Carina_POPA/proiect_CID_Carina_POPA.srscs/sources_1/new/ε x

60 q=>qint);
61 q <= qint;
62 pt<='1';
63 d(3)<='0'; --pt D
64 d(0)<=qint(1); --pt A
65 d(1)<=not qint(0); --pt B
66
67 --pt C
68 u1: mux2 port map(i0=>(not qint(0)) or (not qint(1)),
69                  i1=>qint(0),
70                  a=>qint(2),
71                  y=>d(2));
72
73 --pt ld
74 u3: mux2 port map(i0=>'1',
75                  i1=>(not qint(0)) or (qint(1)),
76                  a=>qint(2),
77                  y=>ldn);
78 end Behavioral;
79
```

➤ Simulare



```
21
22 library IEEE;
23 use IEEE.STD_LOGIC_1164.ALL;
24
25 entity simulare_Carina_POPA is
26 -- Port ( );
27 end simulare_Carina_POPA;
28
29 architecture Behavioral of simulare_Carina_POPA is
30
31 component automat is
32 Port ( cIn : in STD_LOGIC;
33        clk : in STD_LOGIC;
34        q : out STD_LOGIC_VECTOR (3 downto 0));
35 end component automat;
36
37 signal cIn, clk: std_logic;
38 signal q: std_logic_vector(3 downto 0);
39
40 begin
41
```



```
36
37 signal cIn, clk: std_logic;
38 signal q: std_logic_vector(3 downto 0);
39
40 begin
41
42 uut: automat port map(cIn=>cIn,
43                       clk=>clk,
44                       q=>q);
45
46 cIn <= '0' after 0ns, '0' after 80ns, '1' after 120ns;
47
48 process
49 begin
50   clk<='0'; wait for 5ns;
51   clk<='1'; wait for 5ns;
52 end process;
53
54 end Behavioral;
55
```