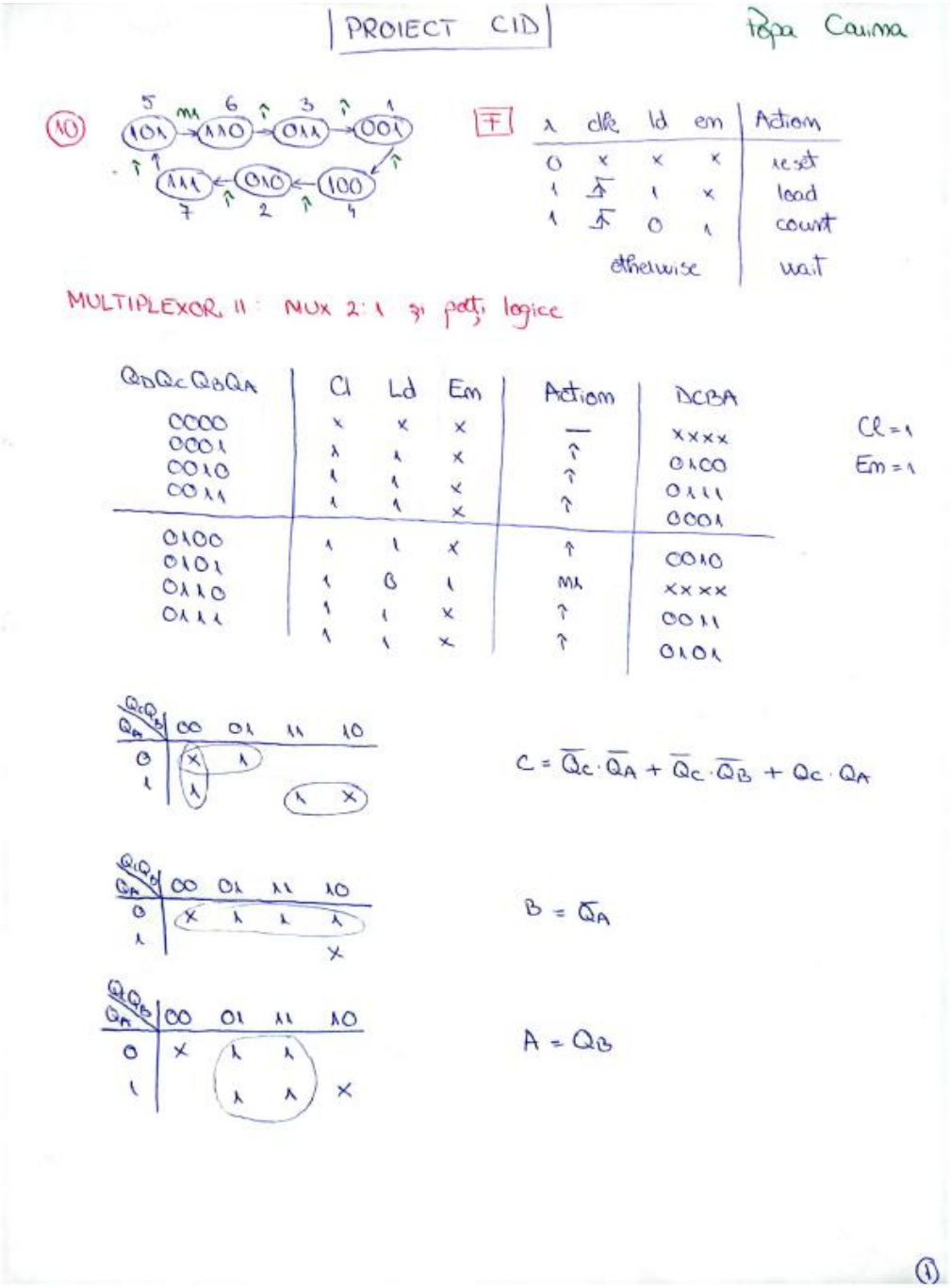
Popa Carina-Ariana
Grupa 2123, semigrupa 2
Proiect CID

Proiect CID



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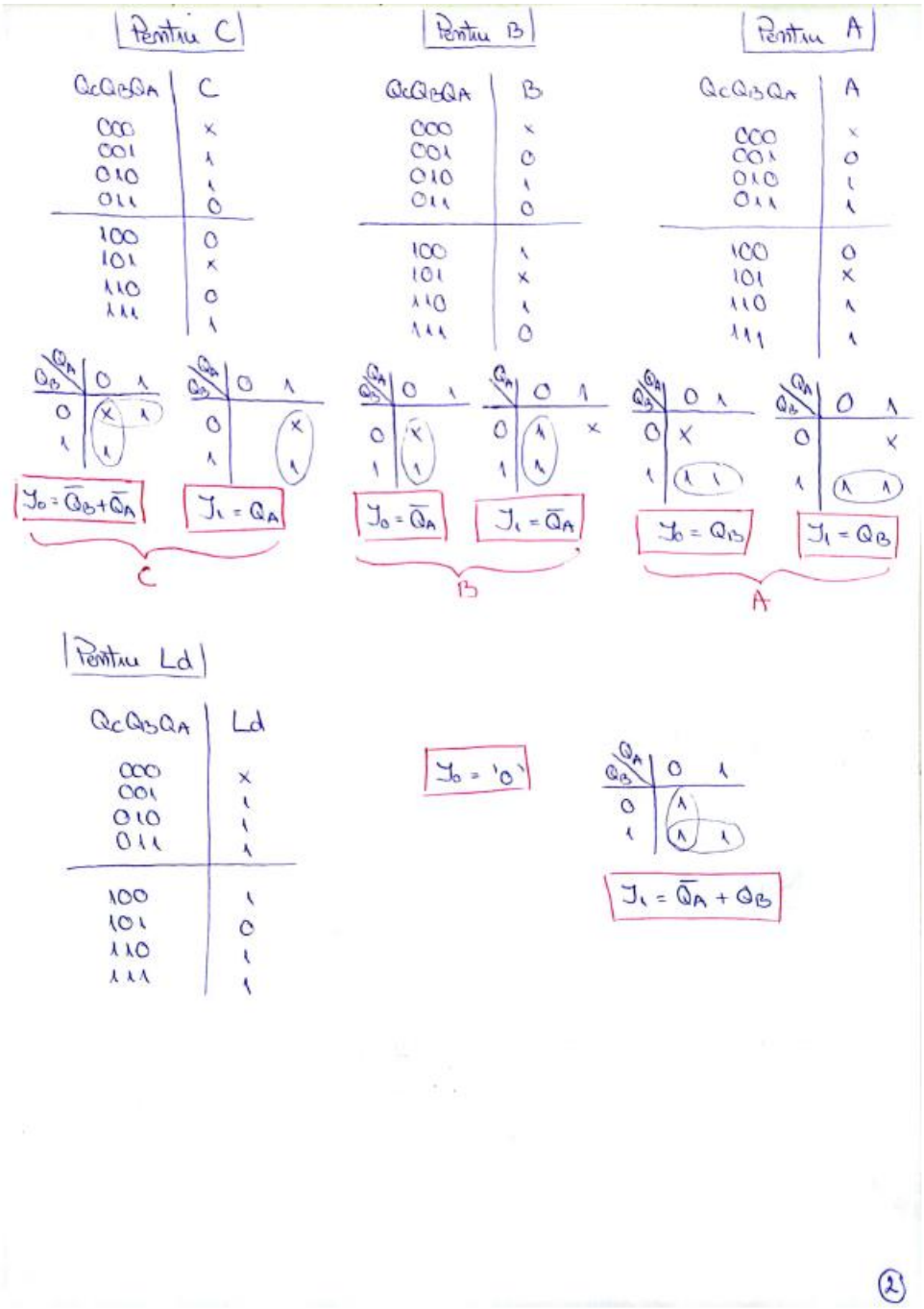
Proiect CID



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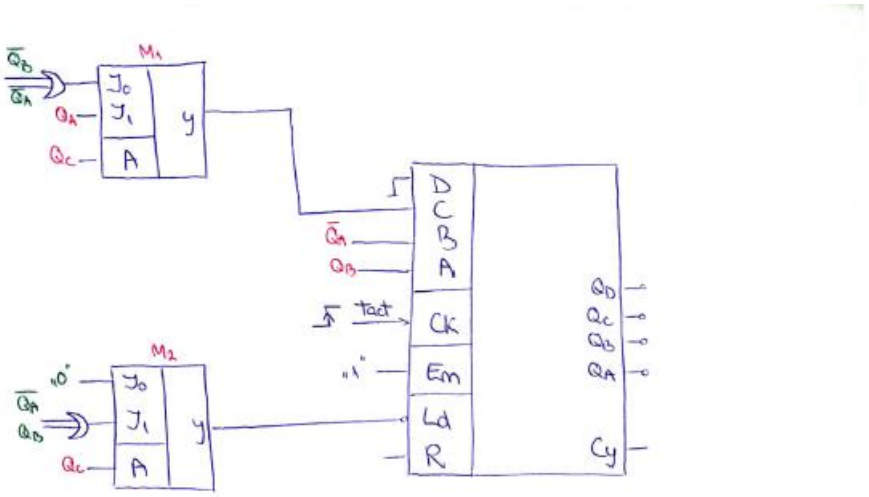
Grupa 2123, semigrupa 2
Proiect CID



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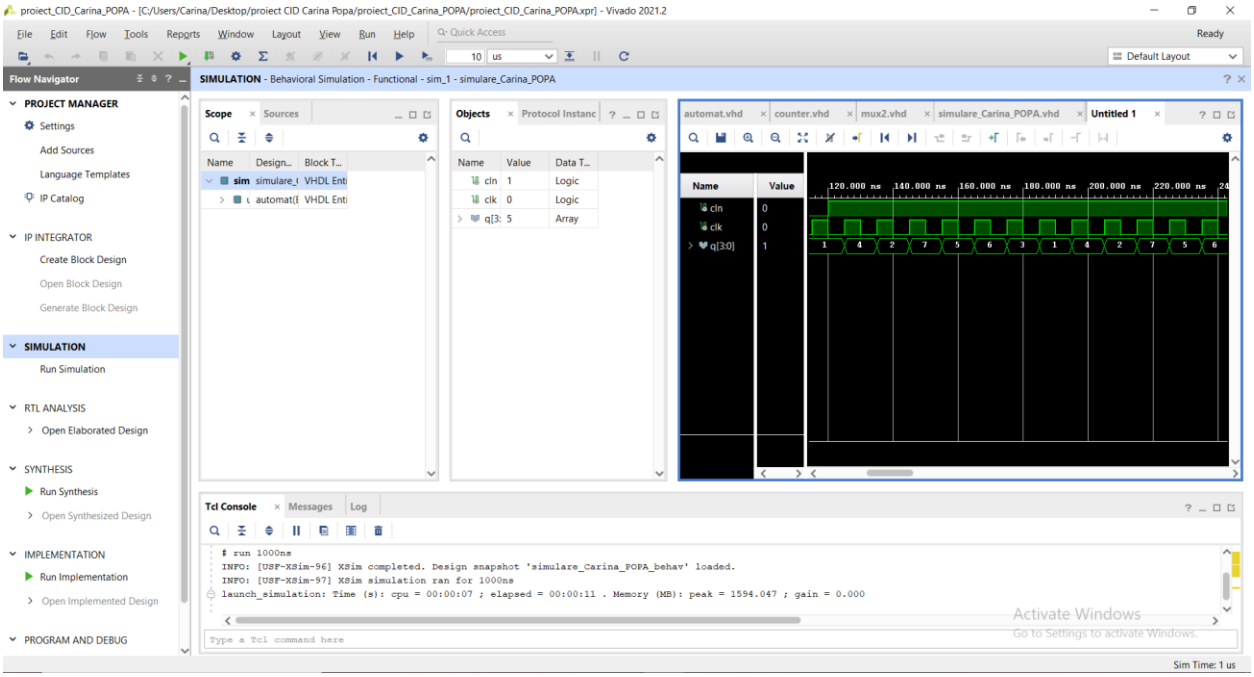
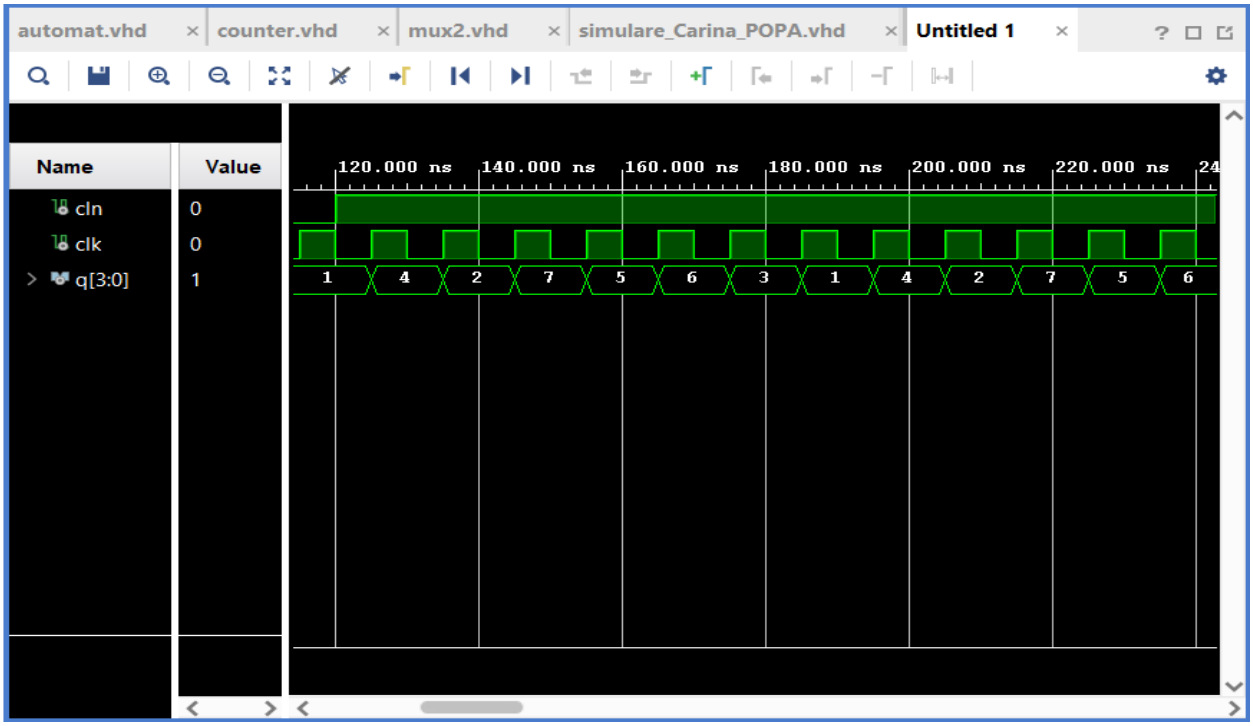
Grupa 2123, semigrupa 2
Proiect CID

- Simulare





Popa Carina-Ariana
Grupa 2123, semigrupa 2
Proiect CID

- Sursă counter

automat.vhd | counter.vhd | mux2.vhd | simulare_Carina_POPA.vhd | Untitled 1

C:/Users/Carina/Desktop/proiect CID Carina Popa/proiect_CID_Carina_POPA/proiect_CID_Carina_POPA.srcs/sources_1/new/c

```
22  library IEEE;
23  use IEEE.STD_LOGIC_1164.ALL;
24  use ieee.std_logic_arith.all;
25  use ieee.std_logic_unsigned.all;
26
27  entity counter is
28      Port ( d : in STD_LOGIC_VECTOR (3 downto 0);
29             clk : in STD_LOGIC;
30             pt : in STD_LOGIC;
31             ldn : in STD_LOGIC;
32             cln : in STD_LOGIC;
33             q : out STD_LOGIC_VECTOR (3 downto 0);
34             cy : out STD_LOGIC);
35  end counter;
36
37  architecture Behavioral of counter is
38
39  signal qint: std_logic_vector(3 downto 0);
40
41  begin
42
```

automat.vhd | counter.vhd | mux2.vhd | simulare_Carina_POPA.vhd | Untitled 1

C:/Users/Carina/Desktop/proiect CID Carina Popa/proiect_CID_Carina_POPA/proiect_CID_Carina_POPA.srcs/sources_1/new/c

```
39  signal qint: std_logic_vector(3 downto 0);
40
41  begin
42
43  process (clk, cln)
44  begin
45      if cln='0' then qint<="0001";
46      elsif rising_edge(clk) then
47          if ldn='1' then qint<=d;
48          elsif pt='1' then qint<=qint+1;
49      else qint<=qint;
50          end if;
51      end if;
52  end process;
53
54  q<=qint;
55  cy<='1' when (qint="1111" and pt='1') else '0';
56
57  end Behavioral;
58
```

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Proiect CID

- Sursă MUX

automat.vhd | counter.vhd | mux2.vhd | simulare_Carina_POPA.vhd | Untitled 1

C:/Users/Carina/Desktop/proiect CID Carina Popa/proiect_CID_Carina_POPA/proiect_CID_Carina_POPA.srcs/sources_1/new/r

```
22  library IEEE;
23  use IEEE.STD_LOGIC_1164.ALL;
24
25  entity mux2 is
26      Port ( i0 : in STD_LOGIC;
27             i1 : in STD_LOGIC;
28             a : in STD_LOGIC;
29             y : out STD_LOGIC);
30  end mux2;
31
32  architecture Behavioral of mux2 is
33
34  begin
35
36  with a select
37  y <= i0 when '0',
38       i1 when '1',
39       i0 when others;
40
41  end Behavioral;
42
```

- Sursă automat

automat.vhd | counter.vhd | mux2.vhd | simulare_Carina_POPA.vhd | Untitled 1

C:/Users/Carina/Desktop/proiect CID Carina Popa/proiect_CID_Carina_POPA/proiect_CID_Carina_POPA.srcs/sources_1/new/a

```
22  library IEEE;
23  use IEEE.STD_LOGIC_1164.ALL;
24
25  entity automat is
26      Port ( cln : in STD_LOGIC;
27             clk : in STD_LOGIC;
28             q : out STD_LOGIC_VECTOR (3 downto 0));
29  end automat;
30
31  architecture Behavioral of automat is
32
33  component counter is
34      Port ( d : in STD_LOGIC_VECTOR (3 downto 0);
35             clk : in STD_LOGIC;
36             pt : in STD_LOGIC;
37             ldn : in STD_LOGIC;
38             cln : in STD_LOGIC;
39             q : out STD_LOGIC_VECTOR (3 downto 0);
40             cy : out STD_LOGIC);
41  end component counter;
42
```

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Proiect CID

automat.vhd | counter.vhd | mux2.vhd | simulare_Carina_POPA.vhd | Untitled 1

C:/Users/Carina/Desktop/proiect CID Carina Popa/proiect_CID_Carina_POPA/proiect_CID_Carina_POPA.srcs/sources_1/new/a

```
41  end component counter;
42
43  component mux2 is
44      Port ( i0 : in STD_LOGIC;
45             i1 : in STD_LOGIC;
46             a : in STD_LOGIC;
47             y : out STD_LOGIC);
48  end component mux2;
49
50  signal qint: std_logic_vector(3 downto 0);
51  signal pt, ldn: std_logic;
52  signal d: std_logic_vector(3 downto 0);
53
54  begin
55   u: counter port map(d=>d,
56                       clk=>clk,
57                       pt=>pt,
58                       cln=>cln,
59                       ldn=>ldn,
60                       q=>qint);
61   q <= qint;
```

automat.vhd | counter.vhd | mux2.vhd | simulare_Carina_POPA.vhd | Untitled 1

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```
60                      q=>qint);
61   q <= qint;
62   pt<='1';
63   d(3)<='0'; --pt D
64   d(0)<=qint(1); --pt A
65   d(1)<=not qint(0); --pt B
66
67  --pt C
68  u1: mux2 port map(i0=>(not qint(0)) or (not qint(1)),
69                    i1=>qint(0),
70                    a=>qint(2),
71                    y=>d(2));
72  --pt ld
73  u3: mux2 port map(i0=>'1',
74                    i1=>(not qint(0)) or (qint(1)),
75                    a=>qint(2),
76                    y=>ldn);
77
78  end Behavioral;
79
```

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Grupa 2123, semigrupa 2
Proiect CID

- Simulare

automat.vhd | counter.vhd | mux2.vhd | simulare_Carina_POPA.vhd | Untitled 1

C:/Users/Carina/Desktop/proiect CID Carina Popa/proiect_CID_Carina_POPA/proiect_CID_Carina_POPA.srcs/sim_1/new/simu

```
21
22      library IEEE;
23      use IEEE.STD_LOGIC_1164.ALL;
24
25      entity simulare_Carina_POPA is
26      --  Port ( );
27      end simulare_Carina_POPA;
28
29      architecture Behavioral of simulare_Carina_POPA is
30
31      component automat is
32          Port ( cln : in STD_LOGIC;
33                 clk : in STD_LOGIC;
34                 q : out STD_LOGIC_VECTOR (3 downto 0));
35      end component automat;
36
37      signal cln,clk: std_logic;
38      signal q: std_logic_vector(3 downto 0);
39
40      begin
41
```

automat.vhd | counter.vhd | mux2.vhd | simulare_Carina_POPA.vhd | Untitled 1

C:/Users/Carina/Desktop/proiect CID Carina Popa/proiect_CID_Carina_POPA/proiect_CID_Carina_POPA.srcs/sim_1/new/simu

```
36
37      signal cln,clk: std_logic;
38      signal q: std_logic_vector(3 downto 0);
39
40      begin
41
42      uut: automat port map(cln=>cln,
43                            clk=>clk,
44                            q=>q);
45
46      cln <= '0' after 0ns, '0' after 80ns, '1' after 120ns;
47
48      process
49      begin
50      clk<='0'; wait for 5ns;
51      clk<='1'; wait for 5ns;
52      end process;
53
54      end Behavioral;
55
```