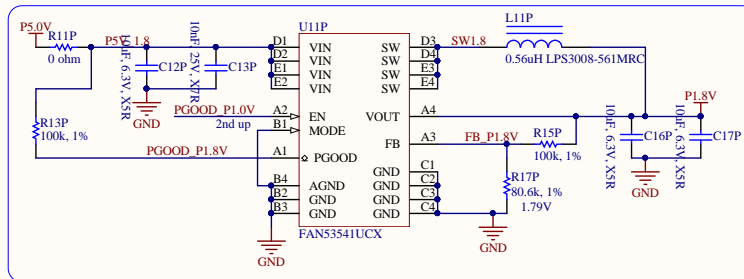
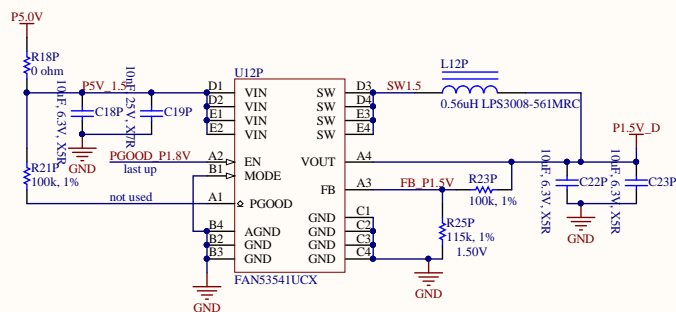


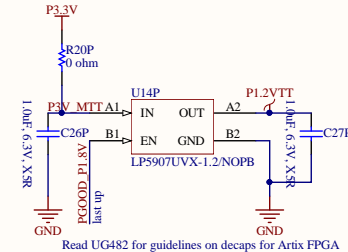
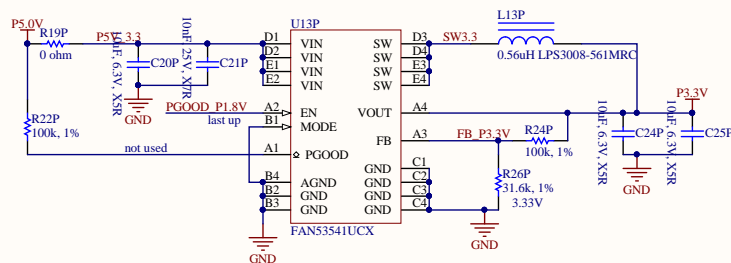
Power-on domain #1 - VCCINT/VCCBRAM



Power-on domain #2 - VCCAUX



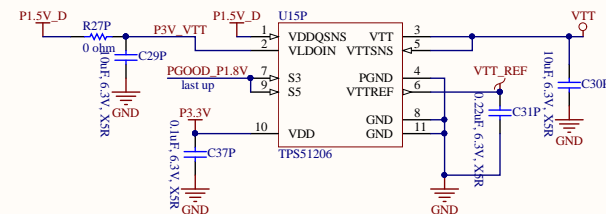
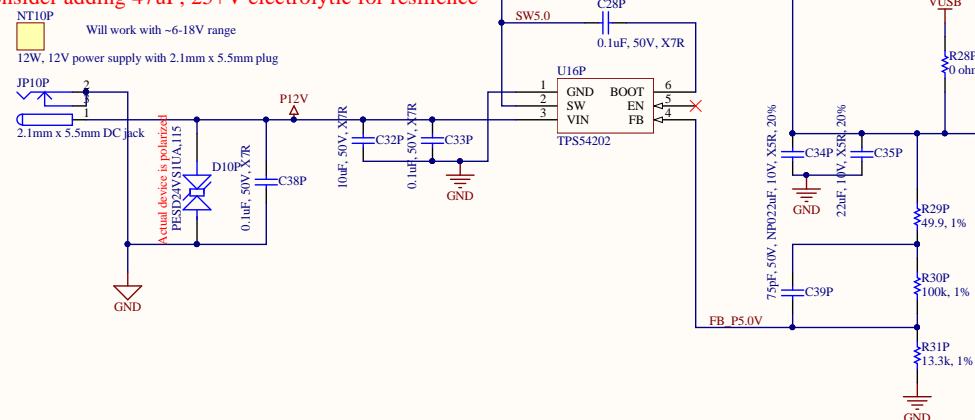
Power-on domain #3 - VCCO



Read UG482 for guidelines on decaps for Artix FPGA

Master down regulator - 5V allows lower-I switcher to be used

Add 12V polarized pin header for fan option  
Consider adding 47uF, 25+V electrolytic for resilience



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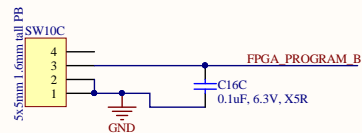
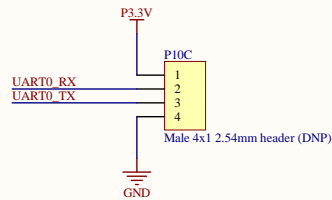


Note: mirrored pinout because connector faces "down" on FPGA board

P11C  
Female 10x2 2.54mm header

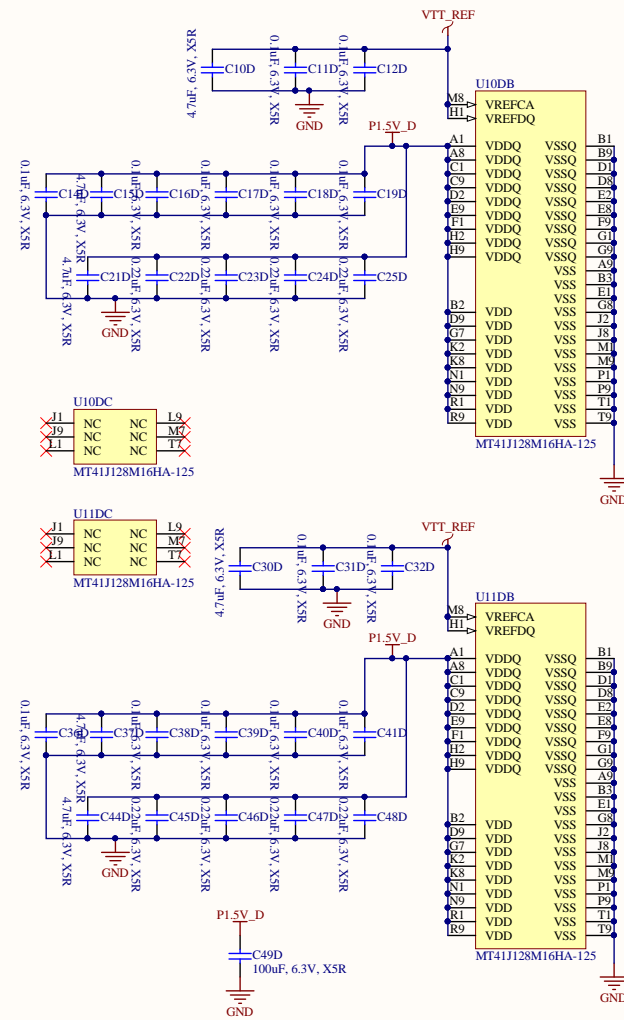
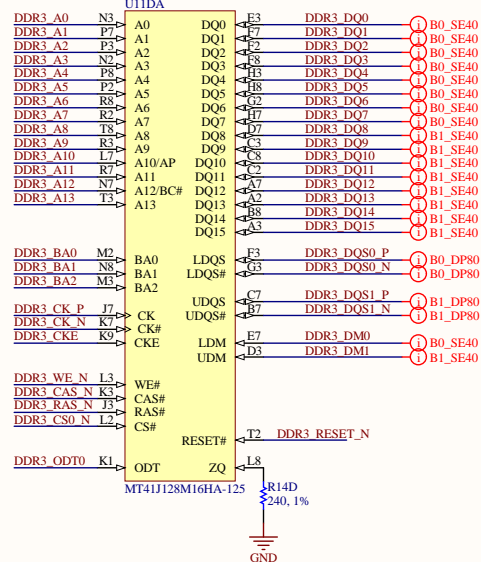
P5.0V

Use "34" option for long tails  
Use "44" option for more connector clearance  
With "34" option, standoff height is 0.635" / 16.13mm  
With "44" option, standoff height is 0.735" / 18.67mm



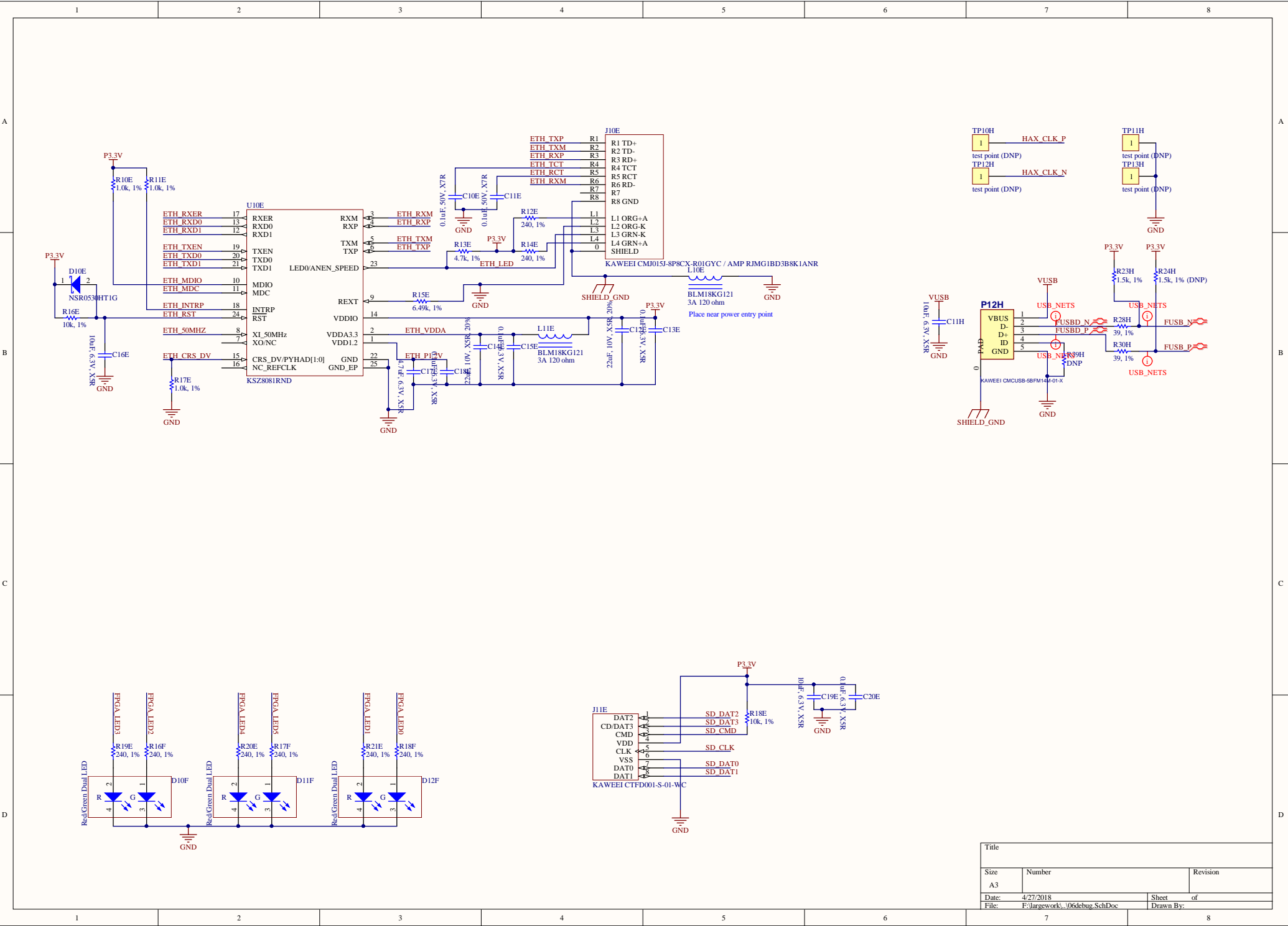
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