Carl Richardson [redacted] [redacted]

Design and simulation of a DAC and a Power supply

Introduction

The goal of this investigation is to design a DAC which can be powered from a mains supply.
This report covers the design of a 4-bit DAC and quantifies its performance. The same is done for three different power supply configurations along with a discussion of the advantages and disadvantages of each one.

Design

4-bit Digital to Analogue converter (DAC)

The 4-bit DAC was implemented by the combination of a weighted summing op-amp and a unity gain inverter. The weighted summing op-amp circuit is shown in figure 1.

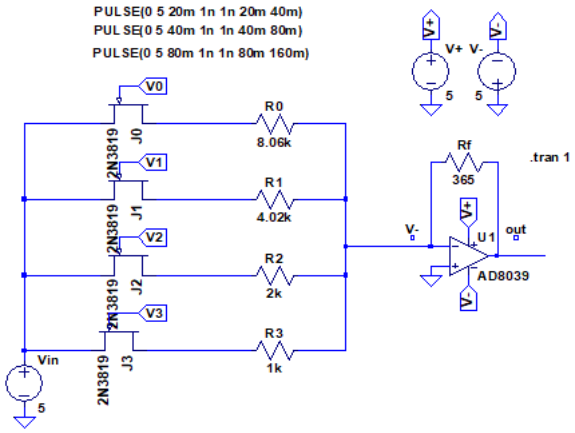

Figure 1: The weighted summing op-amp circuit

The resistor values R_0 to R_3 needed to be accurate because the current flowing through them had to be proportional to the weighting of their corresponding digital input. The resistors were chosen from the E96 series which provided a high accuracy with low component tolerances. The resistor values were chosen as they were the closest from the E96 series which achieved the desired weighting. The JFETS were controlled by ideal digital sources. JFETs were chosen over BJTs because of their high input impedance. This meant less input current was drawn making the circuit more power efficient. The AD8039 op-amp had a supply voltage range of 3-12V and a 425V/us slew rate. These were desirable traits because it meant the device didn't require a precise power supply voltage and it had a fast response to a change in input. The specification required a maximum output of around 3V, so the value of the feedback resistor had to provide a suitable gain. The op-amp was configured as an inverting amplifier, so the output voltage was negative. As shown in figure 2, a unity gain inverting op-amp was added to the end of the circuit to make the output positive.

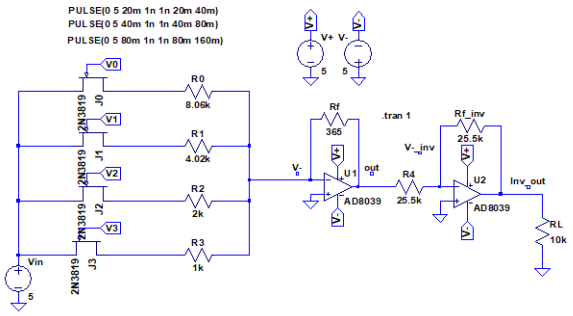

Figure 2: Weighted summing amplifier with a unity gain inverting op-amp

The 25.5KΩ resistor was used as it was large enough to prevent a significant current flowing from the output of the summing amplifier to the input of the unity gain buffer. The value of the feedback resistor had to be the same to achieve unity gain.

AC Power Supply

Three different power supply configurations were simulated. The specification required the power supply to convert a 230Vrms 50Hz mains supply to a dual rail output of ±5V. This meant that each configuration required a step-down transformer and a full bridge rectifier as shown in figure 3.

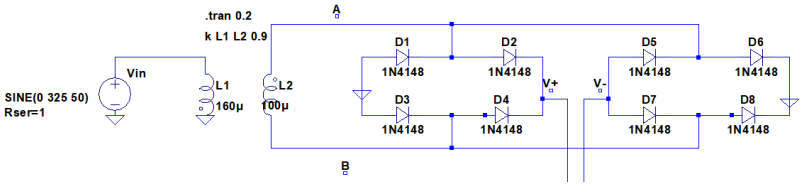

Figure 3: The common components of the different power supply configurations

A non-ideal transformer was used. The model incorporated 10nF of parallel capacitance in each winding and 10% leakage current. The ratio of each winding's inductance varied between configurations. Two full bridge rectifier circuits were used to so that both the positive and negative rectified waveforms could be accessed. A non-ideal diode (1N4148) was used in the bridge. This was chosen due to its high breakdown voltage, V_{BD} = 75V. This meant the secondary voltage of the transformer had a large range of acceptable values.

Basic AC supply

A resistor and smoothing capacitor were connected to both V+ and V- as shown in figure 4.

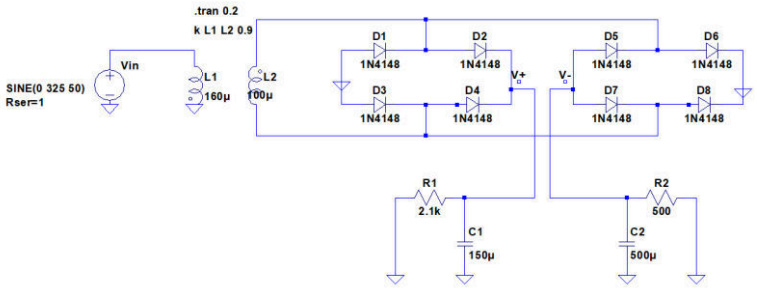

Figure 4: Complete basic supply circuit

The resistors modelled the maximum resistance experienced by the supply rail of the op-amps in the DAC. The capacitors, C_1 and C_2, were connected in parallel to smooth the rectified signal. They had an equivalent series resistance of 1Ω, and the values were calculated to ensure the ripple was less than 5%.

Enhanced AC supply

Linear voltage regulators replaced the capacitors in the basic supply circuit as shown in figure 5. The inductance ratio of the windings in the transformer were increased to provide a larger input voltage to the linear regulators. The capacitors connected to the inputs were much smaller than the capacitors used in the basic power supply as they didn't need to remove as much ripple. LT1121-5 was the positive linear regulator, this was chosen because it had a regulated 5V output voltage for $4.8V<V_{IN}<20V$ at $1mA<I_L<150mA$ and its typical line regulation when $5.5V<\Delta V_{IN}<20V$ at I_L= 1mA was 1.5mV. This device had a maximum sensitivity to a

change in input of 0.027%. LT3015 is the negative linear regulator. Not many negative linear regulators were available, so the adjustable regulator was chosen. The device provided a regulated -5V output for -30V<V_{IN}<-6V at -1.5A<I_L<-1.mA. It had a typical line regulation of 1.5mV when -5.5V<ΔV_{IN}<-30V at I_L= -1mA. This meant the device also had a maximum sensitivity to a change in input of 0.027%. R_2 and R_3 were selected from the E96 series, these resistor values were chosen to provide the adjust pin with its required reference voltage in order to produce a -5V output. The 10nF feedforward capacitor connected between the adjust and the output pin was used to reduce noise and the transient response time.

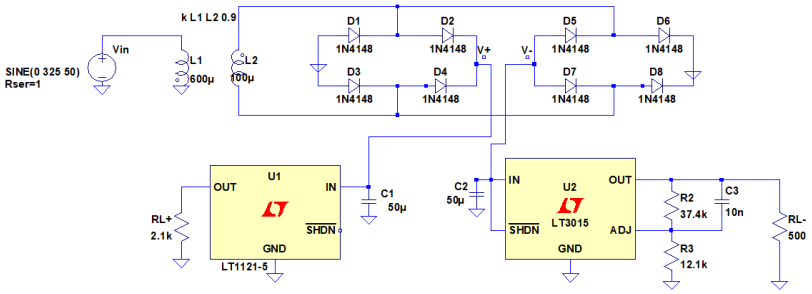

Figure 5: Enhanced AC power supply

<u>Transistor-based linear regulator</u>

The final configuration replaced the positive linear regulator from the enhanced power supply with a transistor based linear regulator. The isolated regulator is shown in figure 6.

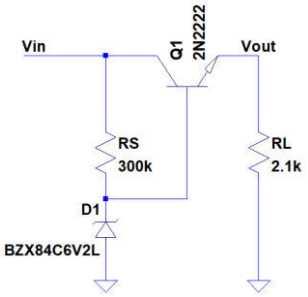

Figure 6: Transistor-based linear regulator

The BZX84C6V2L Zener diode was chosen because it had a breakdown voltage, V_{BV} = 6.2V which was larger than the desired 5V output. The minimum reverse current required to flow through the Zener diode for the breakdown condition to occur was I_{REV} = 1mA. The value of R_S was chosen to ensure the current flowing through the Zener diode was greater than 1mA when V_{IN} ≈ 10V. The NPN 2N2222 BJT was chosen due to its gain being large enough to provide the required output current. The power supply with the transistor-based regulator is shown in figure 7.

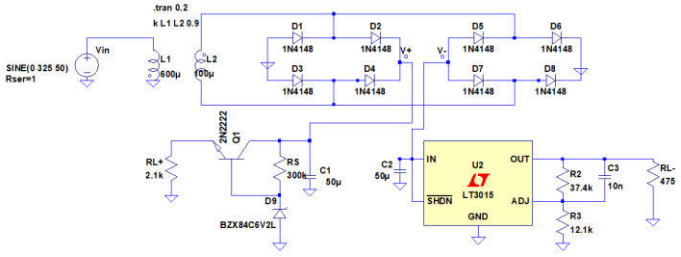

Figure 7: Enhanced power supply with a transistor-based regulator

Functionality

4-bit Digital to Analogue converter (DAC)

The digital inputs controlled how the JFETs were switched. With reference to figure 2, the LSB and the MSB were represented by V_0 and V_3 respectively. This was determined by the resistor values. In a binary system, the weighting of each bit increases by a factor of 2 as it becomes more significant. As the current through each resistor had to be proportional to the weight of its corresponding bit, the resistor value halved (approximately due to E96 resistor series being used) for each increment in the significance of the bit. The current through each resistor summed together at node V-. This current was proportional to the 4-bit binary input. Due to the high input resistance of the op-amp, R_{IN}= 10MΩ, all (approximately) the current flowed through resistor R_f and none (approximately) through R_{IN}. This forced the voltage of the node V- to be the same (approximately) as V+ since there was no volt drop. This behaviour of an op-amp meant the output voltage could be calculated from rearranging the potential divider equation to give equation 1.

$$V_{OUT} \approx (-R_f/R_3)*(V_0/8 + V_1/4 + V_2/2 + V_3)$$

Equation 1: Output of summing amplifier

The specification demanded that the maximum V_{OUT} was around 3V. This meant the maximum output of the summing amplifier was -3V. The value of R_f to ensure this condition was calculated by setting each binary input to logic 1 (maximum V_{IN}). The voltage drops across the parallel resistors, R_0 to R_3, was V_{IN} (neglected resistance of JFETS). These conditions were applied to equation 1, this was rearranged to find R_f, as shown in equation 2.

$$R_f = (-V_{OUT}*R_3/V_{IN})*(8/15) \text{ where } V_{OUT} \text{ is the output of the summing amplifier}$$

Equation 2: Calculation of feedback resistor

The value calculated for R_f was 365Ω. The unity gain buffer functioned in a similar manner to the summing amplifier. All the current from node V_{OUT} flowed through the feedback resistor, $R_{f\text{-}INV}$, which meant the output voltage could be calculated from the potential divider. The resistor values were identical to provide unity gain and high resistance values were used to prevent the loading of unity gain buffer from disturbing V_{OUT}. The output of the unity gain buffer was given by equation 3.

$$V_{INV\text{-}OUT} = -V_{OUT}$$

Equation 3: Calculation of the inverted output

AC Power Supply

Figure 3 shows the commonality across all the power supply configurations. The transformer stepped down the AC mains supply voltage whilst the frequency was maintained. The ratio of the inductances between the windings of the transformer is what determined the amplitude of the secondary voltage. This was varied between the configurations. With respect to ground, the waveforms on the positive and negative nodes of the secondary winding of the transformer are of equal magnitude, but 180° out of phase as shown in figure 8. The diodes in the rectification bridges only allowed current to pass through in one direction. The configuration of the diodes meant that only the positive voltage on nodes A and B were asserted to V+. Only the negative voltage on nodes A and B were asserted to V-. This was shown by figure 9. The frequency of the waveforms on V+ and V- were double that of the mains supply because the waveforms on nodes A and B were 180° out of phase.

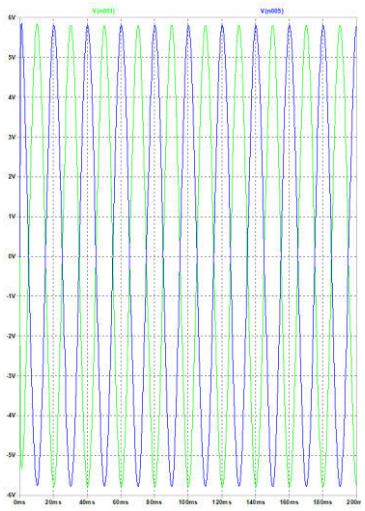

Figure 8: Shows the voltages of node A and B are 180° out of phase

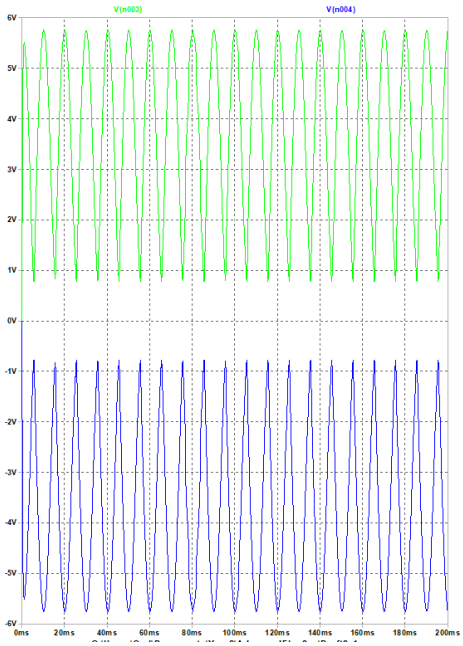

Figure 9: Shows the voltages of V+ (green) and V- (blue) without any load

Basic AC supply

The connection of the parallel RC circuits to V+ and V-, shown in figure 4, caused the waveforms of V+ and V- to have a smoothed response instead of the oscillatory response displayed in figure 9. The capacitor would charge up when the rate of change of |V+| or |V-| was positive and would discharge when the rate of change of |V+| or |V-| was negative. The time constant, R*C, of each parallel RC circuit is what determined the rate the capacitors discharged. Equation 4 was used to calculate the required capacitances to ensure less than 5% ripple occurred. From figure 9, V_P was set to 5V as the amplitude would drop due to loading of the RC circuit. V_O had to be $0.95V_P$ or greater. As the discharge was periodic, the time was set to the period of the waveform; this was the reciprocal of the frequency which was 100Hz. Equation 4 was then rearranged to determine C for the positive and negative outputs.

$$V_O(t) = V_P * \exp(-t/R*C)$$

Equation 4: Voltage of a discharging capacitor

Approximately 4% ripple was expected for V+ and V- when capacitances, C_1 =150uF and C_2 =470uF were used respectively.

Enhanced AC power supply

Figure 10 shows an example of the inner circuitry of a linear series regulator. This was one possible topology the components U1 and U2 of figure 4 could have used to achieve their regulated output. The value of R_1 ensured the minimum current through it was greater than I_{Zmin} for the full range of input voltages. The capacitor connected to the input reduced this range so R_1 was smaller which reduced the power dissipated. This meant the breakdown voltage of the Zener diode had been achieved for the full input range; therefore, the voltage across the Zener diode was a constant reference. The sample circuit was a potential divider which asserted a voltage onto V- which was proportional to V_{OUT}. The differential input (V_{REF}-V-) was amplified. Therefore, when V_{OUT} increased, V- increased and the differential input decreased. This meant V_{BE} decreased and so did the current through the transistor, I_L, which caused V_{OUT} to drop.

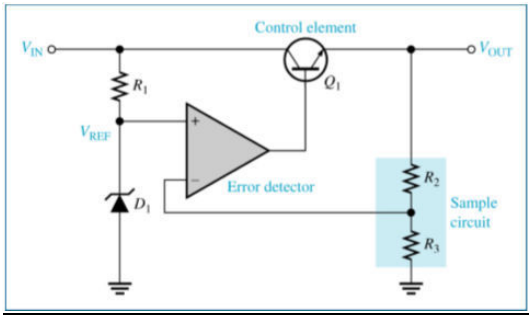

Figure 10: Op-amp based series regulator

Transistor-based linear regulator

This circuit is shown in figure 6. The value of R_S was chosen to ensure the minimum current through it was greater than I_{Zmin} for all possible input values. When the circuit was integrated with the rest of the power supply, a 50uF capacitor, as shown in figure 7, was connected to the input so the range of input voltages was reduced. The value of the resistor was very high (300KΩ) which meant the wasted power was low because there was only a small voltage drop. The breakdown voltage of the Zener diode was used to reference the base of the BJT. This meant the current through the transistor was controlled by the output voltage.

Results

4-bit Digital to Analogue converter (DAC)

Figure 11 shows the response of the DAC as the input incremented through the full range of binary values. Before the graph was plotted, the data was prepared. The data set was reduced so that only one period of the input cycle was plotted. The time column was reduced to 6dp which created multiple voltages at the same time. The voltage column was reduced to 6dp which meant all the voltages at the same time (to 6dp) were equal. Finally, the duplicates were removed. With exception of three outliers, the response of the DAC generally exhibited linear behaviour which was shown by the plot following the trendline. The graph showed an offset error of 0.29V and a maximum input corresponded to a maximum output of 2.93V. Since the desired maximum output voltage was 3V, the accuracy of the device was 97.7%.

Figure 12 shows the response of the DAC to the binary input being incremented by one. The response was half way between the initial and final value when the time was 10.000014ms. As the step response initiated at 10ms, the settling time was 0.014us.

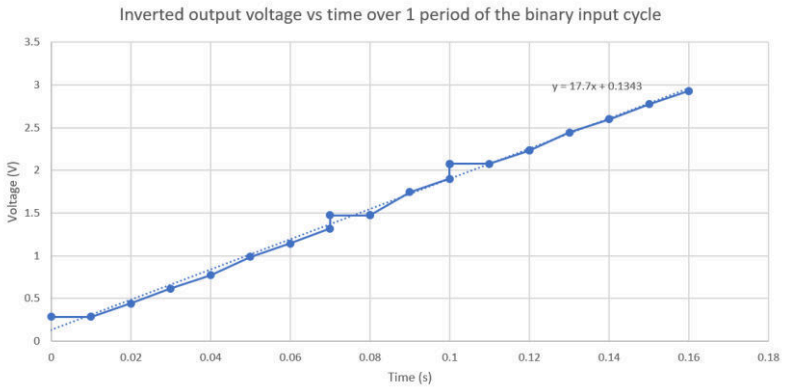

Figure 11: Output voltage as a function of time whilst the binary input was stepped through

Figure 12: Output response as a function of time after the binary input was incremented

Figure 13 shows the current drawn from the positive and negative supply to the op-amps used in the DAC. It demonstrated the current drawn varied as a function of the input. The currents drawn by the positive and negative rails had maximum magnitudes of 2.4mA and 10mA respectively.

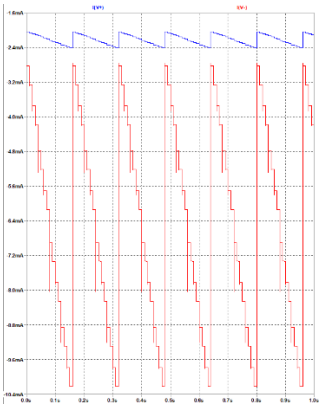

Figure 13: Shows the current drawn from the positive (blue) and negative (red) supply rails as the input range is stepped through

AC Power Supply

Basic AC supply

The dual rail output of the basic supply is shown in figure 13. The peak output voltage of the positive rail was 5.1V. The minimum stable output was 4.95V. The average voltage was 5.03V with a 2.95% ripple. The peak output voltage of the negative rail had a magnitude of 4.95V. The minimum stable magnitude was 4.75V. The average voltage was -4.85V with a 4.04% ripple.

I_{RMS} at the mains was 212A. The input power was calculated by multiplying V_{RMS} and I_{RMS} of the mains supply. The output power was calculated by multiplying the average voltage and the maximum current of each rail and then adding them together. This gave an efficiency of 0.000126%.

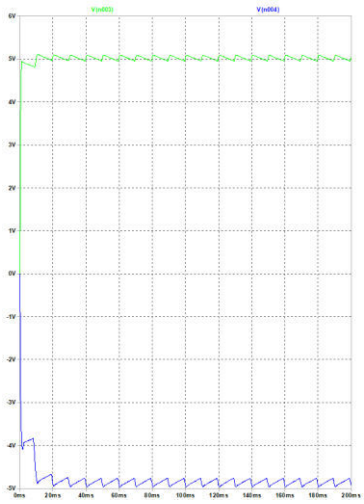

Figure 13: Dual rail output of the basic AC supply

Enhanced AC supply

Figure 14 shows the dual rail output of the AC power supply with a positive and negative linear regulator. The positive rail had a maximum output of 5.01659V and a minimum of 5.01657. This gave an average output of 5.01658V with a 0.0004% ripple. The ripple of the negative rail was to small to be detected within 5dp, so the output was a constant -5.0178V. The efficiency of the device was 0.000126%.

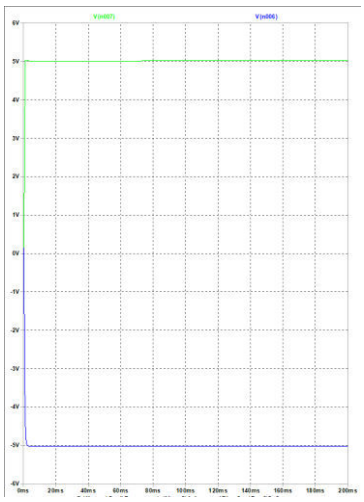

Figure 14: Dual rail output of the enhanced AC supply

Transistor-based linear regulator

This was initially characterised separately from the remainder of the power supply. A sine wave with a 10V DC offset and 0.2V small signal amplitude with a 10Hz frequency was used to model the input waveform. The input and output voltage of the device are shown in figure 15 along with the input current.

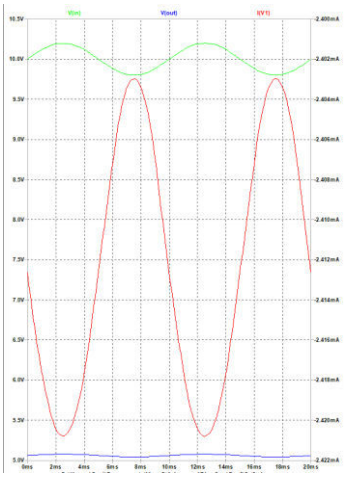

Figure 15: Input current, voltage and output voltage vs time

Over 10ms, the input voltage varied between 9.8V and 10.2V; the input current varied between -2.403mA and -2.421mA and the output voltage increased from 5.06V to 5.061V. The line regulation was 0.001V per Δ0.4V input and the load regulation was 0.001V per Δ18uA input. Its ripple rejection was 400 and its efficiency was 54%. The input power was calculated from the multiplication of $I_{IN\text{-}RMS}$ and $V_{IN\text{-}RMS}$. The output power was calculated from V_{OUT}^2 multiplied by R_L.

The output voltage from the transistor-based linear regulator when it was integrated into the power supply is shown in figure 16. It had V_{MAX} = 5.058V and V_{MIN} = 5.050V; thus, its ripple was 0.16%.

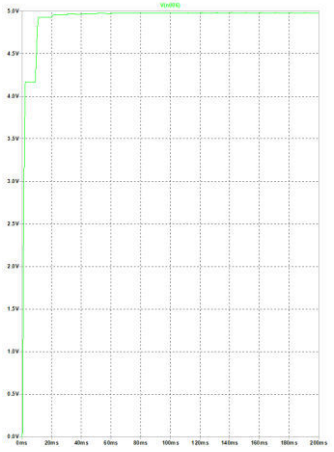

Figure 16: output voltage from the transistor-based linear regulator

Conclusion

The DAC demonstrated a high level of linearity. The results showed three data points which had a significant error; however, two of these outliers appear to be caused by the method used to prepare the data. This is because they aren't equally spaced like the other data points and appear to occur at the same time as other data points on the 2dp resolution time axis. The DAC also demonstrated an accuracy of 97.7%, but this can be misleading as it only compares the maximum expected and simulated values. Finally, the DAC has an offset error of 0.29V; this could have been caused by the offset voltage of the amplifiers. If this could be removed, I would expect the DAC to exhibit an almost ideal response.
The basic power supply performed the worst of the three configurations. It exhibited the highest ripple and its average voltage had the largest error, 0.03V and 0.15V. The enhanced power supply performed the best but used the most expensive components. It outperformed the basic supply with a reduced ripple of 2.95% and 4.04% on the positive and negative rails respectively. The average voltage of each supply had less error, the negative rail improved by a factor of 8. The transistor-based regulator showed better performance than the basic supply, but not as good as the enhanced supply. This would be a good compromise between cost and performance.

The efficiency of each power supply was terrible. However, I think this is an inherent property of any circuit involving a step-down transformer. A better comparison of efficiency would have been to consider the circuits from the nodes V+ and V- as this was the point where the power supplies differed.