



Doc. No.: TD-LO18-SP-2003	Doc. Title: 0.18um Logic Low Leakage 1P6M (1P5M, 1P4M) Salicide 1.8V/5.0V SPICE Model (Version 1.3)	Doc. Rev: 4R	Tech Dev Rev.: 1.3	Page No.: 1/16
------------------------------	-----------------------------------------------------------------------------------------------------------------------	-----------------	-----------------------	-------------------

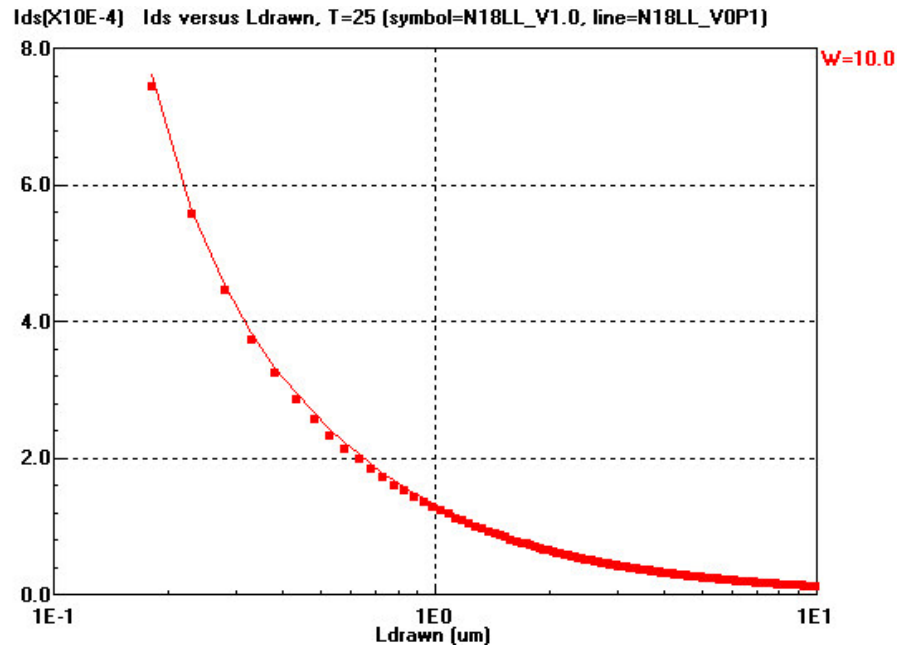


Fig.E1 Idlin versus L at Wdrawn = 10um for 1.8V NMOS; Symbol: Ver 1.3, Line: Ver 0.1

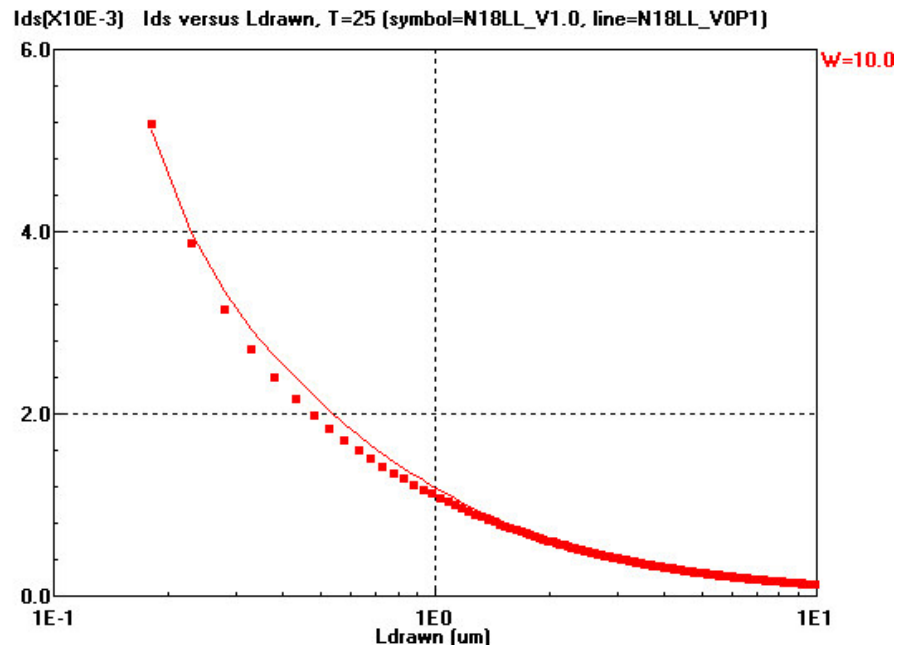


Fig.E2 Idsat versus L at Wdrawn = 10um for 1.8V NMOS; Symbol: Ver 1.3, Line: Ver 0.1

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO18-SP-2003	Doc. Title: 0.18um Logic Low Leakage 1P6M (1P5M, 1P4M) Salicide 1.8V/5.0V SPICE Model (Version 1.3)	Doc. Rev.: 4R	Tech Dev Rev.: 1.3	Page No.: 2/16
------------------------------	--------------------------------------------------------------------------------------------------------------	------------------	-----------------------	-------------------

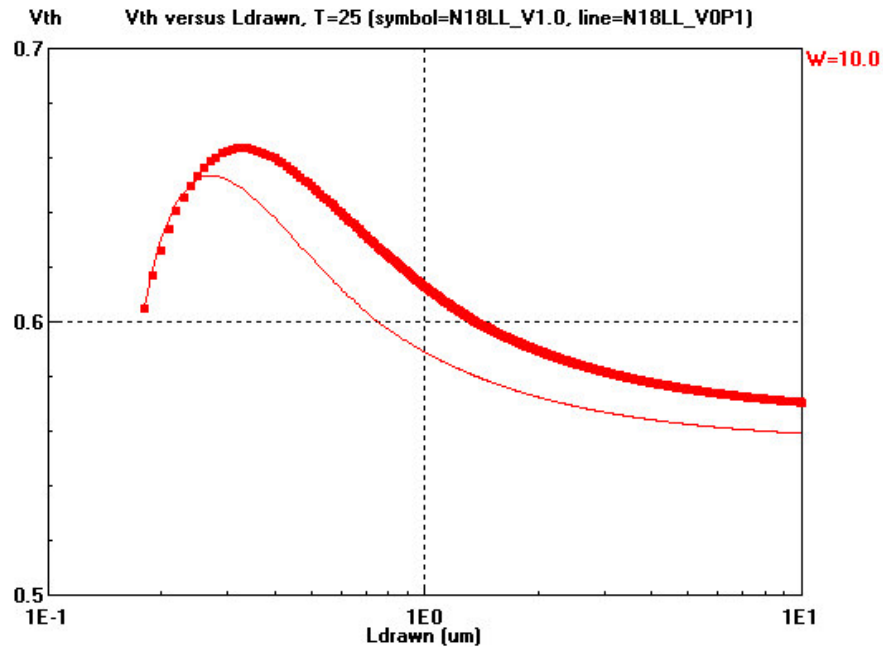


Fig.E3 Vth versus L at Wdrawn = 10um for 1.8V NMOS; Symbol: Ver 1.3, Line: Ver 0.1

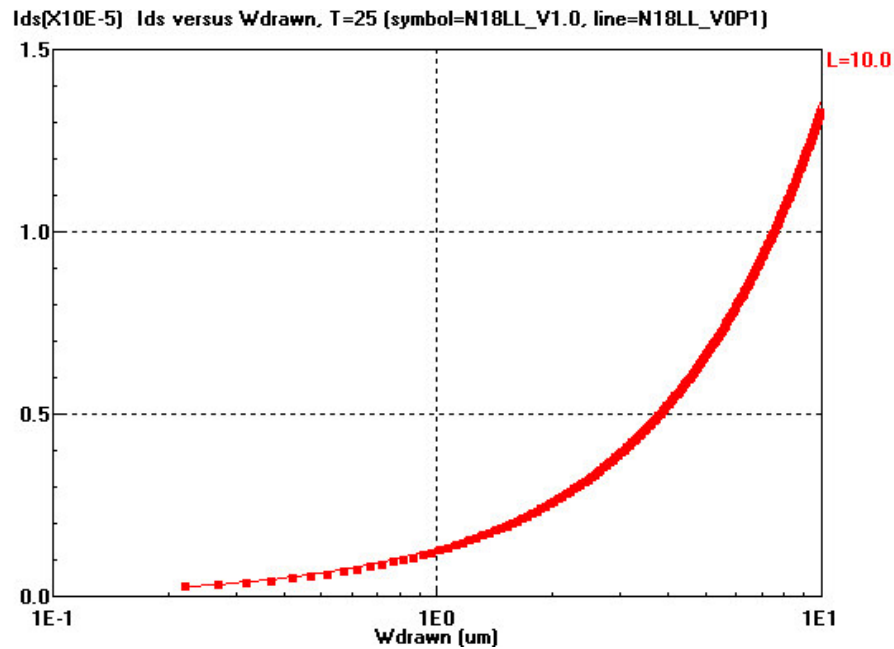


Fig.E4 Idlin versus W at Ldrawn = 10um for 1.8V NMOS; Symbol: Ver 1.3, Line: Ver 0.1

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO18-SP-2003	Doc. Title: 0.18um Logic Low Leakage 1P6M (1P5M, 1P4M) Salicide 1.8V/5.0V SPICE Model (Version 1.3)	Doc. Rev: 4R	Tech Dev Rev.: 1.3	Page No.: 3/16
------------------------------	-----------------------------------------------------------------------------------------------------------------------	-----------------	-----------------------	-------------------

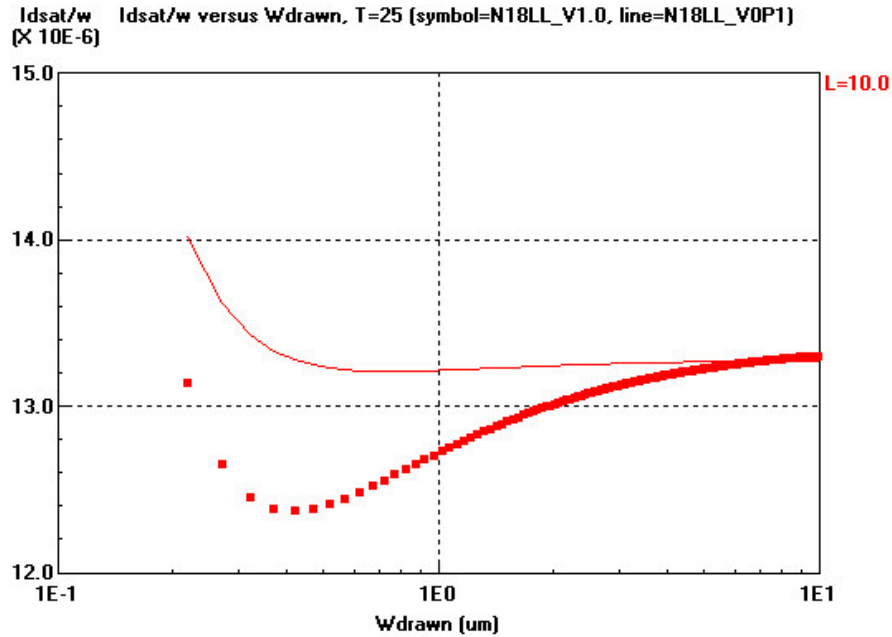


Fig.E5 Idsat/W versus W at Ldrawn = 10um for 1.8V NMOS; Symbol: Ver 1.3, Line: Ver 0.1

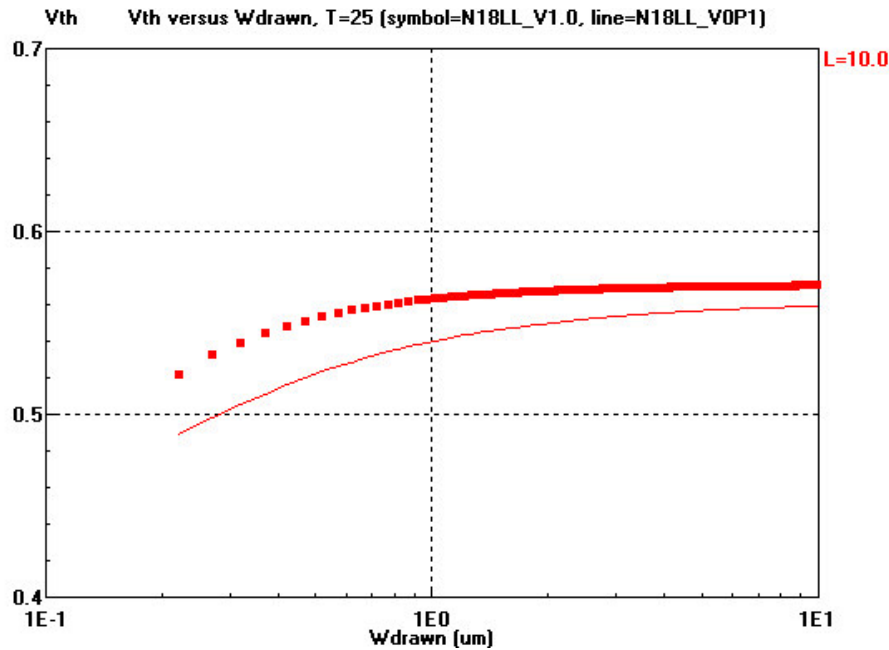


Fig.E6 Vth versus W at Ldrawn = 10um for 1.8V NMOS; Symbol: Ver 1.3, Line: Ver 0.1

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO18-SP-2003	Doc. Title: 0.18um Logic Low Leakage 1P6M (1P5M, 1P4M) Salicide 1.8V/5.0V SPICE Model (Version 1.3)	Doc. Rev: 4R	Tech Dev Rev.: 1.3	Page No.: 4/16
------------------------------	--------------------------------------------------------------------------------------------------------------	-----------------	-----------------------	-------------------

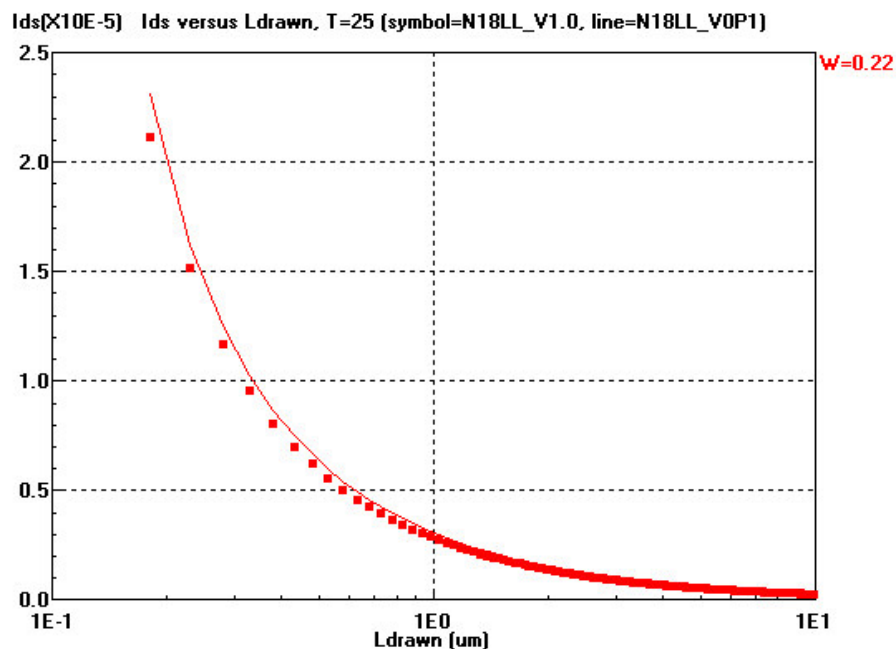


Fig.E7 Idlin versus L at Wdrawn = 0.22um for 1.8V NMOS; Symbol: Ver 1.3, Line: Ver 0.1

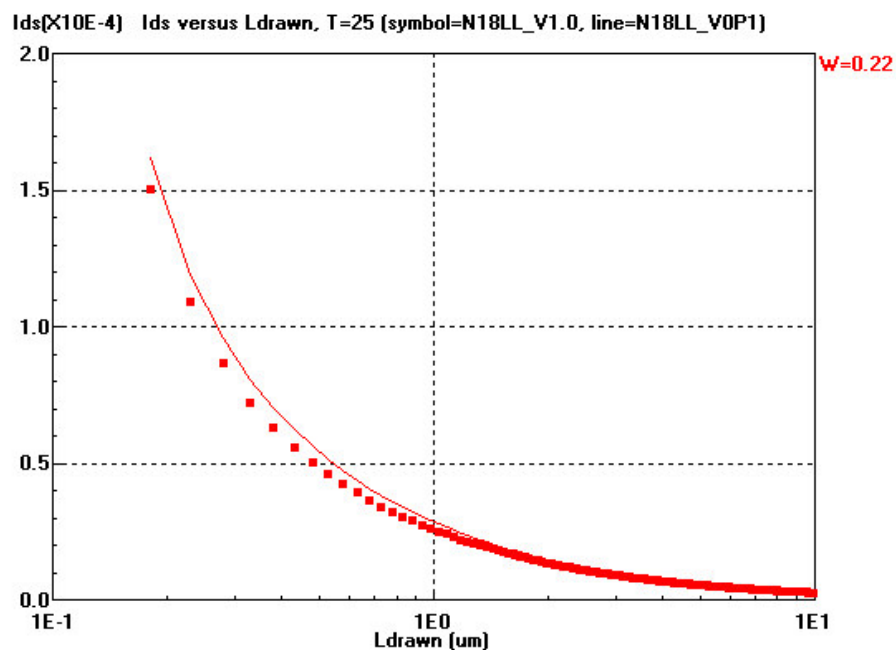


Fig.E8 Idsat versus L at Wdrawn = 0.22um for 1.8V NMOS; Symbol: Ver 1.3, Line: Ver 0.1

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO18-SP-2003	Doc. Title: 0.18um Logic Low Leakage 1P6M (1P5M, 1P4M) Salicide 1.8V/5.0V SPICE Model (Version 1.3)	Doc. Rev.: 4R	Tech Dev Rev.: 1.3	Page No.: 5/16
------------------------------	--------------------------------------------------------------------------------------------------------------	------------------	-----------------------	-------------------

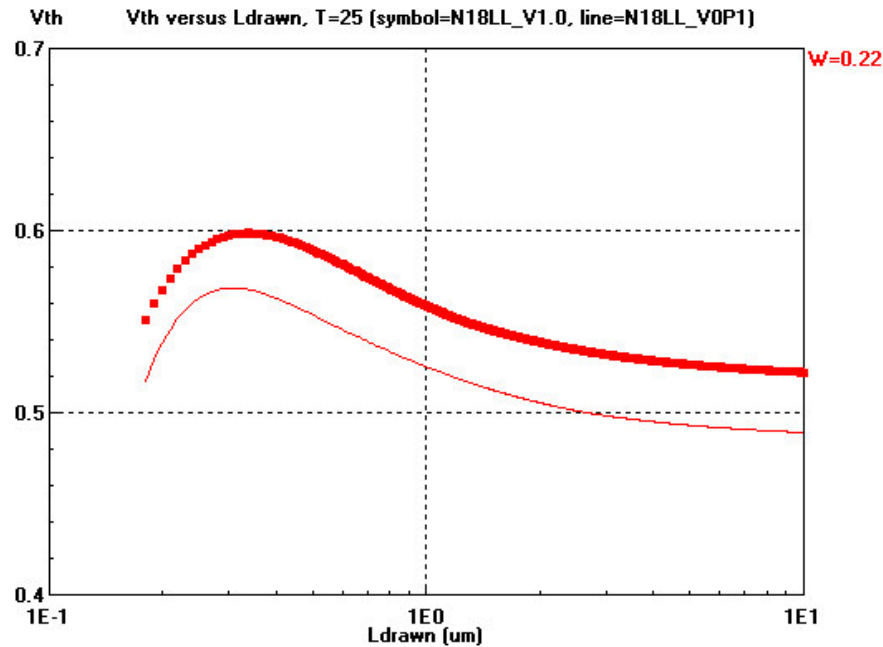


Fig.E9 Vth versus L at Wdrawn = 0.22um for 1.8V NMOS; Symbol: Ver 1.3, Line: Ver 0.1

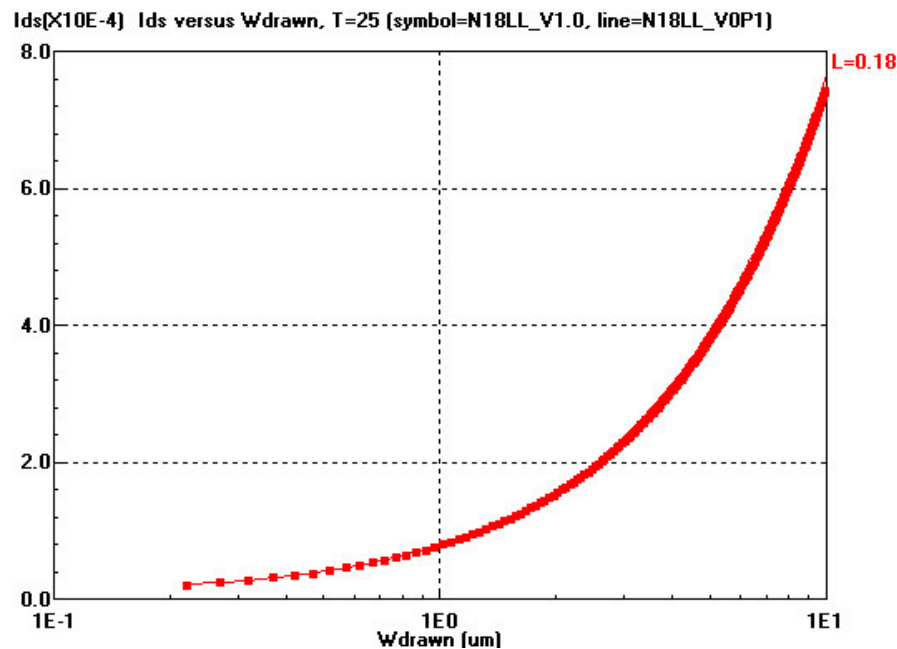


Fig.E10 Idlin versus W at Ldrawn = 0.18um for 1.8V NMOS; Symbol: Ver 1.3, Line: Ver 0.1

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO18-SP-2003	Doc. Title: 0.18um Logic Low Leakage 1P6M (1P5M, 1P4M) Salicide 1.8V/5.0V SPICE Model (Version 1.3)	Doc. Rev: 4R	Tech Dev Rev.: 1.3	Page No.: 6/16
------------------------------	-----------------------------------------------------------------------------------------------------------------------	-----------------	-----------------------	-------------------

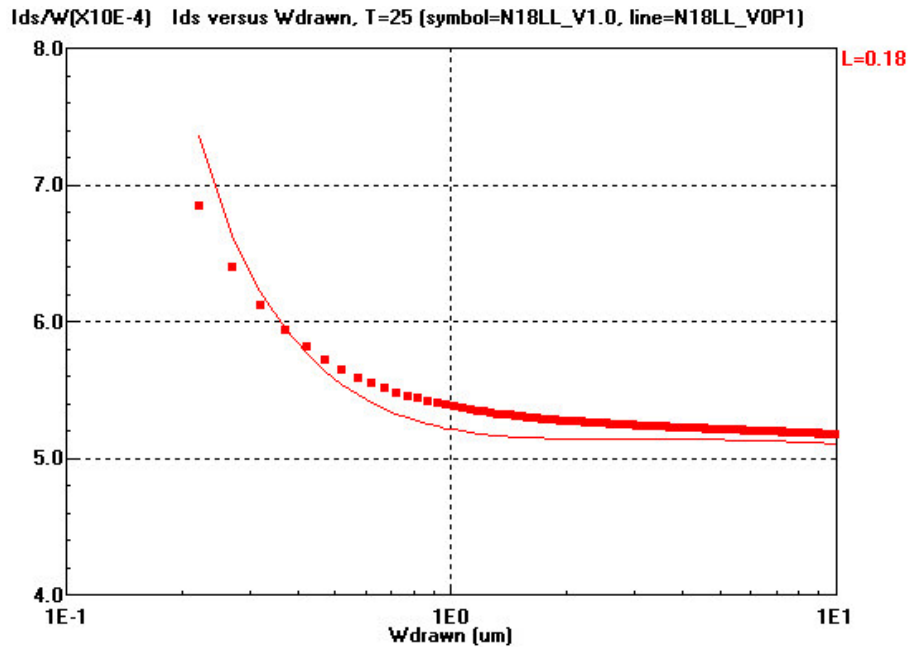


Fig.E11 Idsat/W versus W at Ldrawn = 0.18um for 1.8V NMOS; Symbol: Ver 1.3, Line: Ver 0.1

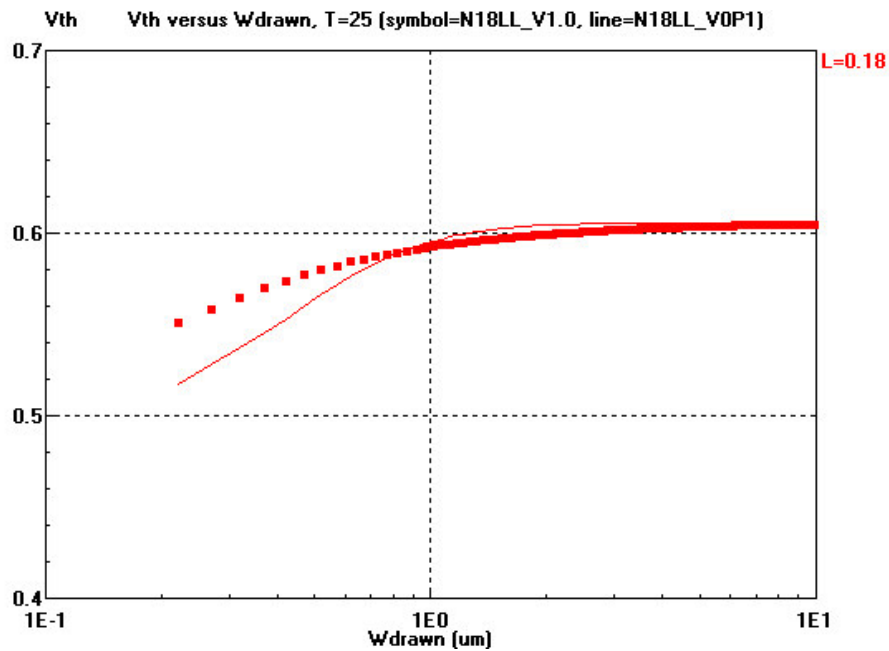


Fig.E12 Vth versus W at Ldrawn = 0.18um for 1.8V NMOS; Symbol: Ver 1.3, Line: Ver 0.1

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO18-SP-2003	Doc. Title: 0.18um Logic Low Leakage 1P6M (1P5M, 1P4M) Salicide 1.8V/5.0V SPICE Model (Version 1.3)	Doc. Rev: 4R	Tech Dev Rev.: 1.3	Page No.: 7/16
------------------------------	--------------------------------------------------------------------------------------------------------------	-----------------	-----------------------	-------------------

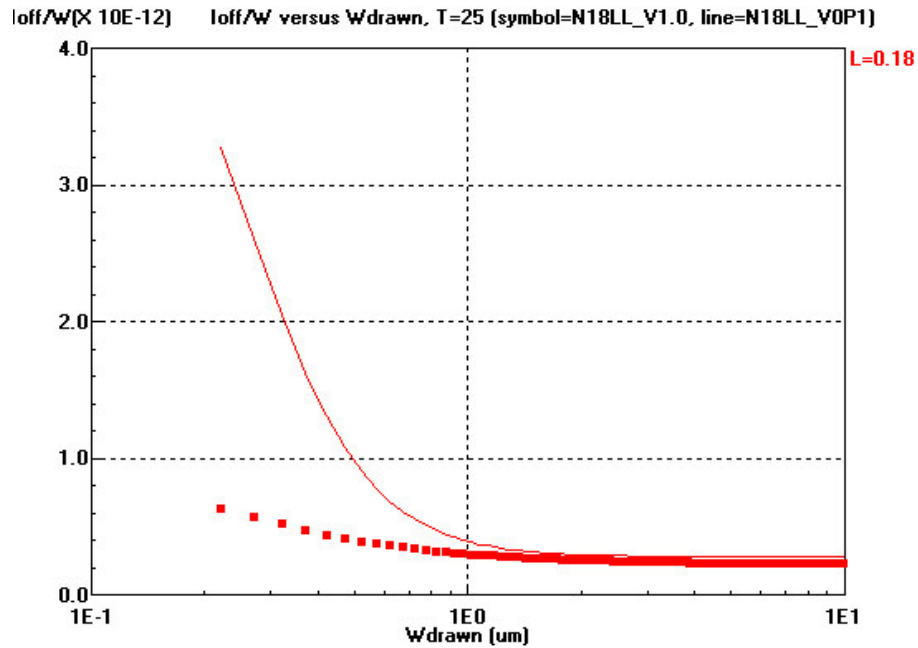


Fig.E13 Ioff/W versus W at Ldrawn = 0.18um for 1.8V NMOS; Symbol: Ver 1.3, Line: Ver 0.1

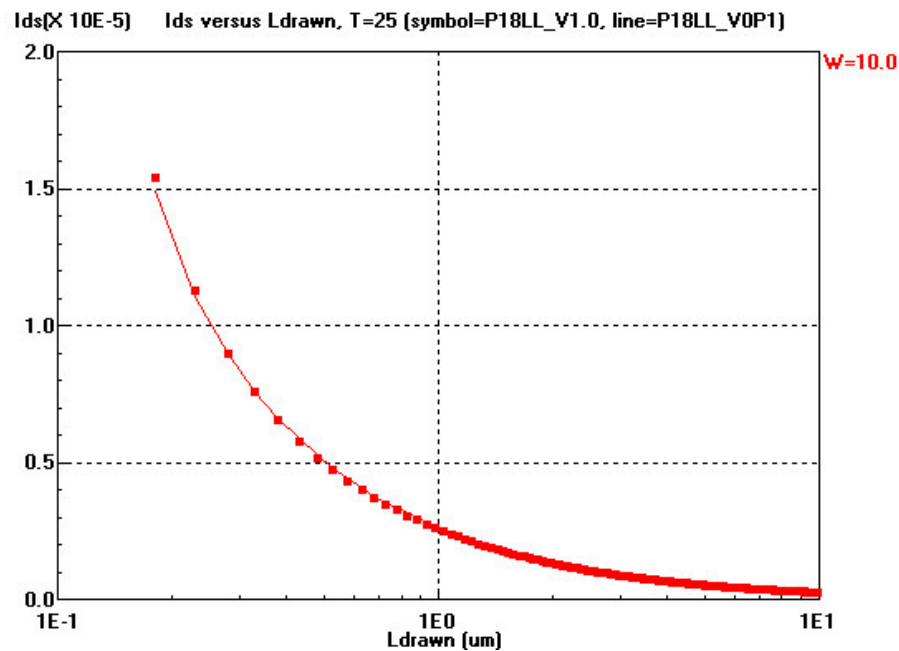


Fig.E14 Idlin versus L at Wdrawn = 10um for 1.8V PMOS; Symbol: Ver 1.3, Line: Ver 0.1

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO18-SP-2003	Doc. Title: 0.18um Logic Low Leakage 1P6M (1P5M, 1P4M) Salicide 1.8V/5.0V SPICE Model (Version 1.3)	Doc. Rev.: 4R	Tech Dev Rev.: 1.3	Page No.: 8/16
------------------------------	--------------------------------------------------------------------------------------------------------------	------------------	-----------------------	-------------------

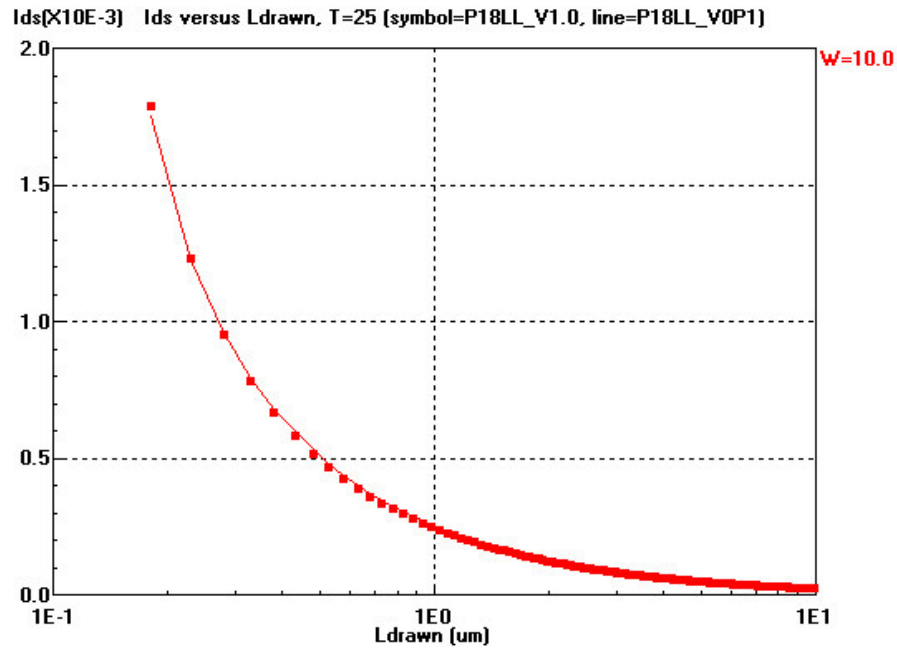


Fig.E15 Idsat versus L at Wdrawn = 10um for 1.8V PMOS; Symbol: Ver 1.3, Line: Ver 0.1

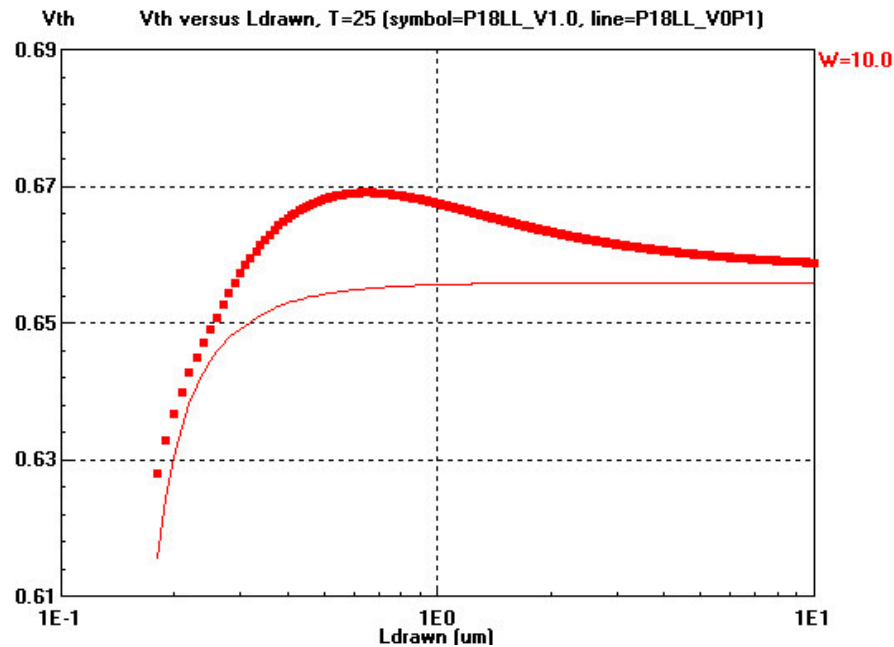


Fig.E16 Vth versus L at Wdrawn = 10um for 1.8V PMOS; Symbol: Ver 1.3, Line: Ver 0.1

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO18-SP-2003	Doc. Title: 0.18um Logic Low Leakage 1P6M (1P5M, 1P4M) Salicide 1.8V/5.0V SPICE Model (Version 1.3)	Doc. Rev.: 4R	Tech Dev Rev.: 1.3	Page No.: 9/16
------------------------------	--------------------------------------------------------------------------------------------------------------	------------------	-----------------------	-------------------

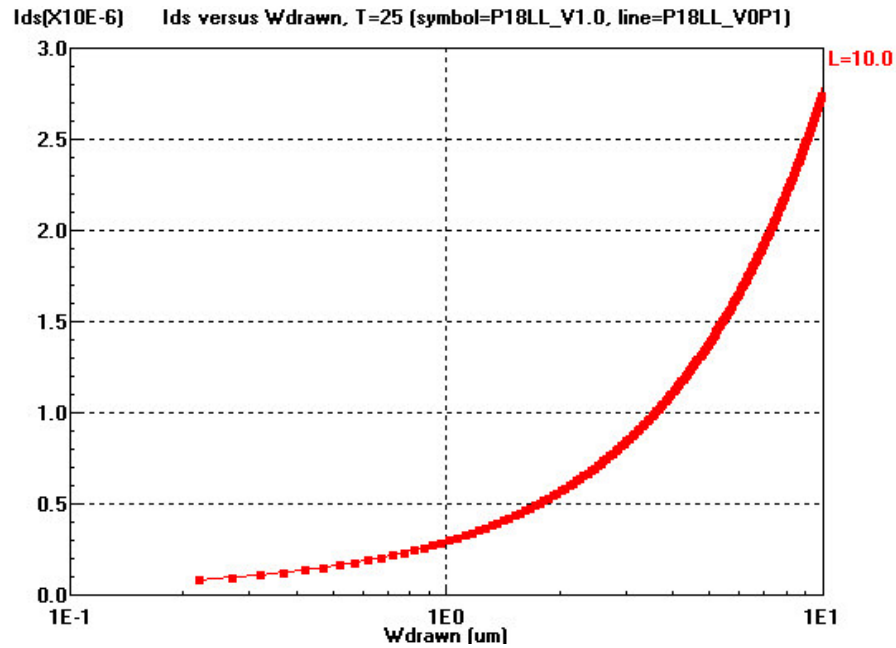


Fig.E17 Idlin versus W at Ldrawn = 10um for 1.8V PMOS; Symbol: Ver 1.3, Line: Ver 0.1

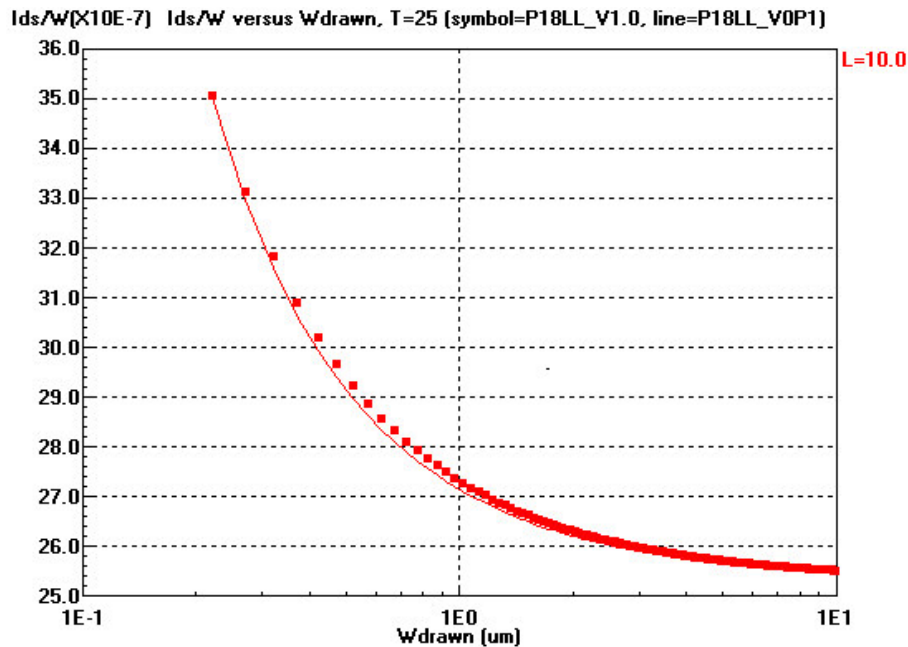


Fig.E18 Idsat/W versus W at Ldrawn = 10um for 1.8V PMOS; Symbol: Ver 1.3, Line: Ver 0.1

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO18-SP-2003	Doc. Title: 0.18um Logic Low Leakage 1P6M (1P5M, 1P4M) Salicide 1.8V/5.0V SPICE Model (Version 1.3)	Doc. Rev: 4R	Tech Dev Rev.: 1.3	Page No.: 10/16
------------------------------	--------------------------------------------------------------------------------------------------------------	-----------------	-----------------------	--------------------

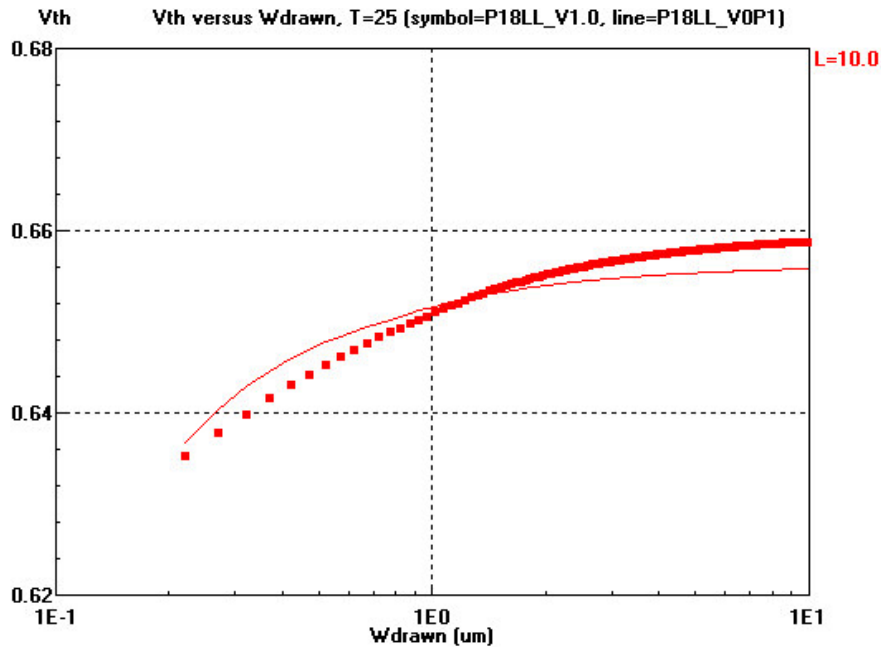


Fig.E19 Vth versus W at Ldrawn = 10um for 1.8V PMOS; Symbol: Ver 1.3, Line: Ver 0.1

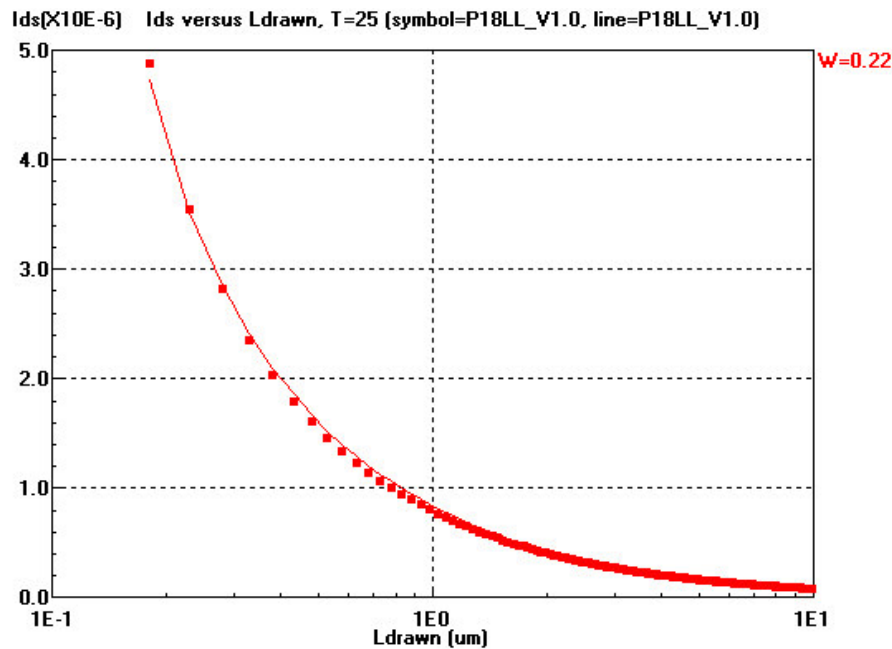


Fig.E20 Idlin versus L at Wdrawn = 0.22um for 1.8V PMOS; Symbol: Ver 1.3, Line: Ver 0.1

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO18-SP-2003	Doc. Title: 0.18um Logic Low Leakage 1P6M (1P5M, 1P4M) Salicide 1.8V/5.0V SPICE Model (Version 1.3)	Doc. Rev: 4R	Tech Dev Rev.: 1.3	Page No.: 11/16
------------------------------	--------------------------------------------------------------------------------------------------------------	-----------------	-----------------------	--------------------

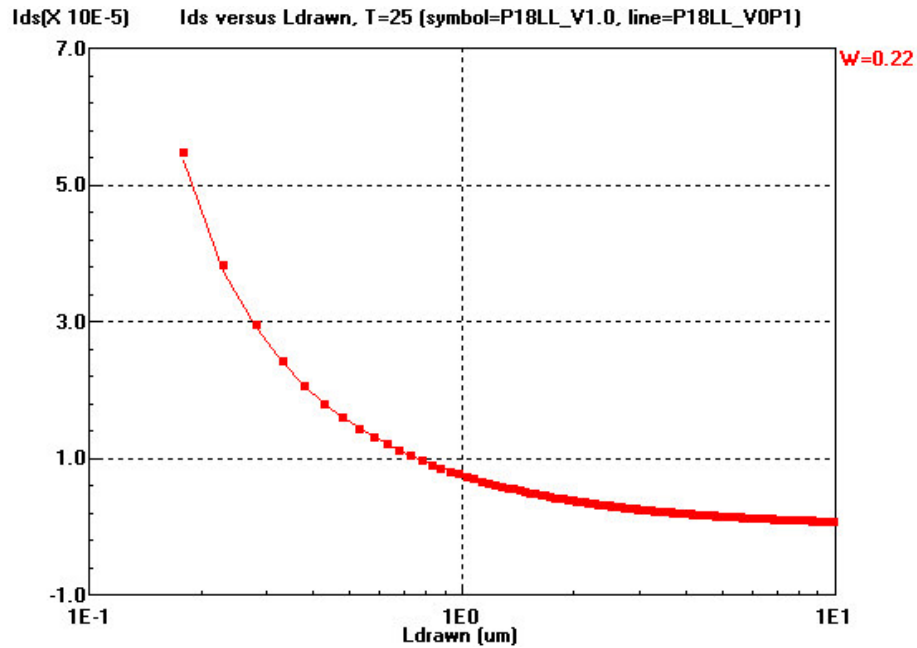


Fig.E21 Idsat versus L at Wdrawn = 0.22um for 1.8V PMOS; Symbol: Ver 1.3, Line: Ver 0.1

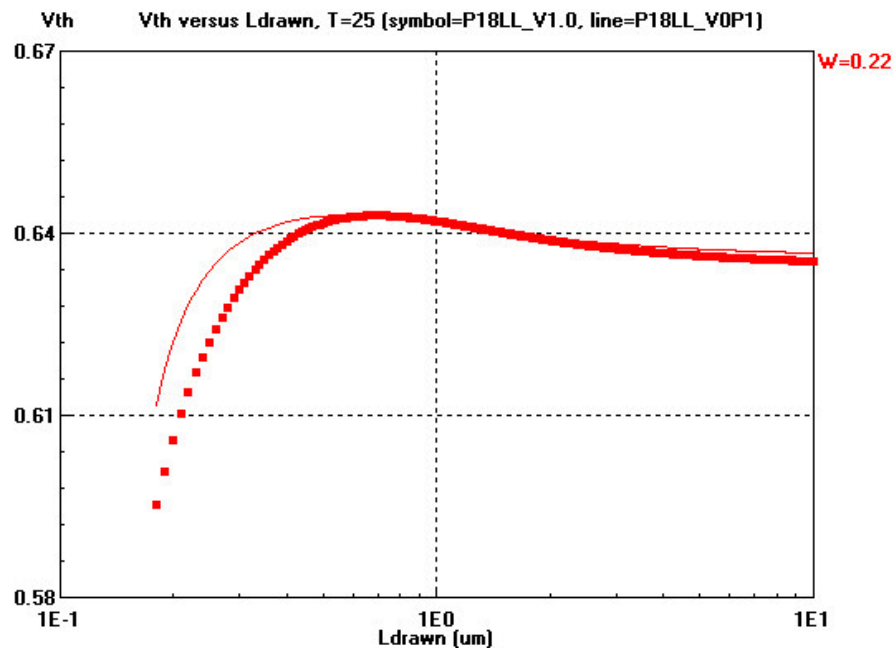


Fig.E22 Vth versus L at Wdrawn = 0.22um for 1.8V PMOS; Symbol: Ver 1.3, Line: Ver 0.1

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO18-SP-2003	Doc. Title: 0.18um Logic Low Leakage 1P6M (1P5M, 1P4M) Salicide 1.8V/5.0V SPICE Model (Version 1.3)	Doc. Rev: 4R	Tech Dev Rev.: 1.3	Page No.: 12/16
------------------------------	--------------------------------------------------------------------------------------------------------------	-----------------	-----------------------	--------------------

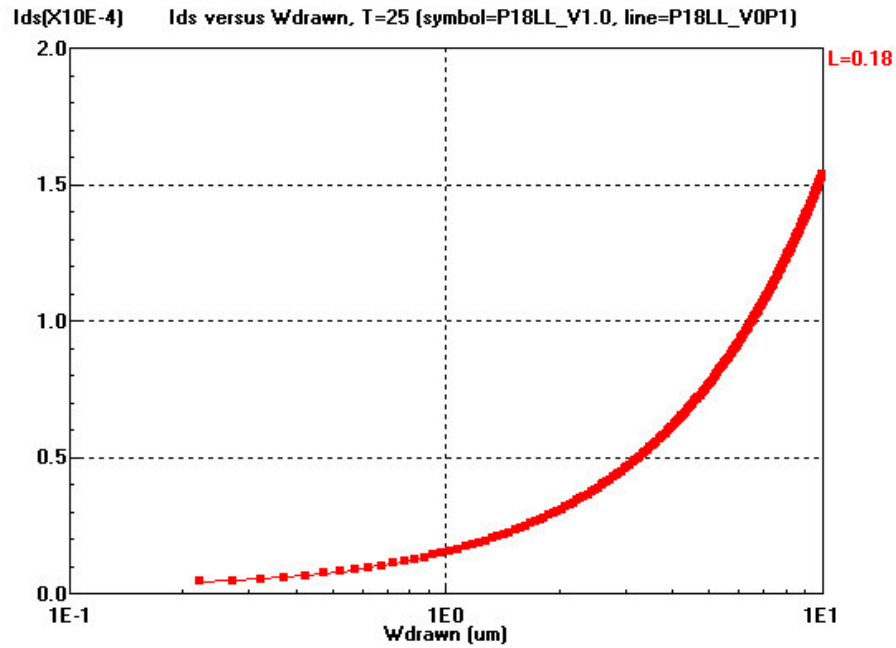


Fig.E23 Idlin versus W at Ldrawn = 0.18um for 1.8V PMOS; Symbol: Ver 1.3, Line: Ver 0.1

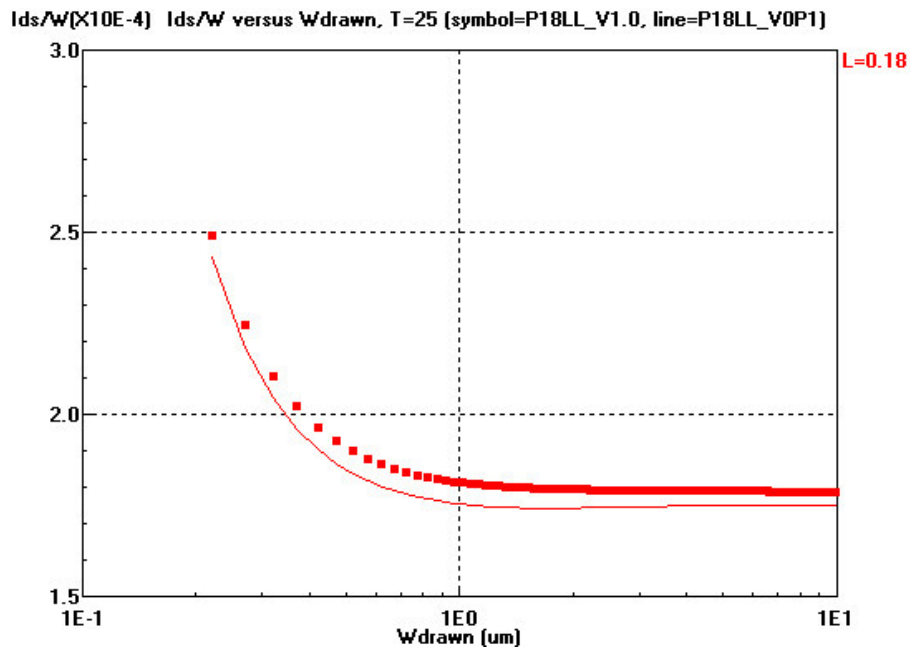


Fig.E24 Idsat/W versus W at Ldrawn = 0.18um for 1.8V PMOS; Symbol: Ver 1.3, Line: Ver 0.1

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO18-SP-2003	Doc. Title: 0.18um Logic Low Leakage 1P6M (1P5M, 1P4M) Salicide 1.8V/5.0V SPICE Model (Version 1.3)	Doc. Rev: 4R	Tech Dev Rev.: 1.3	Page No.: 13/16
------------------------------	-----------------------------------------------------------------------------------------------------------	-----------------	-----------------------	--------------------

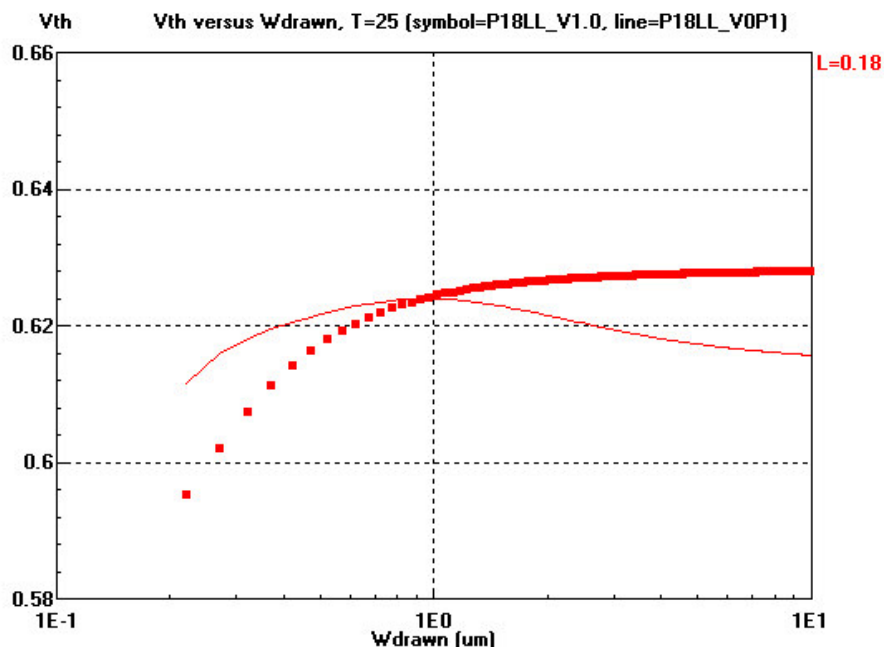


Fig.E25 Vth versus W at Ldrawn = 0.18um for 1.8V PMOS; Symbol: Ver 1.3, Line: Ver 0.1

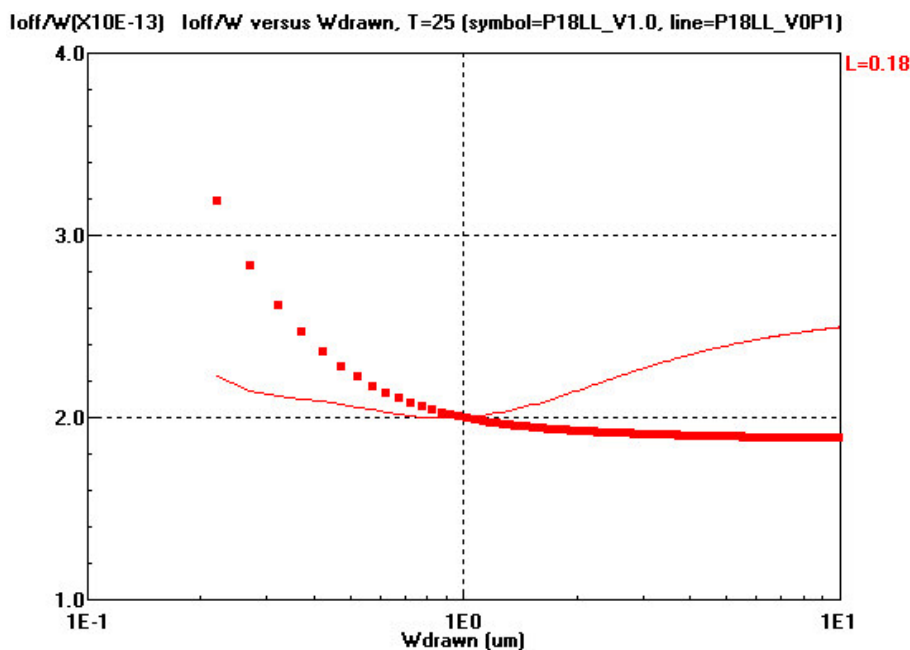


Fig.E26 Ioff/W versus W at Ldrawn = 0.18um for 1.8V PMOS; Symbol: Ver 1.3, Line: Ver 0.1

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO18-SP-2003	Doc. Title: 0.18um Logic Low Leakage 1P6M (1P5M, 1P4M) Salicide 1.8V/5.0V SPICE Model (Version 1.3)	Doc. Rev: 4R	Tech Dev Rev.: 1.3	Page No.: 14/16
------------------------------	-----------------------------------------------------------------------------------------------------------	-----------------	-----------------------	--------------------

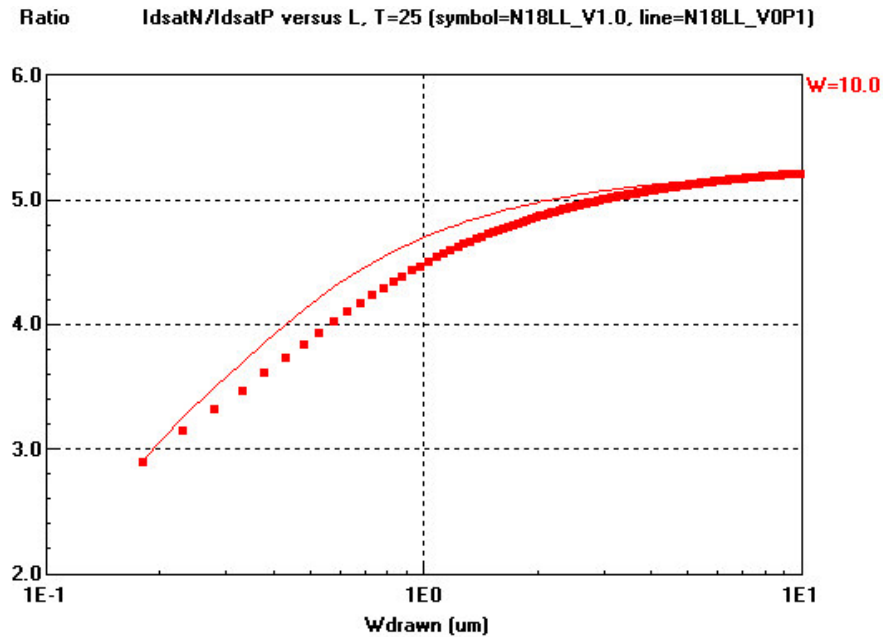


Fig.E27 I_{dsatN}/I_{dsatP} versus L at Wdrawn = 10um for 1.8V MOS; Symbol: Ver 1.3, Line: Ver 0.1

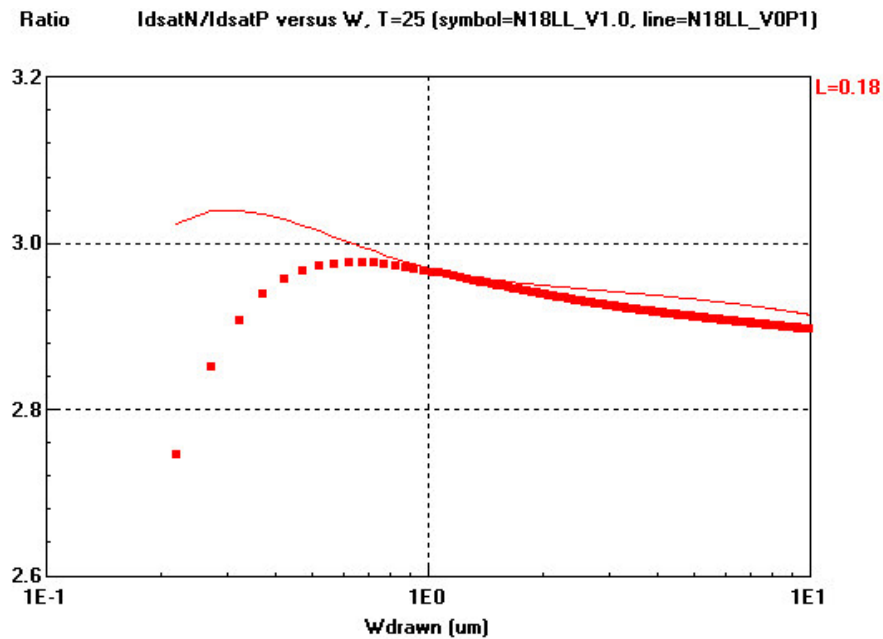


Fig.E28 I_{dsatN}/I_{dsatP} versus W at Ldrawn = 0.18um for 1.8V MOS; Symbol: Ver 1.3, Line: Ver 0.1

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Semiconductor Manufacturing International Corporation

Doc. No.: TD-LO18-SP-2003	Doc. Title: 0.18um Logic Low Leakage 1P6M (1P5M, 1P4M) Salicide 1.8V/5.0V SPICE Model (Version 1.3)	Doc. Rev: 4R	Tech Dev Rev.: 1.3	Page No.: 15/16
------------------------------	--------------------------------------------------------------------------------------------------------------------	-----------------	-----------------------	--------------------

Table E1. Vth, Idsat, and Ioff of 10/0.18 for NMOS 1.8V

L018LL Version 0.1					
N18LL	TT	FF	SS	FNSP	SNFP
Tox (A)	38.5	37.4	39.6	38.5	38.5
Cgdo (fF/um)	0.345	0.3634	0.3266	0.345	0.345
Cgso (fF/um)	0.345	0.3634	0.3266	0.345	0.345
Vth (V)@ 10/0.18	0.605	0.506	0.698	0.528	0.677
Idsat (uA/um)@ 10/0.18	510.83	610.39	424.96	586.1	444.52
Ioff (pA/um)@ 10/0.18	0.285	6.2	0.0165	4.1	0.025
L018LL Version 1.3					
N18LL	TT	FF	SS	FNSP	SNFP
Tox (A)	38.5	37.4	39.6	38.5	38.5
Cgdo (fF/um)	0.368	0.3864	0.3496	0.368	0.368
Cgso (fF/um)	0.368	0.3864	0.3496	0.368	0.368
Vth (V)@ 10/0.18	0.605	0.51	0.696	0.533	0.674
Idsat (uA/um)@ 10/0.18	517.94	628.81	423.4	603.42	443.54
Ioff (pA/um)@ 10/0.18	0.23	4.55	0.0138	2.83	0.0221

Table E2. Vth, Idsat, and Ioff of 10/0.18 for PMOS 1.8V

L018LL Version 0.1					
P18LL	TT	FF	SS	FNSP	SNFP
Tox (A)	38.3	37.2	39.4	38.3	38.3
Cgdo (fF/um)	0.314	0.3308	0.2972	0.314	0.314
Cgso (fF/um)	0.314	0.3308	0.2972	0.314	0.314
Vth (V)@ 10/0.18	0.616	0.535	0.691	0.672	0.554
Idsat (uA/um)@ 10/0.18	175.29	218.85	141.43	147.55	210.91
Ioff (pA/um)@ 10/0.18	0.25	2.97	0.0256	0.0375	2.09
L018LL Version 1.3					
P18LL	TT	FF	SS	FNSP	SNFP
Tox (A)	38.1	37	39.2	38.1	38.1
Cgdo (fF/um)	0.335	0.3518	0.3182	0.335	0.335
Cgso (fF/um)	0.335	0.3518	0.3182	0.335	0.335
Vth (V)@ 10/0.18	0.628	0.545	0.705	0.681	0.571
Idsat (uA/um)@ 10/0.18	178.78	226.36	142.23	149.73	216.09
Ioff (pA/um)@ 10/0.18	0.189	2.62	0.0177	0.0303	1.52

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.



Doc. No.: TD-LO18-SP-2003	Doc. Title: 0.18um Logic Low Leakage 1P6M (1P5M, 1P4M) Salicide 1.8V/5.0V SPICE Model (Version 1.3)	Doc. Rev: 4R	Tech Dev Rev.: 1.3	Page No.: 16/16
------------------------------	--------------------------------------------------------------------------------------------------------------------	-----------------	-----------------------	--------------------

Table E3. Ring Oscillator (inverter) Gate Delay for MOS 1.8V

Version 0.1 (Vdd=1.8V, unit:ps/stage)						
Temp	F.O.	TT	SS	FNSP	SNFP	FF
25C	1	34.64	44.04	35.57	34.19	27.50
125C	1	39.40	50.00	40.00	38.98	31.01
-40C	1	31.21	39.49	32.23	30.86	25.00
25C	3	70.20	88.53	72.31	68.72	55.69
125C	3	79.07	100.00	80.83	77.83	62.43
-40C	3	63.75	79.87	65.90	62.23	50.97
Version 1.3 (Vdd=1.8V, unit:ps/stage)						
Temp	F.O.	TT	SS	FNSP	SNFP	FF
25C	1	36.09	46.01	37.13	35.07	28.17
125C	1	40.81	52.23	41.78	39.73	31.64
-40C	1	32.56	41.23	33.55	31.66	25.65
25C	3	71.16	90.34	73.44	68.98	55.75
125C	3	80.05	101.98	82.18	77.73	62.27
-40C	3	64.52	81.32	66.68	62.57	51.04

The information contained herein is the exclusive property of SMIC, and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of SMIC.