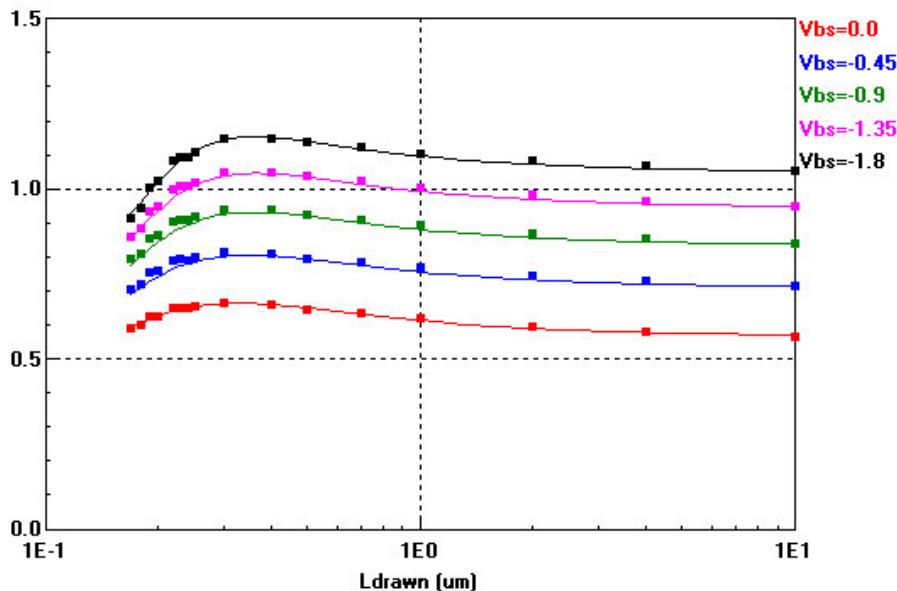
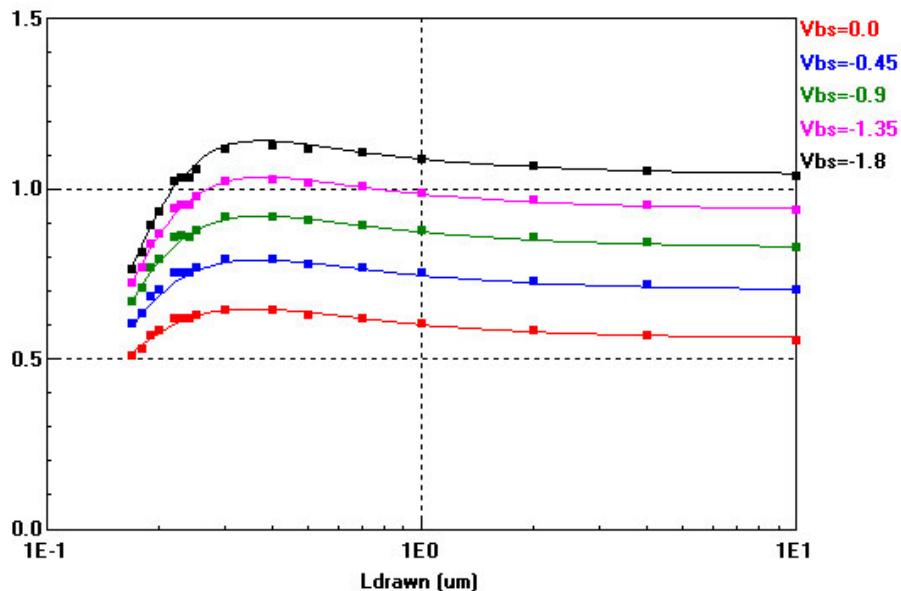


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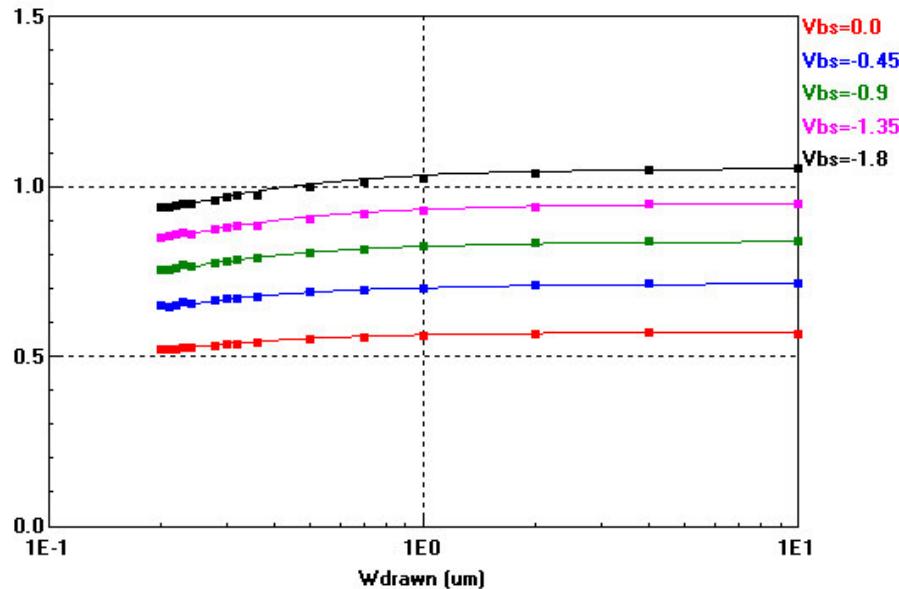
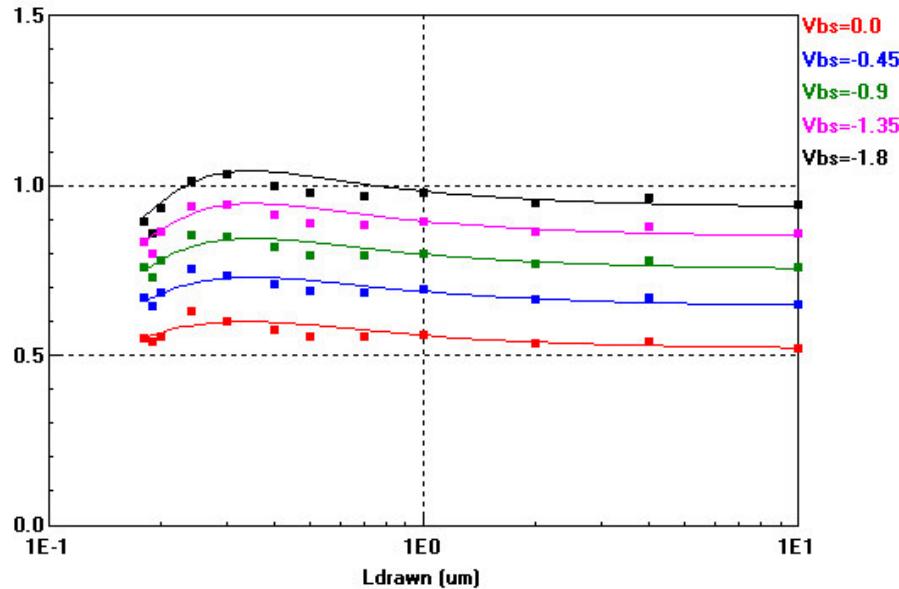
 V_{th} (V) V_{th} versus L at W=10.00 (symbol:measured data, line:model simulation)

 Fig.A1 V_{th} versus L at Wdrawn = 10um for 1.8V NMOS

 V_{tsat} (V) V_{tsat} versus L at W=10.00 [symbol:measured data, line:model simulation]

 Fig.A2 V_{tsat} versus L at Wdrawn = 10um for 1.8V NMOS

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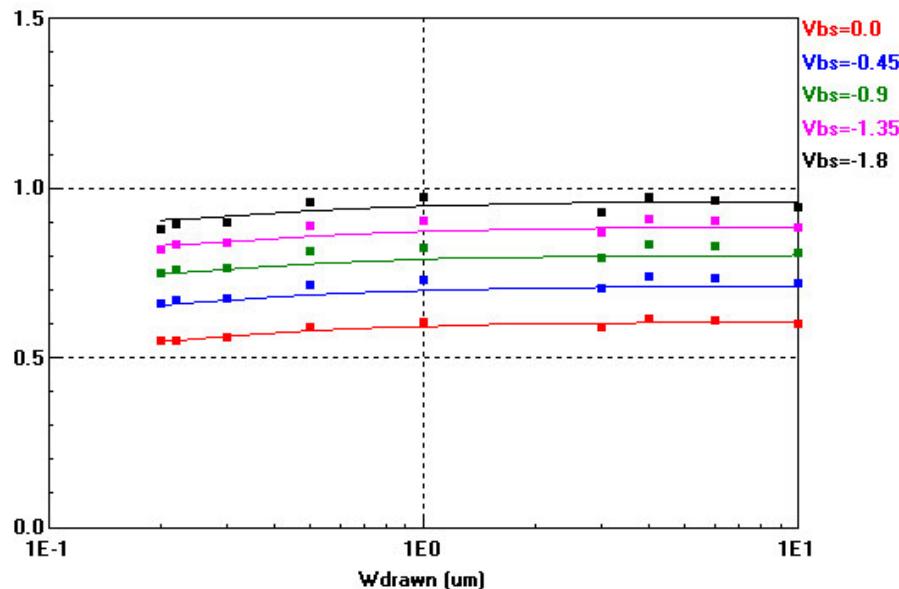


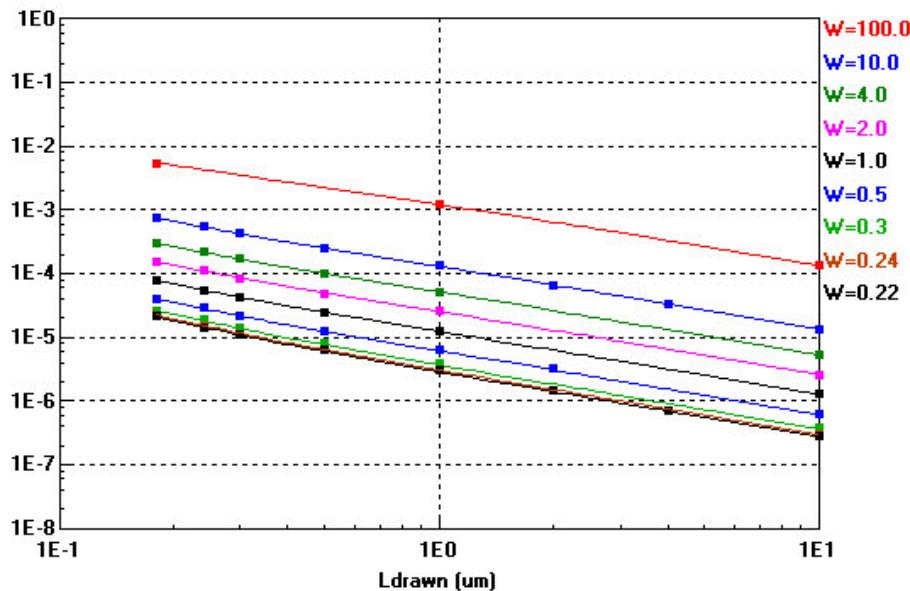
Doc. No.: TD-LO18-SP-2003	Doc. Title: 0.18um Logic Low Leakage 1P6M (1P5M, 1P4M) Salicide 1.8V/5.0V SPICE Model (Version 1.3)	Doc. Rev: 4R	Tech Dev Rev.: 1.3	Page No.: 2/45
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V_{th} [V] V_{th} versus W at L=10.00[symbol:measured data, line:model simulation]Fig.A3 V_{th} versus W at L_{drawn} = 10um for 1.8V NMOSV_{th} [V] V_{th} versus L at W=0.22[symbol:measured data, line:model simulation]Fig.A4 V_{th} versus L at W_{drawn} =0.22um for 1.8V NMOS

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V_{th} (V) V_{th} versus W at L=0.18 (symbol:measured data, line:model simulation)

 Fig.A5 V_{th} versus W at Ldrawn = 0.18um for 1.8V NMOS

I_{ddlin} (A) I_{ddlin} versus L at V_{bs} = 0 (symbol:measured data, line:model simulation)

 Fig.A6 I_{ddlin} versus L with different width array at V_{bs}=0V for 1.8V NMOS

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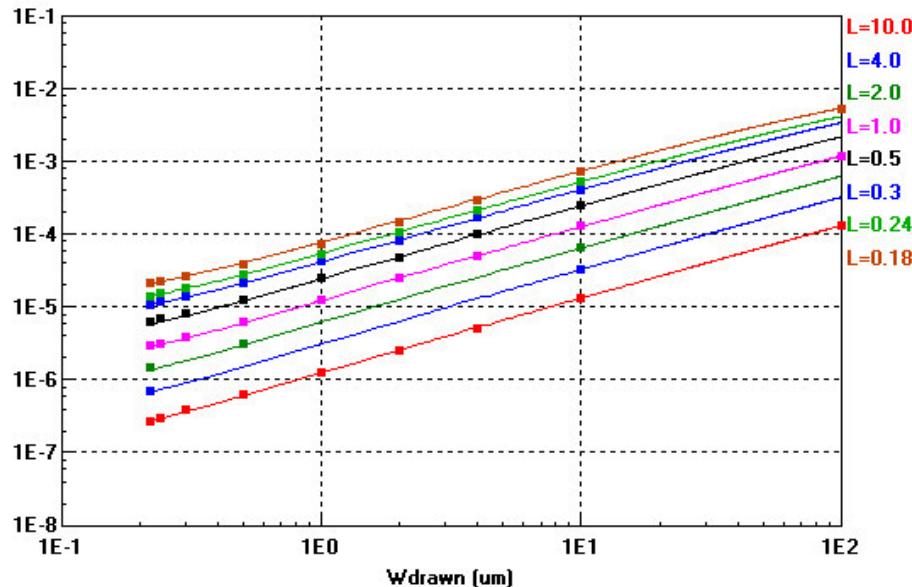
Idlin (A) Idlin versus W at Vbs = 0 (symbol:measured data, line:model simulation)


Fig.A7 Idlin versus W with different length array at Vbs=0V for 1.8V NMOS

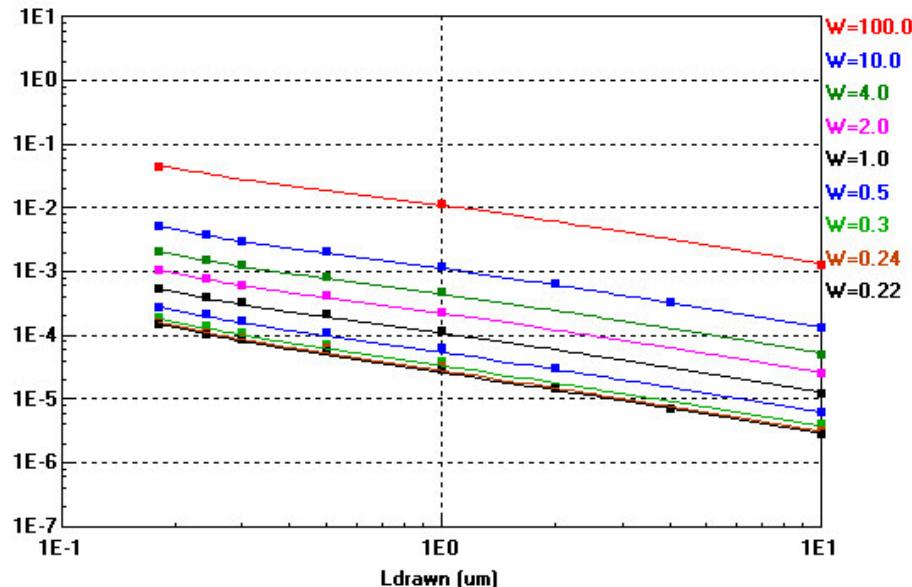
Idsat (A) Idsat versus L at Vbs = 0 (symbol:measured data, line:model simulation)


Fig.A8 Idsat versus L with different width array at Vbs=0V for 1.8V NMOS

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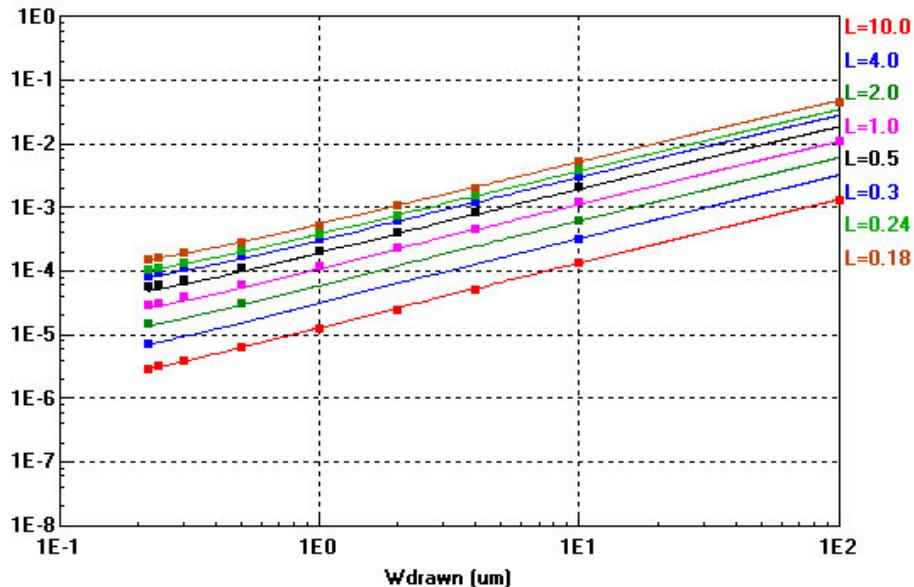
Idsat (A) Idsat versus W at Vbs = 0 (symbol:measured data, line:model simulation)


Fig.A9 Idsat versus W with different length array at Vbs=0V for 1.8V NMOS

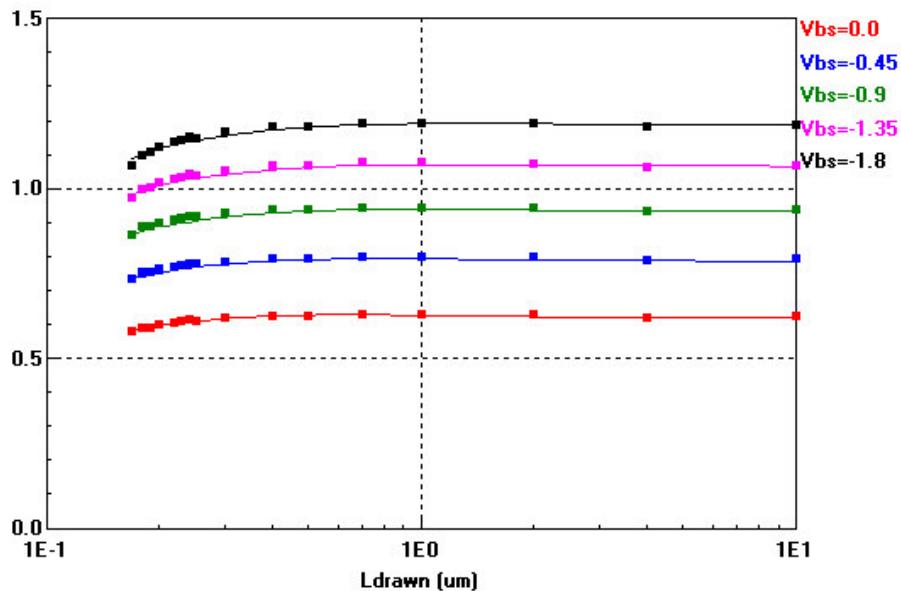
Vth (V) Vth versus L at W=10.00 (symbol:measured data, line:model simulation)


Fig.A10 Vth versus L at Wdrawn = 10um for 1.8V PMOS

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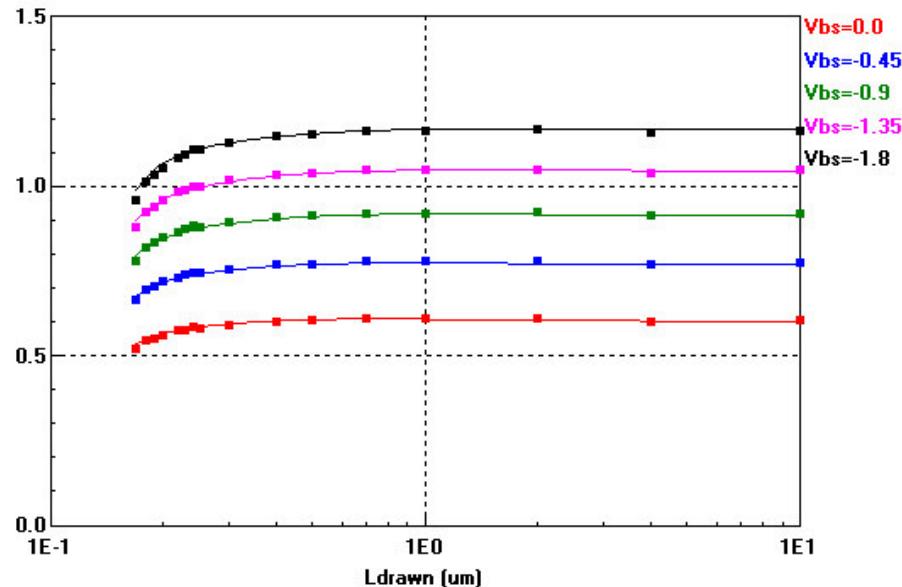
Vtsat (V) Vtsat versus L at W=10.00(symbol:measured data, line:model simulation)


Fig.A11 Vtsat versus L at Wdrawn = 10um for 1.8V PMOS

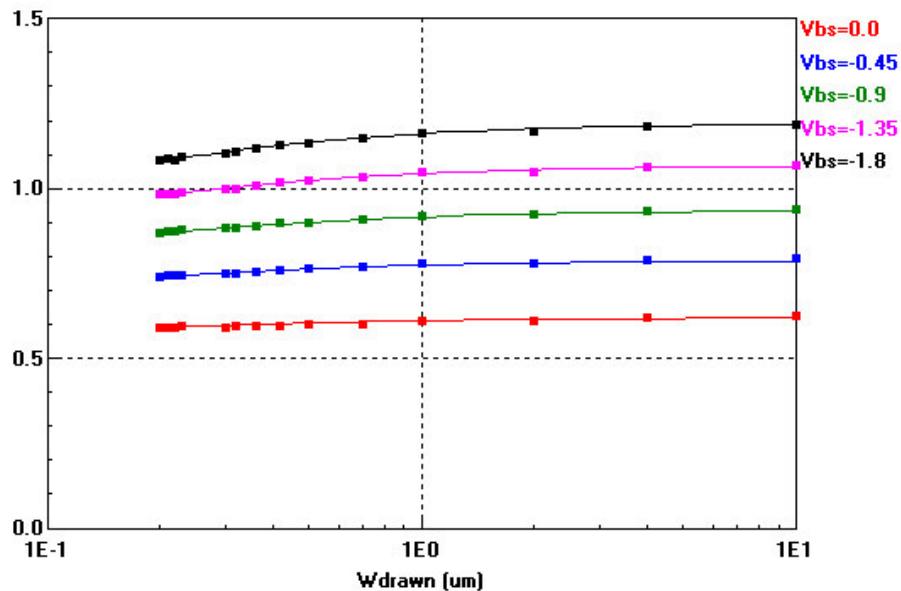
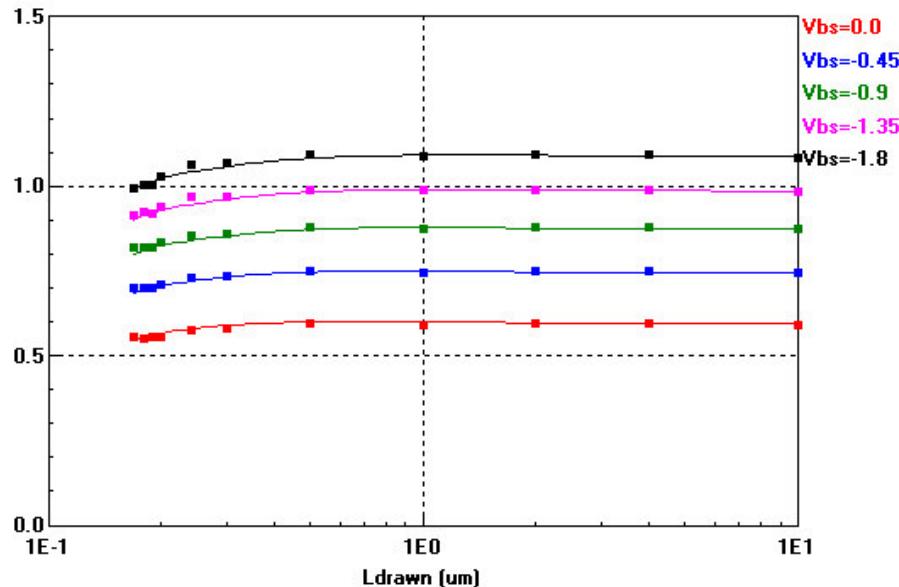
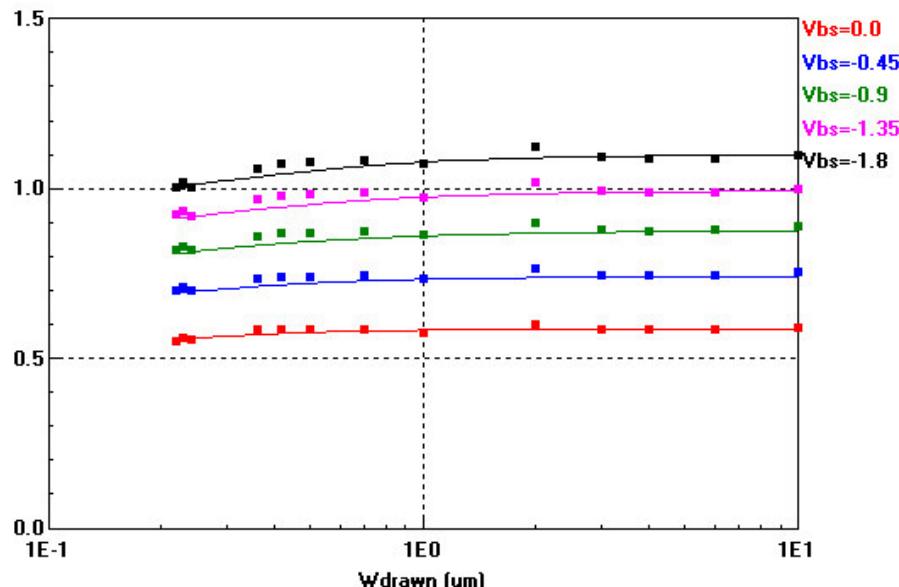
Vth (V) Vth versus W at L=10.00(symbol:measured data, line:model simulation)


Fig.A12 Vth versus W at Ldrawn = 10um for 1.8V PMOS

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 V_{th} [V] V_{th} versus L at W=0.22[symbol:measured data, line:model simulation]

 Fig.A13 V_{th} versus L at W_{drawn} = 0.22um for 1.8V PMOS

 V_{th} [V] V_{th} versus W at L=0.18[symbol:measured data, line:model simulation]

 Fig.A14 V_{th} versus W at L_{drawn} = 0.18um for 1.8V PMOS

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According to: Document Control Procedure; Attachment No.: QR-QUSM-02-2001-002; Rev.:0

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Idlin (A) Idlin versus L at Vbs = 0 [symbol:measured data, line:model simulation]

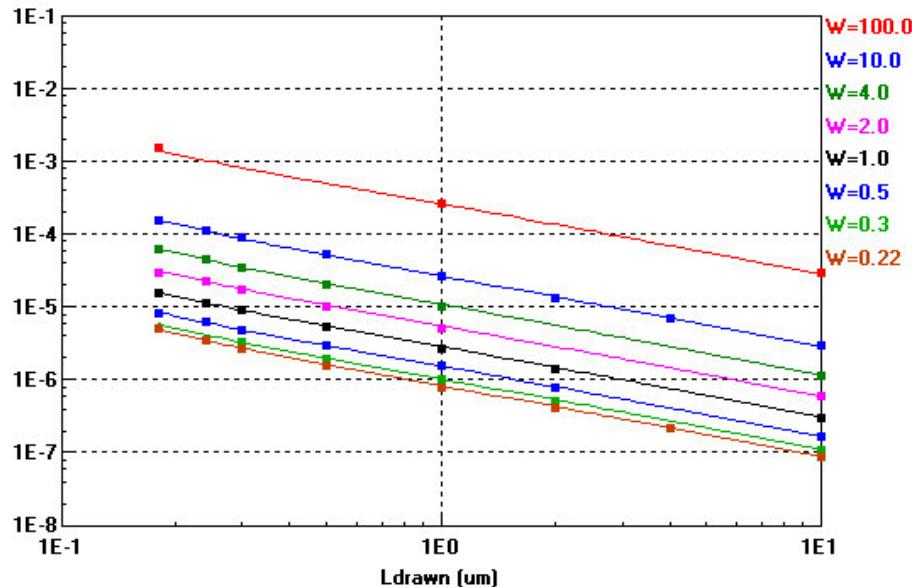


Fig.A15 Idlin versus L with different width array at Vbs=0V for 1.8V PMOS

Idlin (A) Idlin versus W at Vbs = 0 [symbol:measured data, line:model simulation]

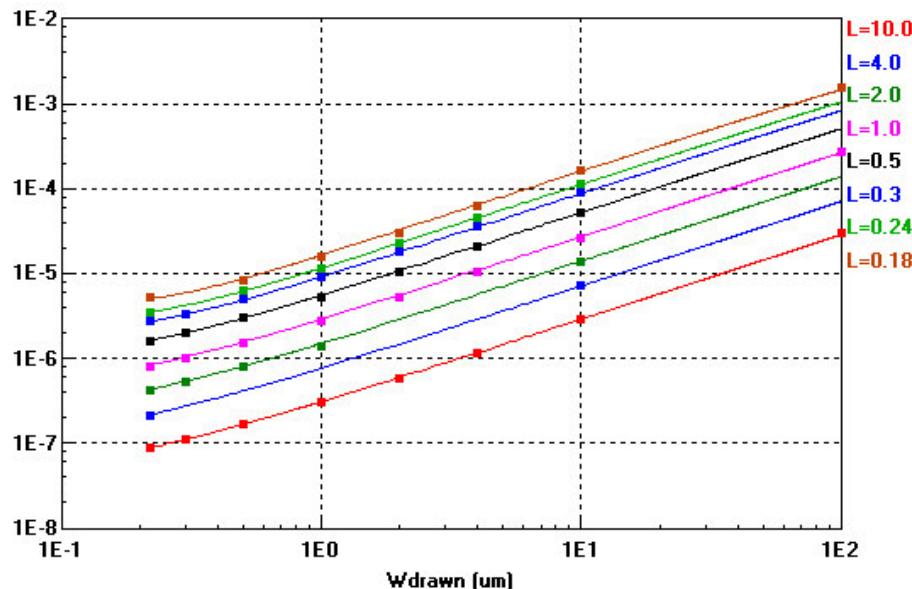


Fig.A16 Idlin versus W with different length array at Vbs=0V for 1.8V PMOS

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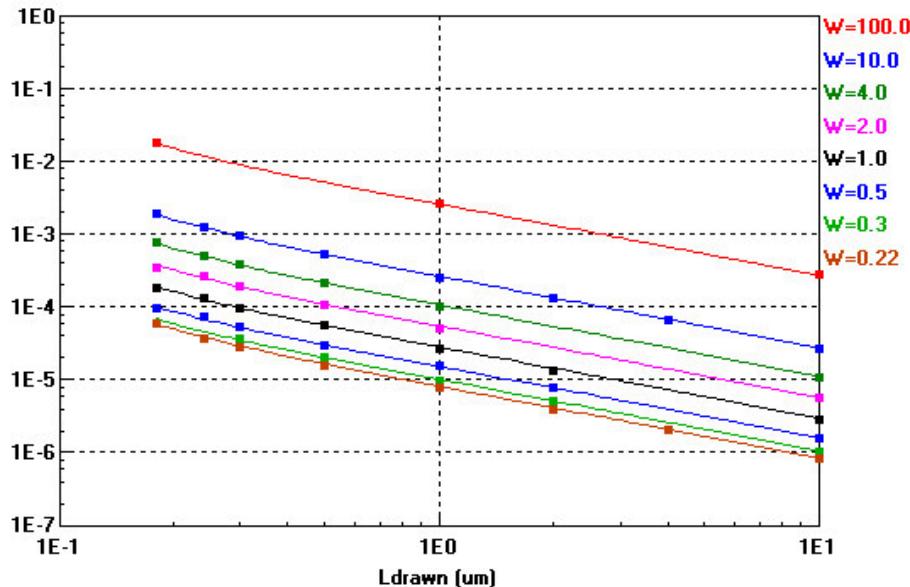
Idsat (A) Idsat versus L at Vbs = 0 [symbol:measured data, line:model simulation]


Fig.A17 Idsat versus L with different width array at Vbs=0V for 1.8V PMOS

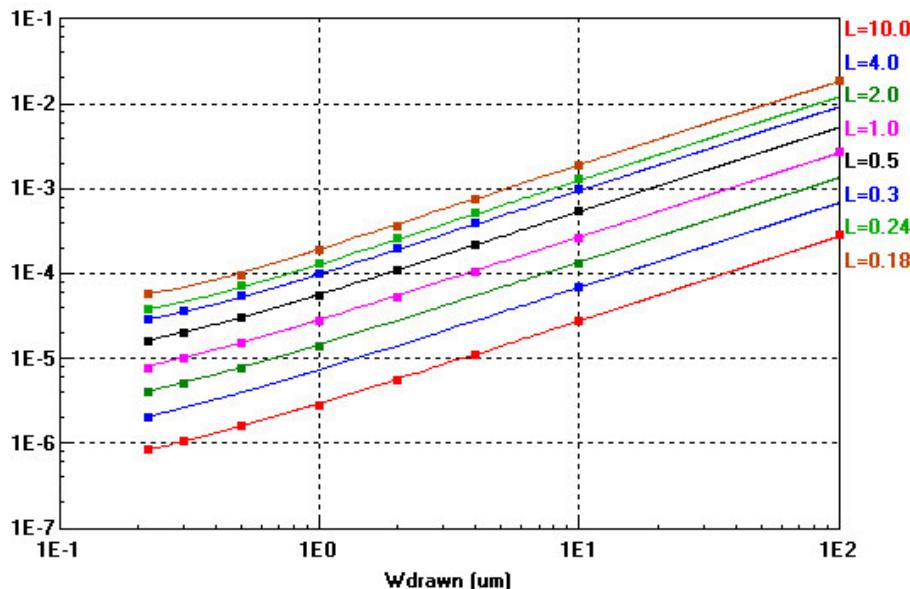
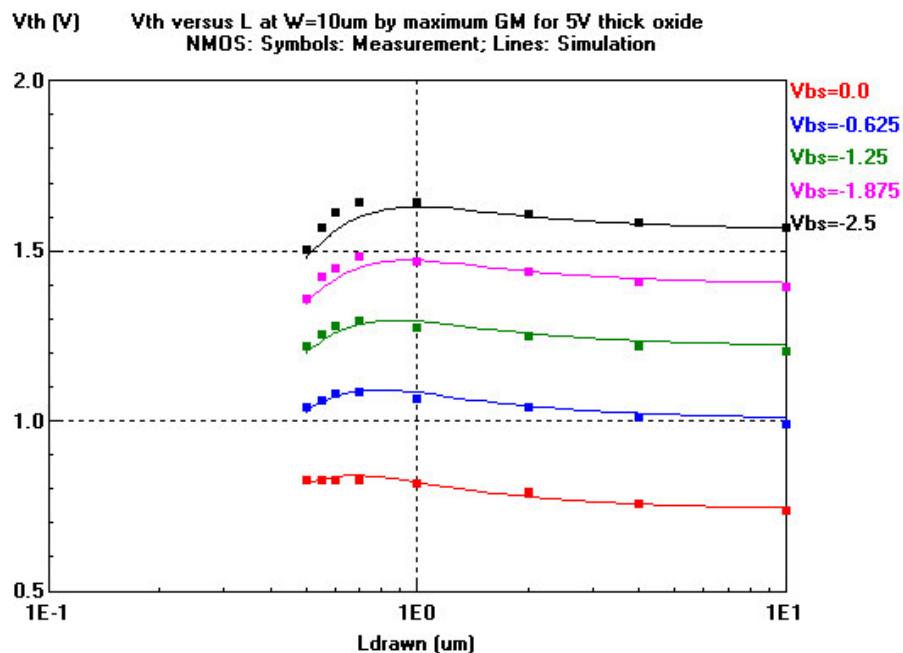
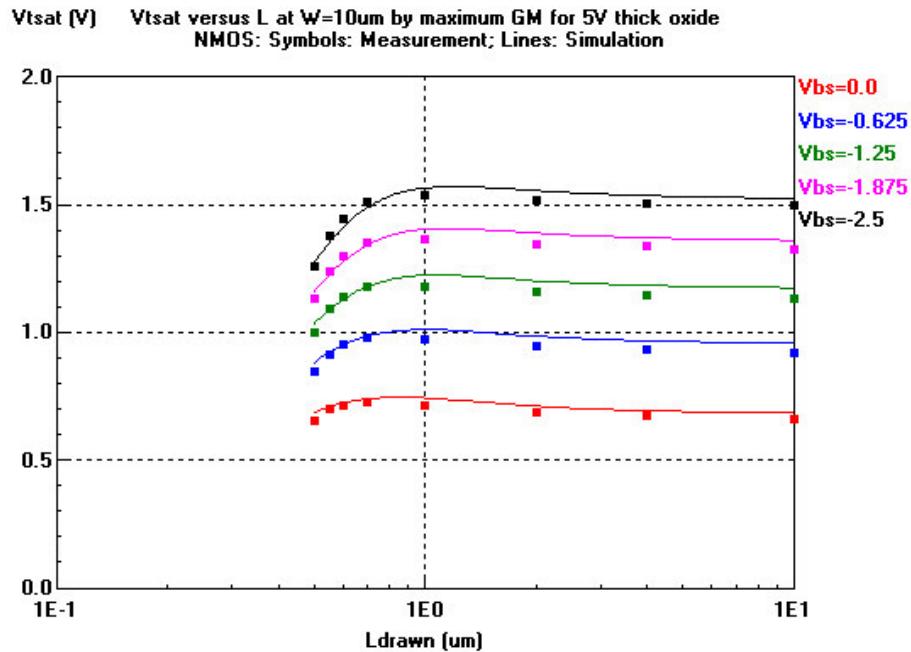
Idsat (A) Idsat versus W at Vbs = 0 [symbol:measured data, line:model simulation]


Fig.A18 Idsat versus W with different length array at Vbs=0V for 1.8V PMOS

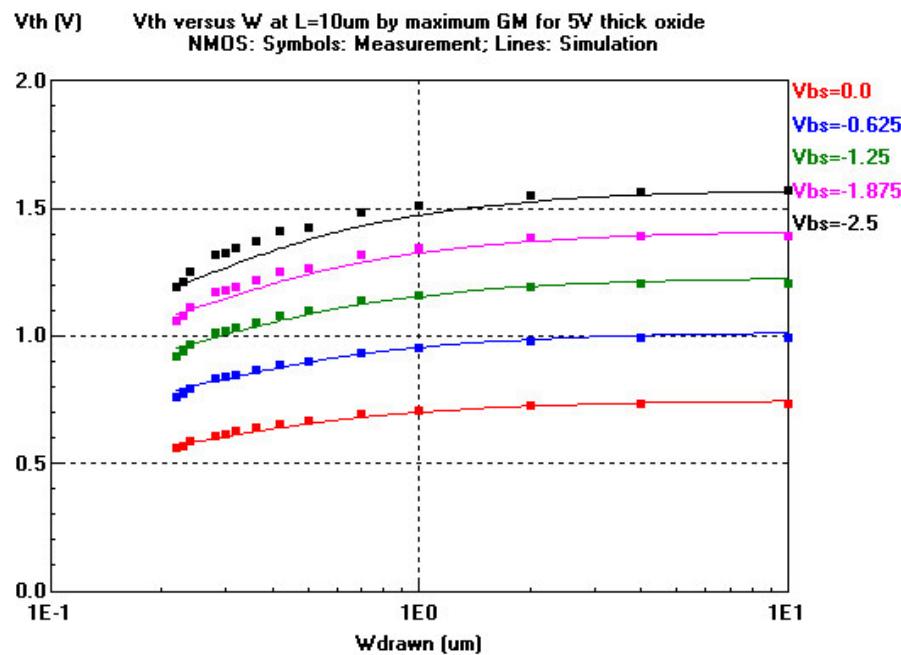
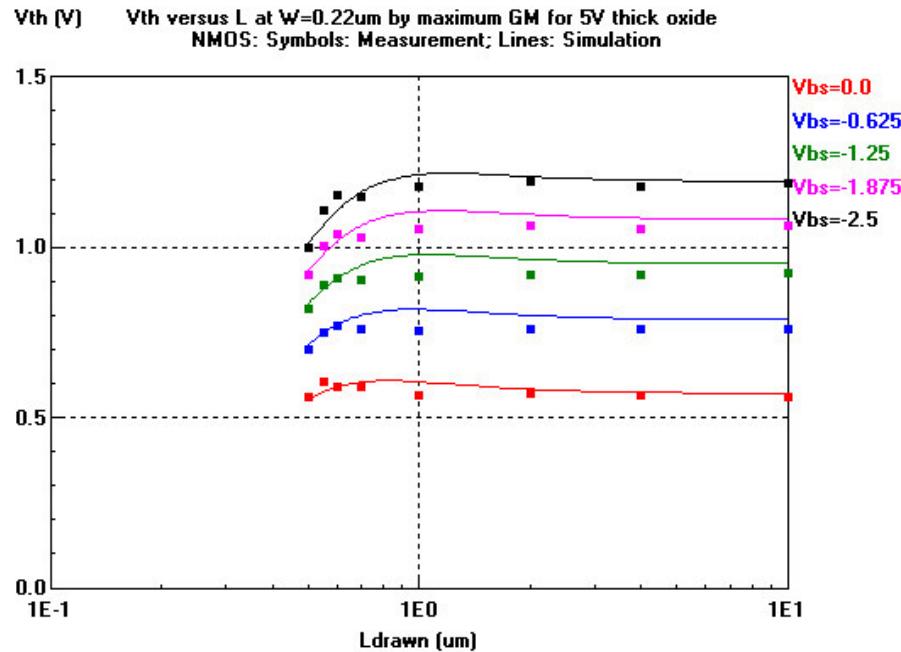
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 Fig.A19 V_{th} versus L at Wdrawn =10um for 5V NMOS

 Fig.A20 V_{tsat} versus L at Wdrawn =10um for 5V NMOS

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 Fig.A21 V_{th} versus W at Ldrawn = 10um for 5V NMOS

 Fig.A22 V_{th} versus L at Wdrawn = 0.22um for 5V NMOS

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TD-LO18-SP-2003	0.18um Logic Low Leakage 1P6M (1P5M, 1P4M) Salicide 1.8V/5.0V SPICE Model (Version 1.3)	4R	Rev.: 1.3	12/45

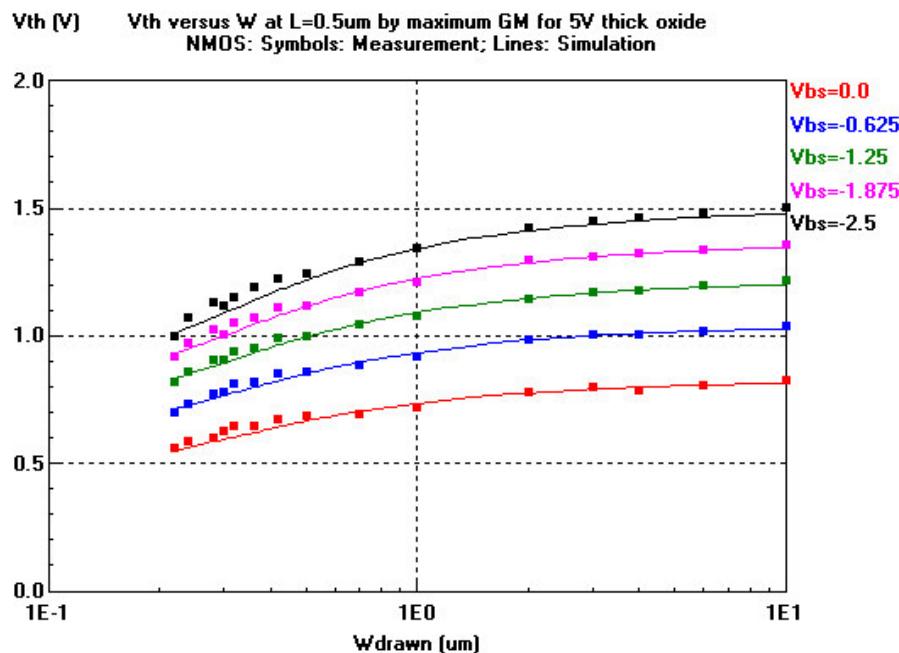


Fig.A23 V_{th} versus W at L_{drawn} = 0.5um for 5V NMOS

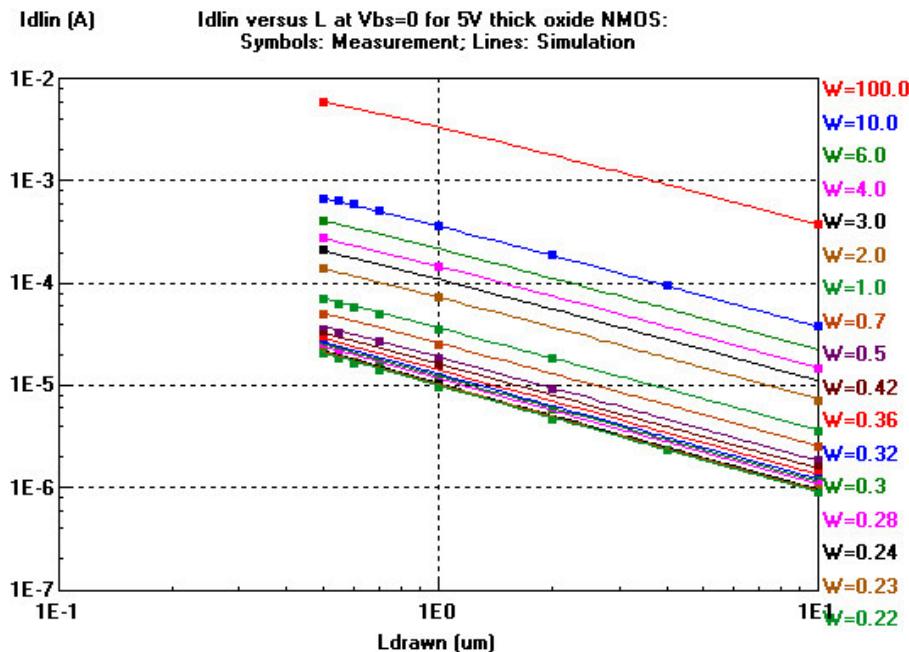


Fig.A24 I_{ddlin} versus L with different width array at V_{bs}=0V for 5V NMOS

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TD-LO18-SP-2003	0.18um Logic Low Leakage 1P6M (1P5M, 1P4M) Salicide 1.8V/5.0V SPICE Model (Version 1.3)	4R	Rev.: 1.3	13/45

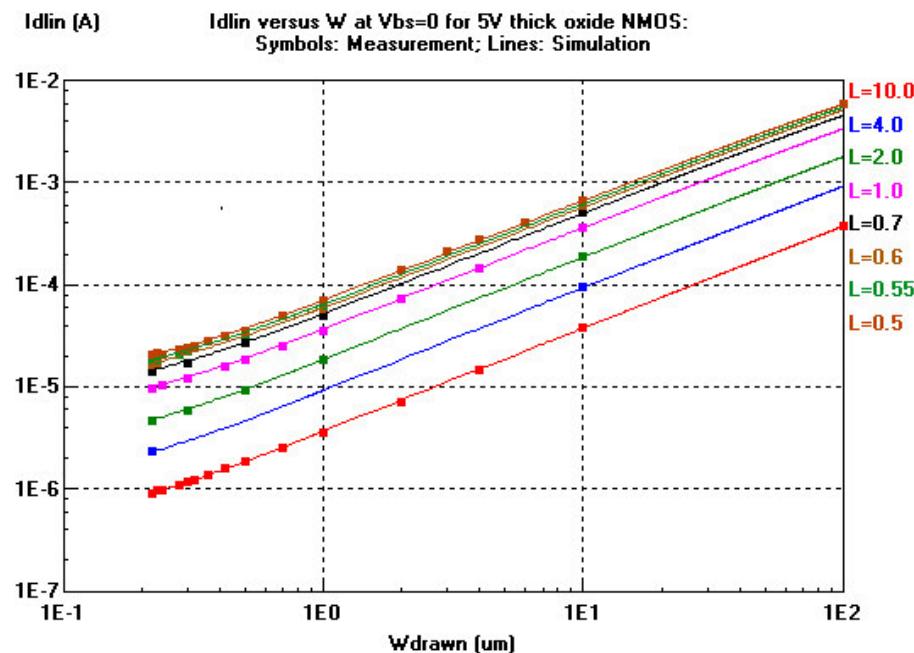


Fig.A25 Idlin versus W with different length array at Vbs=0V for 5V NMOS

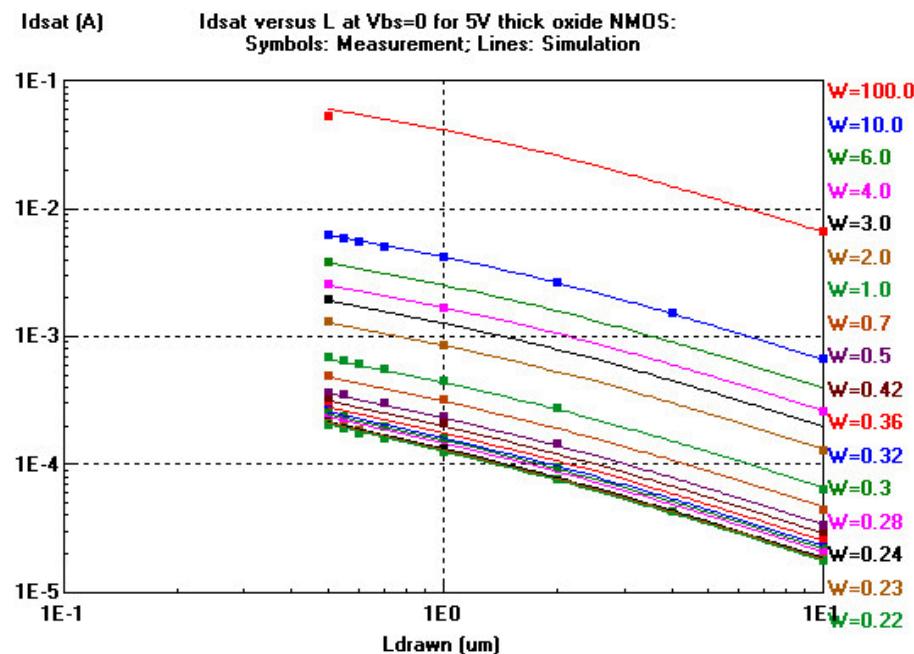


Fig.A26 Idsat versus L with different width array at Vbs=0V for 5V NMOS

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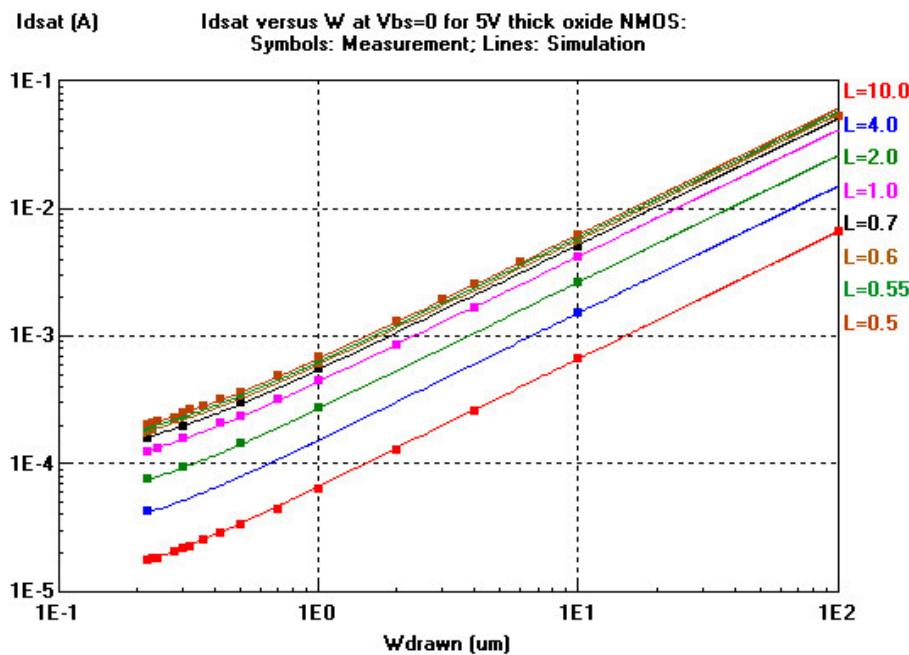


Fig.A27 Idsat versus W with different length array at Vbs=0V for 5V NMOS

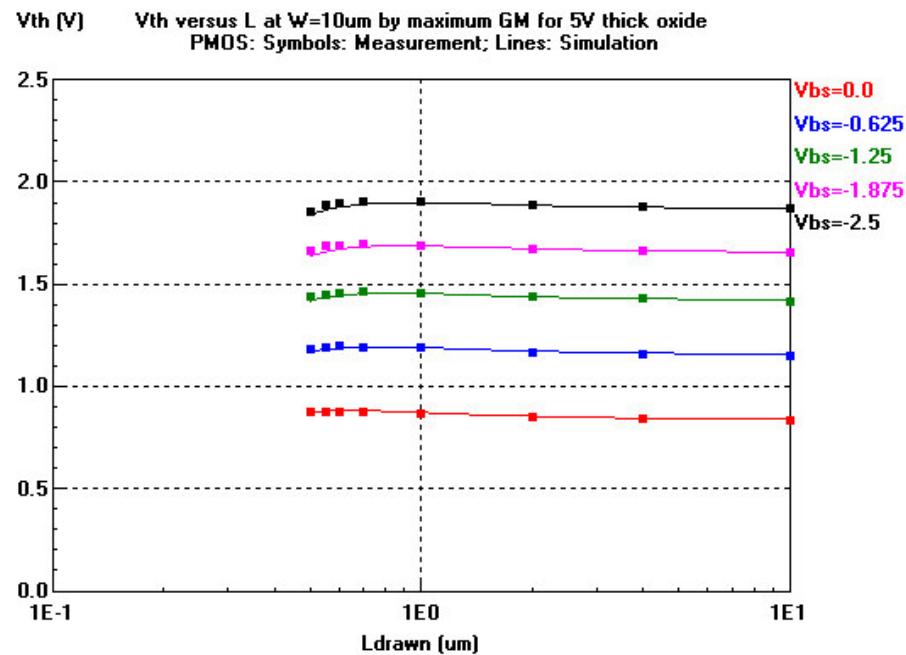


Fig.A28 Vth versus L at Wdrawn =10um for 5V PMOS

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V_{tsat} (V) V_{tsat} versus L at W=10um by maximum GM for 5V thick oxide
PMOS: Symbols: Measurement; Lines: Simulation

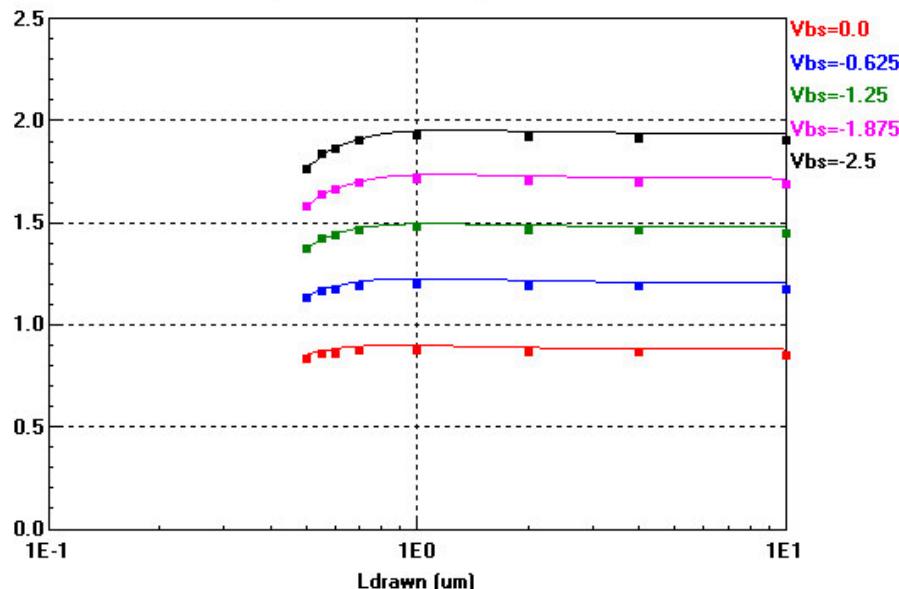


Fig.A29 V_{tsat} versus L at Wdrawn =10um for 5V PMOS

V_{th} (V) V_{th} versus W at L=10um by maximum GM for 5V thick oxide
PMOS: Symbols: Measurement; Lines: Simulation

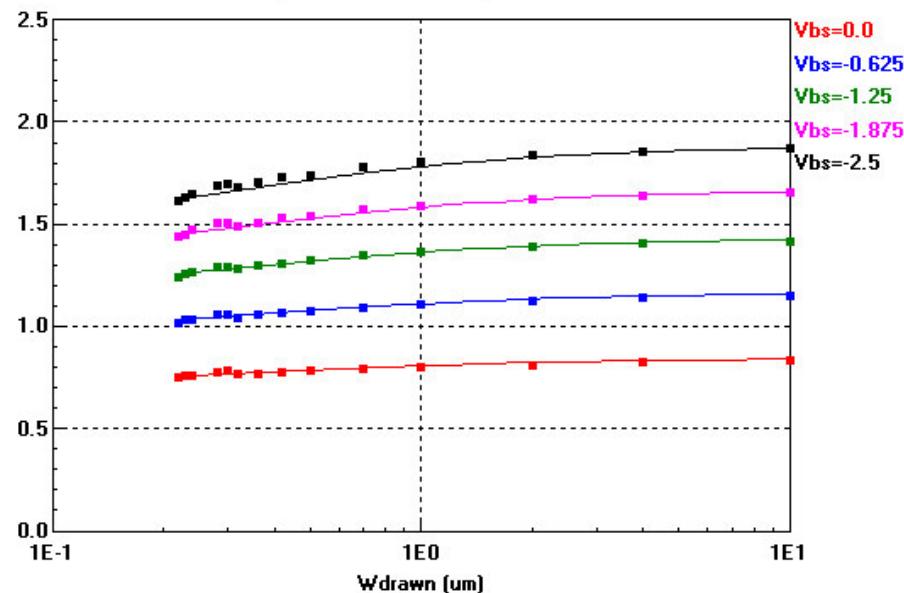


Fig.A30 V_{th} versus W at Ldrawn =10um for 5V PMOS

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TD-LO18-SP-2003	0.18um Logic Low Leakage 1P6M (1P5M, 1P4M) Salicide 1.8V/5.0V SPICE Model (Version 1.3)	4R	Rev.: 1.3	16/45

V_{th} (V) V_{th} versus L at W=0.22um by maximum GM for 5V thick oxide
PMOS: Symbols: Measurement; Lines: Simulation

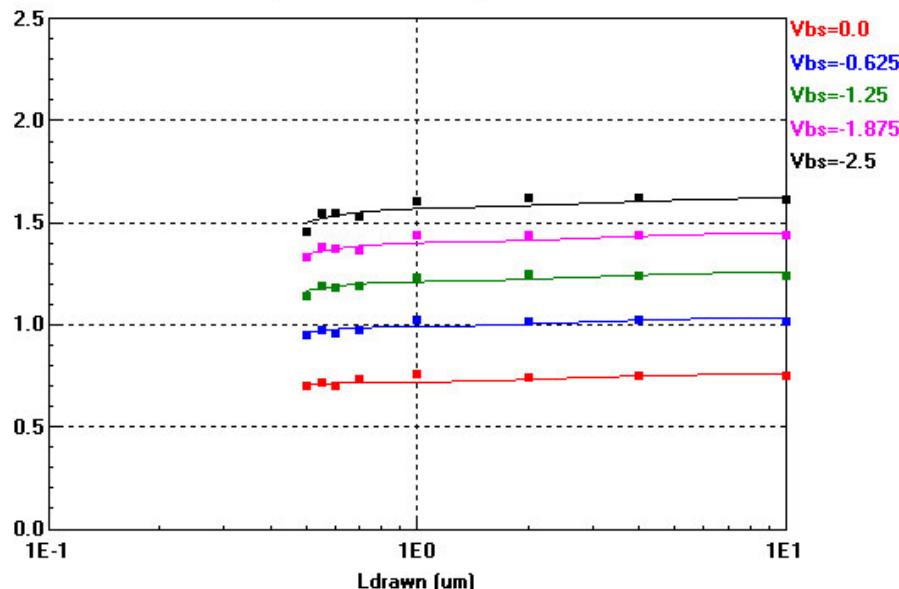


Fig.A31 V_{th} versus L at Wdrawn =0.22um for 5V PMOS

V_{th} (V) V_{th} versus W at L=0.5um by maximum GM for 5V thick oxide
PMOS: Symbols: Measurement; Lines: Simulation

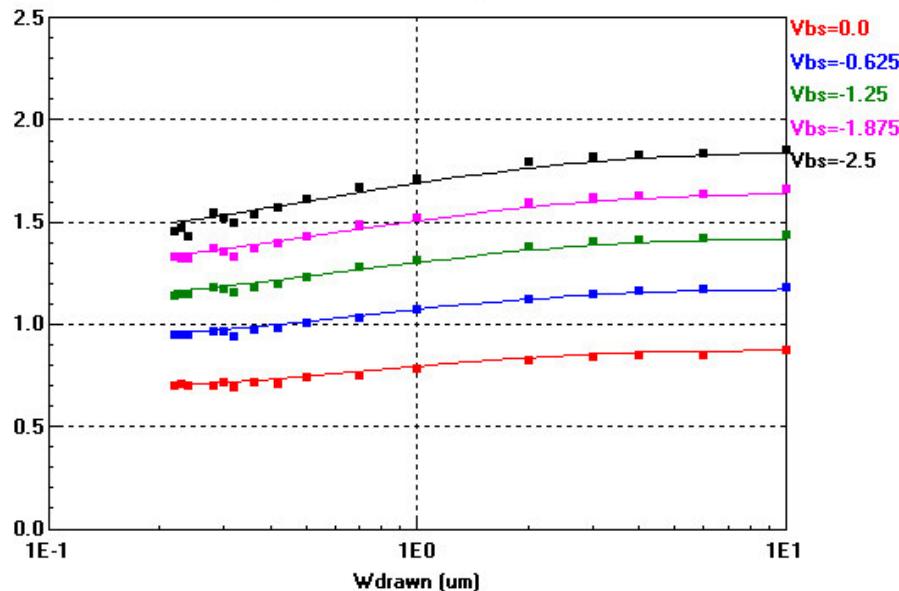


Fig.A32 V_{th} versus W at Ldrawn = 0.5um for 5V PMOS

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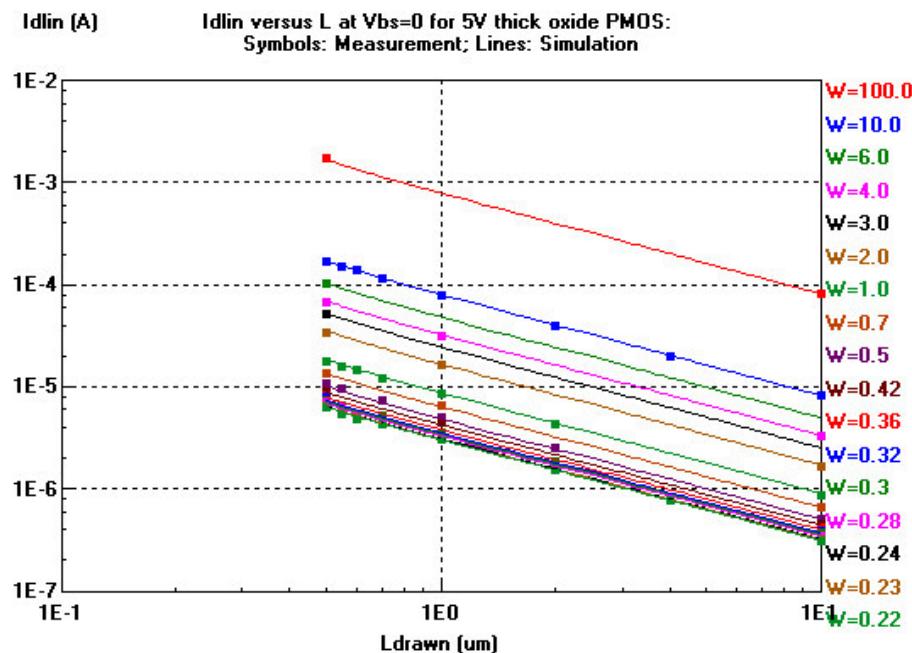


Fig.A33 Idlin versus L with different width array at Vbs=0V for 5V PMOS

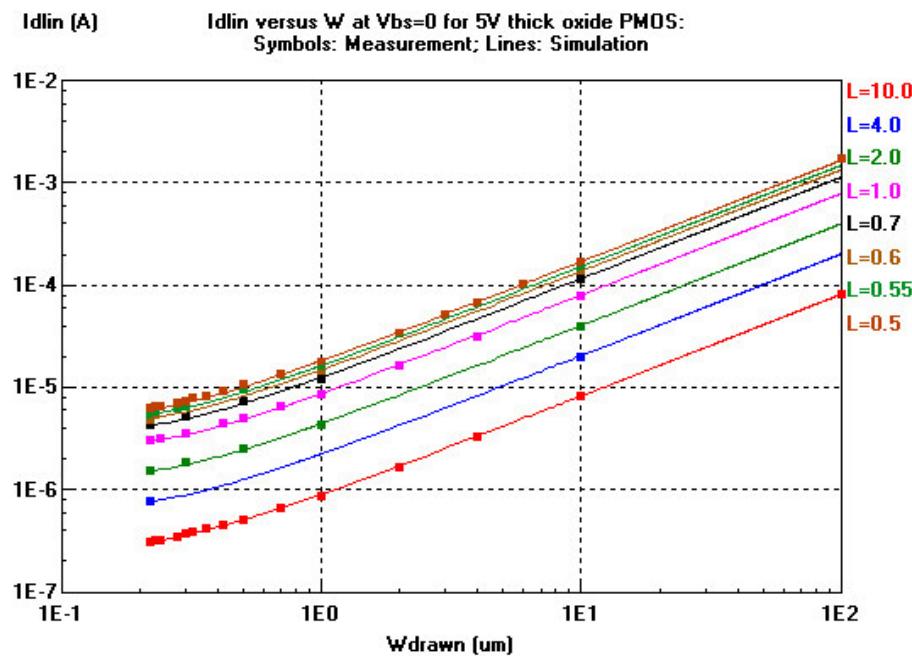


Fig.A34 Idlin versus W with different length array at Vbs=0V for 5V PMOS

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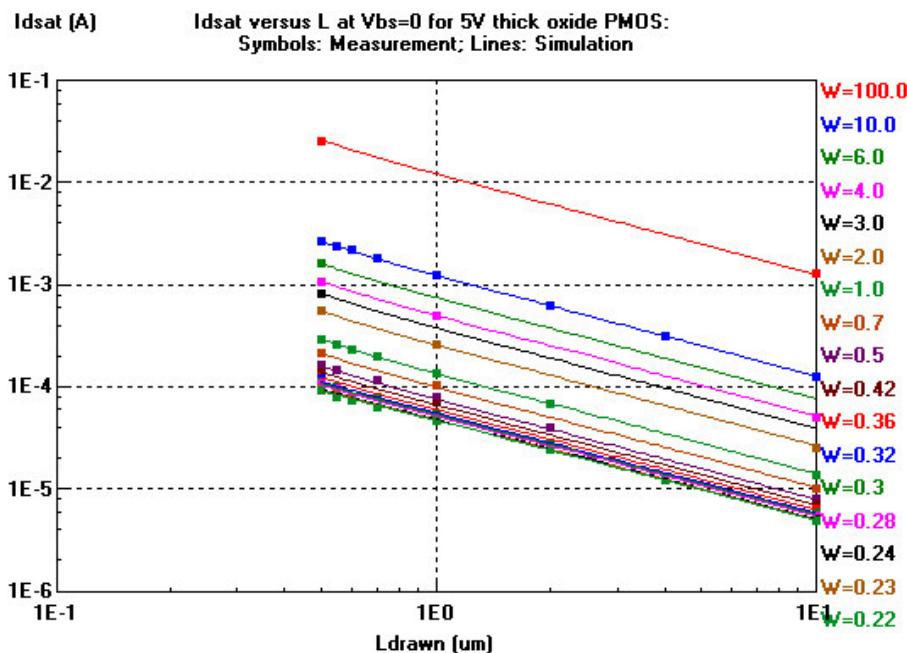


Fig.A35 Idsat versus L with different width array at Vbs=0V for 5V PMOS

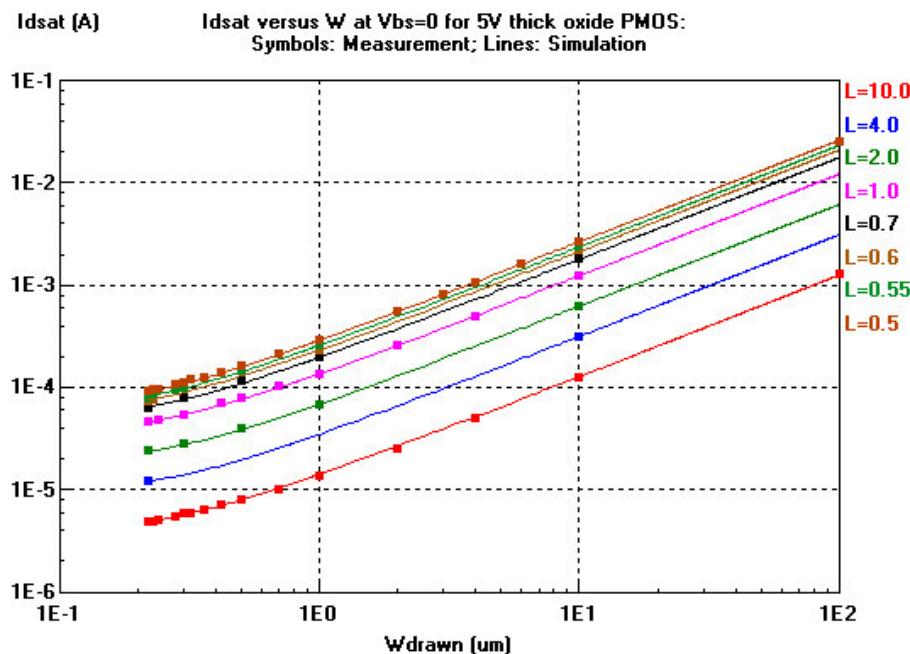


Fig.A36 Idsat versus W with different length array at Vbs=0V for 5V PMOS

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Vth [V] Vth versus T at W=10.00(symbol:measured data, line:model simulation)

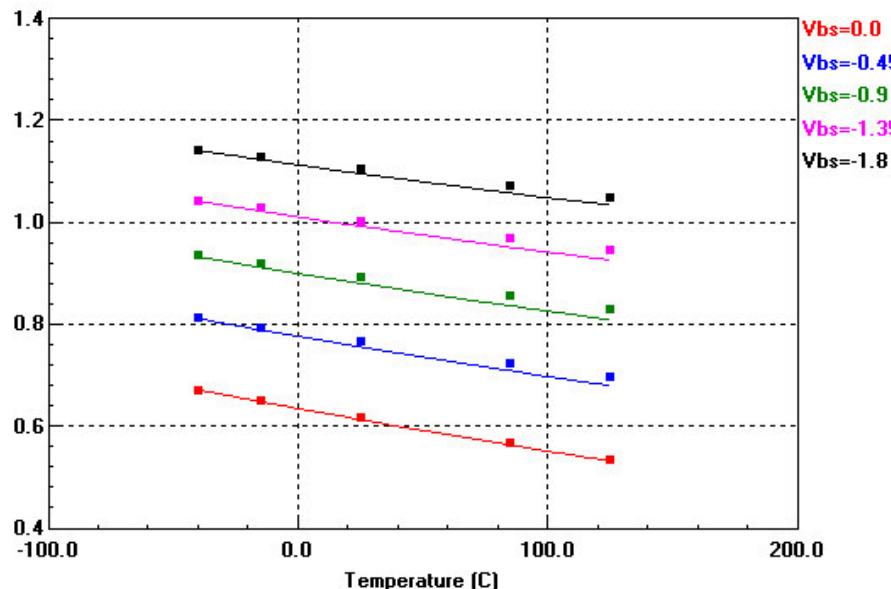


Fig.A37 Vth vs. T measured and simulated plot with various Vbs for 1.8V NMOS 10/10

Vth [V] Vth versus T at W=10.00(symbol:measured data, line:model simulation)

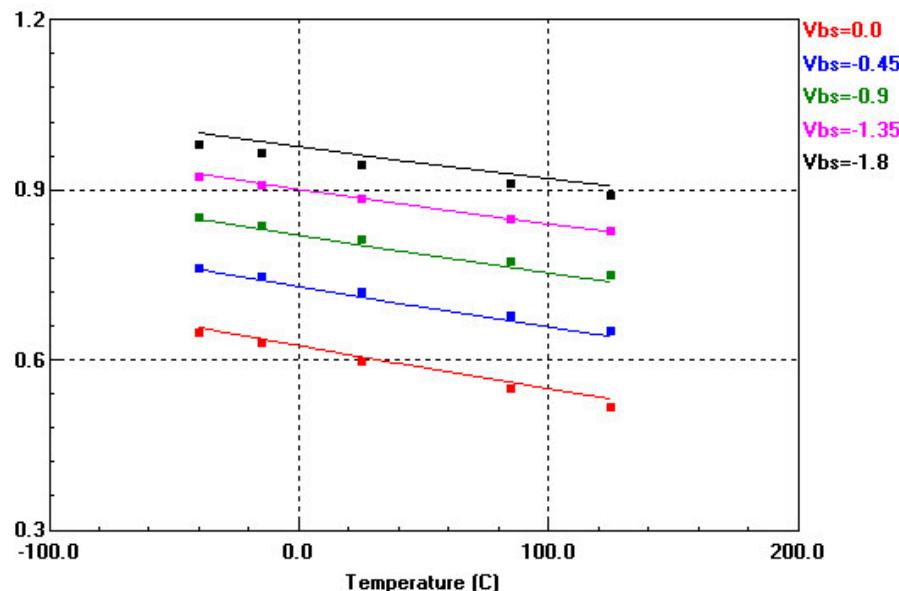


Fig.A38 Vth vs. T measured and simulated plot with various Vbs for 1.8V NMOS 10/0.18

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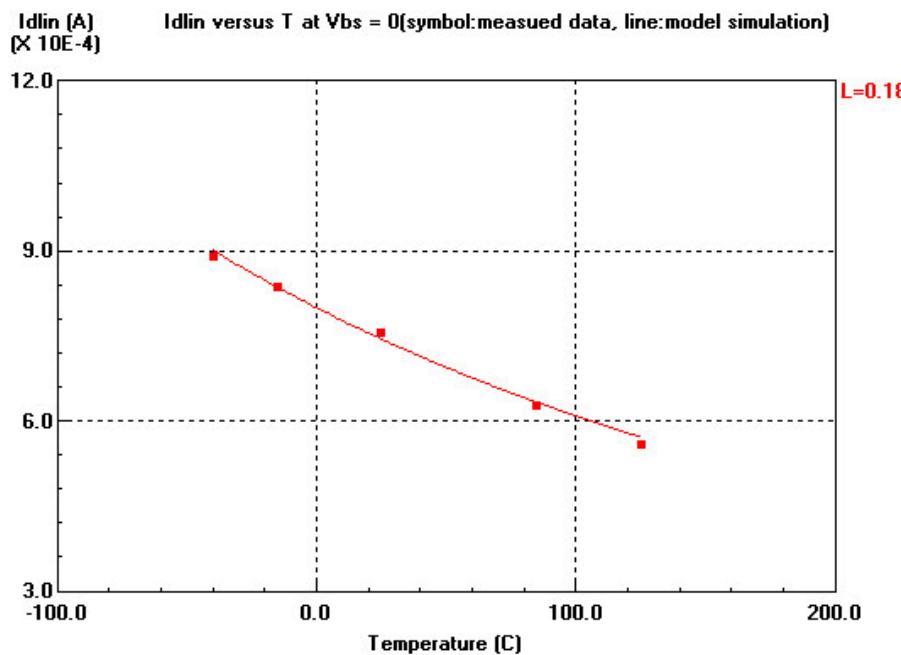


Fig.A39 Idlin vs. T measured and simulated plot with Vbs=0V for 1.8V NMOS 10/0.18

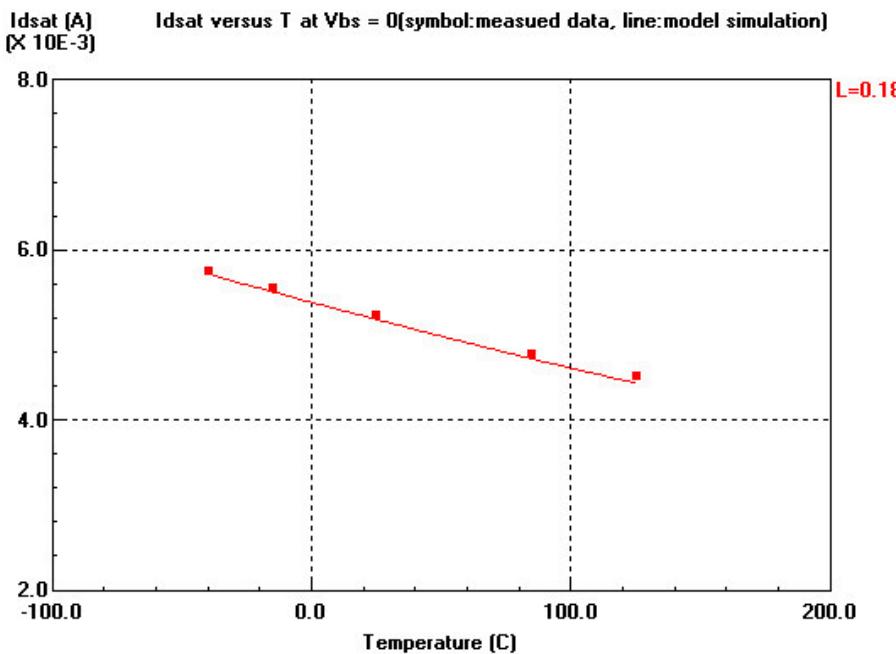


Fig.A40 Idsat vs. T measured and simulated plot with Vbs=0V for 1.8V NMOS 10/0.18

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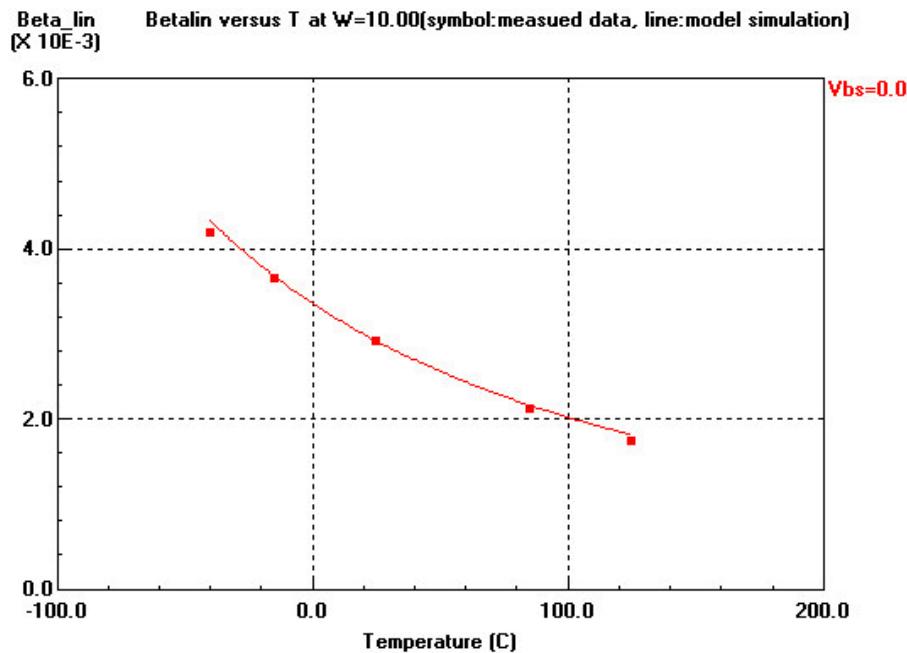


Fig.A41 Betalin vs.T measured and simulated plot for 1.8V NMOS 10/10

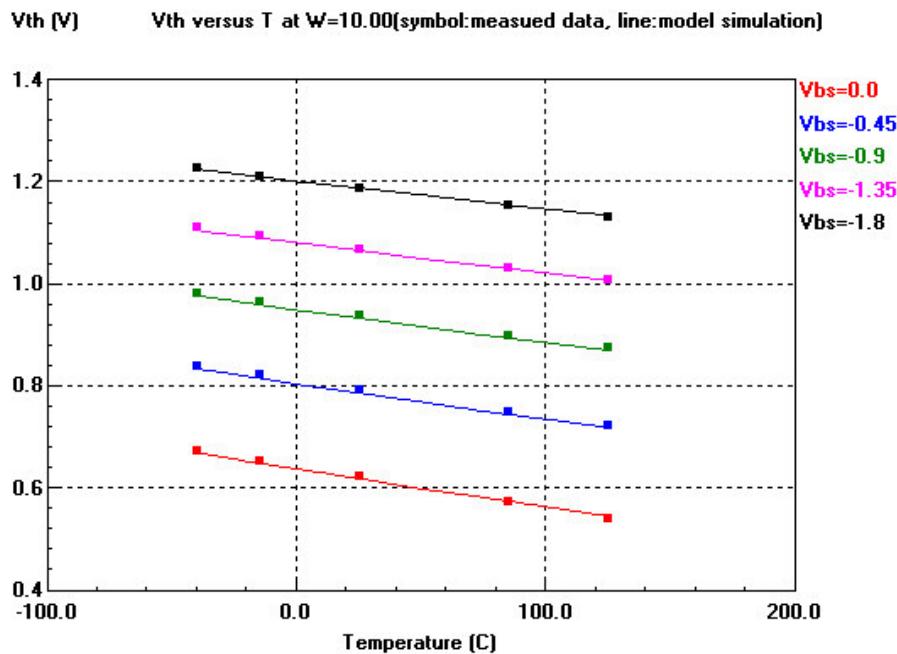
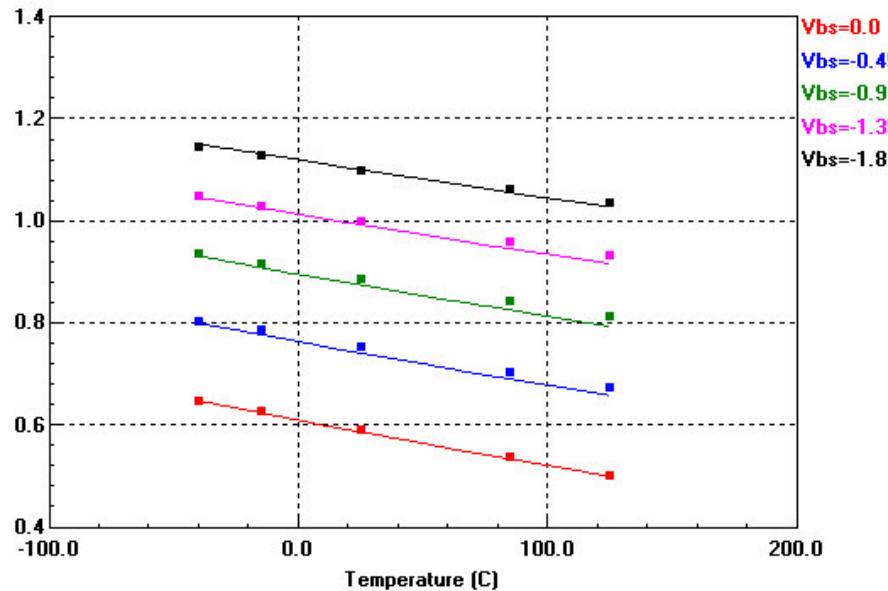
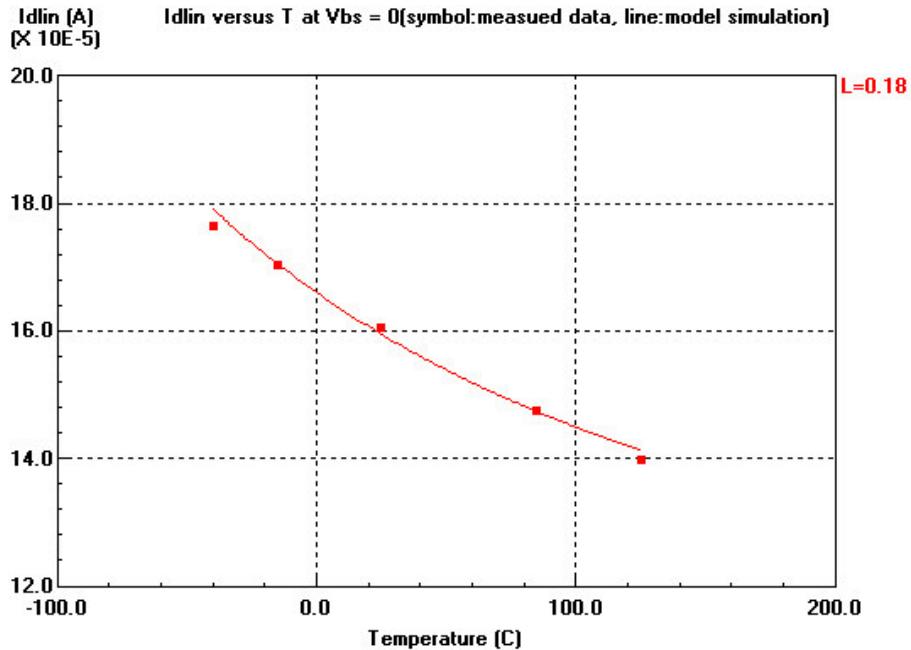


Fig.A42 Vth vs. T measured and simulated plot with various Vbs for 1.8V PMOS 10/10

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V_{th} (V) V_{th} versus T at W=10.00 [symbol:measured data, line:model simulation]Fig.A43 V_{th} vs. T measured and simulated plot with various V_{bs} for 1.8V PMOS 10/0.18Fig.A44 I_{dlin} vs. T measured and simulated plot with V_{bs}=0V for 1.8V PMOS 10/0.18

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Doc. No.: TD-LO18-SP-2003	Doc. Title: 0.18um Logic Low Leakage 1P6M (1P5M, 1P4M) Salicide 1.8V/5.0V SPICE Model (Version 1.3)	Doc. Rev: 4R	Tech Dev Rev.: 1.3	Page No.: 23/45
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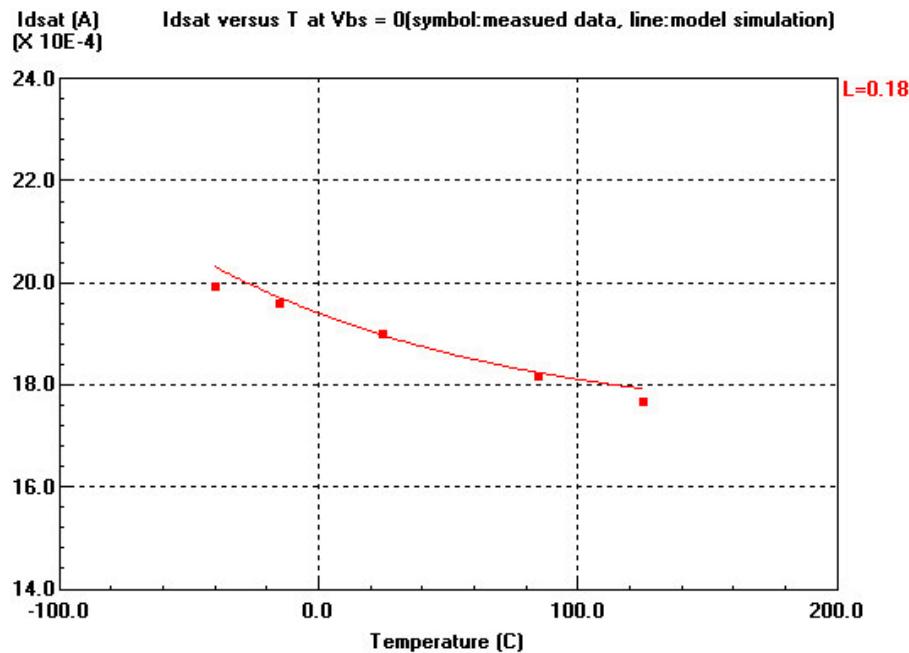


Fig.A45 Idsat vs. T measured and simulated plot with Vbs=0V for 1.8V PMOS 10/0.18

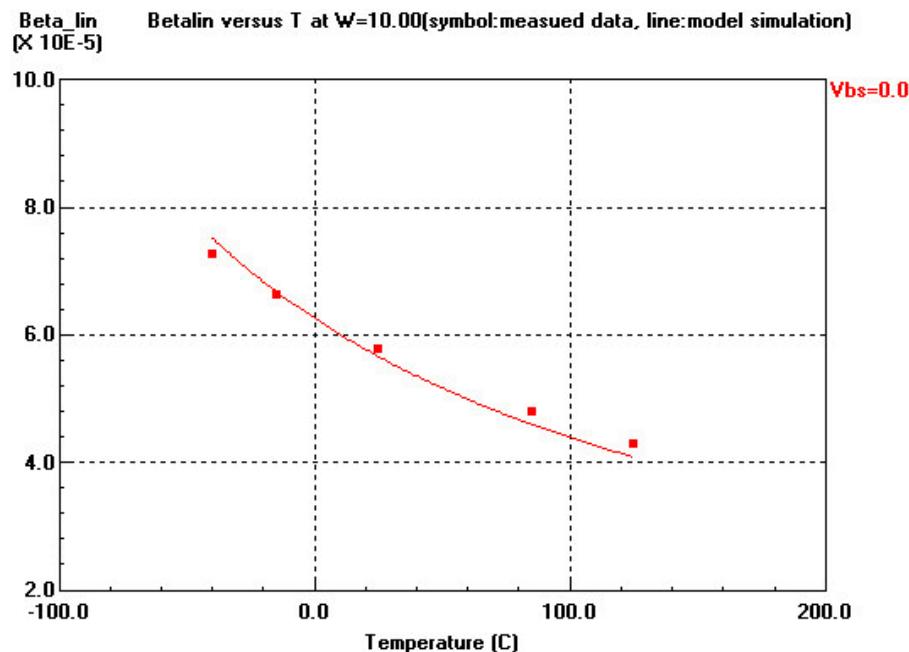


Fig.A46 Betalin vs.T measured and simulated plot for 1.8V PMOS 10/10

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V_{th} [V] V_{th} vs. T at 10/10 by maximum GM for 5V thick oxide NMOS:
Symbols: Measurement; Lines: Simulation

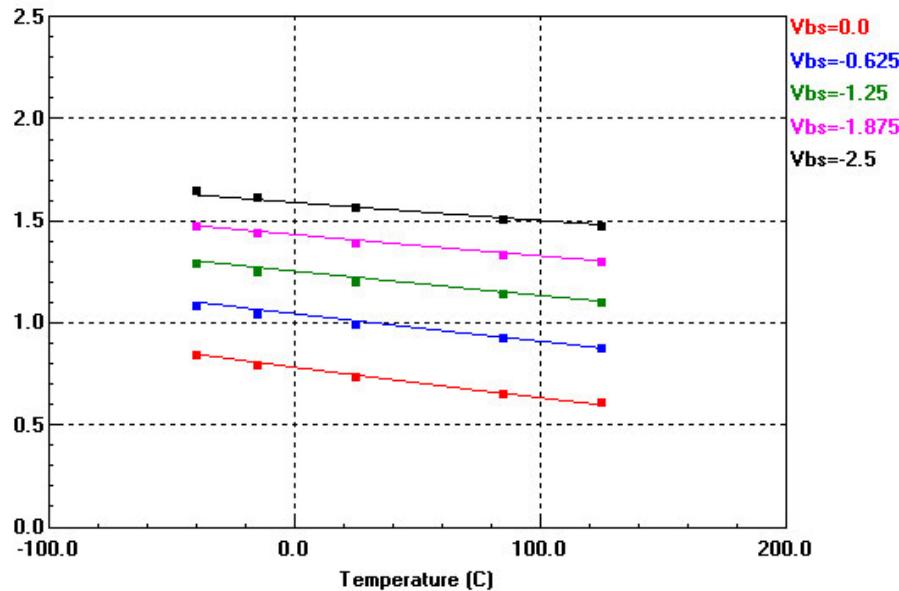


Fig.A47 V_{th} vs. T measured and simulated plot with various V_{bs} for 5V NMOS 10/10

V_{th} [V] V_{th} vs. T at 10/0.5 by maximum GM for 5V thick oxide NMOS:
Symbols: Measurement; Lines: Simulation

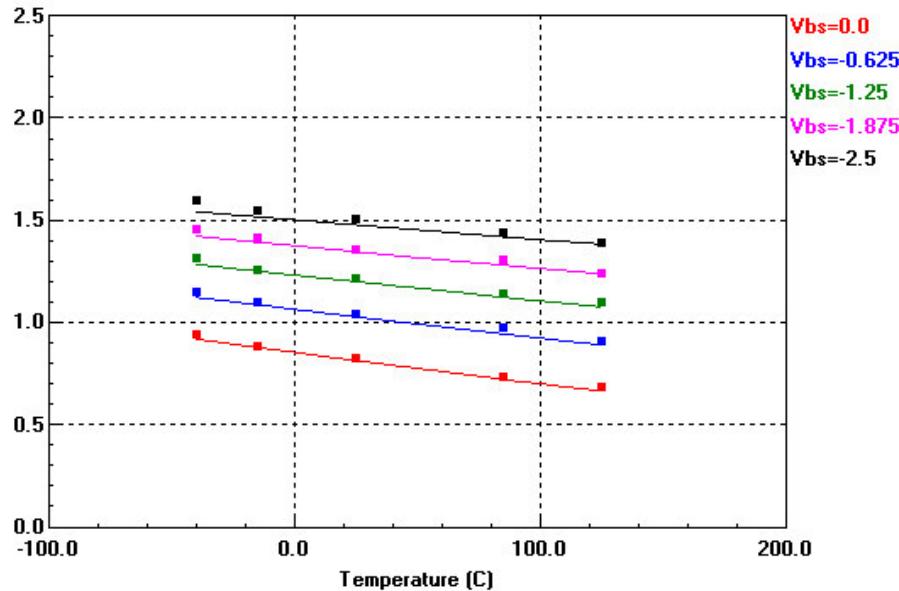


Fig.A48 V_{th} vs. T measured and simulated plot with various V_{bs} for 5V NMOS 10/0.5

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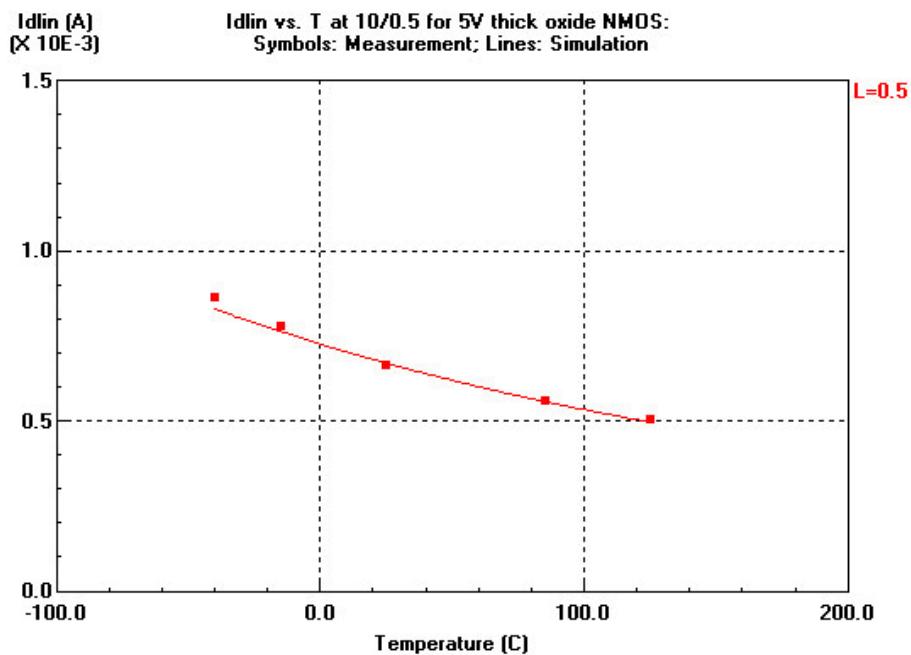


Fig.A49 Idlin vs. T measured and simulated plot with Vbs=0V for 5V NMOS 10/0.5

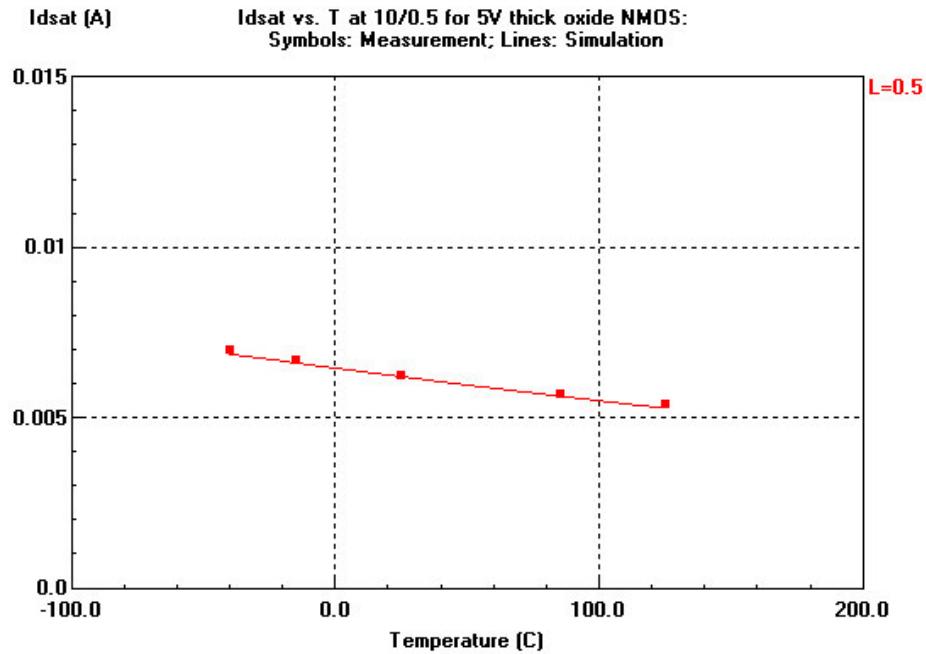


Fig.A50 Idsat vs. T measured and simulated plot with Vbs=0V for 5V NMOS 10/0.5

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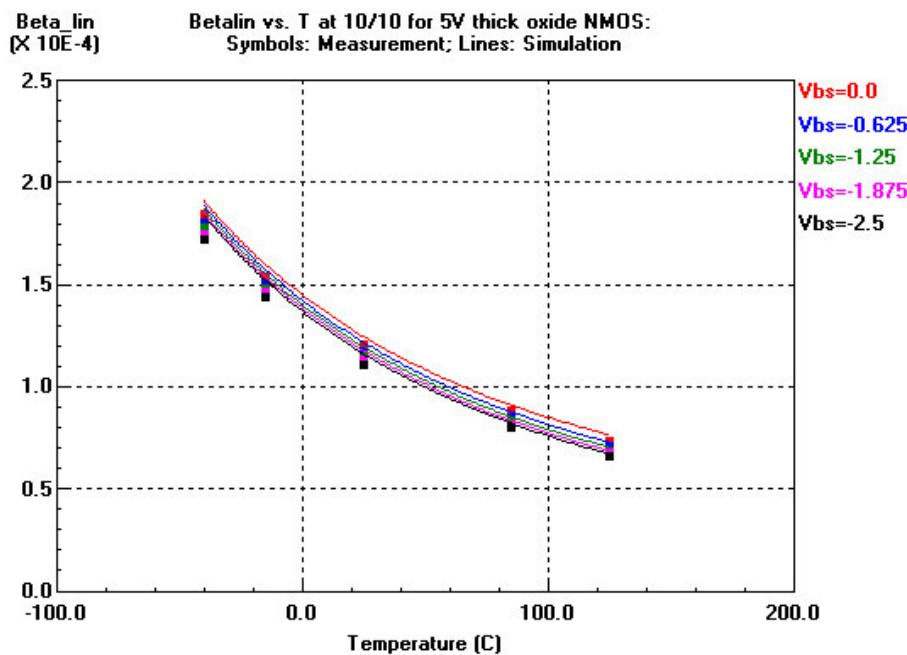


Fig.A51 Betalin vs. T measured and simulated plot for 5V NMOS 10/10

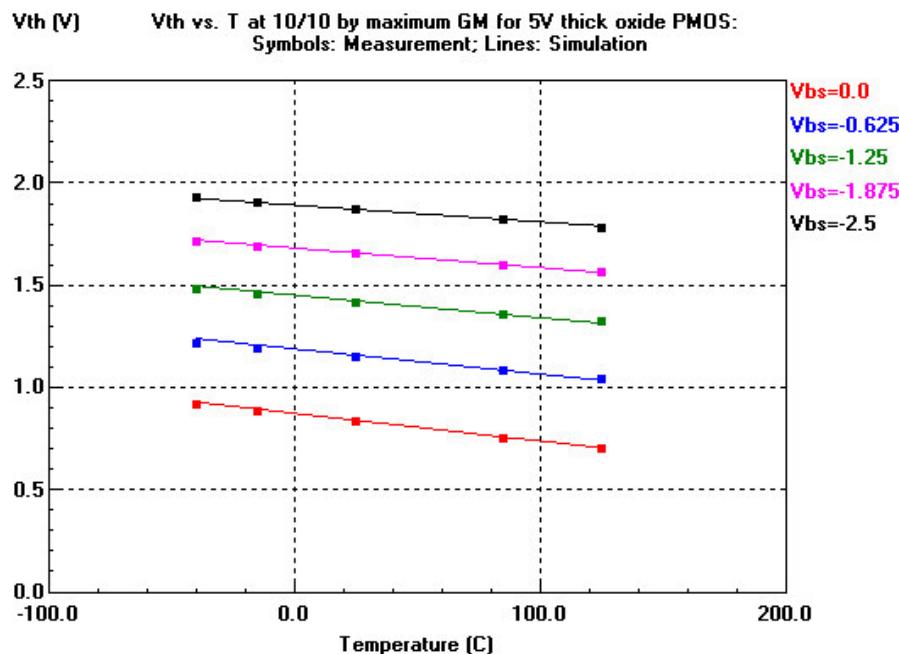


Fig.A52 Vth vs. T measured and simulated plot with various Vbs for 5V PMOS 10/10

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V_{th} (V) V_{th} vs. T at 10/0.5 by maximum GM for 5V thick oxide PMOS:
Symbols: Measurement; Lines: Simulation

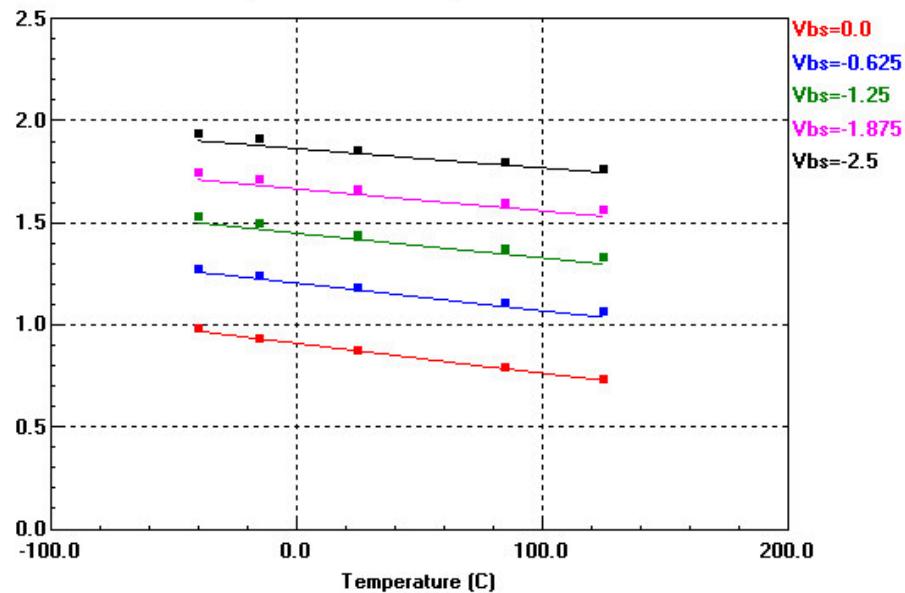


Fig.A53 V_{th} vs. T measured and simulated plot with various V_{bs} for 5V PMOS 10/0.5

I_{dlin} (A)
(X 10E-4) I_{dlin} vs. T at 10/0.5 for 5V thick oxide PMOS:
Symbols: Measurement; Lines: Simulation

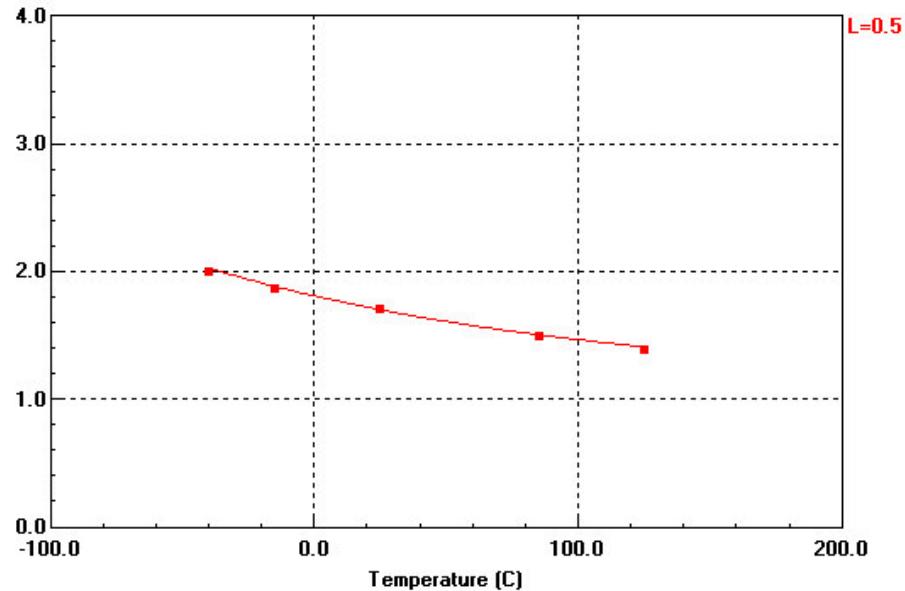


Fig.A54 I_{dlin} vs. T measured and simulated plot with V_{bs}=0V for 5V PMOS 10/0.5

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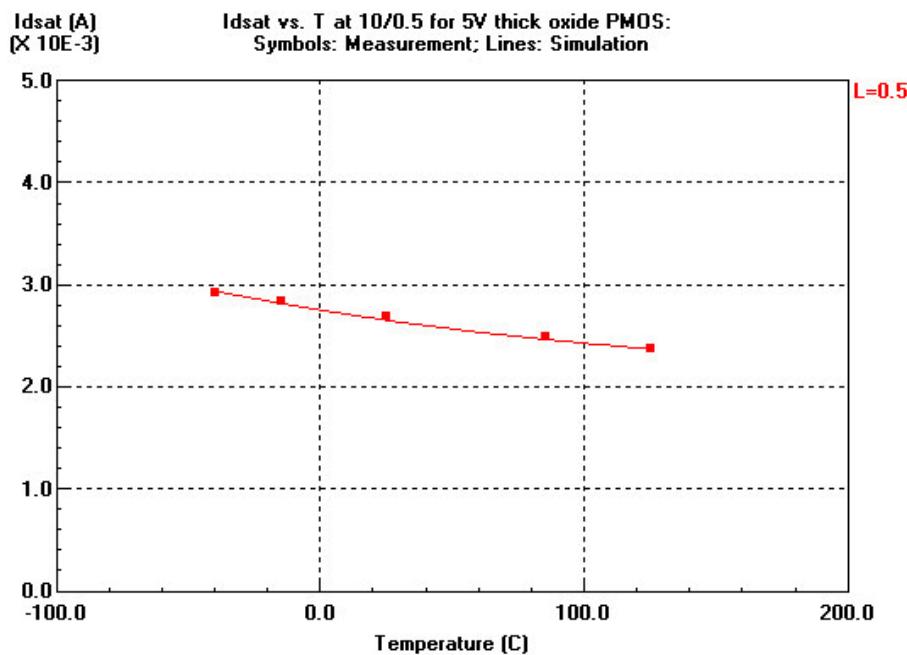


Fig.A55 Idsat vs. T measured and simulated plot with Vbs=0V for 5V PMOS 10/0.5

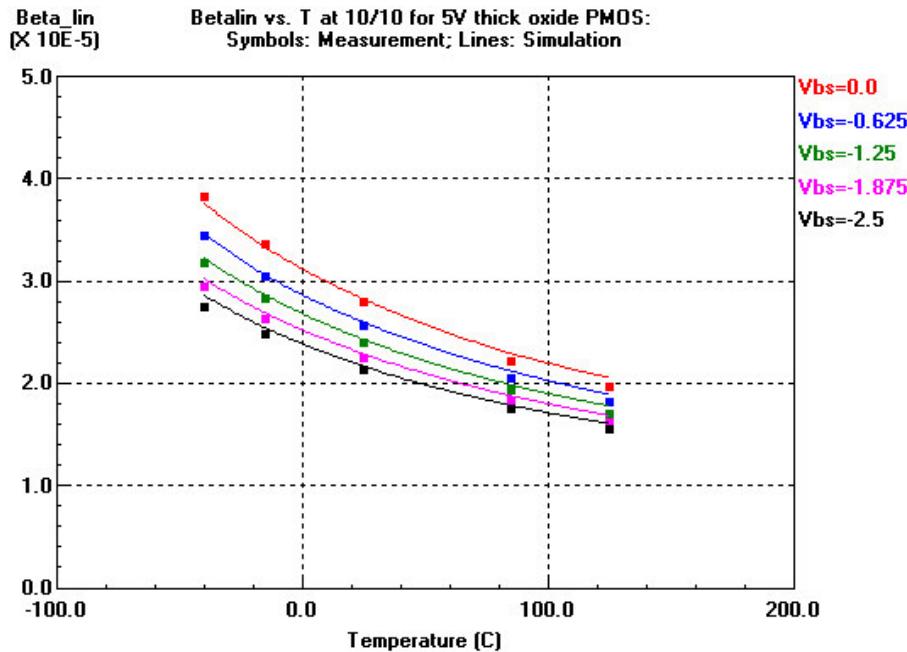


Fig.A56 Betalin vs. T measured and simulated plot for 5V PMOS 10/10

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1.8V inverter R.O. F.O.1 Gate Delay v.s. VDD
@ L=0.18um @ 25C

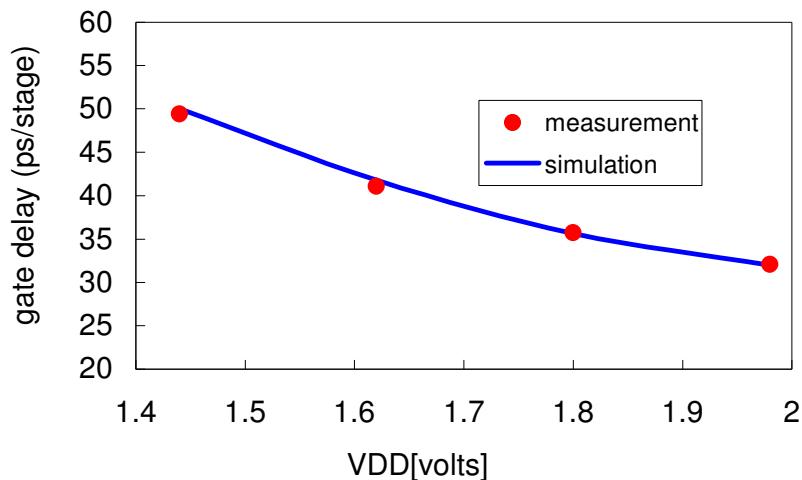


Fig.A57 Gate delay time versus Vdd for 1.8V inverter ring oscillator,
where $W_n/L_n=4/0.18$, $W_p/L_p=6/0.18$ (fan out =1)

1.8V inverter R.O. F.O.3 Gate Delay v.s. VDD
@ L=0.18um @ 25C

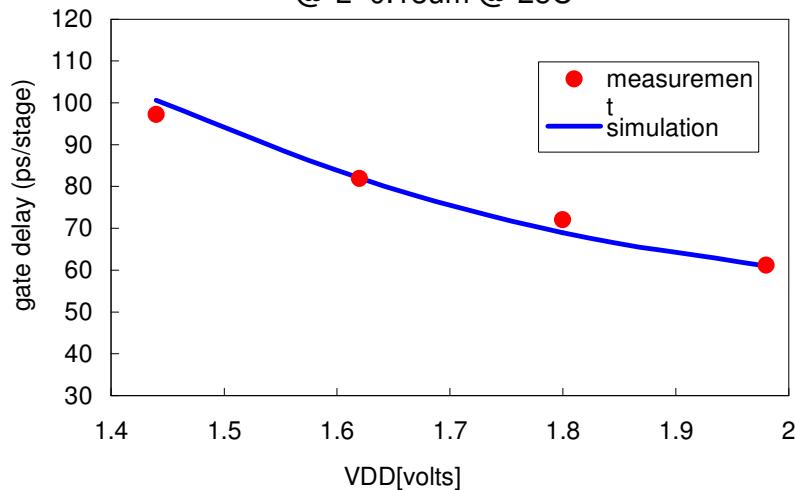


Fig.A58 Gate delay time versus Vdd for 1.8V inverter ring oscillator,
where $W_n/L_n=4/0.18$, $W_p/L_p=6/0.18$ (fan out =3)

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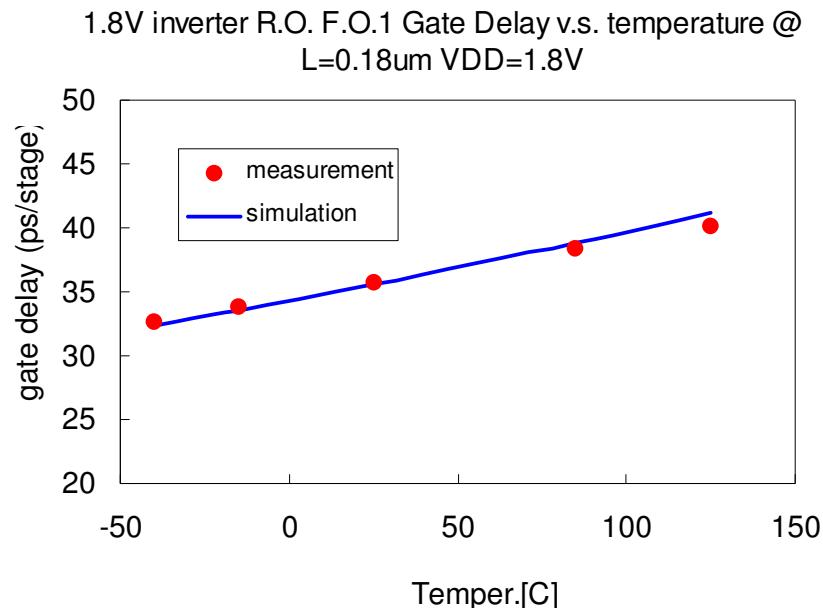


Fig.A59 Gate delay time versus temperature for 1.8V inverter ring oscillator,
where $W_n/L_n=4/0.18$, $W_p/L_p=6/0.18$ (fan out =1)

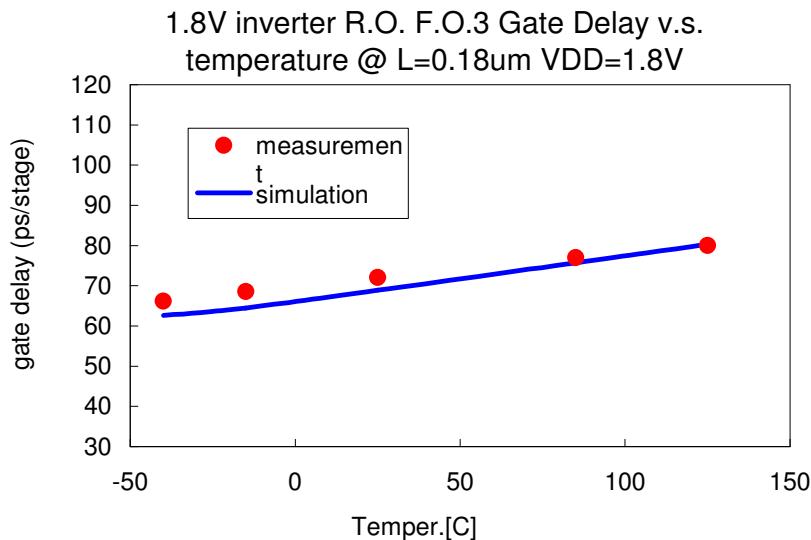


Fig.A60 Gate delay time versus temperature for 1.8V inverter ring oscillator,
where $W_n/L_n=4/0.18$, $W_p/L_p=6/0.18$ (fan out =3)

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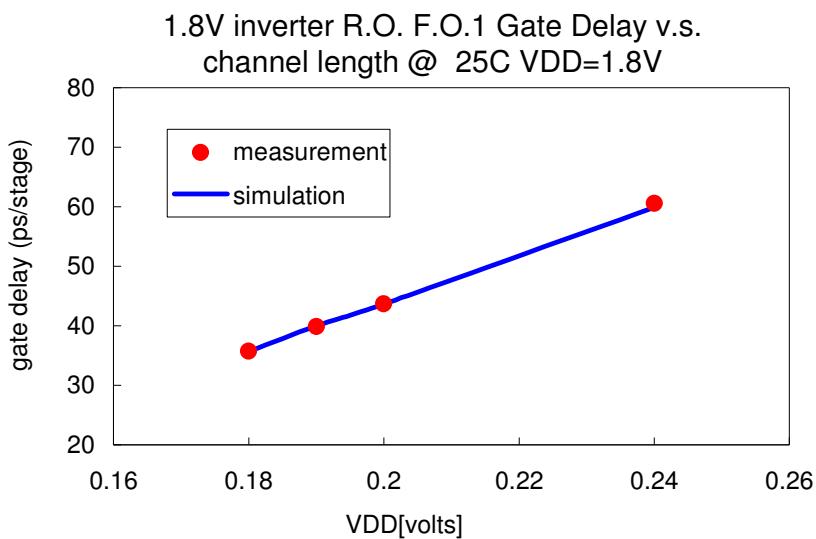


Fig.A61 Gate delay time versus channel length for 1.8V inverter ring oscillator,
where $W_n/W_p = 4/6$ (fan out =1)

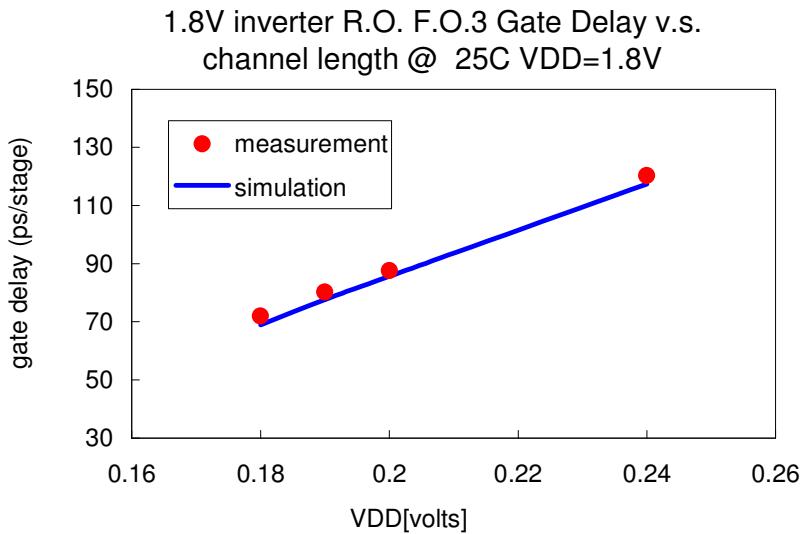


Fig.A62 Gate delay time versus channel length for 1.8V inverter ring oscillator,
where $W_n/W_p = 4/6$ (fan out =3)

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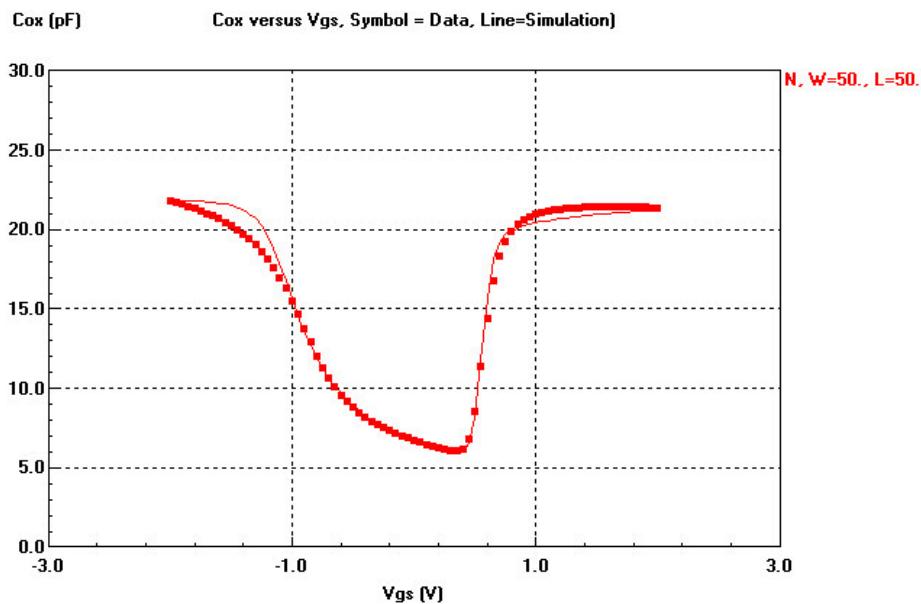


Fig.A63 Fitting results of Cox for 1.8V NMOS

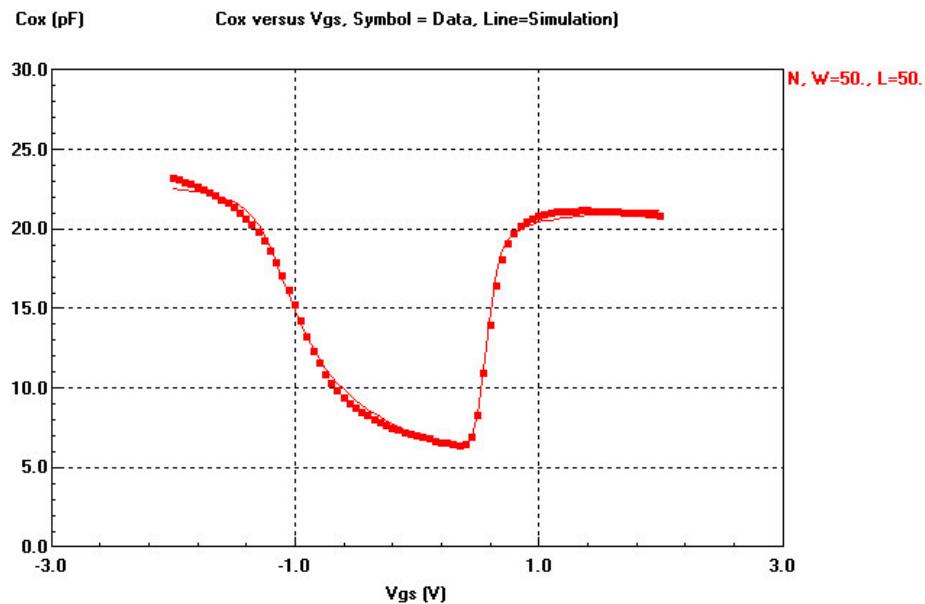


Fig.A64 Fitting results of Cox for 1.8V PMOS

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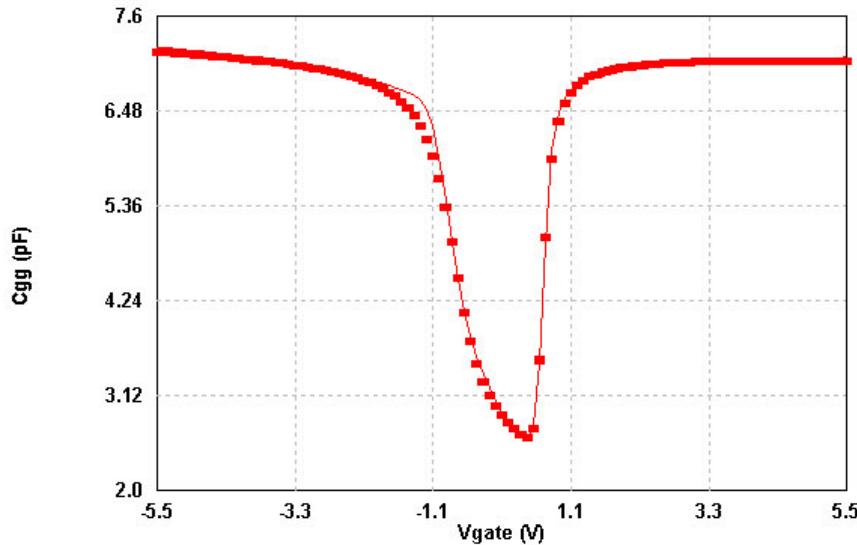
BSIMPro
NCOX50.CV W/L=50.00/50.00 T=25C

Fig.A65 Fitting results of Cox for 5V NMOS

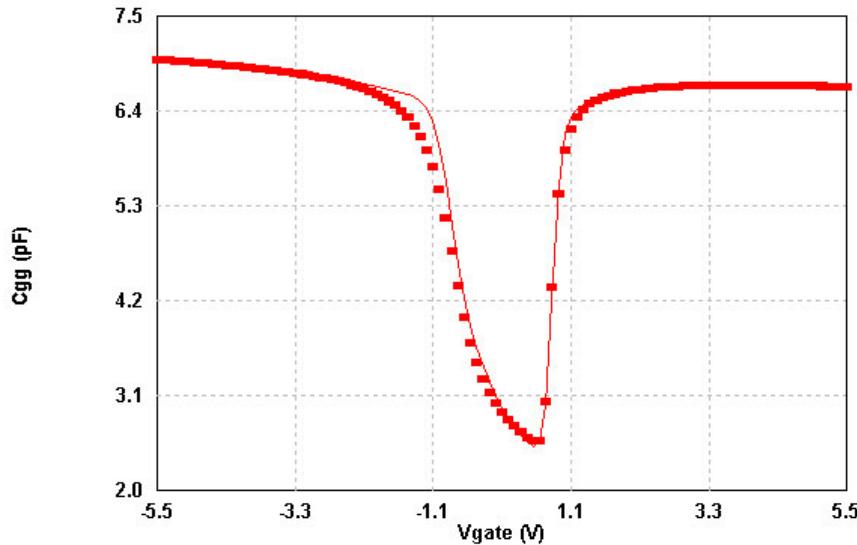
BSIMPro
PCOX50.CV W/L=50.00/50.00 T=25C

Fig.A66 Fitting results of Cox for 5V PMOS

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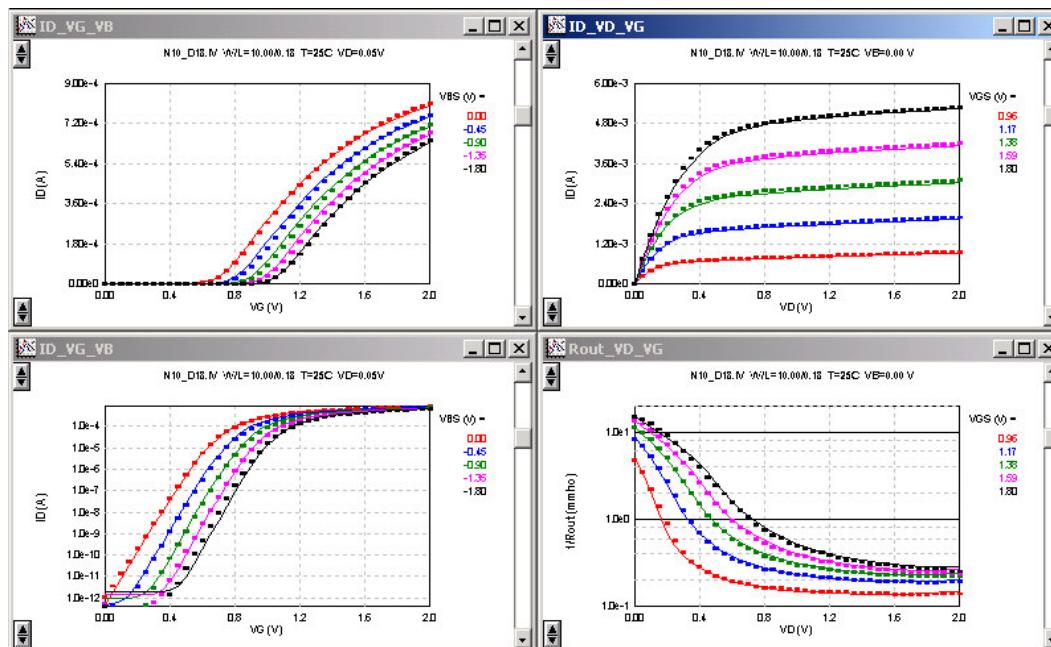


Fig.A67 Fitting ID_VD&VG, subthreshold and gds of 1.8V NMOS W/L=10/0.18 at temp=25C

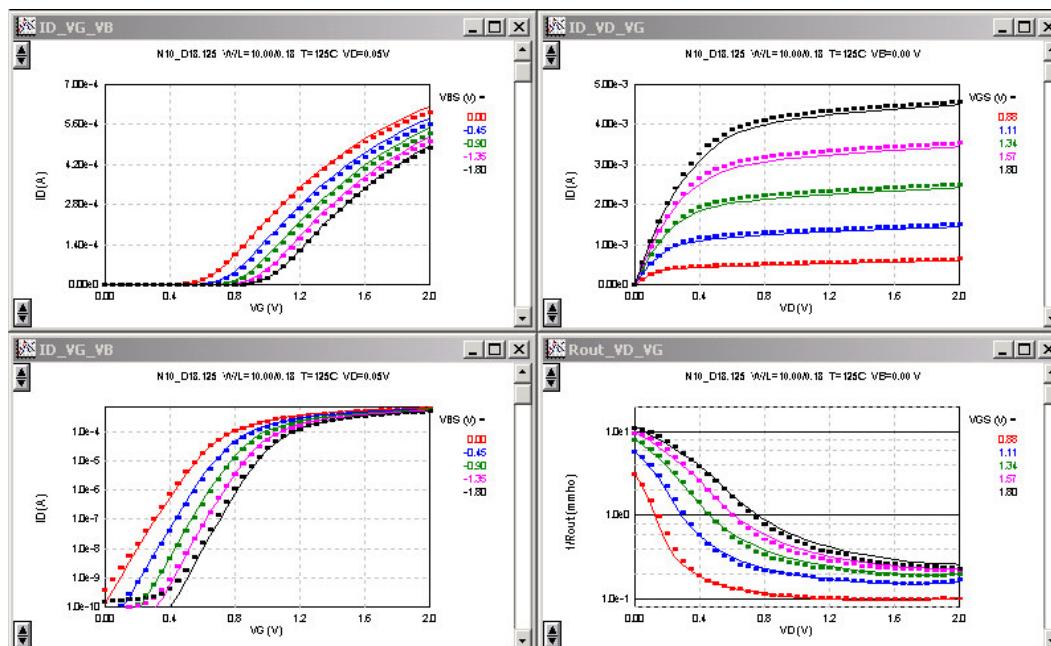


Fig.A68 Fitting ID_VD&VG, subthreshold and gds of 1.8V NMOS W/L=10/0.18 at temp=125C

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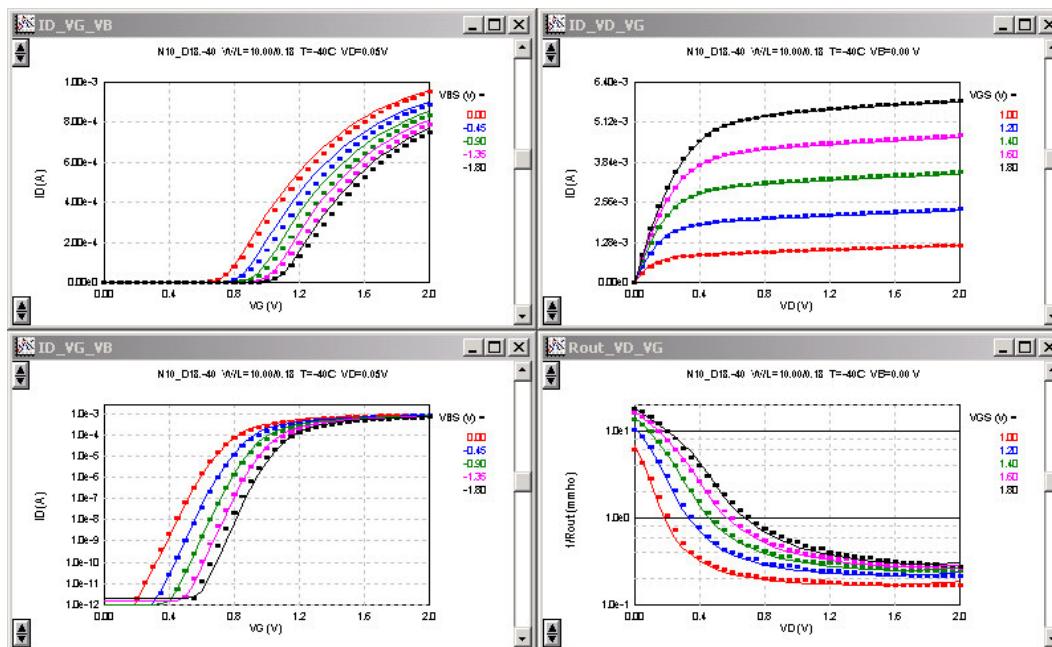


Fig.A69 Fitting ID_VD&VG, subthreshold and gds of 1.8V NMOS W/L=10/0.18 at temp=-40C

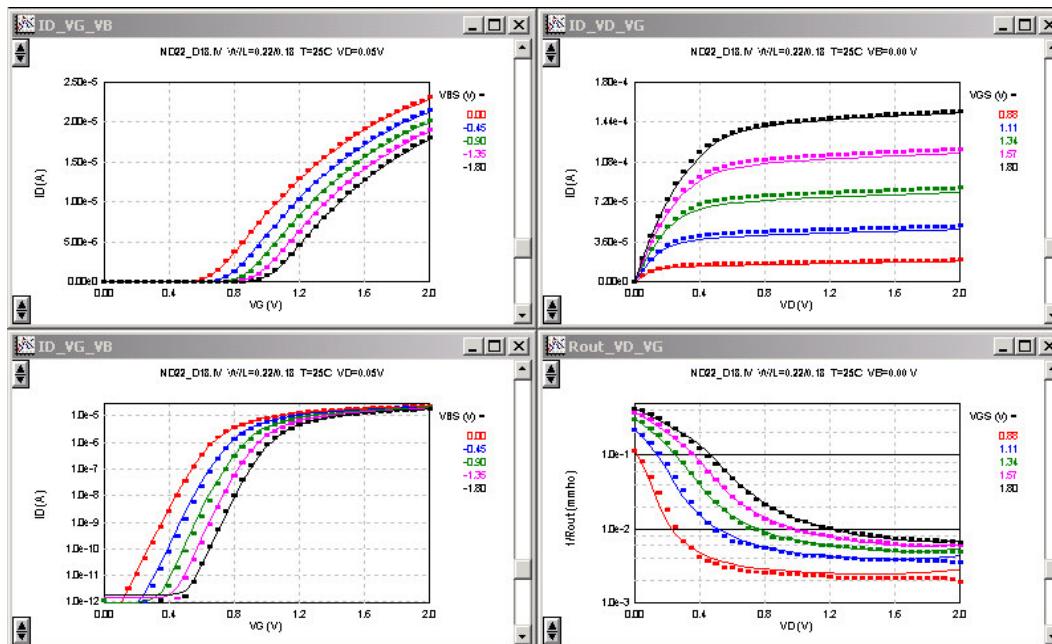


Fig.A70 Fitting ID_VD&VG, subthreshold and gds of 1.8V NMOS W/L=0.22/0.18 at temp=25C

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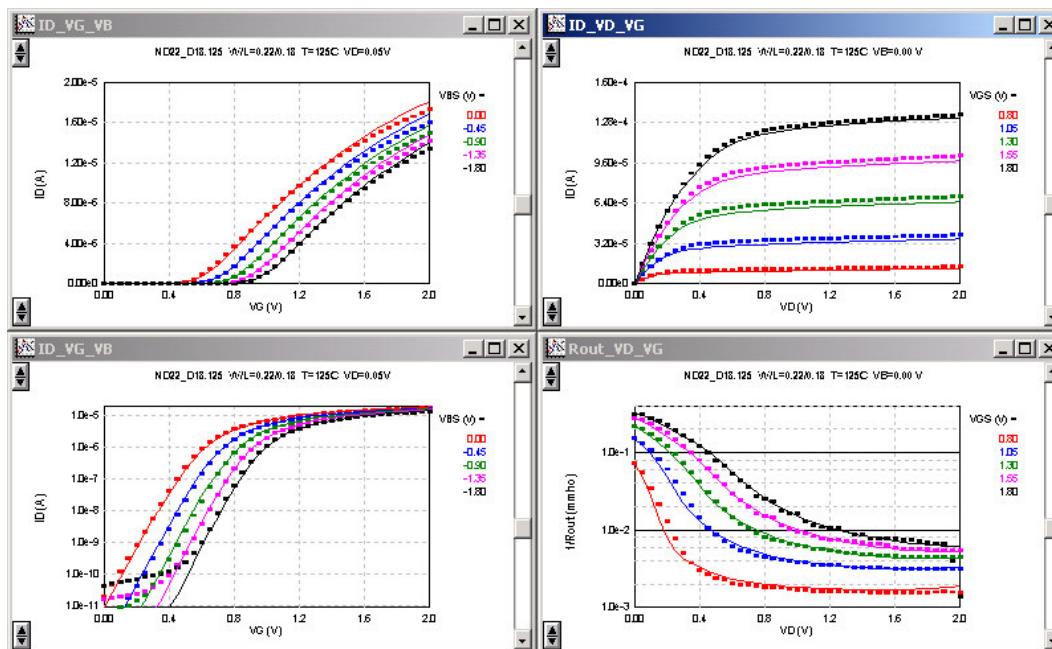


Fig.A71 Fitting ID_VD&VG, subthreshold and gds of 1.8V NMOS W/L=0.22/0.18 at temp=125C

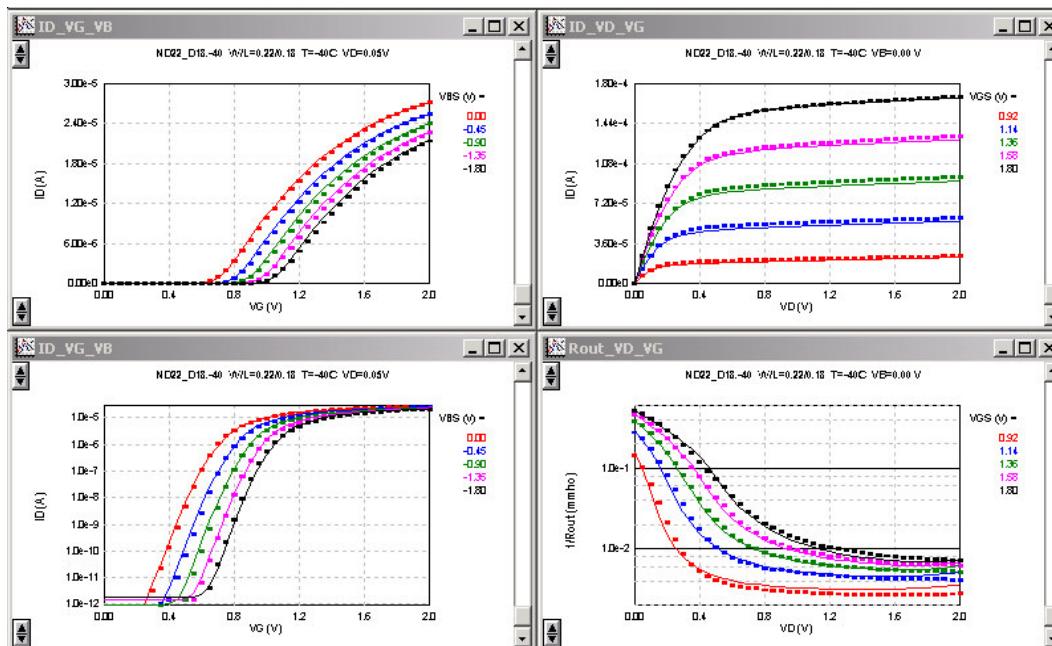


Fig.A72 Fitting ID_VD&VG, subthreshold and gds of 1.8V NMOS W/L=0.22/0.18 at temp=-40C

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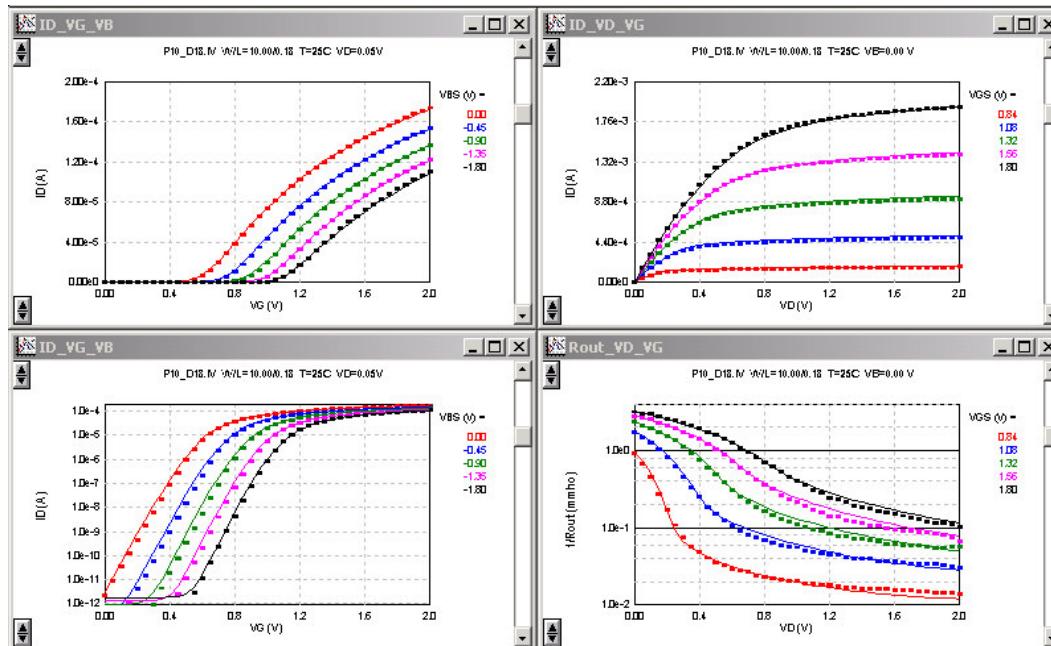


Fig.A73 Fitting ID_VD&VG, subthreshold and gds of 1.8V PMOS W/L=10/0.18 at temp=25C

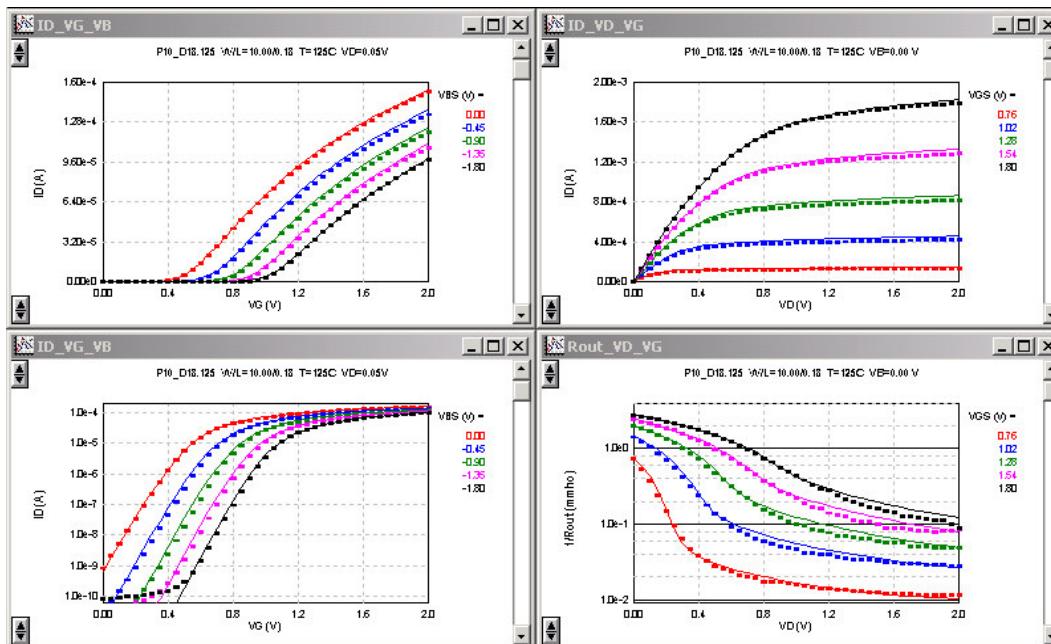


Fig.A74 Fitting ID_VD&VG, subthreshold and gds of 1.8V PMOS W/L=10/0.18 at temp=125C

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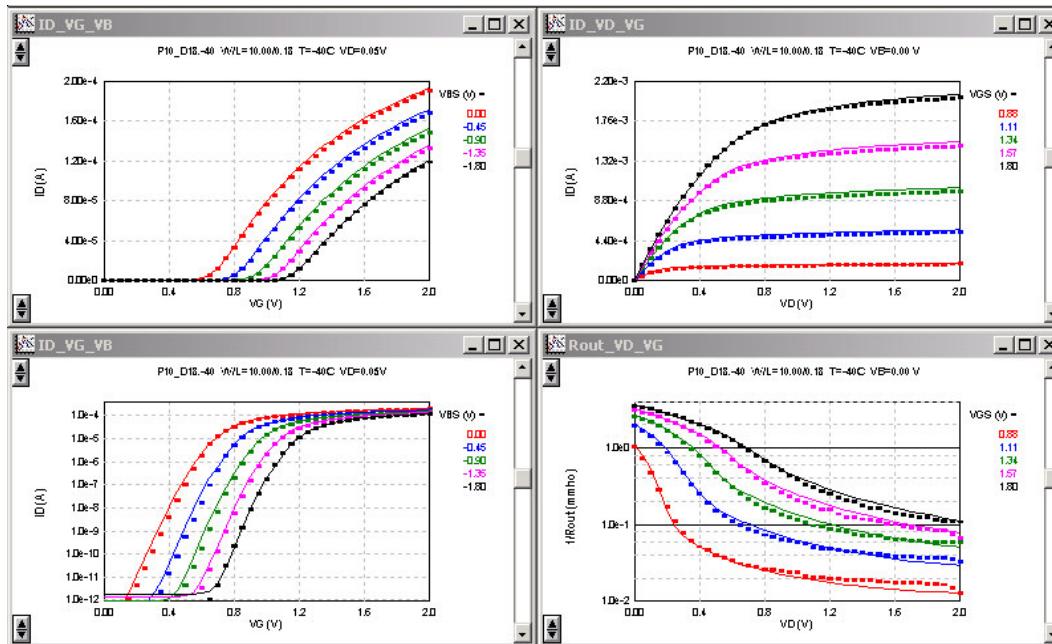


Fig.A75 Fitting ID_VD&VG, subthreshold and gds of 1.8V PMOS W/L=10/0.18 at temp=-40C

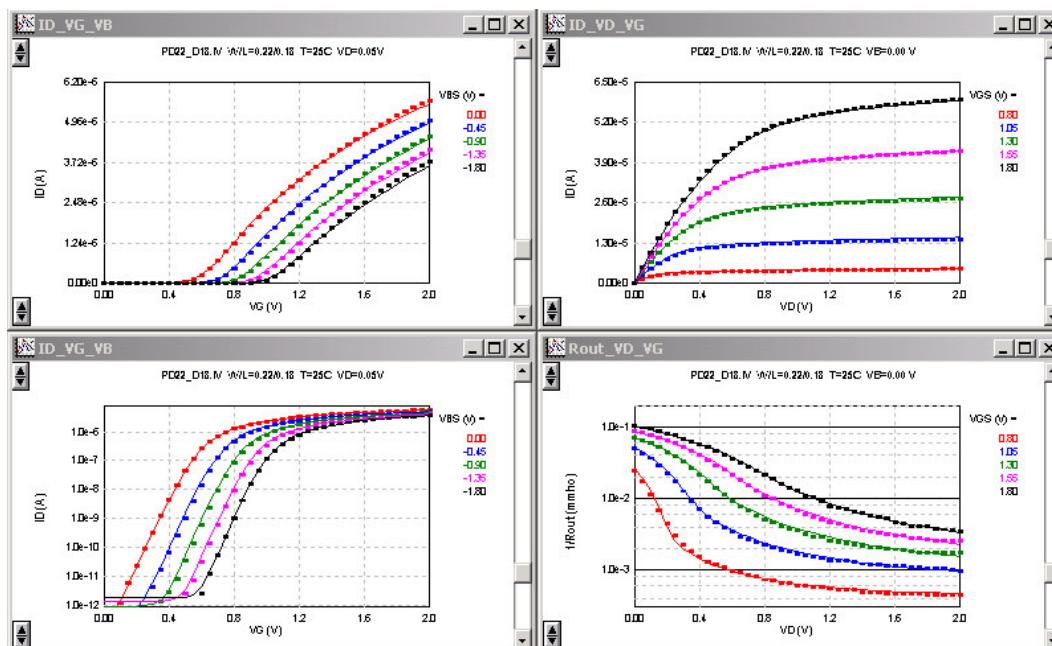


Fig.A76 Fitting ID_VD&VG, subthreshold and gds of 1.8V PMOS W/L=0.22/0.18 at temp=25C

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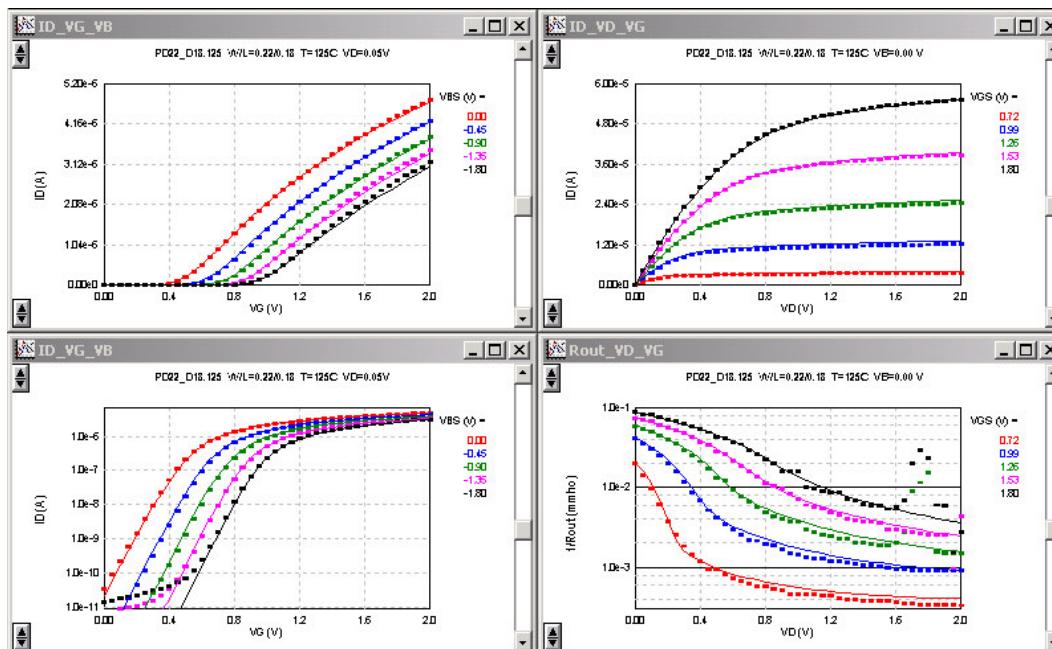


Fig.A77 Fitting ID_VD&VG, subthreshold and gds of 1.8V PMOS W/L=0.22/0.18 at temp=125C

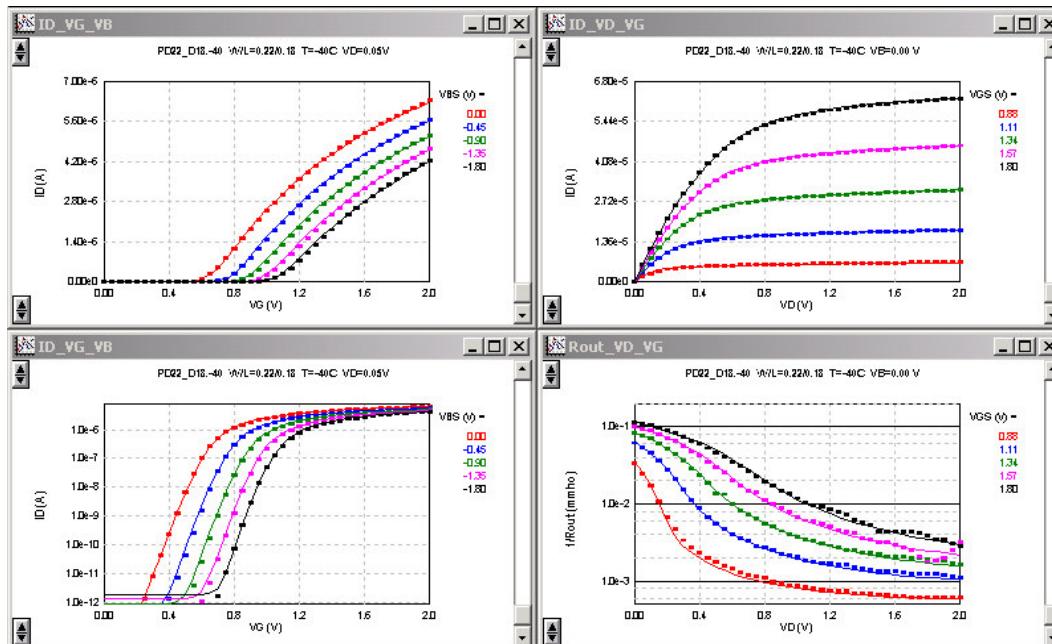


Fig.A78 Fitting ID_VD&VG, subthreshold and gds of 1.8V PMOS W/L=0.22/0.18 at temp=-40C

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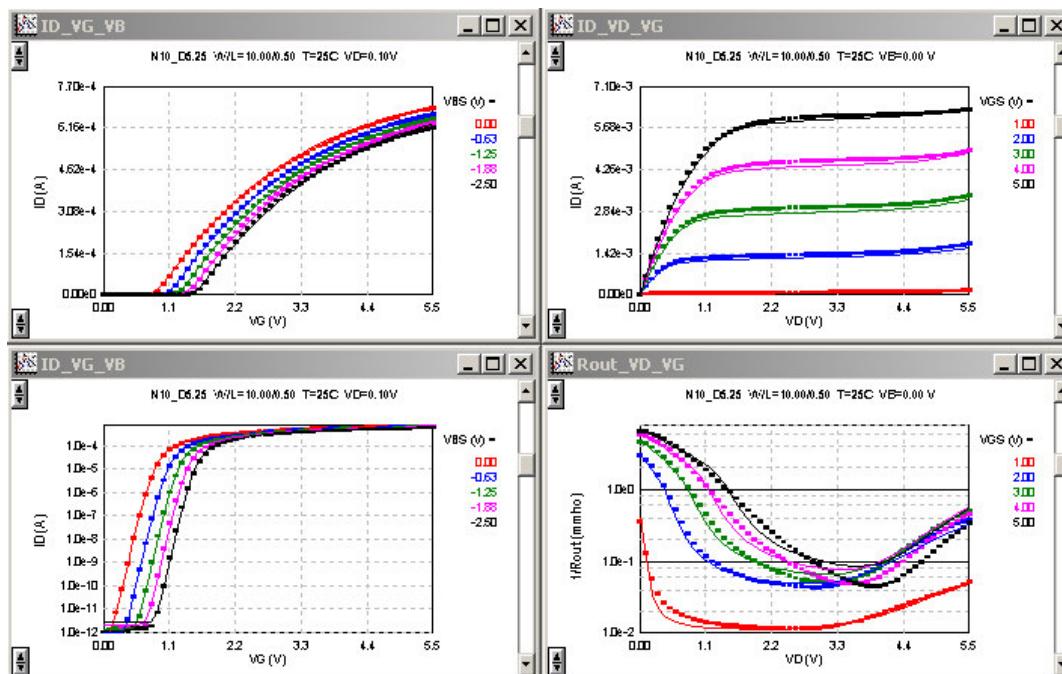


Fig.A79 Fitting ID_VD&VG, subthreshold and gds of 5V NMOS W/L=10/0.5 at temp=25C

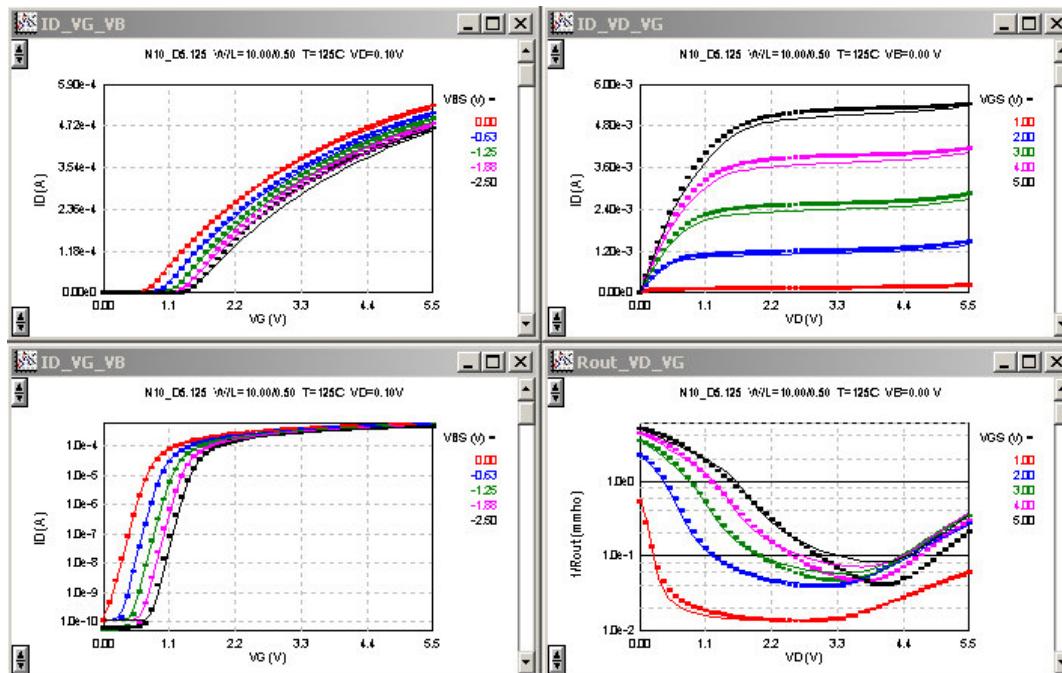


Fig.A80 Fitting ID_VD&VG, subthreshold and gds of 5V NMOS W/L=10/0.5 at temp=125C

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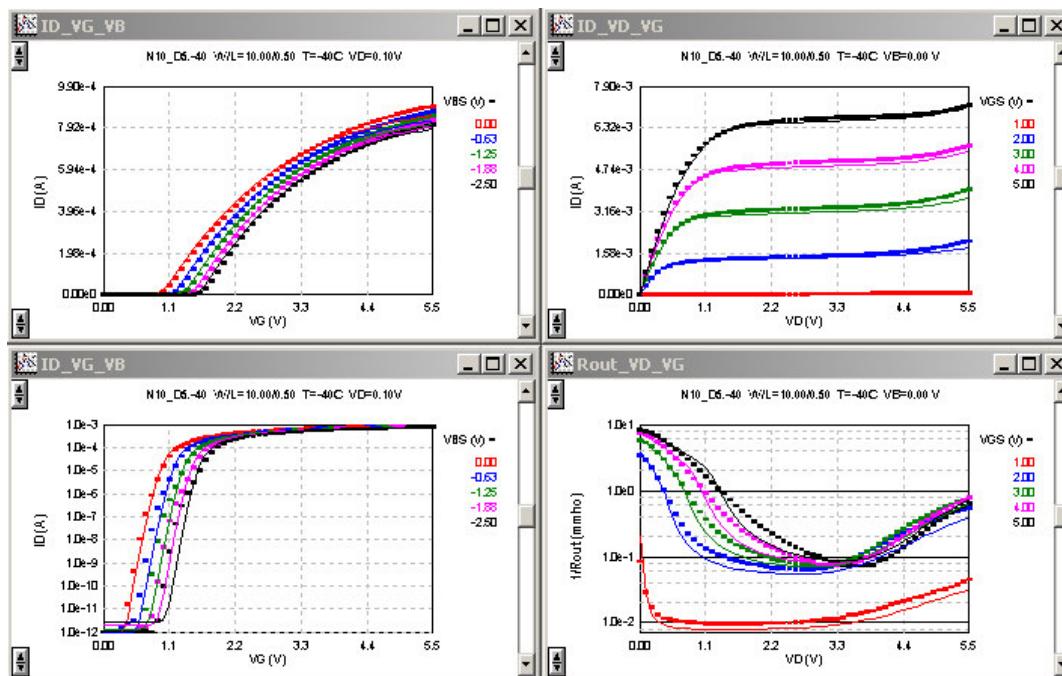


Fig.A81 Fitting ID_VD&VG, subthreshold and gds of 5V NMOS W/L=10/0.5 at temp=-40C

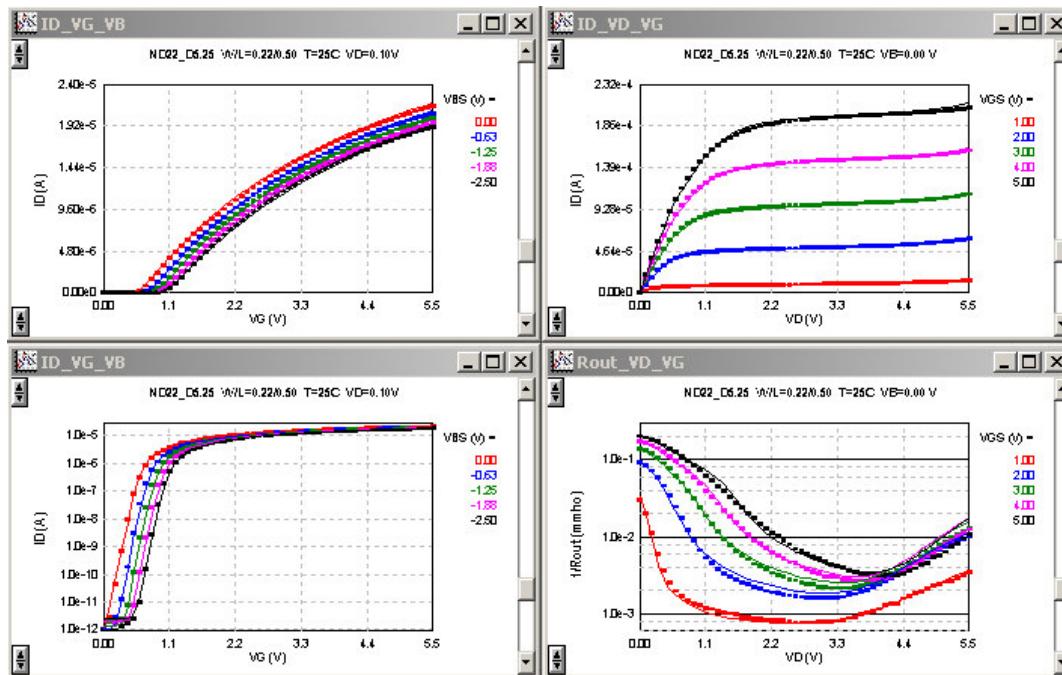


Fig.A82 Fitting ID_VD&VG, subthreshold and gds of 5V NMOS W/L=0.22/0.5 at temp=25C

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TD-LO18-SP-2003		0.18um Logic Low Leakage 1P6M (1P5M, 1P4M) Salicide 1.8V/5.0V SPICE Model (Version 1.3)	4R	Rev.: 1.3	42/45

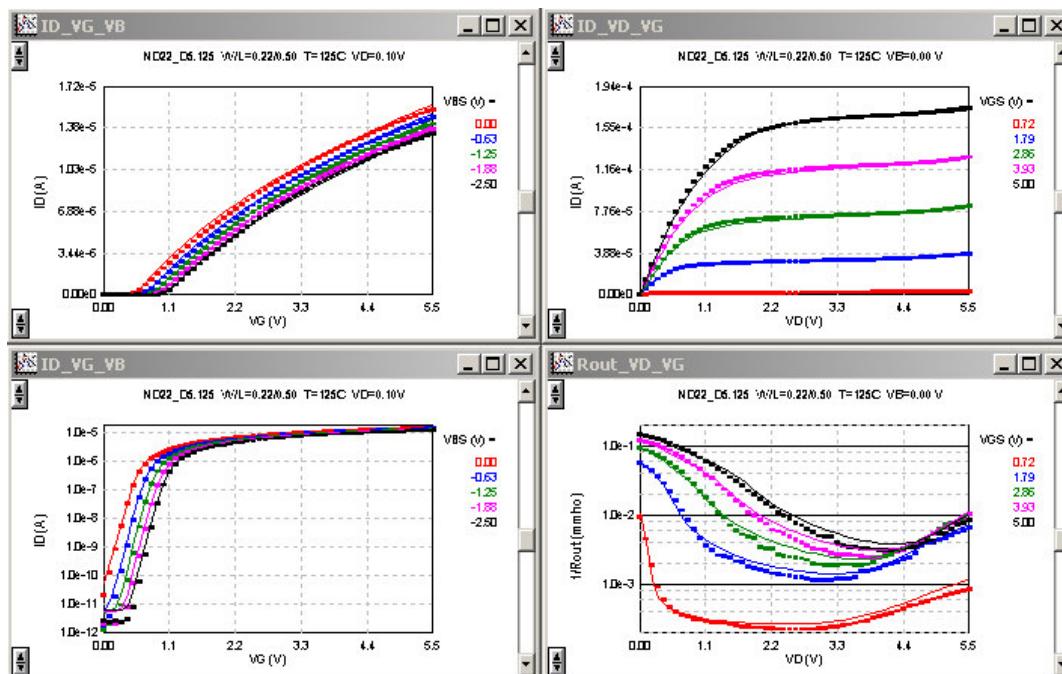


Fig.A83 Fitting ID_VD&VG, subthreshold and gds of 5V NMOS W/L=0.22/0.5 at temp=125C

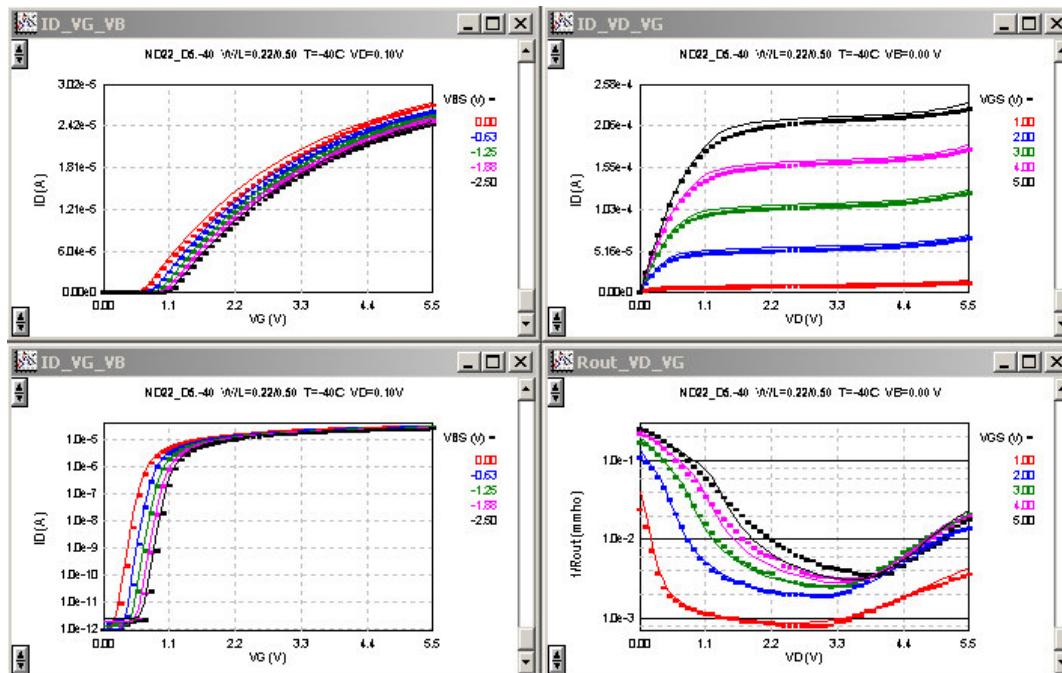


Fig.A84 Fitting ID_VD&VG, subthreshold and gds of 5V NMOS W/L=0.22/0.5 at temp=-40C

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Doc. No.:	Doc. Title:	Doc. Rev:	Tech Dev Rev.:	Page No.:
TD-LO18-SP-2003	0.18um Logic Low Leakage 1P6M (1P5M, 1P4M) Salicide 1.8V/5.0V SPICE Model (Version 1.3)	4R	1.3	43/45

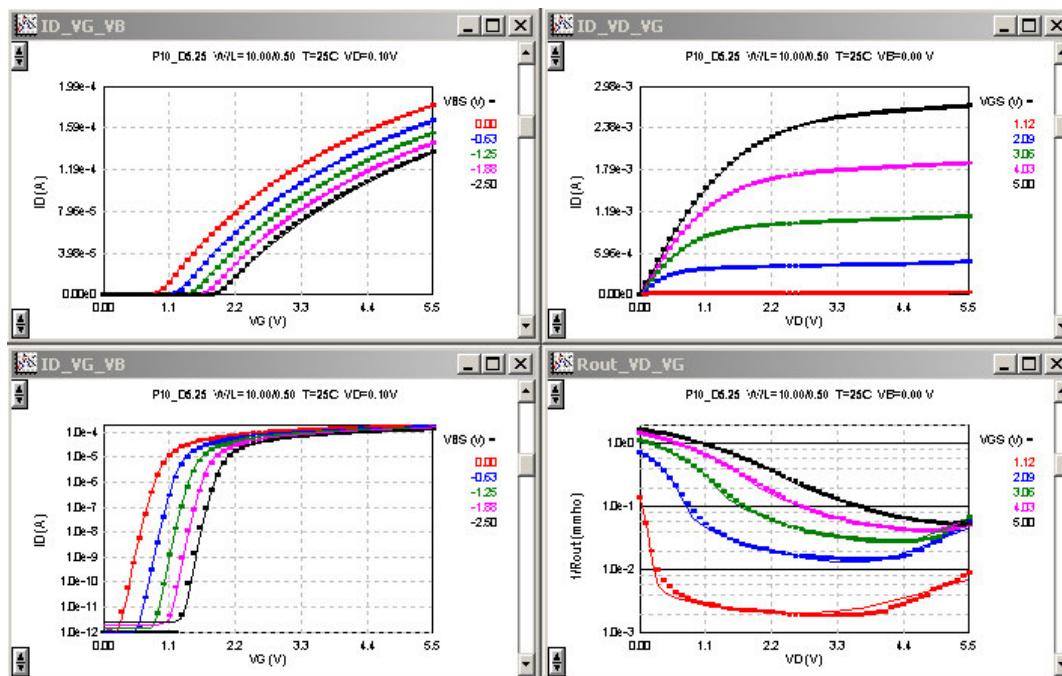


Fig.A85 Fitting ID_VD&VG, subthreshold and gds of 5V PMOS W/L=10/0.5 at temp=25C

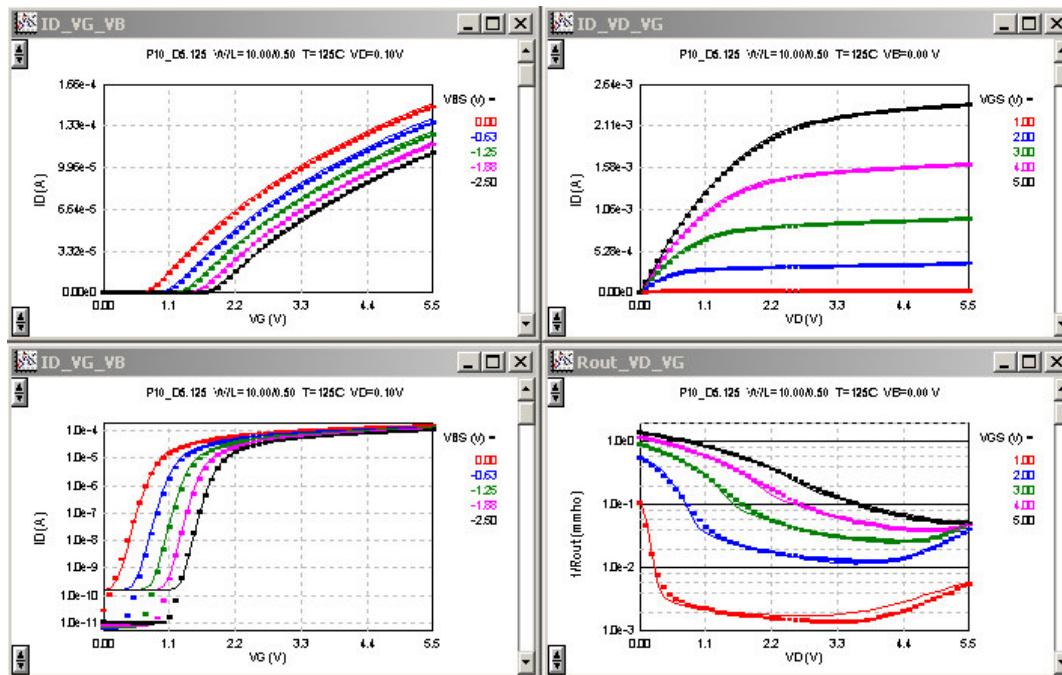


Fig.A86 Fitting ID_VD&VG, subthreshold and gds of 5V PMOS W/L=10/0.5 at temp=125C

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Doc. No.:	Doc. Title:	Doc. Rev:	Tech Dev Rev.:	Page No.:
TD-LO18-SP-2003	0.18um Logic Low Leakage 1P6M (1P5M, 1P4M) Salicide 1.8V/5.0V SPICE Model (Version 1.3)	4R	1.3	44/45

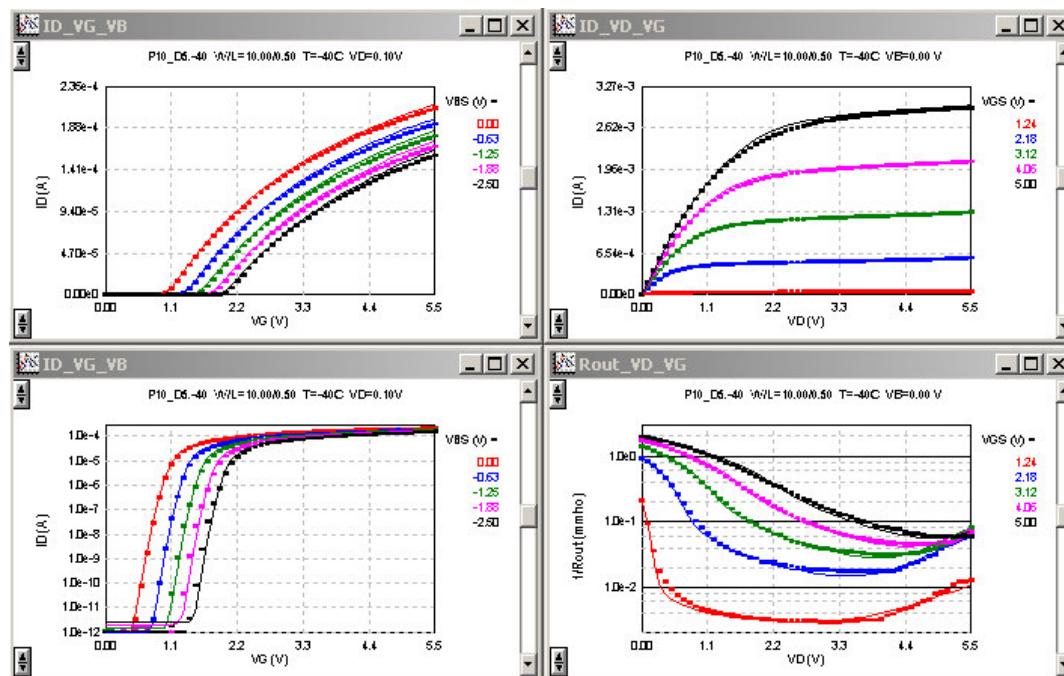


Fig.A87 Fitting ID_VD&VG, subthreshold and gds of 5V PMOS W/L=10/0.5 at temp=-40C

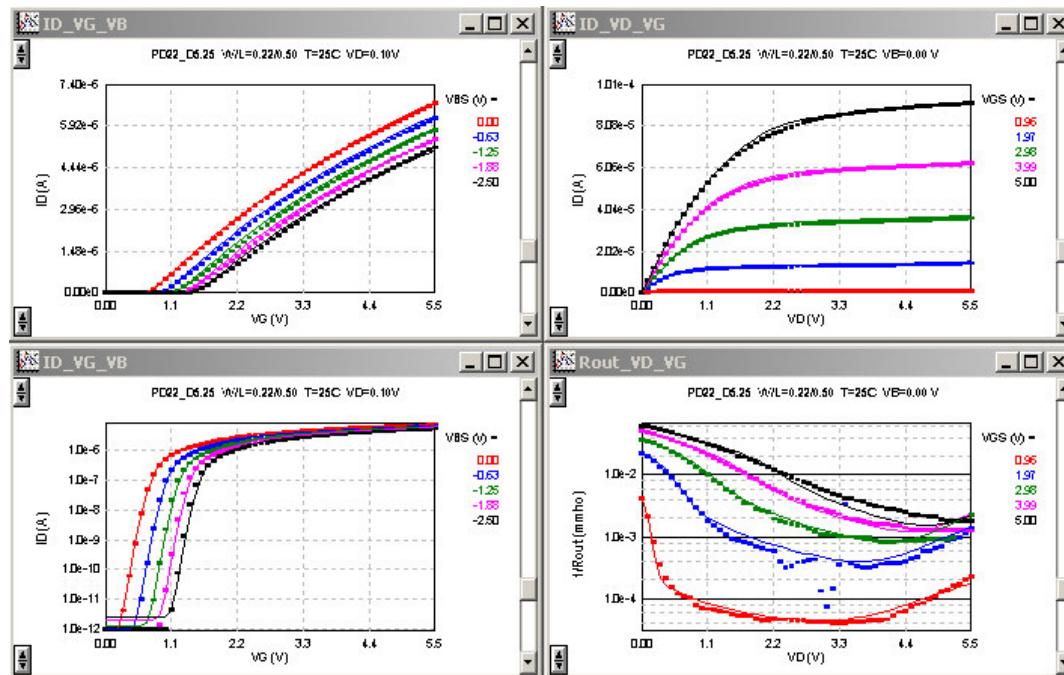


Fig.A88 Fitting ID_VD&VG, subthreshold and gds of 5V PMOS W/L=0.22/0.5 at temp=25C

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Doc. No.:	Doc. Title:	Doc. Rev:	Tech Dev Rev.:	Page No.:
TD-LO18-SP-2003	0.18um Logic Low Leakage 1P6M (1P5M, 1P4M) Salicide 1.8V/5.0V SPICE Model (Version 1.3)	4R	1.3	45/45

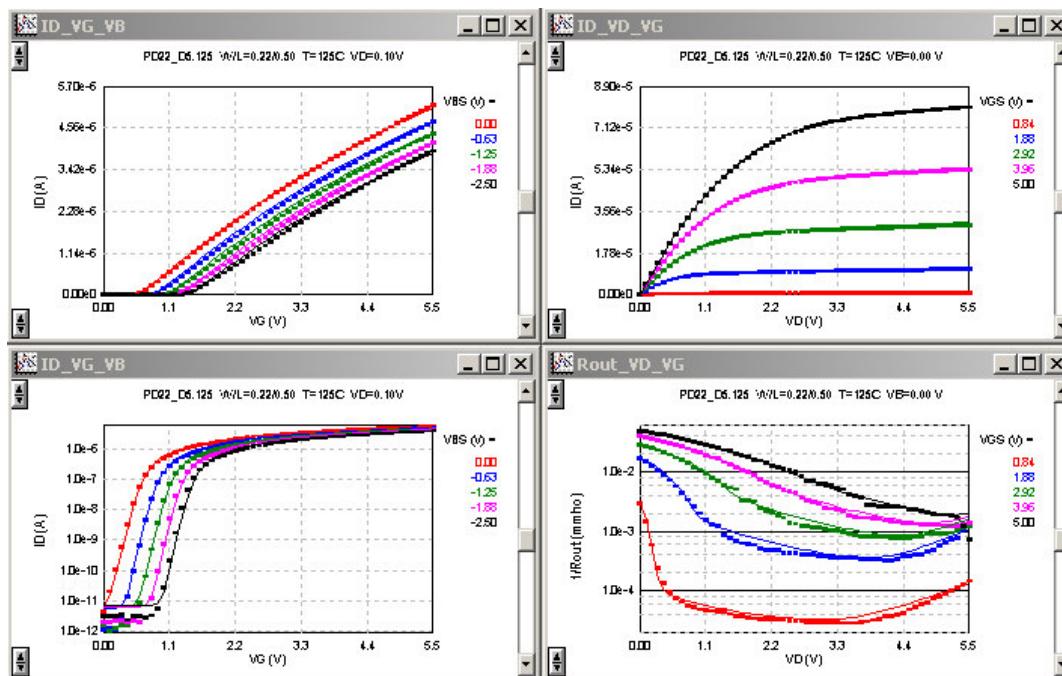


Fig.A89 Fitting ID_VD&VG, subthreshold and gds of 5V PMOS W/L=0.22/0.5 at temp=125C

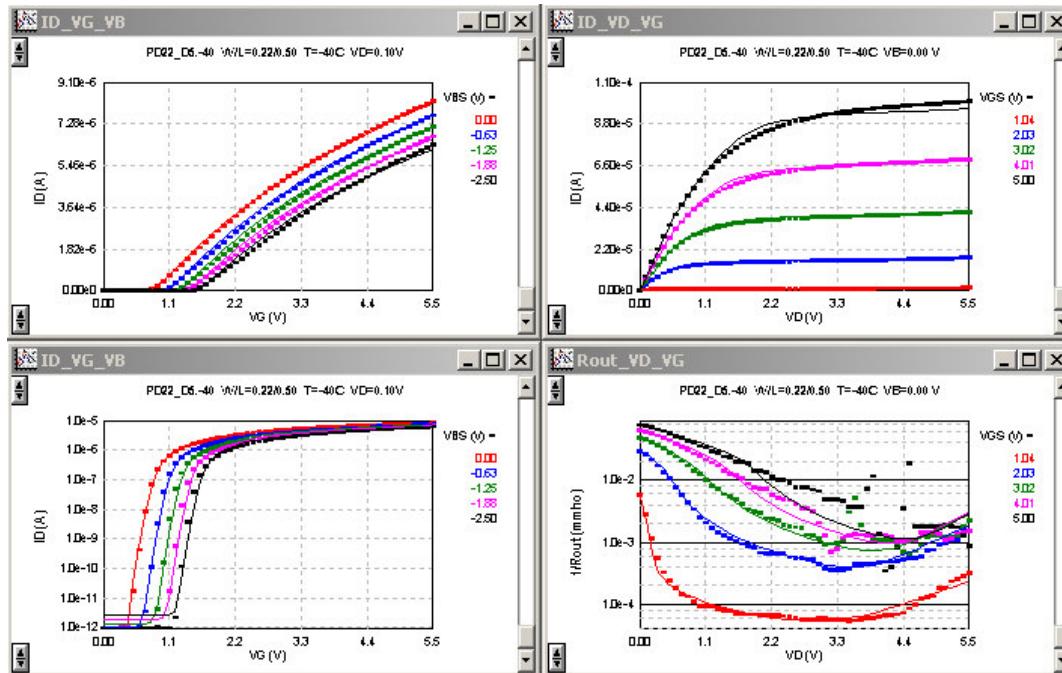


Fig.A90 Fitting ID_VD&VG, subthreshold and gds of 5V PMOS W/L=0.22/0.5 at temp=-40

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