Document Level: (For Engineering & Quality Document/工程暨品质文件专用)

☐ Level 1 - Manual ☑ Level 2 – Procedure/SPEC/Report ☐ Level 3 - Operation Instruction

Security Level:

☐ Security 1 - SMIC Confidential ☑ Security 2 - SMIC Restricted ☐ Security 3 - SMIC Internal

Document Change History

Doc. Rev.	Tech Dev. Rev.	Effective Date	Author	Change Description
0T	0.1	2004-04-07	Yahoo_Lee	Initiate
1R	1.0	2005-2-4	Jully He	All models (MOS, Diode, Resistor, etc) parameters are re-extracted due to process change. All the attachments are updated. In main document, detail information as follows: 1. Update MOS corner model in section 7.2.2. 2. Update ring oscillator verification table in section 7.2.3. 3. Add 1/f noise model in section 7.2.4. 4. Add non-standard (with LDD) SAB resistor model in section 7.6. 5. Add MIM capacitance model in section 7.7 6. Update MOS comparison table in section 7.8.2 and 7.8.3. 7. Update ring simulation table in 7.8.4.
2R	1.1	2005-8-5	Becky Geng	Updated RC_N+, RC_P+, RC_N+Poly, RC_P+Poly and RC_Via PCM SPEC in document file Resistance Table (section 7.6).
3R	1.2	2006-03-14	Judy Zhao	1. Revised resistor NPOSAB, NPOSAB_NSTD, PPOSAB, PPOSAB_NSTD sub-circuit model in "l018ll_io50_v1p2_res.ckt" and "l018ll_io50_v1p2_res_spe.ckt". 2. Revised "Comparison Between MOSFET Model Simulation and Measurement Results" table in section 7.8.2. 3. Revised BJT model parameter CJE, CJC in "l018ll_io50_v1p2_bjt.mdl" and "l018ll_io50_v1p2_bjt_spe.mdl". 4. Revised BJT corner parameter DCJE, DCJC in "l018ll_io50_v1p2.lib" and "l018ll_io50_v1p2_spe.lib" 5. Revised all model card files to version 1.2

4R	1.3	2007-07-31	Ricky Zhu	1. Added eldo format model card files, which include the files of "l018ll_io50_v1p3_eldo.lib", "l018ll_io50_v1p3_eldo.mdl", "l018ll_io50_v1p3_bjt_eldo.mdl", "l018ll_io50_v1p3_res_eldo.mdl", and "l018ll_io50_v1p3_res_eldo.ckt". 2. Added 3T poly resistor model in section of 7.6 and centered the resistor model to match the PCM SPEC in “l018ll_io50_v1p3_res.mdl”, “l018ll_io50_v1p3_res.ckt”,“l018ll_io50_v1p3_res_spe.mdl”, “l018ll_io50_v1p3_res_spe.ckt”, “l018ll_io50_v1p3_res_eldo.mdl” and “l018ll_io50_v1p3_res_eldo.ckt” 3. Revised the corner for the resistor model to match the PCM SPEC in “l018ll_io50_v1p3.lib”, “l018ll_io50_v1p3_spe.lib” and “l018ll_io50_v1p3_eldo.lib”. 4. Revised the sheet resistance table, the valid voltage range and recommand width table, square number 's suggestion for SAB resistance and interface resistor table in section of 7.6. 5. Revised the parameter definition of “temper” to directly expression to avoid the limitation of simulator in the files of “l018ll_io50_v1p3_res.ckt” and “l018ll_io50_v1p3_res_eldo.ckt”. 6. Used the file of res.va to replace res.def. 7. Revised readme files of "l018ll_io50_v1p3_readme.txt", "l018ll_io50_v1p3_spe_readme.txt" and "l018ll_io50_v1p3_eldo_readme.txt". 8. Revised the fitting file of "l018ll_io50_fit_D.doc" and added the 3T resistance's fitting plot of Fig.D10, Fig.D12, Fig.D14, Fig.D16, Fig.D18 and Fig.D20. 9. Revised the section of 8.1 and 8.3. 10. Revised all model card files to version 1.3.

1. Title:

   0.18um Logic Low Leakage 1P6M(1P5M, 1P4M) Salicide 1.8V/5V SPICE model (Version 1.3)

2. Purpose:

   To provide SPICE model for circuit designers who use SMIC 0.18um high voltage salicide process.

3. Scope:

   This document describes the detailed SPICE model parameters for circuit simulation using HSPICE

4. Nomenclature:
   1P4M : Single Poly Quadruple Metal
   1P5M : Single Poly Quintuple Metal
   1P6M : Single Poly Sextuple Metal

5. Reference:
   None

6. Responsibility:

   It is the responsibility of LTD Device division to generate and release SPICE models for internal and external customers.

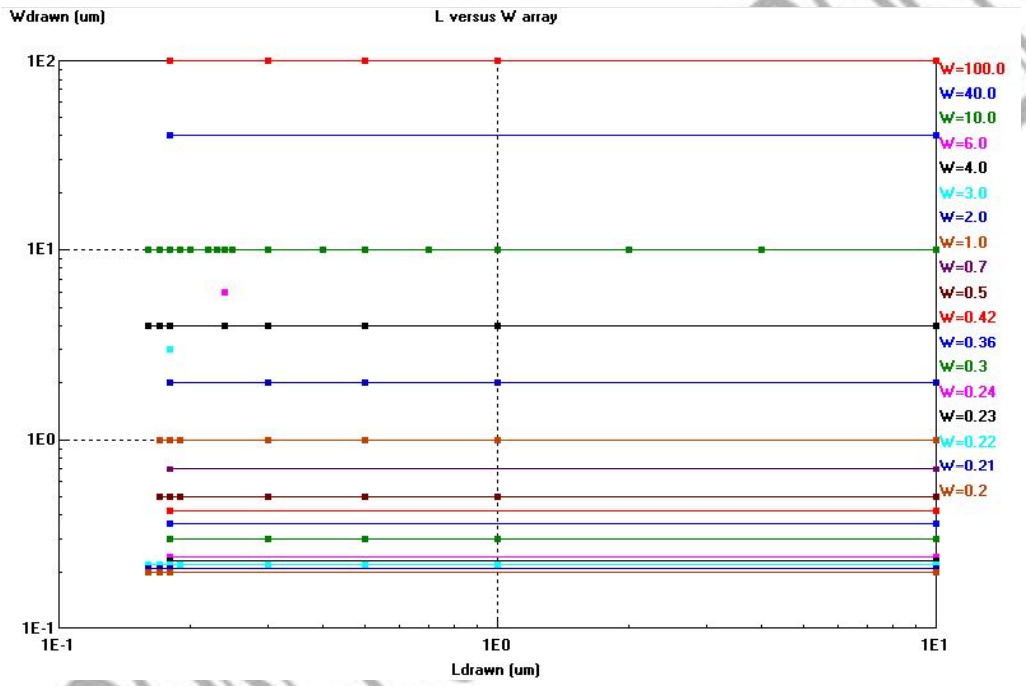
7. Content:

7.1 Wafer Information

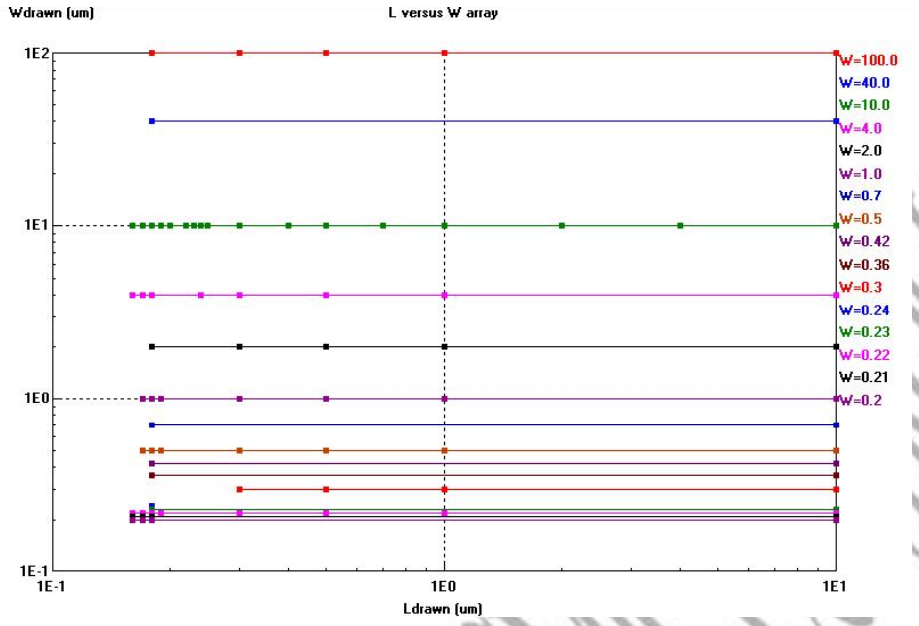
The wafers used for SPICE modeling include transistors of 1.8V and 5V devices. Idsat and Vth of all types of devices are on target or close to the target. The on-target Idsat device sizes are W/L=10/0.18 for 1.8V N&PMOS and W/L=10/0.5 for 5V N&PMOS.

The sizes of MOSFET test structures are graphically shown below. Not all devices are used in the parameter extraction, but most of the devices in the test structures are compared with the model after the parameter extraction to verify the accuracy of the model.

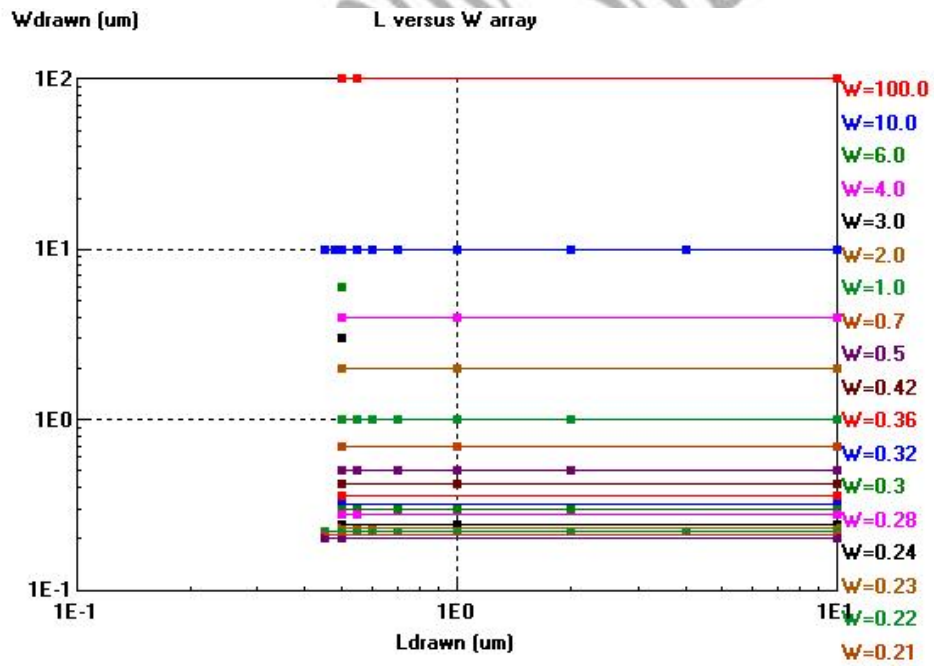
Device sizes for 1.8V NMOS:



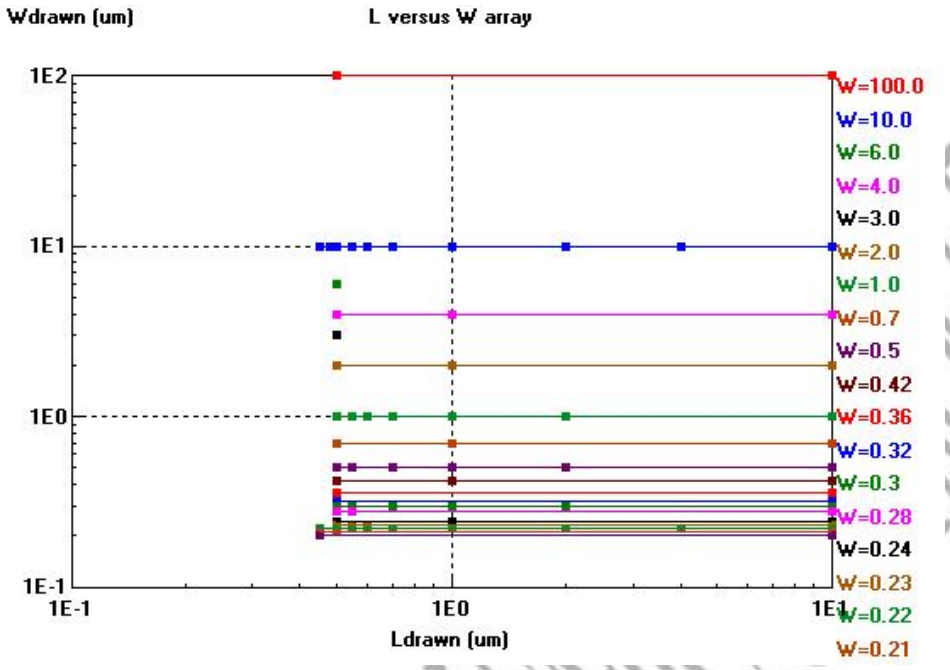
Device sizes for 1.8V PMOS:



Device sizes for 5V NMOS:



Device sizes for 5V PMOS:



The MOS transistors selected for model extraction are based on WAT mean values of Idsat and Vth. Once the Idsat and Vth values of the transistor are close to mean values, the "golden" transistor is selected and used for MOS IV modeling. The other parameters such as Tox, Cgdo, Cj, etc. are obtained on the most suitable die (close to mean values). The wafers used for modeling are BT0321#5 for 1.8V device and AT0812#23 for 5V device, respectively.

The die location of the selected device is (0,0) for 1.8V N/PMOS target device (W/L=10/0.18), (0,0) and (-1,-2) for 5V N/PMOS target device (W/L=10/0.5), respectively. Shown in the next few pages are some wafer mapping plots to show the parameter distribution on the wafers.

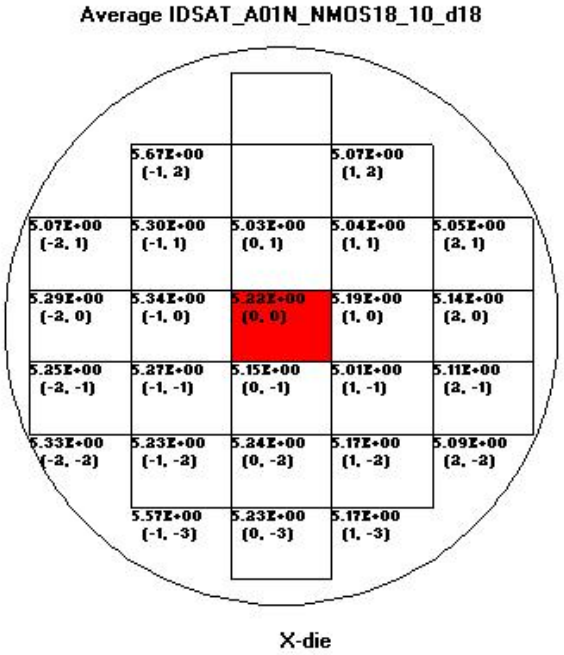


Fig 7.1.1. 1.8V NMOS W/L=10/0.18 Idsat wafer map, Die (0,0) is the selected die for parameter extraction.

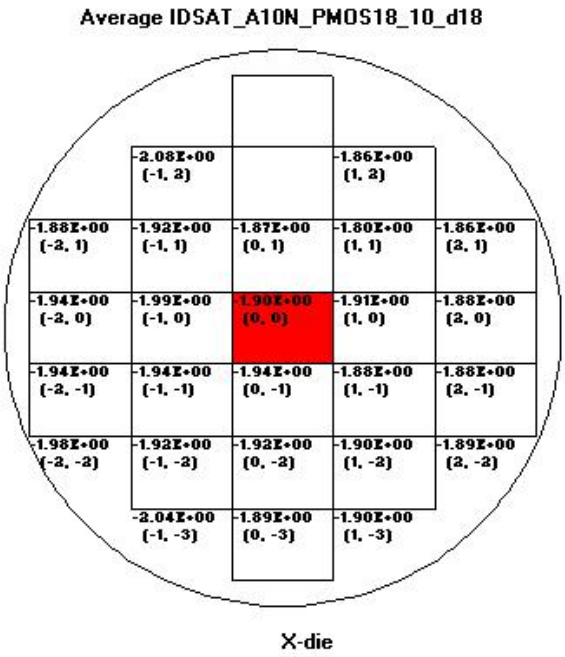


Fig 7.1.2. 1.8V PMOS W/L=10/0.18 Idsat wafer map, Die (0,0) is the selected die for parameter extraction.

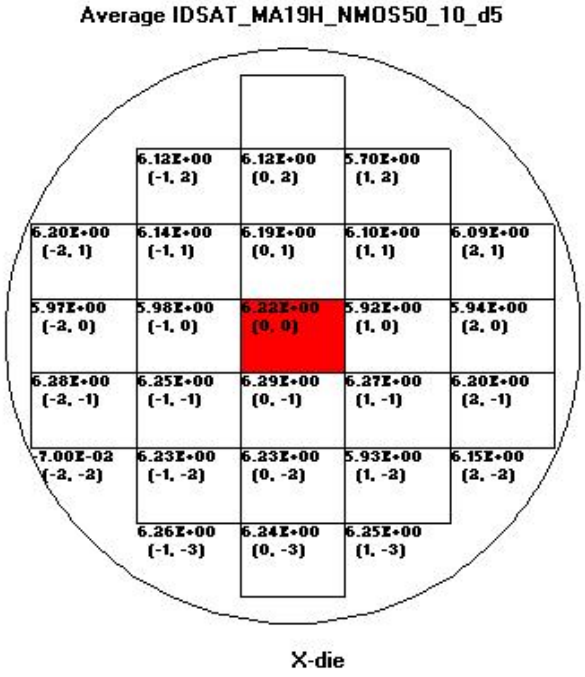


Fig 7.1.3. 5V NMOS W/L=10/0.5 Idsat wafer map, Die(0,0) is the selected die for parameter extraction.

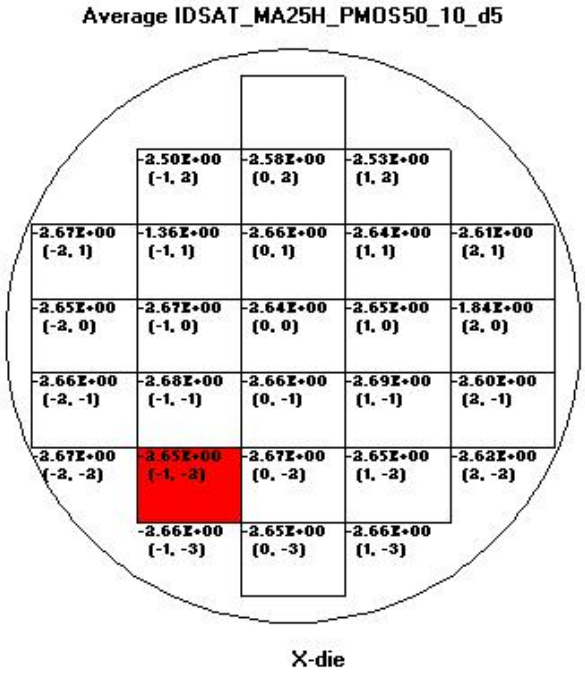


Fig 7.1.4. 5V PMOS W/L=10/0.5 Idsat wafer map, Die (-1,-2) is the selected die for parameter extraction.

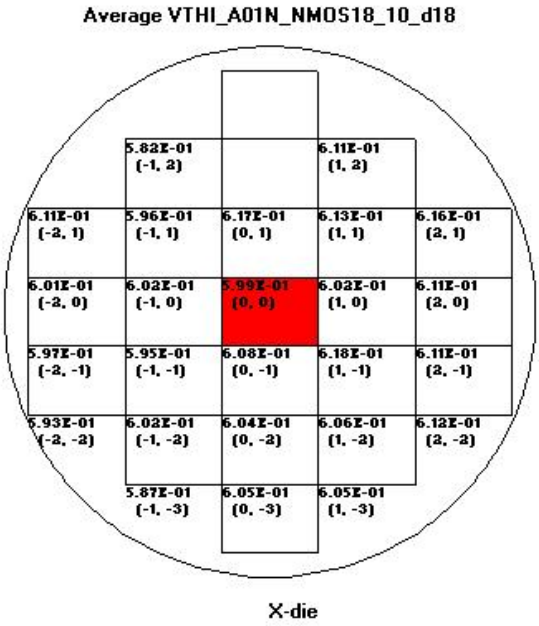


Fig 7.1.5. 1.8V NMOS W/L=10/0.18 Vth wafer map, Die(0,0) is the selected die for parameter extraction.

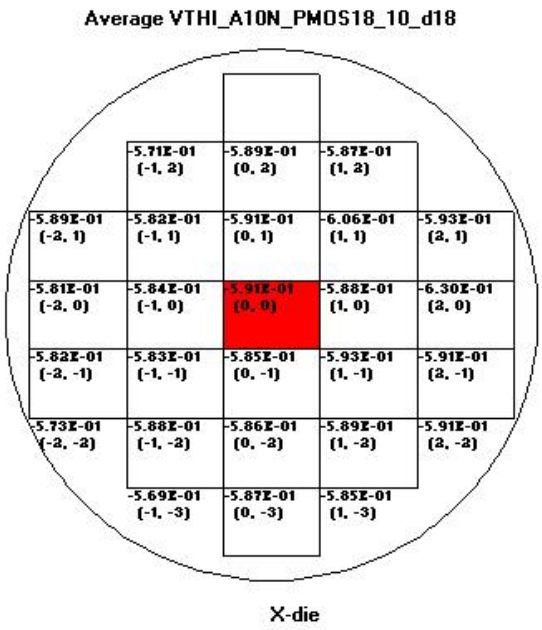


Fig 7.1.6. 1.8V PMOS W/L=10/0.18 Vth wafer map, Die (0,0) is the selected die for parameter extraction.

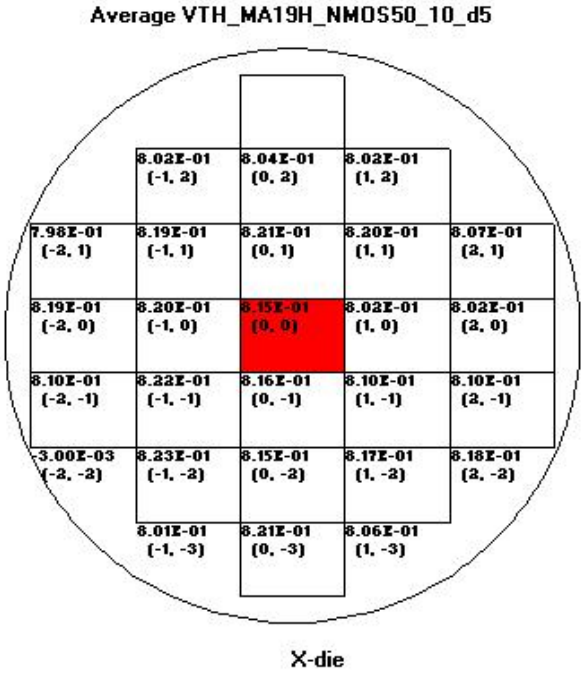


Fig 7.1.7. 5V NMOS W/L=10/0.5 Vth wafer map, Die (0,0) is the selected die for parameter extraction.

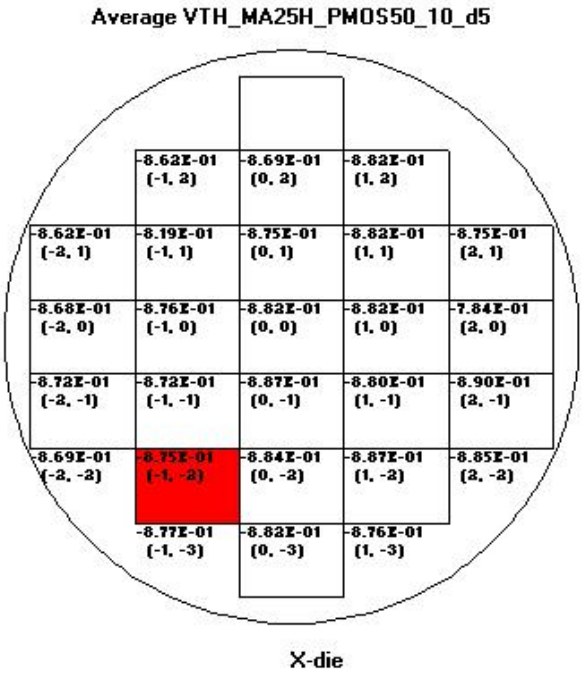


Fig 7.1.8 5V PMOS W/L=10/0.5 Vth wafer map, Die (-1,-2) is the selected die for parameter extraction.

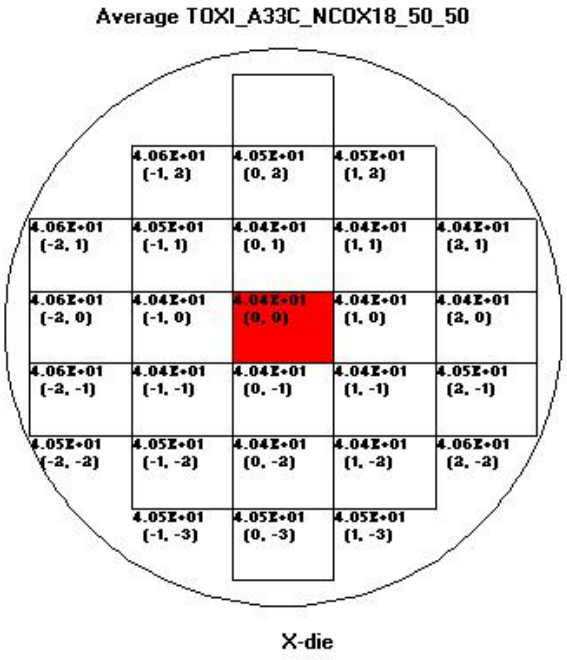


Fig 7.1.9. 1.8V NMOS Tox wafer map, Die (0,0) is the selected die for parameter extraction.

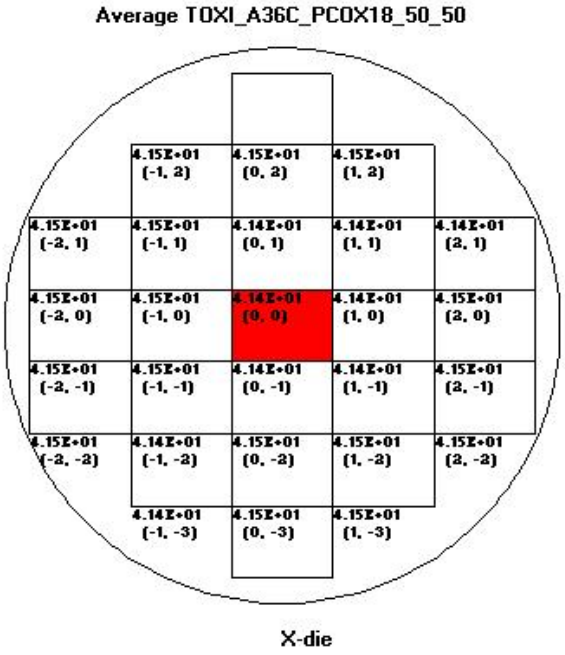


Fig 7.1.10. 1.8V PMOS Tox wafer map, Die (0,0) is the selected die for parameter extraction.

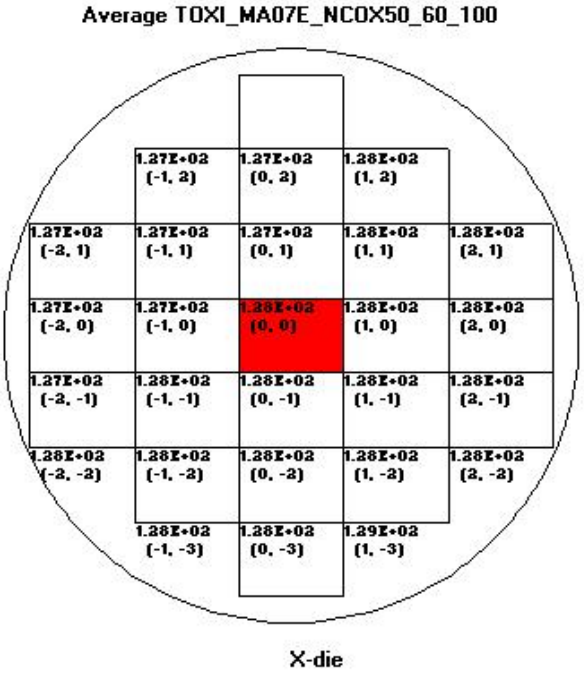


Fig 7.1.11. 5V NMOS Tox wafer map, Die (0,0) is the selected die for parameter extraction.

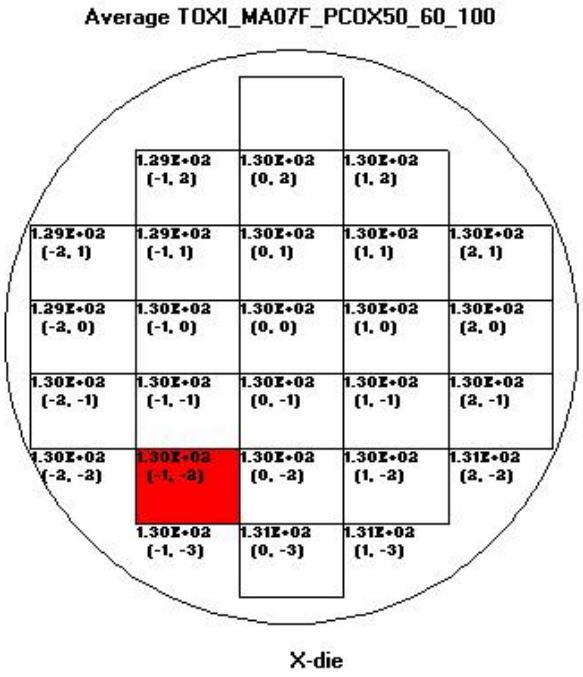


Fig 7.1.12. 5V PMOS Tox wafer map, Die (-1,-2) is the selected die for parameter extraction.

7.2 MOSFET Model

7.2.1 Capability of Model

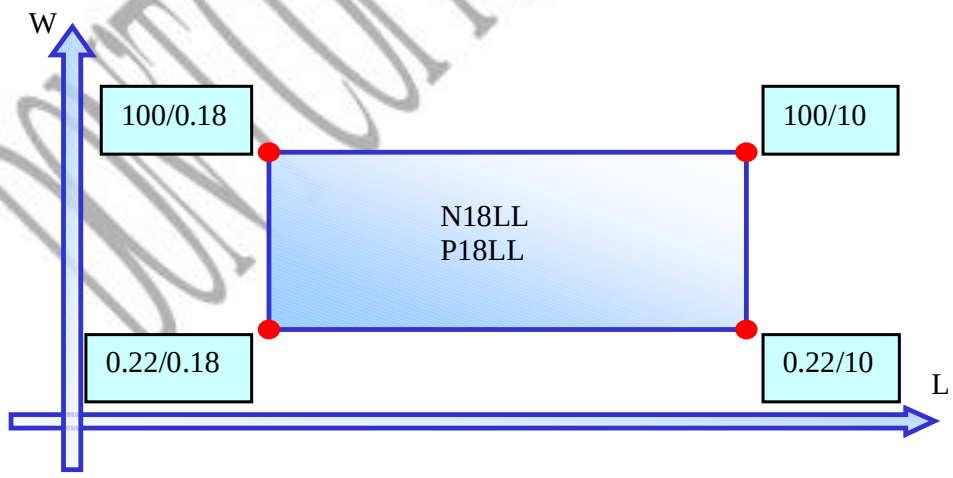
The model parameters are given in HSPICE and Spectre format. If you use simulators other than HSPICE and Spectre (such as Mentor Graphics's Eldo), you need to convert the model parameter format to meet different simulators' input requirement. Please contact SMIC if you need more information regarding the model parameter format of other simulators. All the model files are given in the attachment.

In order to model the bulk-to-source and bulk-to-drain junction diodes accurately, the option ACM=12 in HSPICE is used for the junction diode model.

The temperature range and power supply used to extract model parameters are from -40°C to 125°C, 1.8V for thin-oxide MOSFETs and 5V for thick-oxide MOSFETs, respectively. The transistor sizes used in the extraction are 0.18um≦length≦10um, 0.22um≦width≦100um for 1.8V thin-oxide devices, and 0.5um≦length≦10um, 0.22um≦width≦100um for 5V thick-oxide devices, respectively. Using the model to simulate MOSFETs whose device sizes are outside of this range, especially beyond the minimum geometry, is not recommended because the accuracy of the model cannot be guaranteed. Nevertheless, the continuity of the model has been checked up to 10*Vdd to ensure good convergence behavior during circuit simulation.

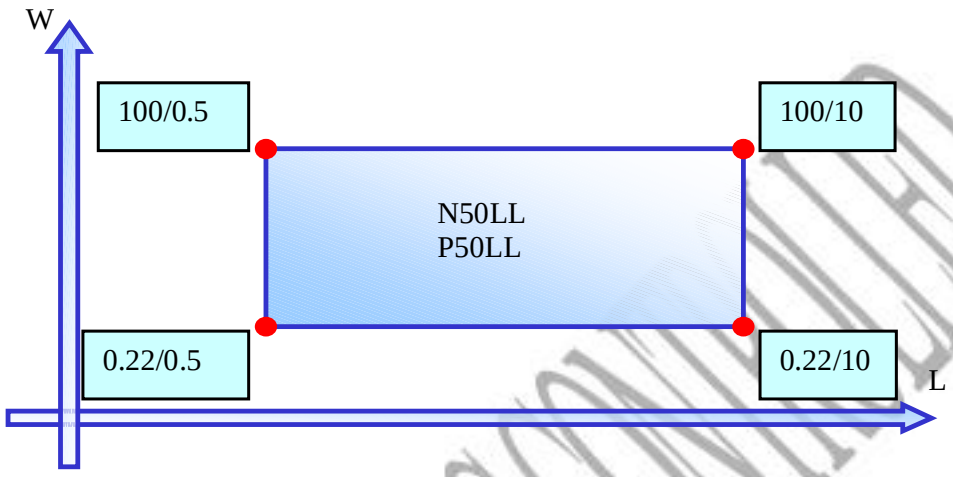
The valid range of device sizes is graphically shown in next page for 1.8V thin-oxide MOSFET models and 5V thick-oxide MOSFET models.

A. 1.8V thin-oxide MOS model



Where n18ll and p18ll are the model names for 1.8V NMOS and PMOS transistors, respectively.

B. 5V thick-oxide MOS model



Where n50ll and p50ll are the model names for 5V NMOS and PMOS transistors, respectively.

7.2.2 Corner Model Table

In order to simulate corner cases, the parameters in the following table should be modified according to the situation chosen.

A. 1.8V thin-oxide MOS

Parameters	Unit	TT	SS	FF	SNFP	FNSP
DTOX_N18LL	m	0	1.1E-10	-1.1E-10	0	0
DXL_N18LL	m	0	1.25E-8	-1.25E-8	1.25E-8	-1.25E-8
DXW_N18LL	m	0	-2.2E-8	2.2E-8	-2.2E-8	2.2E-8
DVTH_N18LL	V	0	0.05	-0.05	0.05	-0.05
DCJ_N18LL	F/m^2	0	5.45E-5	-5.45E-5	5.45E-5	-5.45E-5
DCJSW_N18LL	F/m	0	4.695E-12	-4.695E-12	4.695E-12	-4.695E-12
DCJSWG_N18LL	F/m	0	2.29E-11	-2.29E-11	2.29E-11	-2.29E-11
DCGDO_N18LL	F/m	0	-1.84E-11	1.84E-11	0	0
DCGSO_N18LL	F/m	0	-1.84E-11	1.84E-11	0	0
DPVTH0_N18LL	V	0	4E-16	-4E-16	4E-16	-4E-16
DTOX_P18LL	m	0	1.1E-10	-1.1E-10	0	0
DXL_P18LL	m	0	1.25E-8	-1.25E-8	-1.25E-8	1.25E-8
DXW_P18LL	m	0	-2.2E-8	2.2E-8	2.2E-8	-2.2E-8
DVTH_P18LL	V	0	-0.04	0.04	0.04	-0.04
DCJ_P18LL	F/m^2	0	5.10E-5	-5.10E-5	-5.10E-5	5.10E-5
DCJSW_P18LL	F/m	0	4.24E-12	-4.24E-12	-4.24E-12	4.24E-12
DCJSWG_P18LL	F/m	0	2.14E-11	-2.14E-11	-2.14E-11	2.14E-11
DCGDO_P18LL	F/m	0	-1.68E-11	1.68E-11	0	0
DCGSO_P18LL	F/m	0	-1.68E-11	1.68E-11	0	0
DPVTH0_P18LL	V	0	-4E-16	4E-16	4E-16	-4E-16

where: TT: Typical model
SS: Slow model
FF: Fast model
SNFP: Slow N fast P model
FNSP: Fast N slow P model

B. 5V thick-oxide MOS

Parameters	Unit	TT	SS	FF	SNFP	FNSP
DTOX_N50LL	m	0	5.00E-10	-5.00E-10	0	0
DXL_N50LL	m	0	5.50E-08	-5.50E-08	5.50E-08	-5.50E-08
DXW_N50LL	m	0	-2.20E-08	2.20E-08	-2.20E-08	2.20E-08
DVTH_N50LL	V	0	0.04	-0.04	0.04	-0.04
DCJ_N50LL	F/m^2	0	6.13E-05	-6.13E-05	6.13E-05	-6.13E-05
DCJSW_N50LL	F/m	0	7.90E-12	-7.90E-12	7.90E-12	-7.90E-12
DCJSWG_N50LL	F/m	0	1.97E-11	-1.97E-11	1.97E-11	-1.97E-11
DCGDO_N50LL	F/m	0	-1.87E-11	1.87E-11	0	0
DCGSO_N50LL	F/m	0	-1.87E-11	1.87E-11	0	0
DPVHT0_N50LL	V	0	4.00E-15	-4.00E-15	4.00E-15	-4.00E-15
DTOX_P50LL	m	0	5.00E-10	-5.00E-10	0	0
DXL_P50LL	m	0	5.50E-08	-5.50E-08	-5.50E-08	5.50E-08
DXW_P50LL	m	0	-2.20E-08	2.20E-08	2.20E-08	-2.20E-08
DVTH_P50LL	V	0	-0.05	0.05	0.05	-0.05
DCJ_P50LL	F/m^2	0	5.79E-05	-5.79E-05	-5.79E-05	5.79E-05
DCJSW_P50LL	F/m	0	5.56E-12	-5.56E-12	-5.56E-12	5.56E-12
DCJSWG_P50LL	F/m	0	1.85E-11	-1.85E-11	-1.85E-11	1.85E-11
DCGDO_P50LL	F/m	0	-1.72E-11	1.72E-11	0	0
DCGSO_P50LL	F/m	0	-1.72E-11	1.72E-11	0	0

where: TT: Typical model
SS: Slow model
FF: Fast model
SNFP: Slow N fast P model
FNSP: Fast N slow P model

7.2.3 Ring Oscillator Verification

The MOSFET models are also verified by comparing the measured ring oscillator speed with HSPICE simulation results for different types and dimensions of ring oscillators: the inverter, NAND gate and NOR gate ring oscillators with fanout=1 and fanout=3. The results are shown in the following tables. For completeness, ring oscillator simulations at different power supply and temperatures also included.

Due to the minor variation between the poly CD of ring oscillators and the device test structures, DXL, DXW, DLUA, DLVSAT and DVTH0 parameters used in the simulation are adjusted to fit Idsat of each ring oscillator measured (In released typical model, DXL=DXW=DLUA=DLVSAT=DVTH0=0). The adjustment of DXL, DXW, DLUA, DLVSAT and DVTH0 are also listed in the table. Furthermore, to take into account the interconnection parasitic resistance and capacitance effect, the parasitic resistance and capacitance are extracted from ring oscillator layout and included in the HSPICE netlist.

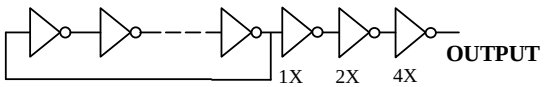
The drawn sizes of the ring oscillator and the adjusted parameters for 1.8V model are listed as follows:

1.8V inverter, NAND and NOR measured size table						
	drawn size	model fitting parameter				
		DXL	DXW	DLUA	DLVSAT	DVTH0
F.O.1	NMOS 4/0.18	-5.00E-09	4.00E-08	4.50E-17	-1.10E-03	2.00E-02
	PMOS 6/0.18	-4.00E-09	3.00E-08	-4.75E-17	-1.60E-03	-4.00E-02
	NMOS 4/0.19	-5.00E-09	4.00E-08	4.50E-17	-1.50E-03	2.00E-02
	PMOS 6/0.19	-4.00E-09	3.00E-08	-5.25E-17	-1.80E-03	-4.00E-02
	NMOS 4/0.20	-5.00E-09	4.00E-08	4.50E-17	-1.20E-03	2.00E-02
	PMOS 6/0.20	-4.00E-09	3.00E-08	-6.35E-17	-1.80E-03	-4.00E-02
F.O.3	NMOS 4/0.18	-1.20E-08	4.00E-08	5.00E-17	-1.50E-03	2.00E-02
	PMOS 6/0.18	-1.00E-08	3.00E-08	-6.25E-17	0	-4.00E-02
	NMOS 4/0.19	-1.20E-08	4.00E-08	5.50E-17	-1.50E-03	2.00E-02
	PMOS 6/0.19	-1.00E-08	3.00E-08	-1.85E-17	-1.70E-03	-4.00E-02
	NMOS 4/0.20	-1.20E-08	4.00E-08	5.00E-17	-1.40E-03	2.00E-02
	PMOS 6/0.20	-1.00E-08	3.00E-08	-2.15E-17	-1.80E-03	-4.00E-02

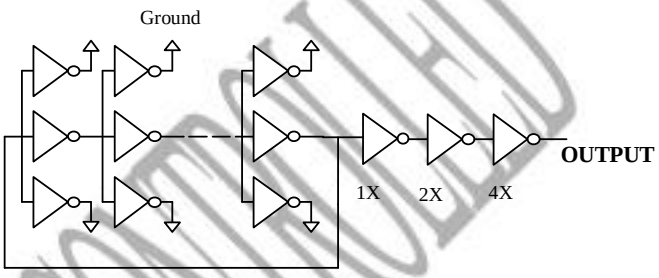
A. Inverter ring oscillator

Schematic and Descriptions of Inverter-Type Ring Oscillator

F.O.1



F.O.3



The area and perimeter parameters are set according to SMIC 0.18um ring oscillator layout.

For fan-out 1 simulation, they are:
pmos …. as=2.31p ad=2.31p ps=12.77u pd=12.77u
nmos …. as=1.54p ad=1.54p ps=8.77u pd=8.77u

For fan-out 3 simulation, they are:
Inveter:
pmos ….. as=1.05p ad=2.31p ps=6.35u pd=12.77u
nmos ….. as=0.7p ad=1.54p ps=4.35u pd=8.77u
load-1:
pmos ….. as=2.31p ad=1.05p ps=12.77u pd=6.35u
nmos ….. as=1.54p ad=0.7p ps=8.77u pd=4.35u
load-2:
pmos ….. as=1.05p ad=1.05p ps=6.35u pd=6.35u
nmos ….. as=0.7p ad=0.7p ps=4.35u pd=4.35u

1.8V Inverter Ring Simulation and Measurement Results

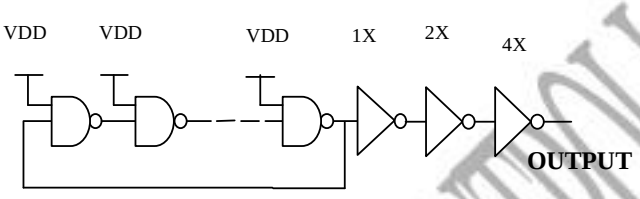
Temp(C)	VDD(V)	F. O.	Channel Length (Ln/Lp) (um/um)	Measurement (ps/gate)	Simulation (ps/gate)
25	1.98	1	0.18	31.96	32.07
25	1.8	1	0.18	35.66	35.70
25	1.62	1	0.18	41.77	41.08
25	1.44	1	0.18	50.05	49.43
125	1.8	1	0.18	41.16	40.09
85	1.8	1	0.18	38.87	38.40
-15	1.8	1	0.18	33.58	33.84
-40	1.8	1	0.18	32.28	32.60
25	1.98	1	0.19	34.82	35.62
25	1.8	1	0.19	39.99	39.84
25	1.62	1	0.19	47.86	46.00
25	1.44	1	0.19	59.63	55.69
125	1.8	1	0.19	46.81	45.30
85	1.8	1	0.19	43.28	43.03
-15	1.8	1	0.19	37.24	37.56
-40	1.8	1	0.19	35.94	36.06
25	1.98	1	0.2	38.32	39.00
25	1.8	1	0.2	43.65	43.71
25	1.62	1	0.2	52.44	50.67
25	1.44	1	0.2	65.38	61.65
125	1.8	1	0.2	51.16	49.68
85	1.8	1	0.2	48.20	47.38
-15	1.8	1	0.2	40.63	41.07
-40	1.8	1	0.2	39.17	39.33

Temp(C)	VDD(V)	F. O.	Channel Length (Ln/Lp) (um/um)	Measurement (ps/gate)	Simulation (ps/gate)
25	1.98	3	0.18	61.02	61.15
25	1.8	3	0.18	68.94	72.01
25	1.62	3	0.18	82.04	81.92
25	1.44	3	0.18	100.65	97.18
125	1.8	3	0.18	80.36	80.07
85	1.8	3	0.18	75.71	76.95
-15	1.8	3	0.18	64.50	68.50
-40	1.8	3	0.18	62.65	66.19
25	1.98	3	0.19	67.68	72.38
25	1.8	3	0.19	77.74	80.32
25	1.62	3	0.19	91.88	91.82
25	1.44	3	0.19	110.18	109.61
125	1.8	3	0.19	88.67	90.08
85	1.8	3	0.19	84.72	86.32
-15	1.8	3	0.19	71.92	76.02
-40	1.8	3	0.19	69.84	73.18
25	1.98	3	0.2	74.54	78.73
25	1.8	3	0.2	85.63	87.67
25	1.62	3	0.2	101.73	100.64
25	1.44	3	0.2	123.41	120.80
125	1.8	3	0.2	99.50	98.83
85	1.8	3	0.2	94.12	94.55
-15	1.8	3	0.2	80.24	79.40
-40	1.8	3	0.2	77.25	78.23

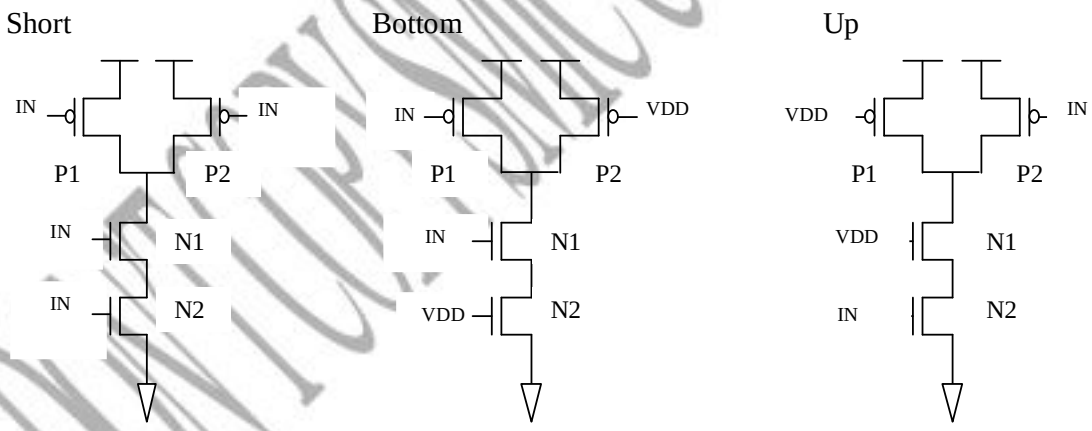
B.NAND ring oscillator

Schematic and Descriptions of NAND Type Ring Oscillator

F.O.1



Schematics of NAND Gate unit cells



The area and perimeter parameters are set according to SMIC 0.18um ring oscillator layout.
For NAND simulation, they are:

		as	ps	ad	pd
F.O.1	P1	2.31p	12.77u	1.05p	6.35u
	P2	2.31p	12.77u	1.05p	6.35u
	N1	1.54p	8.77u	0.12p	4.06u
	N2	0.12p	4.06u	1.54p	8.77u

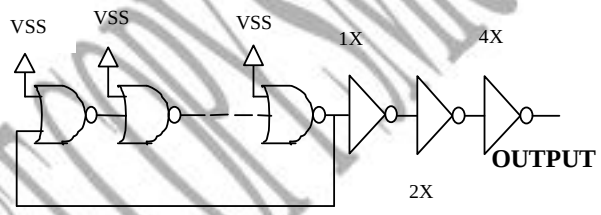
1.8V NAND Type Ring Simulation and Measurement Results

Type	Temp(C)	VDD(V)	F. O.	Channel Length (Ln/Lp) (um/um)	Measurement (ps/gate)	Simulation (ps/gate)
short	25	1.98	1	0.18	44.99	48.97
short	25	1.8	1	0.18	50.80	54.74
short	25	1.62	1	0.18	59.48	63.24
short	25	1.44	1	0.18	73.82	76.70
short	125	1.8	1	0.18	59.65	64.26
short	85	1.8	1	0.18	56.13	60.50
short	-15	1.8	1	0.18	47.19	50.81
short	-40	1.8	1	0.18	45.20	48.31

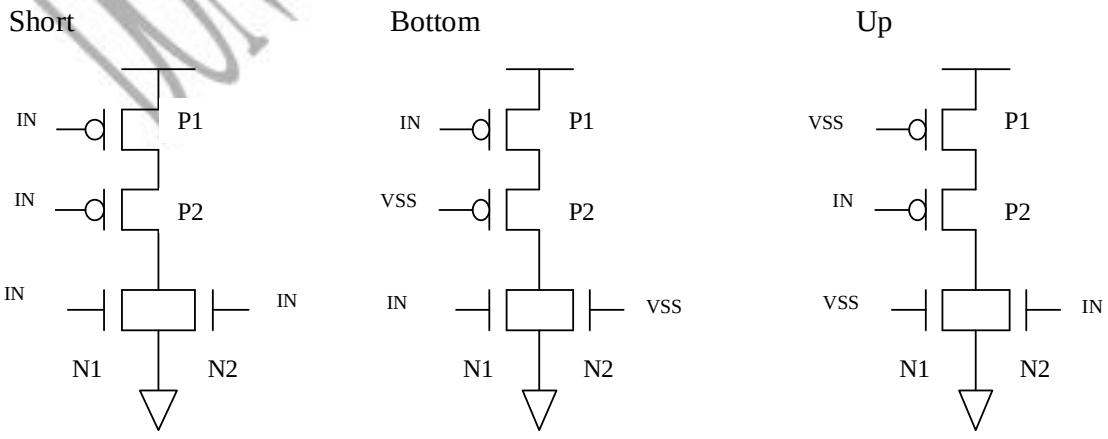
C. NOR ring oscillator

Schematic and Descriptions of NOR Type Ring Oscillator

F.O.1



Schematics of NOR Gate unit cells



The area and perimeter parameters are set according to SMIC 0.18um ring oscillator layout. For NOR simulation, they are:

		as	ps	ad	pd
F.O.1	P1	2.31p	12.77u	0.18p	6.06u
	P2	0.18p	6.06u	2.31p	12.77u
	N1	1.54p	8.77u	0.7p	4.35u
	N2	1.54p	8.77u	0.7p	4.35u

1.8V NOR Ring Simulation and Measurement Results

Type	Temp(C)	VDD(V)	F. O.	Channel Length (Ln/Lp) (um/um)	Measurement (ps/gate)	Simulation (ps/gate)
short	25	1.98	1	0.18	62.02	63.03
short	25	1.8	1	0.18	71.58	71.50
short	25	1.62	1	0.18	85.25	83.73
short	25	1.44	1	0.18	106.46	102.71
short	125	1.8	1	0.18	81.35	79.14
short	85	1.8	1	0.18	78.25	76.31
short	-15	1.8	1	0.18	67.21	67.79
short	-40	1.8	1	0.18	63.73	65.22

7.2.4 1/f Noise Model

MOSFET 1/f noise parameters are characterized for HSPICE NLEV=3. The noise equation is shown below. There are two parameters, AF and KF, in this model.

$$\textbf{Flicker Noise} = \left[\frac{\mathbf{KF} \cdot \mathbf{gm}^2}{\mathbf{Cox} \cdot \mathbf{Weff} \cdot \mathbf{Leff} \cdot \mathbf{f}^{\mathbf{AF}}} \right]^{1/2}$$

It's well known that the 1/f noise model can't fit the whole range of biases (Vgs, Vds, and Vbs). To make this model more accurate, we provide different values of AF and KF for different bias conditions and device sizes as shown in the table. You should select the appropriate values of AF and KF for your design. Besides, we provided the different set of AF and KF values which fit the whole range of biases (Vgs, Vds, Vbs) for each transistor. We also provided one set of AF and KF values fitting for all transistors and put the parameters to our model cards. Please refer to the following tables.

A.1.8V thin oxide NMOS

Table A1: AF and KF for different bias conditions and device sizes of 1.8V thin oxide NMOS.

W/L	VGS	VDS	AF	KF
10/1	0.7	0.3	0.60	8.47E-26
	0.7	0.6	0.60	8.47E-26
	0.7	0.9	0.60	8.47E-26
	0.7	1.8	0.60	8.47E-26
	1.2	0.3	0.77	4.31E-25
	1.2	0.6	0.77	4.31E-25
	1.2	0.9	0.77	4.31E-25
	1.2	1.8	0.77	4.31E-25
	1.8	0.3	0.89	1.72E-24
	1.8	0.6	0.89	1.72E-24
	1.8	0.9	0.89	1.72E-24
	1.8	1.8	0.89	1.72E-24

W/L	VGS	VDS	AF	KF
10/0.5	0.7	0.3	0.77	5.14E-25
	0.7	0.6	0.77	5.14E-25
	0.7	0.9	0.77	5.14E-25
	0.7	1.8	0.77	5.14E-25
	1.2	0.3	0.82	6.37E-25
	1.2	0.6	0.82	6.37E-25
	1.2	0.9	0.82	6.37E-25
	1.2	1.8	0.82	6.37E-25
	1.8	0.3	0.91	2.40E-24
	1.8	0.6	0.91	2.40E-24
	1.8	0.9	0.91	2.40E-24
	1.8	1.8	0.91	2.40E-24

W/L	VGS	VDS	AF	KF
10/0.3	0.7	0.3	0.65	3.49E-25
	0.7	0.6	0.65	3.49E-25
	0.7	0.9	0.65	3.49E-25
	0.7	1.8	0.65	3.49E-25
	1.2	0.3	0.90	1.53E-24
	1.2	0.6	0.90	1.53E-24
	1.2	0.9	0.90	1.53E-24
	1.2	1.8	0.90	1.53E-24
	1.8	0.3	0.92	2.73E-24
	1.8	0.6	0.92	2.73E-24
	1.8	0.9	0.92	2.73E-24
	1.8	1.8	0.92	2.73E-24

W/L	VGS	VDS	AF	KF
10/0.18	0.7	0.3	0.58	1.10E-25
	0.7	0.6	0.58	1.10E-25
	0.7	0.9	0.58	1.10E-25
	0.7	1.8	0.58	1.10E-25
	1.2	0.3	0.66	2.62E-25
	1.2	0.6	0.66	2.62E-25
	1.2	0.9	0.66	2.62E-25
	1.2	1.8	0.66	2.62E-25
	1.8	0.3	0.80	1.26E-24
	1.8	0.6	0.80	1.26E-24
	1.8	0.9	0.80	1.26E-24
	1.8	1.8	0.80	1.26E-24

Table A2: AF and KF for each transistor with different size and global range parameters for all transistors of 1.8V thin oxide NMOS.

W/L	AF	KF
10/1	0.9	1.70E-24
10/0.5	0.91	1.40E-24
10/0.3	0.92	2.70E-24
10/0.18	0.8	1.25E-24
Global range parameters	0.88	1.70E-24

Note: Global range parameters are used in the model card.

B.1.8V thin-oxide PMOS

Table B1: AF and KF for different bias conditions and device sizes of 1.8V thin oxide PMOS.

W/L	VGS	VDS	AF	KF
10/1	0.7	0.3	0.57	6.25E-26
	0.7	0.6	0.57	6.25E-26
	0.7	0.9	0.57	6.25E-26
	0.7	1.8	0.57	6.25E-26
	1.2	0.3	1.05	4.23E-24
	1.2	0.6	1.05	4.23E-24
	1.2	0.9	1.05	4.23E-24
	1.2	1.8	1.05	4.23E-24
	1.8	0.3	1.12	2.46E-23
	1.8	0.6	1.12	2.46E-23
	1.8	0.9	1.12	2.46E-23
	1.8	1.8	1.12	2.46E-23

W/L	VGS	VDS	AF	KF
10/0.5	0.7	0.3	0.70	1.27E-25
	0.7	0.6	0.70	1.32E-25
	0.7	0.9	0.72	1.62E-25
	0.7	1.8	0.73	1.50E-25
	1.2	0.3	1.09	7.29E-24
	1.2	0.6	1.09	7.29E-24
	1.2	0.9	1.09	7.29E-24
	1.2	1.8	1.09	7.29E-24
	1.8	0.3	1.09	2.17E-23
	1.8	0.6	1.09	2.17E-23
	1.8	0.9	1.09	2.17E-23
	1.8	1.8	1.09	2.17E-23

W/L	VGS	VDS	AF	KF
10/0.3	0.7	0.3	1.01	1.24E-24
	0.7	0.6	1.01	1.24E-24
	0.7	0.9	1.01	1.24E-24
	0.7	1.8	1.01	1.24E-24
	1.2	0.3	1.07	3.96E-24
	1.2	0.6	1.07	3.96E-24
	1.2	0.9	1.07	3.96E-24
	1.2	1.8	1.07	3.96E-24
	1.8	0.3	1.26	5.26E-23
	1.8	0.6	1.26	5.26E-23
	1.8	0.9	1.26	5.26E-23
	1.8	1.8	1.26	5.26E-23

W/L	VGS	VDS	AF	KF
10/0.18	0.7	0.3	0.93	6.96E-25
	0.7	0.6	0.93	6.96E-25
	0.7	0.9	0.93	6.96E-25
	0.7	1.8	0.93	6.96E-25
	1.2	0.3	1.12	7.72E-24
	1.2	0.6	1.12	7.72E-24
	1.2	0.9	1.12	7.72E-24
	1.2	1.8	1.12	7.72E-24
	1.8	0.3	1.20	2.97E-23
	1.8	0.6	1.20	2.97E-23
	1.8	0.9	1.20	2.97E-23
	1.8	1.8	1.20	2.97E-23

Table B2: AF and KF for each transistor with different size and global range parameters for all transistors of 1.8V thin oxide PMOS.

W/L	AF	KF
10/1	1.1	2.40E-23
10/0.5	1.1	2.10E-23
10/0.3	1.25	5.20E-23
10/0.18	1.2	2.90E-23
Global range parameters	1.16	2.80E-23

Note: Global range parameters are used in the model card.

C. 5V thin-oxide NMOS

Table C1: AF and KF for different bias conditions and device sizes of 5V thin oxide NMOS.

W/L	VGS	VDS	AF	KF
10/1	1	0.6	0.76	1.50E-24
	1	1.2	0.76	1.50E-24
	1	2.5	0.76	1.50E-24
	1	5	0.76	1.50E-24
	2.5	0.6	0.85	2.50E-24
	2.5	1.2	0.85	2.50E-24
	2.5	2.5	0.85	2.50E-24
	2.5	5	0.85	2.50E-24
	5	0.6	0.86	3.00E-24
	5	1.2	0.86	3.00E-24
	5	2.5	0.86	3.00E-24
	5	5	0.86	3.00E-24

W/L	VGS	VDS	AF	KF
10/0.6	1	0.6	0.77	1.60E-24
	1	1.2	0.77	1.60E-24
	1	2.5	0.77	1.60E-24
	1	5	0.77	1.60E-24
	2.5	0.6	0.86	2.81E-24
	2.5	1.2	0.86	2.81E-24
	2.5	2.5	0.86	2.81E-24
	2.5	5	0.86	2.81E-24
	5	0.6	0.87	3.50E-24
	5	1.2	0.87	3.50E-24
	5	2.5	0.87	3.50E-24
	5	5	0.87	3.50E-24

W/L	VGS	VDS	AF	KF
10/0.5	1	0.6	0.80	2.26E-24
	1	1.2	0.80	2.26E-24
	1	2.5	0.80	2.26E-24
	1	5	0.80	2.26E-24
	2.5	0.6	0.88	3.24E-24
	2.5	1.2	0.88	3.24E-24
	2.5	2.5	0.88	3.24E-24
	2.5	5	0.88	3.24E-24
	5	0.6	0.9	4.60E-24
	5	1.2	0.9	4.60E-24
	5	2.5	0.9	4.60E-24
	5	5	0.9	4.60E-24

Table C2: AF and KF for each transistor with different size and global range parameters for all transistors of 5V thin oxide NMOS.

W/L	AF	KF
10/1	0.84	1.77E-24
10/0.6	0.86	2.71E-24
10/0.5	0.89	3.96E-24
Global range parameters	0.88	3.07E-24

Note: Global range parameters are used in the model card.

D. 5V thin oxide PMOS

Table D1: AF and KF for different bias conditions and device sizes of 5V thin oxide PMOS

W/L	VGS	VDS	AF	KF
10/1	1.2	0.6	0.85	1.87E-25
	1.2	1.2	0.85	1.87E-25
	1.2	2.5	0.85	1.87E-25
	1.2	5	0.85	1.87E-25
	2.5	0.6	0.95	3.75E-24
	2.5	1.2	0.95	3.75E-24
	2.5	2.5	0.95	3.75E-24
	2.5	5	0.95	3.75E-24
	5	0.6	1.09	7.76E-23
	5	1.2	1.09	7.76E-23
	5	2.5	1.09	7.76E-23
	5	5	1.09	7.76E-23

W/L	VGS	VDS	AF	KF
10/0.6	1.2	0.6	0.88	1.98E-25
	1.2	1.2	0.88	1.98E-25
	1.2	2.5	0.88	1.98E-25
	1.2	5	0.88	1.98E-25
	2.5	0.6	0.97	4.50E-24
	2.5	1.2	0.97	4.50E-24
	2.5	2.5	0.97	4.50E-24
	2.5	5	0.97	4.50E-24
	5	0.6	1.09	9.08E-23
	5	1.2	1.09	9.08E-23
	5	2.5	1.09	9.08E-23
	5	5	1.09	9.08E-23

W/L	VGS	VDS	AF	KF
10/0.5	1.2	0.6	0.92	2.40E-25
	1.2	1.2	0.92	2.40E-25
	1.2	2.5	0.92	2.40E-25
	1.2	5	0.92	2.40E-25
	2.5	0.6	1.05	8.90E-24
	2.5	1.2	1.05	8.90E-24
	2.5	2.5	1.05	8.90E-24
	2.5	5	1.05	8.90E-24
	5	0.6	1.10	9.50E-23
	5	1.2	1.10	9.50E-23
	5	2.5	1.10	9.50E-23
	5	5	1.10	9.50E-23

Table D2: AF and KF for each transistor with different size and global range parameters for all transistors of 5V thin oxide PMOS.

W/L	AF	KF
10/1	1.05	4.17E-23
10/0.6	1.06	5.81E-23
10/0.5	1.09	8.04E-23
Global range parameters	1.06	5.03E-23

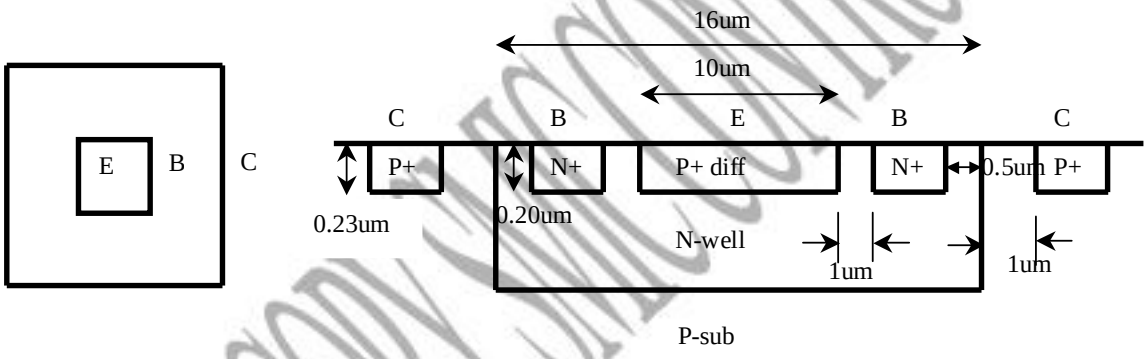
Note: Global range parameters are used in the model card.

7.3 Bipolar Gummel-Poon Model

7.3.1 Capability of Model

BJT parameters were extracted from a vertical P+/Nwell/Psub test structure. Parameter fitting is focused on the forward mid-current and constant BF region. The parameters are extracted from data with temperature range from -40°C to 125°C. HSPICE bipolar Gummel-Poon Level-1 model is used. BJT model is usually not scalable. We provide three types BJT models, pnp18a100ll, pnp18a25ll and pnp18a4ll. The emitter and base area is 10*10 um^2 and 16*16 um^2 for pnp18a100ll, is 5*5 um^2 and 11*11 um^2 for pnp18a25ll, is 2*2 um^2 and 8*8 um^2 for pnp18a4ll.

The BJT GDSII and layer definition files are provided in the attachment (l018ll_io50_layer.map is the layer definition file; PNP18A100.gds, PNP18A25.gds and PNP18A4.gds are the GDSII data files). The top view and cross section of 1.8V BJT test structure are shown as below:



7.4 Diode Model

7.4.1 Capability of Model

Diode parameters were extracted from N+/Psub, P+/Nwell and Nwell/Psub test structures. The parameters were extracted from data with temperature range from -40°C to 125°C. HSPICE Diode Level-3 model is used. All 1.8V thin-oxide and 5V thick-oxide diodes are provided. The sizes of test structures for parameters extraction are: 60*60um^2 for 1.8V N+/Psub and P+/Nwell, 60*200um^2 for 5V N+/Psub and P+/Nwell, 80*120um^2 for Nwell/Psub, respectively. All of the related diode GDSII files are listed in the attachments. (DIO_NPW18.gds, DIO_PNW18.gds, DIO_NPW50.gds, DIO_PNW50.gds and DIO_NWPS.gds).

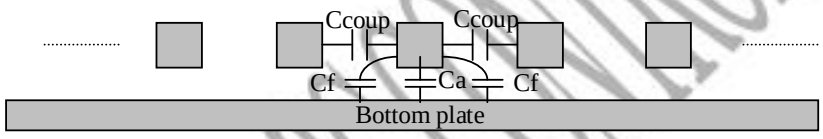
7.5 Interconnection Model

7.5.1. Descriptions for the Interconnect Capacitance

This model is for 0.18um Logic Low Leakage Salicide 1P6M FSG process. The interconnect capacitance table is calculated from Synopsys's Raphael simulation. Two kinds of structures are simulated. They are conduction lines above an infinite ground plane (structure-1) and conduction lines between two infinite ground planes (structure-2). The simulation results of typical, fast and slow cases for both structure-1 and structure-2 are listed in a separate file. (please refer to the attachment: l018ll_io50_interconnect_struct_1.txt, l018ll_io50_interconnect_struct_2.txt).

A. The structures and definition of each capacitance component

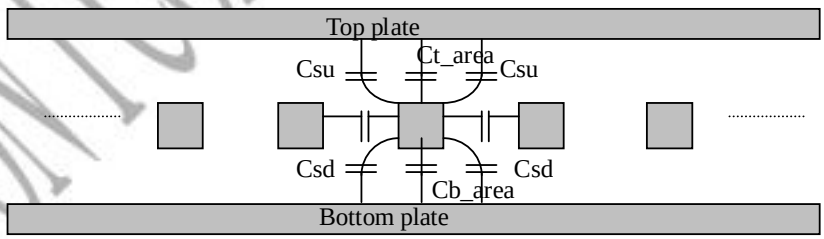
Structure 1 is (a) conduction lines above an infinite ground plane as shown below.



*** Definitions of various capacitances:

Ctotal [fF/um]: total capacitance of a conductor to all others.
Ccoup [fF/um]: coupling capacitance between two conductors in the same layer.
Cbottom [fF/um]: capacitance between a conductor to the bottom ground plane. (=Ca+2*Cf)
Cf [fF/um]: fringing capacitance.

Structure 2 is (b) conduction lines between two infinite ground planes as shown below.



*** Definitions of various capacitances:

Ctotal [fF/um]: total capacitance of a conductor to all others.
Ccoup [fF/um]: coupling capacitance between two conductors in the same layer.
Cbottom [fF/um]: capacitance between a conductor to the bottom ground plane. (=Cb_area+2*Csd)
Ctop[fF/um]: capacitance between a conductor to the top ground plane. (=Ct_area+2*Csu)
Csd[fF/um]: Side-wall down capacitance coefficient.
Csu[fF/um]: Side-wall up capacitance coefficient.

B. The methodology of corner model simulation

Fast Case: Thickness = (1- 0.5 * process variation) * typical thickness
Width = (1- 0.5 * process variation) * typical width
Slow Case : Thickness = (1 + 0.5 * process variation) * typical thickness
Width = (1+ 0.5 * process variation) * typical width

The minimum or maximum dielectric thickness are computed by subtracting or adding the statistical sum of all dielectric thickness variations between the two layers of interest. Let $\Delta T_{total} = \sqrt{\sum_i (\Delta t_i)^2}$, where ΔT_{total} is the effective total variation between two layers.

Δt_i is the variations of interlayer dielectrics among metal, air, and substrates.

$\Delta t_i = T_i * (0.5 * \beta_i)$, where T_i is the dielectric thickness and β_i is the thickness variation.

$TH_i = T_i \pm \Delta T_{total} * \frac{\Delta t_i}{\sum_i T_i * 0.5 * \beta_i}$, where TH_i is the final thickness of the dielectric

.

7.5.2. Related Process Data and Information for Interconnection

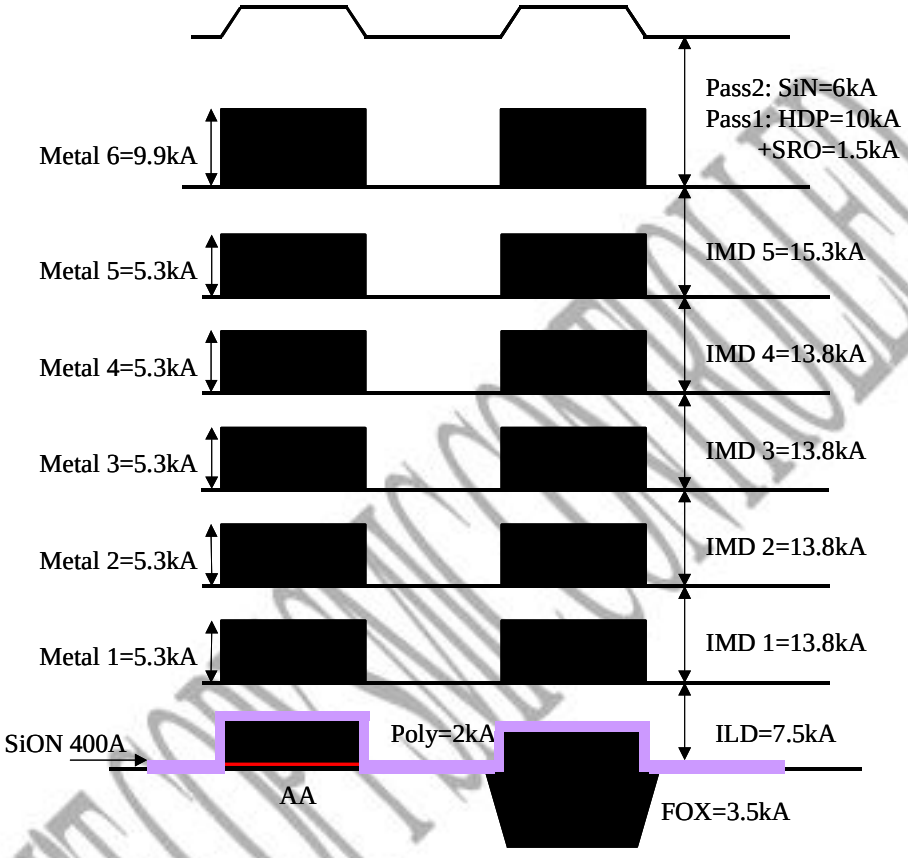
A. Conductor layers

Conductor Name	Typical Thickness (A)	Variation (%)	Min. Width (um)	Variation (%)	Min. Space (um)	Variation (%)
M6	9900	(+/-10%)	0.44	(+/-10%)	0.46	(+/-10%)
M5	5300	(+/-10%)	0.28	(+/-10%)	0.28	(+/-10%)
M4	5300	(+/-10%)	0.28	(+/-10%)	0.28	(+/-10%)
M3	5300	(+/-10%)	0.28	(+/-10%)	0.28	(+/-10%)
M2	5300	(+/-10%)	0.28	(+/-10%)	0.28	(+/-10%)
M1	5300	(+/-10%)	0.23	(+/-10%)	0.23	(+/-10%)
Poly	2000	(+/-10%)	0.18	(+/-5%)	0.25	(+/-5%)

B. Dielectric layers

Dielectric Name	Thickness(A)	Variation(+/-%)(3 sigma)	Dielectric Constant
Pass2	6000(SiN)	(+/-10%)	7.9
Pass1	10000(HDP Ox)+1500(SRO)	(+/-10%)	HDP Ox 4.2/SRO 4.2
IMD5	11800(FSG)+3500(USG)	(FSG:+/-20%,USG:+/-3%)	FSG 3.7/USG 4.2
IMD4	11800(FSG)+2000(USG)	(FSG:+/-20%,USG:+/-3%)	FSG 3.7/USG 4.2
IMD3	11800(FSG)+2000(USG)	(FSG:+/-20%,USG:+/-3%)	FSG 3.7/USG 4.2
IMD2	11800(FSG)+2000(USG)	(FSG:+/-20%,USG:+/-3%)	FSG 3.7/USG 4.2
IMD1	11800(FSG)+2000(USG)	(FSG:+/-20%,USG:+/-3%)	FSG 3.7/USG 4.2
ILD1b	2000*(BPSG) + 5500(PE TEOS)	(+/-20%)	4.2
ILD1a	400(SiON)	(+/-10%)	4.3
FOX(STI)	3500	(+/-17%)	4

C. Cross section of interconnection structures



7.6 Resistance Table

For information related to 1P6M (1P4M, 1P5M) process, please refer to SMIC's PCM SPEC.
Sheet resistance table:

Type	Sheet resistance			Unit	TC1	TC2	JC1A	JC1B	JC2A	JC2B	DW (um)
	best	typical	worst								
NW_RS (STI)	795	890	1059	Ω /sq	2.73E-03	1.65E-06	1.10E-03	3.01E-07	-6.61E-09	3.16E-13	1.83E-01
NW_RS (AA)	340	441	540	Ω /sq	3.02E-03	8.06E-06	-3.89E-03	3.34E-07	-1.85E-08	2.49E-13	7.25E-02
N+_RS	4.79	7.57	9.79	Ω /sq	3.12E-03	3.022E-08	9.10E-06	6.25E-09	4.72E-08	2.79E-12	-4.14E-02
N+_RS (SAB)	36.9	57.5	78	Ω /sq	1.51E-03	4.22E-07	2.13E-04	-2.64E-09	1.75E-08	2.04E-13	-2.62E-02
N+_NSTD_RS (SAB)	36.9	57.5	78	Ω /sq	1.51E-03	4.22E-07	2.13E-04	-2.64E-09	1.75E-08	2.04E-13	-2.62E-02
P+_RS	3.12	6.75	9.12	Ω /sq	3.08E-03	7.034E-07	6.40E-05	-7.34E-09	4.40E-08	2.16E-12	-2.80E-02
P+_RS (SAB)	76.1	116.2	156.2	Ω /sq	1.41E-03	6.87E-07	-6.82E-06	-8.98E-12	9.85E-09	5.20E-14	-1.37E-03
P+_NSTD_RS (SAB)	88.9	129	169	Ω /sq	1.41E-03	6.87E-07	-6.82E-06	-8.98E-12	9.85E-09	5.20E-14	-4.90E-02
N+Poly_RS	5.53	7.87	9.53	Ω /sq	3.07E-03	-5.36E-08	-1.16E-04	1.28E-07	9.63E-08	1.98E-11	-1.89E-02
N+Poly_3T_RS	5.53	7.87	9.53	Ω /sq	3.07E-03	-5.36E-08	-1.16E-04	1.28E-07	9.63E-08	1.98E-11	-1.89E-02
N+Poly_RS (SAB)	233.5	271.6	309.7	Ω /sq	-1.35E-03	2.29E-06	8.23E-04	-4.36E-08	-1.45E-08	-2.17E-13	4.71E-02
N+Poly_3T_RS (SAB)	233.5	271.6	309.7	Ω /sq	-1.35E-03	2.29E-06	8.23E-04	-4.36E-08	-1.45E-08	-2.17E-13	4.71E-02
N+Poly_NSTD_RS (SAB)	234.9	273	311.1	Ω /sq	-1.35E-03	2.29E-06	8.23E-04	-4.36E-08	-1.45E-08	-2.17E-13	9.86E-03
N+Poly_NSTD_3T_RS (SAB)	234.9	273	311.1	Ω /sq	-1.35E-03	2.29E-06	8.23E-04	-4.36E-08	-1.45E-08	-2.17E-13	9.86E-03
P+Poly_RS	6.9	9.78	11.9	Ω /sq	2.92E-03	-2.30E-08	-4.67E-05	6.58E-08	8.88E-08	1.23E-11	-1.35E-02
P+Poly_3T_RS	6.9	9.78	11.9	Ω /sq	2.92E-03	-2.30E-08	-4.67E-05	6.58E-08	8.88E-08	1.23E-11	-1.35E-02
P+Poly_RS (SAB)	262.6	311.3	359.9	Ω /sq	-1.63E-04	7.46E-07	1.09E-04	-8.08E-09	-1.27E-09	-2.73E-14	2.73E-02
P+Poly_3T_RS (SAB)	262.6	311.3	359.9	Ω /sq	-1.63E-04	7.46E-07	1.09E-04	-8.08E-09	-1.27E-09	-2.73E-14	2.73E-02
P+Poly_NSTD_RS (SAB)	262.6	311.3	359.9	Ω /sq	-1.63E-04	7.46E-07	1.09E-04	-8.08E-09	-1.27E-09	-2.73E-14	2.73E-02
P+Poly_NSTD_3T_RS (SAB)	262.6	311.3	359.9	Ω /sq	-1.63E-04	7.46E-07	1.09E-04	-8.08E-09	-1.27E-09	-2.73E-14	2.73E-02
Metal1_RS	0.055	0.078	0.101	Ω /sq	3.49E-03	6.93E-07	---	---	---	---	-4.93E-03
Metal2_RS	0.055	0.078	0.101	Ω /sq	3.60E-03	7.60E-07	---	---	---	---	6.00E-03
Metal3_RS	0.055	0.078	0.101	Ω /sq	3.60E-03	7.60E-07	---	---	---	---	6.00E-03
Metal4_RS	0.055	0.078	0.101	Ω /sq	3.60E-03	7.60E-07	---	---	---	---	6.00E-03
Metal5_RS	0.055	0.078	0.101	Ω /sq	3.60E-03	7.60E-07	---	---	---	---	6.00E-03
Metal6_RS	0.027	0.036	0.045	Ω /sq	3.89E-03	1.01E-06	---	---	---	---	-4.41E-02
N+_RC (0.22*0.22)	1	15	30	Ohm/ct	---	---	---	---	---	---	---
P+_RC (0.22*0.22)	1	15	30	Ohm/ct	---	---	---	---	---	---	---

Type	Sheet resistance			Unit	TC1	TC2	JC1A	JC1B	JC2A	JC2B	DW (um)
	best	typical	worst								
N+Poly_RC (0.22*0.22)	1	15	30	Ohm/ct	---	---	---	---	---	---	---
P+Poly_RC (0.22*0.22)	1	15	30	Ohm/ct	---	---	---	---	---	---	---
Via1_RC (0.26*0.26)	1	4	10	Ohm/ct	---	---	---	---	---	---	---
Via2_RC (0.26*0.26)	1	4	10	Ohm/ct	---	---	---	---	---	---	---
Via3_RC (0.26*0.26)	1	4	10	Ohm/ct	---	---	---	---	---	---	---
Via4_RC (0.26*0.26)	1	4	10	Ohm/ct	---	---	---	---	---	---	---
Via5_RC (0.36*0.36)	1	2	8	Ohm/ct	---	---	---	---	---	---	---

* Standard resistors are defined for without LDD layer implanted; non-standard resistors are defined for with LDD layer implanted.

* For with SAB resistor, there are some resistors without obvious difference between non-standard and standard type, e.g., N+RS_SAB, P+Poly_SAB and P+Poly_3T_SAB.

* For without SAB resistor, there is no difference between non-standard and standard type, because the resistance is dominated by salicide.

* The square number is suggested to be larger than 5 for N+_RS(SAB), N+_NSTD_RS(SAB), P+_RS(SAB),P+_NSTD_RS(SAB), N+Poly_RS(SAB), N+Poly_NSTD_RS(SAB), N+Poly_3T_RS(SAB), N+Poly_NSTD_3T_RS(SAB), P+Poly_RS(SAB), P+Poly_NSTD_RS(SAB), P+Poly_3T_RS(SAB) and P+Poly_NSTD_3T_RS(SAB).
* N+Poly_3T_RS, P+Poly_3T_RS, N+Poly_3T_RS(SAB), N+Poly_NSTD_3T_RS(SAB), P+Poly_3T_RS(SAB),P+Poly_NSTD_3T_RS(SAB) are poly resistor for three terminal.
* N+Poly_RS, P+Poly_RS, N+Poly_RS(SAB),N+Poly_NSTD_RS(SAB), P+Poly_RS(SAB) and P+Poly_NSTD_RS(SAB) are poly resistor for two terminal.

* The resistance as a function of temperature is described by the following equation:
  $R(T) = R0 * [1 + TC1 * dT + TC2 * (dT)^2]$, where $dT = T - Tnominal$ (25°C).
  Valid temperature range: -40°C ~ 125°C.

* R0 = RSH * L / (W - 2 * DW) ; where RSH is the sheet resistance, L is the drawn length, W is the drawn width.

* The resistance as a function of terminal voltage is described by:
  $R(V) = R0 * [1 + VC1 * V + VC2 * V^2]$, where V is the voltage across the resistor.

  VC1 = Jc1a + Jc1b / L, VC2 = (Jc2a + Jc2b / L) / L, where Jc1a, Jc1b, Jc2a, and Jc2b are the current density coefficient.

The valid voltage range and recommend with of resistors model are list as following table:

Type	Valid voltage range	Recommend Width (um)
NW_RS(STI)	0V ~ 3.3V	≥1.0
NW_RS(AA)	0V ~ 3.3V	≥1.0
N+_RS	0V ~ 3.3V	------
N+_RS(SAB)	0V ~ 3.3V	≥0.5
N+_NSTD _RS (SAB)	0V ~ 3.3V	≥0.5
P+_RS	-3.3V ~ 0V	------
P+_RS(SAB)	-3.3V ~ 0V	≥0.5
P+_NSTD _RS (SAB)	-3.3V ~ 0V	≥0.5
N+Poly_RS	-3.3V ~ 3.3V	------
N+Poly_3T_RS	-3.3V ~ 3.3V	------
N+Poly_RS(SAB)	-3.3V ~ 3.3V	≥0.5
N+Poly_3T_RS (SAB)	-3.3V ~ 3.3V	≥0.5
N+Poly_NSTD _RS (SAB)	-3.3V ~ 3.3V	≥0.5
N+Poly_NSTD_3T_ RS (SAB)	-3.3V ~ 3.3V	≥0.5
P+Poly_RS	-3.3V ~ 3.3V	------
P+Poly_3T_RS	-3.3V ~ 3.3V	------
P+Poly_RS(SAB)	-3.3V ~ 3.3V	≥0.5
P+Poly_3T_RS (SAB)	-3.3V ~ 3.3V	≥0.5
P+Poly_NSTD _RS (SAB)	-3.3V ~ 3.3V	≥0.5
P+Poly_NSTD_3T_ RS (SAB)	-3.3V ~ 3.3V	≥0.5

Interface resistance table for non-silicide resistor:

Type	Rintc (Ohm)	Rint0 (Ohm-m)	Rint1 (Ohm-m^2)	RintTC1	RintTC2	RintJc1a	RintJc1b	RintJc2a	RintJc2b
N+_RS(SAB)	12.25	2.18E-05	0	1.81E-03	7.75E-07	-1.56E-03	7.95E+02	4.07E-02	2.44E+04
N+_NSTD_RS (SAB)	12.25	2.18E-05	0	1.81E-03	7.75E-07	-1.56E-03	7.95E+02	4.07E-02	2.44E+04
P+_RS(SAB)	15.446	4.37E-05	0	1.38E-03	6.47E-07	9.03E-04	-4.74E+02	1.00E-02	1.74E+04
P+_NSTD_RS (SAB)	15.446	4.37E-05	0	1.38E-03	6.47E-07	9.03E-04	-4.74E+02	1.00E-02	1.74E+04
N+Poly_RS(SAB)	23.415	9.50E-05	0	-9.76E-04	1.70E-06	1.20E-03	-9.43E+02	-4.78E-02	-8.34E+04
N+Poly_3T_RS(SAB)	23.415	9.50E-05	0	-9.76E-04	1.70E-06	1.20E-03	-9.43E+02	-4.78E-02	-8.34E+04
N+Poly_NSTD_RS (SAB)	23.415	9.50E-05	0	-9.76E-04	1.70E-06	1.20E-03	-9.43E+02	-4.78E-02	-8.34E+04
N+Poly_NSTD_3T_RS (SAB)	23.415	9.50E-05	0	-9.76E-04	1.70E-06	1.20E-03	-9.43E+02	-4.78E-02	-8.34E+04
P+Poly_RS(SAB)	29.965	1.18E-04	0	-2.76E-04	3.25E-07	2.63E-04	-2.60E+02	4.74E-03	-5.30E+04
P+Poly_3T_RS(SAB)	29.965	1.18E-04	0	-2.76E-04	3.25E-07	2.63E-04	-2.60E+02	4.74E-03	-5.30E+04
P+Poly_NSTD_RS (SAB)	29.965	1.18E-04	0	-2.76E-04	3.25E-07	2.63E-04	-2.60E+02	4.74E-03	-5.30E+04
P+Poly_NSTD_3T_RS (SAB)	29.965	1.18E-04	0	-2.76E-04	3.25E-07	2.63E-04	-2.60E+02	4.74E-03	-5.30E+04

* The interface resistance(Rint) between non-silicide and silicide is extracted as below.

Rtotal = R0 + 2 * Rint + 2 * Rc , where Rc is the contact resistance.

$$Rint = (Rintc + Rint0 / (W - 2*DW) + Rint1 / (W - 2*DW)^2) * Rinttcoef$$

$$* (1 + RintVC1 * V + RintVC2 * V^2),$$

where V is the voltage across the interface region.

$Rinttcoef = 1 + RintTC1 * dT + RintTC2 * (dT)^2$, where dT = T - Tnominal (25°C)

RintVC1 = RintJc1a + RintJc1b * (W - 2*DW)

RintVC2 = RintJc2a + RintJc2b * (W - 2*DW)

We use four-terminal structure to extract the interface resistance, the interface resistance is defined as the resistance between sense-1 and current forcing terminal, please refer to test structure in Fig7.6.2.
When design non-silicide resistor, please according to the layout of Fig7.6.2 for interface region definition.

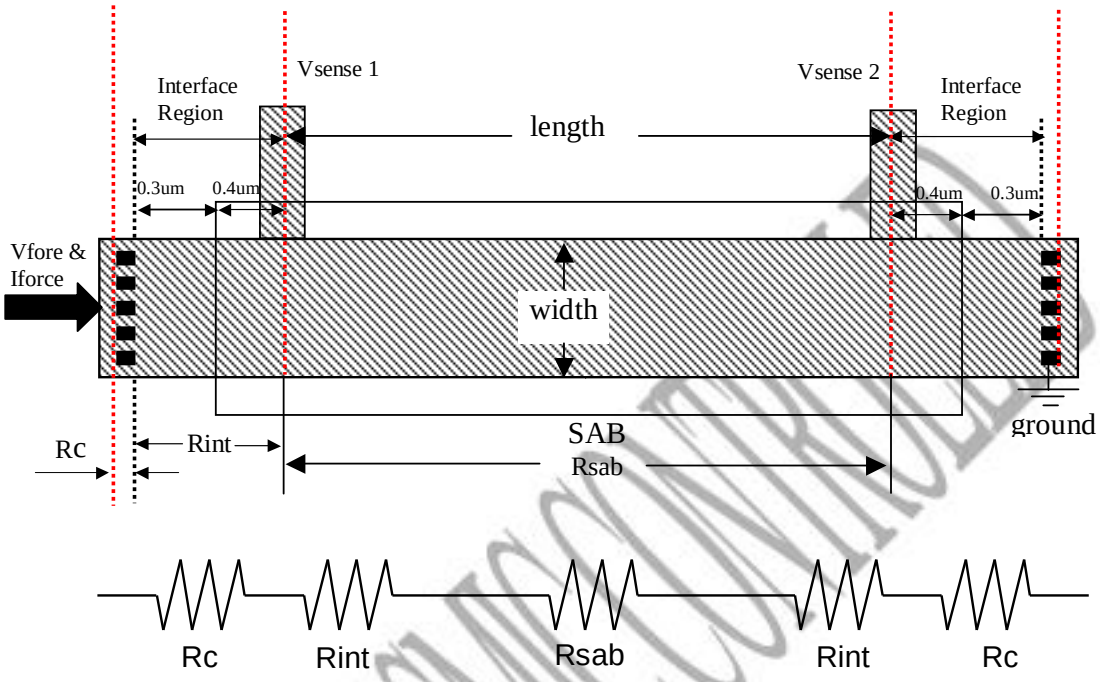


Figure 7.6.2 non-silicide resistor structure

* In order to provide more accurate parameters for resistor, the resistor macro models which include both diodes and corner cases are listed in the attachment.
(l018ll_io50_v1p3_res.ckt, l018ll_io50_v1p3. lib,
l018ll_io50_v1p3_res_spe.ckt, l018ll_io50_v1p3_spe. lib
l018ll_io50_v1p3_res_eldo.ckt, l018ll_io50_v1p3_eldo. lib)

* Note: Rc does not appear in the netlist because we have subtracted it in Rint extraction. On the other hand, Rc is a layout-dependent factor and its value varies with contact number. The designers can calculate Rc based on the resistor table and layout. Then, put it in the netlist.

7.7 MIM Capacitance Table

0.18um Low Leakage MIM Capacitor Voltage & Temperature Coefficient				
Area (um^2)	C0 (fF/um^2)	VC 1 (ppm/V)	VC 2 (ppm/V^2)	TC 1 (ppm/C)
400	0.971	-30.06	-15.41	-33.63
900		-36.39	-14.37	-32.70
1600		-33.98	-14.86	-37.00
2500		-36.00	-14.92	-35.91
Global Area		-34.11	-14.89	-34.82

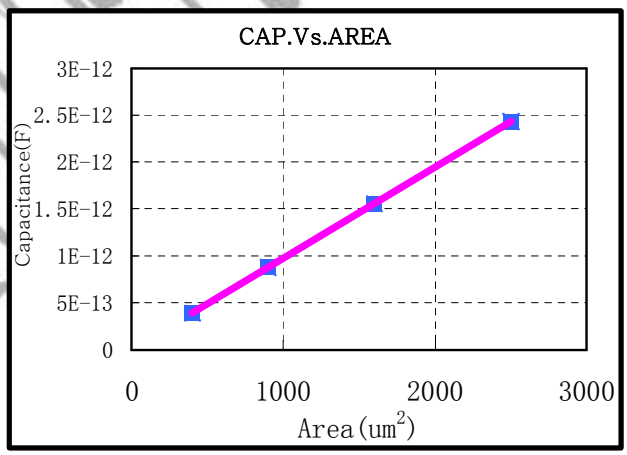
* Note: The parameters listed in the row of Global Area are used for fitting all MIM capacitors.

* The capacitance as a function of temperature is described by the following equation:
  C(T) = C0 * [1 + TC1 * dT], where dT = T - Tnominal (25°C).
  Valid temperature range: -55°C ~ 125°C.

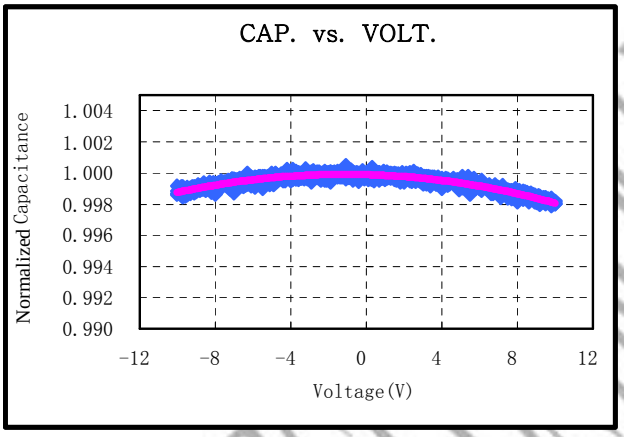
* The capacitance as a function of terminal voltage is described by:
  C(V) = C0 * [1 + VC1 * V + VC2 * V²], where V is the voltage across the capacitor.

* C0 is extracted from the scalable formula by giving area.

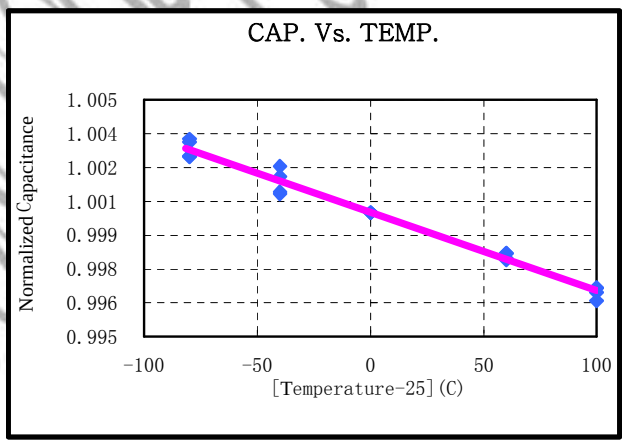
The slope of fitting line is C0 (0.971fF/um^2) in the figure.



* VC1 and VC2 are extracted from the normalized capacitance at 25C. (C0=1 at V=0)
The following figure shows the normalized capacitance versus voltage for global area, both voltage coefficients VC1= -34.11ppm/V and VC2= -14.89ppm/V^2, respectively.



* TC1 is extracted from the normalized capacitance at different temperature.(C0=1 at T=25C)
The figure below shows the normalized capacitance versus temperature for global area. The temperature coefficient TC1 is -34.82 ppm/C.



7.8 Appendix

7.8.1 MOSFET Model Parameters Description for HSPICE Level 49 (BSIM3V3.2). (Reference: UCB BSIM3V3 manual and HSPICE manual)

Parameters	Comments
LEVEL	MOSFET model level, set to 49 for HSPICE model
LMIN	Minimum channel length
LMAX	Maximum channel length
WMIN	Minimum channel width
WMAX	Maximum channel width
TNOM	Temperature at which parameters are extracted
BINUNIT	Bin unit scale selector
VTH0	Threshold voltage of long channel device at Vbs=0 and small Vds
K1	First-order body effect coefficient
K2	Second-order body effect coefficient
K3	Narrow width effect coefficient
K3B	Body effect coefficient of K3
W0	Narrow width effect coefficient
NCH	Channel doping concentration
NLX	Lateral non-uniform doping parameter along channel
XT	Doping depth
VBX	Vbs at which the depletion region width equals xt
VBI	Substrate junction built-in potential
VBM	Maximum applied body bias in Vth calculation
DVT0	First coefficient of short channel effects on Vth
DVT1	Second coefficient of short channel effects on Vth
DVT2	Body-bias coefficient of short channel effects on Vth
DVT0W	First coefficient of narrow width effects on Vth for small channel length
DVT1W	Second coefficient of narrow width effects on Vth for small channel length
DVT2W	Body-bias coefficient of narrow width effects on Vth for small channel length
A0	Bulk charge effect coefficient for channel length
A1	First non-saturation effect parameter
A2	Second non-saturation effect parameter
NSUB	Substrate doping coefficient
NGATE	Poly-Gate doping concentration
XJ	Source/Drain junction depth
LINT	Length offset fitting parameter from I-V without bias
WINT	Width offset fitting parameter from I-V without bias
WL	Coefficient of length dependence for width offset
WLN	Power of length dependence for width offset
WW	Coefficient of width dependence for width offset
WWN	Power of width dependence for width offset

LL	Coefficient of length dependence for length offset
LLN	Power of length dependence for length offset
LW	Coefficient of width dependence for length offset
LWN	Power of width dependence for length offset
LWL	Coefficient of length and width cross term for length offset
XL	The masking and etching effects of channel length
XW	The masking and etching effects of channel width
DWG	Coefficient of Weff′s gate dependence
DWB	Coefficient of Weff′s substrate bias dependence
TOX	Gate oxide thickness
TOXM	Nominal TOX at which parameter are extracted
RDSW	Width dependence of drain-source resistance
PRWB	Body effect coefficient of RDSW
PRWG	Gate bias effect coefficient of RDSW
U0	Mobility at TEMP=TNOM
VSAT	Saturation velocity at TEMP=TNOM
UA	First-order mobility degradation coefficient
UB	Second-order mobility degradation coefficient
UC	Body-effect of mobility degradation coefficient
AGS	Gate bias coefficient of Abulk
B0	Bulk charge effect coefficient for channel width
B1	Bulk charge effect width offset
KETA	Body-bias coefficient of bulk charge effect
MOBMOD	Mobility model selector
DROUT	L dependence coefficient of DIBL correction parameter in Rout
ALPHA0	The first parameter of impact ionization current
BETA0	The second parameter of impact ionization current
DELTA	Effective Vds parameter
EM	Saturation field
PCLM	Channel length modulation coefficient
PDIBLC1	First output resistance DIBL effect correction parameter
PDIBLC2	Second output resistance DIBL effect correction parameter
PDIBLCB	Body-effect coefficient of DIBL correction parameter
PSCBE1	First substrate current body-effect parameter
PSCBE2	Second substrate current body-effect parameter
PVAG	Gate dependence of early voltage
CDSC	Source/drain and channel coupling capacitance
CDSCB	Body-bias sensitivity of CDSC
CDSCD	Drain-bias sensitivity of CDSC
NFACTOR	Subthreshold swing coefficient
CIT	Interface trap capacitance
VOFF	Offset voltage in the subthreshold region at large Wand L
DSUB	DIBL coefficient exponent in the subthreshold region
ETA0	DIBL coefficient in the subthreshold region

ETAB	Body-bias coefficient for the subthreshold DIBL effect
JS	Source/drain junction saturation current per unit area
JSW	Sidewall bulk junction saturation current
N	Emission current for MOS diode
CJ	Zero-bias area junction capacitance
CJSW	Zero-bias sidewall junction capacitance by FOX side
PB	P/N junction potential
PBSW	P/N sidewall junction potential
MJ	Area junction grading coefficient
MJSW	Sidewall junction grading coefficient
CGSO	Non LDD region source-gate overlap capacitance per channel length
CGDO	Non LDD region drain-gate overlap capacitance per channel length
CGBO	Gate bulk overlap capacitance per unit channel length
CGS1	Lightly doped source-gate region overlap capacitance
CGD1	Lightly doped drain-gate region overlap capacitance
CKAPPA	Coefficient for lightly doped region overlap capacitance fringing field capacitance
CF	Fringing field capacitance
DLC	Length offset fitting parameter from C-V
DLW	Width offset fitting parameter from C-V
CAPMOD	Intrinsic charge model
NQSMOD	Flag for NQS model
XPART	Channel charge partitioning rate flag
ELM	Elmore constant of the channel
TLEV	DC temperature selector
TLEVC	AC temperature selector
KT1	Temperature coefficient for threshold voltage
KT1L	Channel length dependence of the temperature coefficient for threshold voltage
KT2	Body-bias coefficient of Vth temperature effect
AT	Temperature coefficient for VSAT
UA1	Temperature coefficient for UA
UB1	Temperature coefficient for UB
UC1	Temperature coefficient for UC
UTE	Mobility temperature exponent
PRT	Temperature coefficient for RDSW
CTA	Junction capacitance temperature coefficient
CTP	Sidewall capacitance temperature coefficient
PTA	Junction potential temperature coefficient
PTP	Junction sidewall potential temperature coefficient
XTI	Saturation current temperature exponent
ACM	Area calculation method for MOS source/drain diode ACM=2 : for lightly doped drain technology ACM=3 : Extension of ACM=2 model that deals with shared source/drain

RSH	Source/drain diffusion sheet resistance
RD	Lightly doped region's sheet resistance for drain side
RS	Lightly doped region's sheet resistance for source side
RDC	Additional drain resistance due to contact resistance
RSC	Additional source resistance due to contact resistance
GEO	GEO=0 : indicates the drain and source of the devices are not shared by other devices GEO=1 : indicates the drain is shared with another device GEO=2 : indicates the source is shared with another device GEO=3 : indicates the drain and source are shared with shared device

7.8.2 Comparison Between MOSFET Model Simulation and Measurement Results

A. 1.8V thin oxide MOS model

The measured and simulation results for Vth & Idsat at different temperatures are listed in the following tables. In order to do the comparison, some model parameters are changed so that the models are restored to their original values as they were directly extracted from raw data. Here, we restore vth0= -0.59 for 1.8V PMOS.

For thin oxide NMOS, Vth is calculated at Vds=0.05V and Ids=0.1uA*W/L, Idsat is measured and simulated at Vds=Vgs=1.8V and Vbs=0V.

For thin oxide PMOS, Vth is calculated at Vds=-0.05V and Ids=-0.1uA*W/L, Idsat is measured and simulated at Vds=Vgs=-1.8V and Vbs=0V.

NMOS 1.8V		Vth(V)@25C		Vth(V)@125C		Vth(V)@-40C	
W (um)	L (um)	Meas.	Simu.	Meas.	Simu.	Meas.	Simu.
100	10	0.566	0.571	----------	----------	----------	----------
100	0.18	0.617	0.607	----------	----------	----------	----------
10	10	0.567	0.571	0.483	0.488	0.620	0.630
10	4	0.580	0.578	0.534	0.495	0.670	0.637
10	2	0.595	0.590	0.562	0.508	0.696	0.648
10	1	0.618	0.613	0.578	0.532	0.718	0.671
10	0.5	0.645	0.650	----------	----------	----------	----------
10	0.3	0.665	0.663	----------	----------	----------	----------
10	0.2	0.627	0.626	----------	----------	----------	----------
10	0.18	0.598	0.605	0.517	0.531	0.648	0.657
4	10	0.568	0.570	0.483	0.488	0.622	0.628
4	1	0.618	0.612	0.533	0.531	0.669	0.670
4	0.5	0.647	0.648	----------	----------	----------	----------
4	0.3	0.662	0.660	----------	----------	----------	----------
4	0.18	0.617	0.603	----------	----------	----------	----------
2	10	0.567	0.568	0.483	0.486	0.620	0.626
2	1	0.610	0.609	0.526	0.529	0.662	0.667
2	0.5	0.637	0.645	----------	----------	----------	----------
2	0.3	0.659	0.657	----------	----------	----------	----------
2	0.18	0.611	0.599	----------	----------	----------	----------
1	10	0.560	0.563	0.477	0.482	0.613	0.622
1	1	0.601	0.604	0.518	0.524	0.653	0.662
1	0.5	0.631	0.639	0.546	0.559	0.682	0.696
1	0.3	0.641	0.649	0.553	0.572	0.693	0.705
1	0.18	0.604	0.593	0.518	0.518	0.659	0.645
0.5	10	0.548	0.553	0.466	0.473	0.601	0.611
0.5	0.3	0.620	0.634	----------	----------	----------	----------
0.5	0.18	0.590	0.579	0.504	0.503	0.644	0.633
0.3	10	0.536	0.537	0.452	0.457	0.589	0.594
0.3	0.3	0.601	0.614	0.514	0.535	0.655	0.671
0.22	10	0.521	0.522	0.439	0.442	0.573	0.579
0.22	1	0.560	0.559	0.476	0.479	0.614	0.616
0.22	0.3	0.600	0.598	0.515	0.518	0.656	0.655
0.22	0.18	0.548	0.551	0.461	0.473	0.602	0.606

NMOS 1.8V		Idsat(A)@25C		Idsat(A)@125C		Idsat(A)@-40C	
W (um)	L (um)	Meas.	Simu.	Meas.	Simu.	Meas.	Simu.
100	10	1.31E-03	1.33E-03	----------	----------	----------	----------
100	0.18	4.48E-02	4.76E-02	----------	----------	----------	----------
10	10	1.31E-04	1.33E-04	9.10E-05	9.86E-05	1.74E-04	1.74E-04
10	4	3.27E-04	3.22E-04	2.29E-04	2.40E-04	4.20E-04	4.18E-04
10	2	6.38E-04	6.11E-04	4.54E-04	4.59E-04	8.02E-04	7.83E-04
10	1	1.19E-03	1.11E-03	8.72E-04	8.50E-04	1.45E-03	1.39E-03
10	0.5	2.06E-03	1.93E-03	----------	----------	----------	----------
10	0.3	3.07E-03	2.96E-03	----------	----------	----------	----------
10	0.2	4.58E-03	4.54E-03	----------	----------	----------	----------
10	0.18	5.23E-03	5.18E-03	4.52E-03	4.43E-03	5.75E-03	5.71E-03
4	10	5.11E-05	5.28E-05	3.60E-05	3.92E-05	6.78E-05	6.89E-05
4	1	4.70E-04	4.42E-04	3.47E-04	3.39E-04	5.69E-04	5.55E-04
4	0.5	8.21E-04	7.70E-04	----------	----------	----------	----------
4	0.3	1.25E-03	1.19E-03	----------	----------	----------	----------
4	0.18	2.02E-03	2.09E-03	----------	----------	----------	----------
2	10	2.51E-05	2.60E-05	1.79E-05	1.94E-05	3.32E-05	3.40E-05
2	1	2.34E-04	2.19E-04	1.73E-04	1.68E-04	2.86E-04	2.75E-04
2	0.5	4.12E-04	3.84E-04	----------	----------	----------	----------
2	0.3	6.17E-04	5.95E-04	----------	----------	----------	----------
2	0.18	1.05E-03	1.06E-03	----------	----------	----------	----------
1	10	1.24E-05	1.27E-05	8.80E-06	9.50E-06	1.63E-05	1.65E-05
1	1	1.18E-04	1.08E-04	8.71E-05	8.32E-05	1.44E-04	1.35E-04
1	0.5	2.10E-04	1.91E-04	1.67E-04	1.51E-04	2.47E-04	2.31E-04
1	0.3	3.25E-04	2.99E-04	2.67E-04	2.45E-04	3.66E-04	3.48E-04
1	0.18	5.29E-04	5.39E-04	4.60E-04	4.62E-04	5.80E-04	5.94E-04
0.5	10	6.36E-06	6.20E-06	4.57E-06	4.68E-06	8.34E-06	8.02E-06
0.5	0.3	1.69E-04	1.55E-04	----------	----------	----------	----------
0.5	0.18	2.77E-04	2.84E-04	2.42E-04	2.45E-04	3.03E-04	3.12E-04
0.3	10	3.94E-06	3.75E-06	2.85E-06	2.87E-06	5.14E-06	4.81E-06
0.3	0.3	1.11E-04	9.99E-05	9.02E-05	8.28E-05	1.25E-04	1.15E-04
0.22	10	2.87E-06	2.89E-06	2.09E-06	2.23E-06	3.73E-06	3.68E-06
0.22	1	2.87E-05	2.60E-05	2.16E-05	2.05E-05	3.53E-05	3.20E-05
0.22	0.3	8.44E-05	8.03E-05	7.09E-05	6.68E-05	9.46E-05	9.25E-05
0.22	0.18	1.53E-04	1.51E-04	1.33E-04	1.31E-04	1.67E-04	1.66E-04

PMOS 1.8V		Vth(V)@25C		Vth(V)@125C		Vth(V)@-40C	
W (um)	L (um)	Meas.	Simu.	Meas.	Simu.	Meas.	Simu.
100	10	0.619	0.619	----------	----------	----------	----------
100	0.18	0.588	0.587	----------	----------	----------	----------
10	10	0.624	0.618	0.542	0.546	0.675	0.670
10	4	0.620	0.620	0.546	0.547	0.680	0.671
10	2	0.629	0.623	0.548	0.549	0.682	0.674
10	1	0.630	0.627	0.544	0.553	0.679	0.678
10	0.5	0.627	0.627	----------	----------	----------	----------
10	0.3	0.619	0.617	----------	----------	----------	----------
10	0.2	0.599	0.595	----------	----------	----------	----------
10	0.18	0.592	0.586	0.500	0.499	0.649	0.647
4	10	0.619	0.617	0.539	0.545	0.670	0.668
4	1	0.628	0.625	0.493	0.552	0.640	0.677
4	0.5	0.623	0.626	----------	----------	----------	----------
4	0.3	0.612	0.616	----------	----------	----------	----------
4	0.18	0.583	0.586	----------	----------	----------	----------
2	10	0.611	0.615	0.533	0.543	0.661	0.666
2	1	0.622	0.624	0.511	0.550	0.659	0.675
2	0.5	0.620	0.624	----------	----------	----------	----------
2	0.3	0.602	0.614	----------	----------	----------	----------
2	0.18	0.601	0.585	----------	----------	----------	----------
1	10	0.612	0.611	0.534	0.540	0.661	0.661
1	1	0.616	0.620	0.537	0.548	0.665	0.671
1	0.5	0.609	0.621	0.532	0.547	0.658	0.673
1	0.3	0.598	0.611	0.518	0.536	0.648	0.665
1	0.18	0.576	0.583	0.489	0.496	0.631	0.643
0.5	10	0.599	0.604	0.523	0.536	0.648	0.653
0.5	0.3	0.588	0.604	----------	----------	----------	----------
0.5	0.18	0.586	0.576	0.502	0.489	0.639	0.637
0.3	10	0.591	0.597	0.514	0.531	0.639	0.645
0.3	0.3	0.576	0.596	0.497	0.523	0.626	0.648
0.22	10	0.592	0.594	0.516	0.529	0.639	0.640
0.22	1	0.591	0.600	0.516	0.534	0.637	0.648
0.22	0.3	0.581	0.589	0.498	0.514	0.632	0.642
0.22	0.18	0.550	0.554	0.457	0.463	0.608	0.618

PMOS18		Idsat(A)@25C		Idsat(A)@125C		Idsat(A)@-40C	
W (um)	L (um)	Meas.	Simu.	Meas.	Simu.	Meas.	Simu.
100	10	2.82E-04	2.73E-04	----------	----------	----------	----------
100	0.18	1.85E-02	1.81E-02	----------	----------	----------	----------
10	10	2.75E-05	2.75E-05	2.38E-05	2.44E-05	3.10E-05	3.19E-05
10	4	6.79E-05	6.84E-05	5.99E-05	6.06E-05	7.54E-05	7.89E-05
10	2	1.31E-04	1.35E-04	1.16E-04	1.20E-04	1.43E-04	1.56E-04
10	1	2.60E-04	2.67E-04	2.32E-04	2.38E-04	2.80E-04	3.05E-04
10	0.5	5.42E-04	5.33E-04	----------	----------	----------	----------
10	0.3	9.83E-04	9.35E-04	----------	----------	----------	----------
10	0.2	1.65E-03	1.60E-03	----------	----------	----------	----------
10	0.18	1.90E-03	1.90E-03	1.77E-03	1.79E-03	1.99E-03	2.03E-03
4	10	1.10E-05	1.11E-05	9.52E-06	9.84E-06	1.24E-05	1.29E-05
4	1	1.03E-04	1.08E-04	9.22E-05	9.60E-05	1.11E-04	1.24E-04
4	0.5	2.15E-04	2.15E-04	----------	----------	----------	----------
4	0.3	3.88E-04	3.77E-04	----------	----------	----------	----------
4	0.18	7.62E-04	7.61E-04	----------	----------	----------	----------
2	10	5.57E-06	5.68E-06	4.82E-06	5.00E-06	6.27E-06	6.60E-06
2	1	5.22E-05	5.49E-05	4.72E-05	4.86E-05	5.74E-05	6.30E-05
2	0.5	1.08E-04	1.09E-04	----------	----------	----------	----------
2	0.3	1.95E-04	1.90E-04	----------	----------	----------	----------
2	0.18	3.52E-04	3.81E-04	----------	----------	----------	----------
1	10	2.83E-06	2.95E-06	2.44E-06	2.57E-06	3.19E-06	3.45E-06
1	1	2.71E-05	2.84E-05	2.40E-05	2.50E-05	2.99E-05	3.28E-05
1	0.5	5.54E-05	5.63E-05	4.96E-05	5.00E-05	6.02E-05	6.42E-05
1	0.3	9.86E-05	9.76E-05	8.99E-05	8.79E-05	1.05E-04	1.09E-04
1	0.18	1.86E-04	1.93E-04	1.73E-04	1.81E-04	1.94E-04	2.06E-04
0.5	10	1.57E-06	1.59E-06	1.33E-06	1.37E-06	1.80E-06	1.88E-06
0.5	0.3	5.41E-05	5.21E-05	----------	----------	----------	----------
0.5	0.18	9.57E-05	1.01E-04	8.95E-05	9.48E-05	1.16E-04	1.08E-04
0.3	10	1.04E-06	1.05E-06	8.69E-07	8.85E-07	1.21E-06	1.25E-06
0.3	0.3	3.62E-05	3.52E-05	3.23E-05	3.09E-05	3.96E-05	3.98E-05
0.22	10	8.36E-07	8.40E-07	6.82E-07	6.94E-07	9.98E-07	1.01E-06
0.22	1	7.79E-06	8.20E-06	6.57E-06	6.88E-06	9.07E-06	9.72E-06
0.22	0.3	2.87E-05	2.93E-05	2.55E-05	2.55E-05	3.17E-05	3.32E-05
0.22	0.18	5.87E-05	5.82E-05	5.42E-05	5.44E-05	6.16E-05	6.16E-05

B. 5V thick oxide MOS model

The measured and simulation results for Vth & Idsat at different temperatures are listed in the following tables. We use the mean value of WAT mapping data as the measured results. For thick oxide NMOS, Vth is calculated at Vds=0.1V, Vgs=5V and MaxGm. Idsat is measured and simulated at Vds=Vgs=5V and Vbs=0V. For thick oxide PMOS, Vth is calculated at Vds=-0.1V, Vgs=-5V and MaxGm. Idsat is measured and simulated at Vds=Vgs=-5V and Vbs=0V.

NMOS 5V		Vth(V)@25C		Vth(V)@125C		Vth(V)@-40C	
W (um)	L (um)	Meas.	Simu.	Meas.	Simu.	Meas.	Simu.
100	10	0.735	0.748	0.609	0.599	0.838	0.849
10	10	0.744	0.744	0.61	0.596	0.843	0.845
10	4	0.759	0.755	0.623	0.607	0.838	0.856
10	2	0.782	0.776	0.646	0.625	0.857	0.877
10	1	0.816	0.818	0.688	0.674	0.897	0.92
10	0.7	0.84	0.836	------	------	------	------
10	0.6	0.847	0.833	------	------	------	------
10	0.5	0.815	0.814	0.681	0.664	0.941	0.918
6	0.5	0.804	0.807	------	------	------	------
4	10	0.741	0.737	------	------	------	------
4	1	0.808	0.809	0.675	0.666	0.89	0.909
4	0.5	0.807	0.799	------	------	------	------
3	0.5	0.797	0.791	------	------	------	------
2	1	0.786	0.792	0.658	0.644	0.868	0.89
1	10	0.711	0.698	------	------	------	------
1	2	0.729	0.722	------	------	------	------
1	1	0.757	0.752	------	------	------	------
1	0.7	0.774	0.763	------	------	------	------
1	0.5	0.748	0.733	0.611	0.604	0.815	0.824
0.7	10	0.694	0.679	------	------	------	------
0.7	1	0.726	0.73	------	------	------	------
0.7	0.5	0.718	0.703	------	------	------	------
0.5	10	0.672	0.655	0.542	0.522	0.756	0.746
0.5	0.7	0.709	0.708	------	------	------	------
0.5	0.55	0.683	0.686	------	------	------	------
0.5	0.5	0.684	0.66	------	------	------	------
0.32	10	0.625	0.61	------	------	------	------
0.32	0.5	0.626	0.604	------	------	------	------
0.3	10	0.619	0.603	0.5	0.486	0.705	0.688
0.3	1	0.635	0.64	------	------	------	------
0.3	0.7	0.647	0.642	------	------	------	------
0.3	0.55	0.634	0.616	------	------	------	------
0.24	10	0.581	0.58	------	------	------	------
0.24	1	0.61	0.615	------	------	------	------
0.22	10	0.568	0.571	0.446	0.45	0.645	0.651
0.22	4	0.572	0.574	0.45	0.464	0.65	0.648
0.22	2	0.576	0.583	------	------	------	------
0.22	0.7	0.59	0.604	------	------	------	------
0.22	0.5	0.552	0.547	0.466	0.464	0.627	0.596

NMOS 5V		Idsat(A)@25C		Idsat(A)@125C		Idsat(A)@-40C	
W (um)	L (um)	Meas.	Simu.	Meas.	Simu.	Meas.	Simu.
100	10	6.55E-03	6.56E-03	4.20E-03	4.48E-03	9.29E-03	8.96E-03
10	10	6.61E-04	6.58E-04	4.25E-04	4.49E-04	9.38E-04	8.99E-04
10	4	1.54E-03	1.50E-03	1.03E-03	1.06E-03	1.99E-03	1.98E-03
10	2	2.67E-03	2.63E-03	1.94E-03	1.93E-03	3.26E-03	3.30E-03
10	1	4.15E-03	4.19E-03	3.29E-03	3.30E-03	4.82E-03	4.93E-03
10	0.7	5.09E-03	5.15E-03	------	------	------	------
10	0.6	5.57E-03	5.61E-03	------	------	------	------
10	0.5	6.22E-03	6.20E-03	5.38E-03	5.27E-03	7.00E-03	6.86E-03
6	0.5	3.80E-03	3.74E-03	------	------	------	------
4	10	2.59E-04	2.63E-04	------	------	------	------
4	1	1.69E-03	1.68E-03	1.33E-03	1.32E-03	1.94E-03	1.99E-03
4	0.5	2.55E-03	2.51E-03	------	------	------	------
3	0.5	1.95E-03	1.89E-03	------	------	------	------
2	1	8.59E-04	8.50E-04	6.78E-04	6.68E-04	9.85E-04	1.00E-03
1	10	6.35E-05	6.58E-05	------	------	------	------
1	2	2.74E-04	2.68E-04	------	------	------	------
1	1	4.43E-04	4.34E-04	------	------	------	------
1	0.7	5.47E-04	5.41E-04	------	------	------	------
1	0.5	6.83E-04	6.60E-04	5.86E-04	5.60E-04	7.56E-04	7.30E-04
0.7	10	4.48E-05	4.64E-05	------	------	------	------
0.7	1	3.19E-04	3.11E-04	------	------	------	------
0.7	0.5	4.97E-04	4.78E-04	------	------	------	------
0.5	10	3.34E-05	3.38E-05	2.27E-05	2.35E-05	4.59E-05	4.54E-05
0.5	0.7	3.00E-04	2.90E-04	------	------	------	------
0.5	0.55	3.30E-04	3.37E-04	------	------	------	------
0.5	0.5	3.68E-04	3.58E-04	------	------	------	------
0.32	10	2.28E-05	2.29E-05	------	------	------	------
0.32	0.5	2.64E-04	2.56E-04	------	------	------	------
0.3	10	2.18E-05	2.18E-05	1.47E-05	1.54E-05	2.92E-05	2.90E-05
0.3	1	1.58E-04	1.53E-04	------	------	------	------
0.3	0.7	1.97E-04	1.95E-04	------	------	------	------
0.3	0.55	2.32E-04	2.30E-04	------	------	------	------
0.24	10	1.84E-05	1.85E-05	------	------	------	------
0.24	1	1.33E-04	1.33E-04	------	------	------	------
0.22	10	1.73E-05	1.75E-05	1.20E-05	1.25E-05	2.36E-05	2.32E-05
0.22	4	4.18E-05	4.12E-05	2.98E-05	2.98E-05	5.43E-05	5.32E-05
0.22	2	7.60E-05	7.46E-05	------	------	------	------
0.22	0.7	1.59E-04	1.62E-04	------	------	------	------
0.22	0.5	2.01E-04	2.05E-04	1.74E-04	1.72E-04	2.25E-04	2.27E-04

PMOS 5V		Vth(V)@25C		Vth(V)@125C		Vth(V)@-40C	
W (um)	L (um)	Meas.	Simu.	Meas.	Simu.	Meas.	Simu.
100	10	0.838	0.838	0.699	0.704	0.917	0.933
10	10	0.839	0.834	0.699	0.701	0.918	0.928
10	4	0.849	0.839	0.709	0.705	0.93	0.934
10	2	0.861	0.847	0.718	0.712	0.942	0.943
10	1	0.875	0.872	0.734	0.735	0.964	0.962
10	0.7	0.88	0.882	------	------	------	------
10	0.6	0.88	0.882	------	------	------	------
10	0.5	0.873	0.865	0.736	0.723	0.984	0.968
6	0.5	0.864	0.862	------	------	------	------
4	10	0.832	0.829	------	------	------	------
4	1	0.86	0.866	0.716	0.729	0.943	0.956
4	0.5	0.858	0.857	------	------	------	------
3	0.5	0.849	0.85	------	------	------	------
2	1	0.839	0.848	0.699	0.713	0.918	0.944
1	10	0.802	0.805	------	------	------	------
1	2	0.812	0.817	------	------	------	------
1	1	0.81	0.824	------	------	------	------
1	0.7	0.806	0.82	------	------	------	------
1	0.5	0.797	0.795	0.65	0.653	0.874	0.885
0.7	10	0.792	0.795	------	------	------	------
0.7	1	0.795	0.803	------	------	------	------
0.7	0.5	0.774	0.762	------	------	------	------
0.5	10	0.784	0.784	0.66	0.665	0.857	0.866
0.5	0.7	0.767	0.772	------	------	------	------
0.5	0.55	0.745	0.751	------	------	------	------
0.5	0.5	0.745	0.742	------	------	------	------
0.32	10	0.776	0.768	------	------	------	------
0.32	0.5	0.732	0.717	------	------	------	------
0.3	10	0.773	0.766	0.663	0.662	0.854	0.84
0.3	1	0.76	0.74	------	------	------	------
0.3	0.7	0.748	0.73	------	------	------	------
0.3	0.55	0.715	0.721	------	------	------	------
0.24	10	0.767	0.761	------	------	------	------
0.24	1	0.734	0.725	------	------	------	------
0.22	10	0.77	0.759	0.642	0.662	0.827	0.823
0.22	4	0.769	0.75	0.644	0.652	0.827	0.815
0.22	2	0.755	0.731	------	------	------	------
0.22	0.7	0.73	0.718	------	------	------	------
0.22	0.5	0.71	0.701	0.586	0.571	0.791	0.791

PMOS 5V		Idsat(A)@25C		Idsat(A)@125C		Idsat(A)@-40C	
W (um)	L (um)	Meas.	Simu.	Meas.	Simu.	Meas.	Simu.
100	10	1.28E-03	1.26E-03	9.96E-04	1.04E-03	1.58E-03	1.54E-03
10	10	1.27E-04	1.27E-04	9.91E-05	1.05E-04	1.56E-04	1.56E-04
10	4	3.14E-04	3.15E-04	2.49E-04	2.61E-04	3.78E-04	3.84E-04
10	2	6.21E-04	6.22E-04	5.06E-04	5.21E-04	7.32E-04	7.49E-04
10	1	1.23E-03	1.24E-03	1.06E-03	1.05E-03	1.43E-03	1.45E-03
10	0.7	1.81E-03	1.79E-03	------	------	------	------
10	0.6	2.13E-03	2.13E-03	------	------	------	------
10	0.5	2.66E-03	2.65E-03	2.38E-03	2.37E-03	2.93E-03	2.94E-03
6	0.5	1.60E-03	1.60E-03	------	------	------	------
4	10	5.05E-05	5.18E-05	------	------	------	------
4	1	5.03E-04	5.01E-04	4.26E-04	4.28E-04	5.74E-04	5.88E-04
4	0.5	1.06E-03	1.08E-03	------	------	------	------
3	0.5	8.00E-04	8.13E-04	------	------	------	------
2	1	2.56E-04	2.57E-04	2.17E-04	2.19E-04	2.93E-04	3.02E-04
1	10	1.37E-05	1.41E-05	------	------	------	------
1	2	6.82E-05	6.86E-05	------	------	------	------
1	1	1.36E-04	1.36E-04	------	------	------	------
1	0.7	1.94E-04	1.97E-04	------	------	------	------
1	0.5	2.80E-04	2.89E-04	2.55E-04	2.57E-04	3.12E-04	3.19E-04
0.7	10	1.01E-05	1.04E-05	------	------	------	------
0.7	1	1.02E-04	9.98E-05	------	------	------	------
0.7	0.5	2.09E-04	2.11E-04	------	------	------	------
0.5	10	7.98E-06	7.93E-06	6.09E-06	6.34E-06	1.01E-05	9.93E-06
0.5	0.7	1.13E-04	1.09E-04	------	------	------	------
0.5	0.55	1.40E-04	1.42E-04	------	------	------	------
0.5	0.5	1.59E-04	1.58E-04	------	------	------	------
0.32	10	6.00E-06	5.85E-06	------	------	------	------
0.32	0.5	1.14E-04	1.12E-04	------	------	------	------
0.3	10	5.74E-06	5.64E-06	4.35E-06	4.38E-06	7.44E-06	7.17E-06
0.3	1	5.53E-05	5.37E-05	------	------	------	------
0.3	0.7	7.78E-05	7.61E-05	------	------	------	------
0.3	0.55	9.45E-05	9.73E-05	------	------	------	------
0.24	10	5.06E-06	5.08E-06	------	------	------	------
0.24	1	4.81E-05	4.82E-05	------	------	------	------
0.22	10	4.86E-06	4.94E-06	3.63E-06	3.72E-06	6.44E-06	6.39E-06
0.22	4	1.20E-05	1.22E-05	9.20E-06	9.27E-06	1.57E-05	1.56E-05
0.22	2	2.38E-05	2.41E-05	------	------	------	------
0.22	0.7	6.35E-05	6.56E-05	------	------	------	------
0.22	0.5	8.84E-05	9.04E-05	8.02E-05	7.94E-05	9.94E-05	9.53E-05

7.8.3 Comparison Between MOSFET Model Simulation and PCM spec

In this section, simulations for five corner cases using the corner model table are compared to the PCM corner spec.

A. Comparison on NMOS & PMOS PCM spec with typical case simulation results

1.8V thin oxide MOS

Parameters	Unit	PCM spec.	Simulated Result
VTH_N(10/0.18)	V	0.6	0.605
ISAT_N(10/0.18)	mA	5.00	5.18
VTH_P(10/0.18)	V	-0.61	-0.628
ISAT_P(10/0.18)	mA	-1.80	-1.79

5V thick oxide MOS

Parameters	Unit	PCM spec.	Simulated Result
VTH_N(10/0.5)	V	0.82	0.817
ISAT_N(10/0.5)	mA	6	6.20
VTH_P(10/0.5)	V	-0.86	-0.875
ISAT_P(10/0.5)	mA	-2.6	-2.65

B. Comparison of the lower bound PCM spec for both N & PMOS with slow N slow P corner case simulation

1.8V thin oxide MOS

Parameters	Unit	PCM spec.	Simulated Result
VTH_N(10/0.18)	V	0.7	0.696
ISAT_N(10/0.18)	mA	4.10	4.23
VTH_P(10/0.18)	V	-0.71	-0.705
ISAT_P(10/0.18)	mA	-1.2	-1.42

5V thick oxide MOS

Parameters	Unit	PCM spec.	Simulated Result
VTH_N(10/0.5)	V	0.92	0.914
ISAT_N(10/0.5)	mA	5	5.53
VTH_P(10/0.5)	V	-0.96	-0.971
ISAT_P(10/0.5)	mA	-2.1	-2.18

C. Comparison of the upper bound PCM spec for both N & PMOS with fast N fast P corner case simulation

1.8V thin oxide MOS

Parameters	Unit	PCM spec.	Simulated Result
VTH_N(10/0.18)	V	0.5	0.51
ISAT_N(10/0.18)	mA	5.90	6.29
VTH_P(10/0.18)	V	-0.51	-0.545
ISAT_P(10/0.18)	mA	-2.40	-2.26

5V thick oxide MOS

Parameters	Unit	PCM spec.	Simulated Result
VTH_N(10/0.5)	V	0.72	0.71
ISAT_N(10/0.5)	mA	7	6.97
VTH_P(10/0.5)	V	-0.76	-0.771
ISAT_P(10/0.5)	mA	-3.1	-3.3

D. Comparison on the lower bound NMOS, upper bound PMOS PCM spec with SNFP (slow N fast P) corner case simulation

1.8V thin oxide MOS

Parameters	Unit	PCM spec.	Simulated Result
VTH_N(10/0.18)	V	0.7	0.674
ISAT_N(10/0.18)	mA	4.10	4.44
VTH_P(10/0.18)	V	-0.51	-0.571
ISAT_P(10/0.18)	mA	-2.40	-2.16

5V thick oxide MOS

Parameters	Unit	PCM spec.	Simulated Result
VTH_N(10/0.5)	V	0.92	0.873
ISAT_N(10/0.5)	mA	5	5.76
VTH_P(10/0.5)	V	-0.76	-0.81
ISAT_P(10/0.5)	mA	-3.1	-3.17

E. Comparison of the upper bound NMOS and lower bound PMOS PCM spec with FNSP (fast N slow P) corner case simulation

1.8V thin oxide MOS

Parameters	Unit	PCM spec.	Simulated Result
VTH_N(10/0.18)	V	0.5	0.533
ISAT_N(10/0.18)	mA	5.90	6.03
VTH_P(10/0.18)	V	-0.71	-0.681
ISAT_P(10/0.18)	mA	-1.20	-1.50

5V thick oxide MOS

Parameters	Unit	PCM spec.	Simulated Result
VTH_N(10/0.5)	V	0.72	0.749
ISAT_N(10/0.5)	mA	7	6.69
VTH_P(10/0.5)	V	-0.96	-0.932
ISAT_P(10/0.5)	mA	-2.1	-2.27

7.8.4 Worst-Case Simulation Results of Inverter, NAND and NOR Ring-Oscillator

In the corner simulation, the effective areas and peripheries follow the minimum design rules. For 1.8V device, the W/L of NMOS and PMOS are 4/0.18 and 6/0.18 respectively. The model used in the section is centering model. Here, we don't use AS, AD PS and PD in the netlist for simulation.

1.8V Inverter ring-oscillator: (Vdd=1.8V, unit=ps/gate)

Temp	F.O.	TT	SS	FNSP	SNFP	FF
25C	1	36.09	46.01	37.13	35.07	28.17
125C	1	40.81	52.23	41.78	39.73	31.64
-40C	1	32.56	41.23	33.55	31.66	25.65
25C	3	71.16	90.34	73.44	68.98	55.75
125C	3	80.05	101.98	82.18	77.73	62.27
-40C	3	64.52	81.32	66.68	62.57	51.04

1.8V NAND ring-oscillator: (Vdd=1.8V, unit=ps/gate)

Temp	F.O.	TT	SS	FNSP	SNFP	FF
25C	1	56.73	72.05	55.78	57.95	44.54
125C	1	66.79	85.35	65.35	68.25	51.90
-40C	1	49.91	62.82	49.24	50.92	39.65
25C	3	133.60	168.99	131.31	137.14	105.18
125C	3	156.65	199.50	153.05	161.04	122.09
-40C	3	117.84	147.66	116.32	120.71	93.93

1.8V NOR ring-oscillator: (Vdd=1.8V, unit=ps/gate)

Temp	F.O.	TT	SS	FNSP	SNFP	FF
25C	1	82.03	106.22	88.04	76.03	62.54
125C	1	91.03	118.23	97.21	84.48	69.02
-40C	1	74.31	95.64	79.83	69.03	57.19
25C	3	195.60	253.44	212.91	179.19	149.35
125C	3	216.95	280.69	234.33	198.32	163.99
-40C	3	177.75	230.05	193.10	163.56	136.97

7.8.5 Model fitting and QA results

Due to the size limitation of the document, all the fitting plots for 0.18um Low Leakage 1P6M Salicide 1.8V/5V SPICE Model are given in five attachments named "l018ll_io50_fit_A.doc", "l018ll_io50_fit_B. doc", "l018ll_io50_fit_C. doc", "l018ll_io50_fit_D. doc", "l018ll_io50_fit_E. doc" and "l018ll_io50_fit_F. doc". They are described in six sections (section A, B, C, D, E and F). In the plots, L = Ldrawn + XL; W= Wdrawn +XW.

	Lot number	Wafer number	Description
Section A	BT0321 AT0812	#5 (1.8V) #23 (5V)	Comparison between measurement and simulation results for MOS I-V and C-V
Section B	AT0391	#22	Comparison between measurement and simulation results for vertical PNP bipolar I-V
Section C	AT0391 AT0812	#22 (1.8V) #23 (5V)	Comparison between measurement and simulation results for junction diode I-V and C-V
Section D	AT0348	#4	Comparison between measurement and simulation results for resistors
Section E			Model Comparison between Version 0.1 and Version 1.3
Section F	BT0321 AT0812	#5 (1.8V) #23 (5V)	Comparison between measurement and simulation results for 1/f Noise

A. Comparison between measurement and simulation results (for MOS IV&CV)

Fig.A85 Fitting ID_VD&VG, subthreshold and gds of 5V PMOS W/L=10/0.5 at temp=25C
Fig.A86 Fitting ID_VD&VG, subthreshold and gds of 5V PMOS W/L=10/0.5 at temp=125C
Fig.A87 Fitting ID_VD&VG, subthreshold and gds of 5V PMOS W/L=10/0.5 at temp=-40C
Fig.A88 Fitting ID_VD&VG, subthreshold and gds of 5V PMOS W/L=0.22/0.5 at temp=25C
Fig.A89 Fitting ID_VD&VG, subthreshold and gds of 5V PMOS W/L=0.22/0.5 at temp=125C
Fig.A90 Fitting ID_VD&VG, subthreshold and gds of 5V PMOS W/L=0.22/0.5 at temp=-40

B. Comparison between measurement and simulation results (for Bipolar IV)

Fig.B1 Fitting results of 1.8V vertical PNP(10X10) bipolar model at temp=25C
Fig.B2 Fitting results of 1.8V vertical PNP(10X10) bipolar model at temp=125C
Fig.B3 Fitting results of 1.8V vertical PNP(10X10) bipolar model at temp=-40C
Fig.B4 Fitting results of 1.8V vertical PNP(5X5) bipolar model at temp=25C
Fig.B5 Fitting results of 1.8V vertical PNP(5X5) bipolar model at temp=125C
Fig.B6 Fitting results of 1.8V vertical PNP(5X5) bipolar model at temp=-40C
Fig.B7 Fitting results of 1.8V vertical PNP(2X2) bipolar model at temp=25C
Fig.B8 Fitting results of 1.8V vertical PNP(2X2) bipolar model at temp=125C
Fig.B9 Fitting results of 1.8V vertical PNP(2X2) bipolar model at temp=-40C

C. Comparison between measurement and simulation result (for junction diode IV&CV)

Fig.C1 Fitting results of 1.8V N+/Pwell diode CV model at temp=25C
Fig.C2 Fitting results of 1.8V N+/Pwell diode CV model at temp=125C
Fig.C3 Fitting results of 1.8V N+/Pwell diode CV model at temp=-40C
Fig.C4 Fitting results of 1.8V NMOS Cjgate at temp=25C
Fig.C5 Fitting results of 1.8V P+/Nwell diode CV model at temp=25C
Fig.C6 Fitting results of 1.8V P+/Nwell diode CV model at temp=125C
Fig.C7 Fitting results of 1.8V P+/Nwell diode CV model at temp=-40C
Fig.C8 Fitting results of 1.8V PMOS Cjgate at temp=25C
Fig.C9 Fitting results of 5V N+/Pwell diode CV model at temp=25C
Fig.C10 Fitting results of 5V N+/Pwell diode CV model at temp=125C
Fig.C11 Fitting results of 5V N+/Pwell diode CV model at temp= -40C
Fig.C12 Fitting results of 5V NMOS Cjgate at temp=25C
Fig.C13 Fitting results of 5V P+/Nwell diode CV model at temp=25C
Fig.C14 Fitting results of 5V P+/Nwell diode CV model at temp=125C
Fig.C15 Fitting results of 5V P+/Nwell diode CV model at temp= -40C
Fig.C16 Fitting results of 5V PMOS Cjgate at temp=25C
Fig.C17 Fitting results of Nwell/Psub diode CV model at temp=25C
Fig.C18 Fitting results of Nwell/Psub diode CV model at temp=125C
Fig.C19 Fitting results of 1.8V N+/Pwell diode IV model at temp=25C
Fig.C20 Fitting results of 1.8V N+/Pwell diode IV model at temp=125C
Fig.C21 Fitting results of 1.8V N+/Pwell diode IV model at temp=-40C
Fig.C22 Fitting results of 1.8V P+/Nwell diode IV model at temp=25C
Fig.C23 Fitting results of 1.8V P+/Nwell diode IV model at temp=125C

D. Comparison between measurement and simulation results (for Resistance)

E. Comparison between version 0.1 and version 1.3

F. Comparison between measurement and simulation result (for MOS noise)

8.Attachment

8.1 ASCII files:

l018ll_io50_v1p3_readme.txt (HSPICE format)
l018ll_io50_v1p3.lib (HSPICE format)
l018ll_io50_v1p3.mdl (HSPICE format)
l018ll_io50_v1p3_bjt.mdl (HSPICE format)
l018ll_io50_v1p3_res.mdl (HSPICE format)
l018ll_io50_v1p3_res.ckt (HSPICE format)
l018ll_io50_v1p3_mim.mdl (HSPICE format)
l018ll_io50_v1p3_readme_spe.txt (Spectre format)
l018ll_io50_v1p3_spe.lib (Spectre format)
l018ll_io50_v1p3_spe.mdl (Spectre format)
l018ll_io50_v1p3_bjt_spe.mdl (HSPICE format)
l018ll_io50_v1p3_res_spe.mdl (Spectre format)
l018ll_io50_v1p3_res_spe.ckt (Spectre format)
l018ll_io50_v1p3_mim_spe.mdl (Spectre format)
l018ll_io50_v1p3_readme_eldo.txt (ELDO format)
l018ll_io50_v1p3_eldo.lib (ELDO format)
l018ll_io50_v1p3_eldo.mdl (ELDO format)
l018ll_io50_v1p3_bjt_eldo.mdl (ELDO format)
l018ll_io50_v1p3_res_eldo.mdl (ELDO format)
l018ll_io50_v1p3_res_eldo.ckt (ELDO format)
l018ll_io50_v1p3_mim_eldo.mdl (ELDO format)
res.va (Spectre format)
l018ll _Interconnect_Struct_1.txt
l018ll _Interconnect_Struct_2.txt
l018ll _io50_layer.map

8.2 GDSII files:

DIO_NPW18.gds
DIO_PNW18.gds
DIO_NPW50.gds
DIO_PNW50.gds
DIO_NWPS.gds
PNP18A100.gds
PNP18A25.gds
PNP18A4.gds

8.3 Plot files:

l018ll_io50 _fit_A.doc
l018ll_io50_ fit_B.doc
l018ll_io50 _fit_C.doc

l018ll_io50 _fit_D.doc
l018ll_io50 _fit_E.doc
l018ll_io50 _fit_F.doc