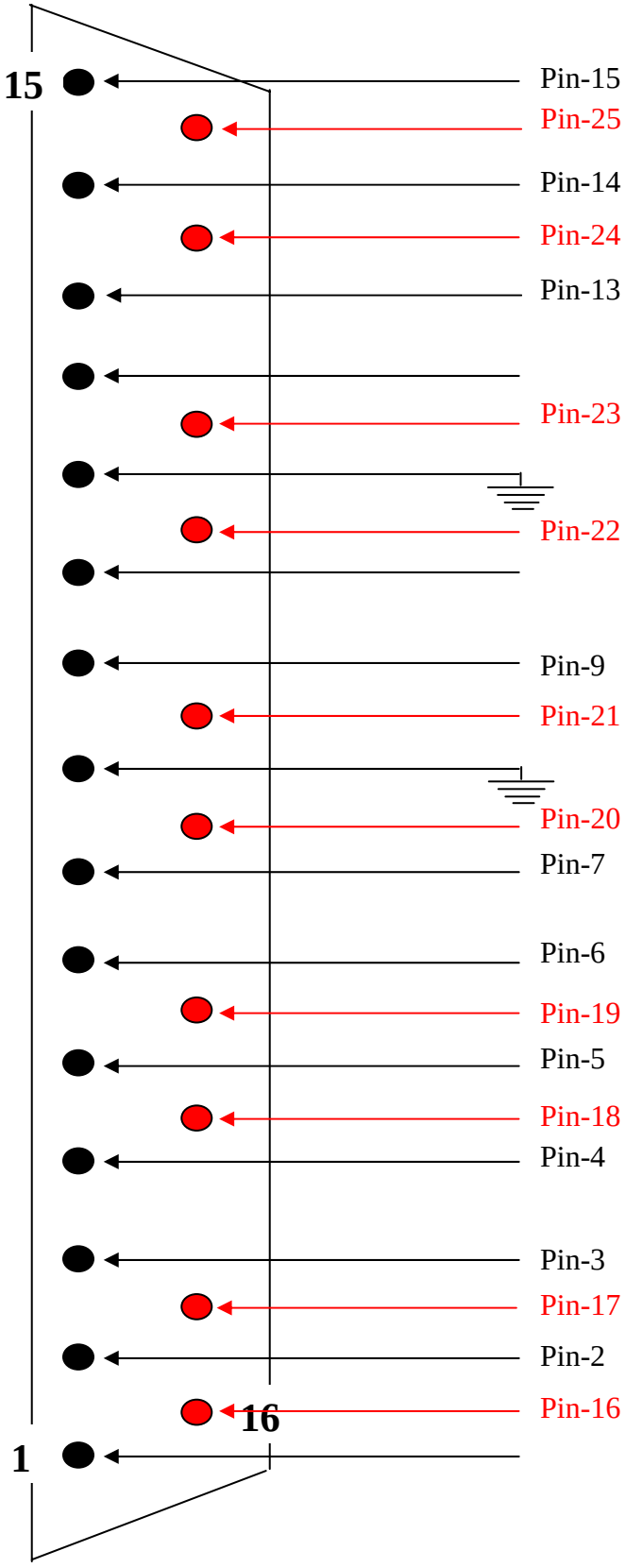
SDLC Design Review

Channel “A” IO Pin Descriptions (DB25 Connector)

PIN	NAME	DESCRIPTION	OUTPUT DRVR
1	ChA_GPout1	General Purpose Output	50Ω Driver
14	ChA_GPout2	General Purpose Output	50Ω Driver
2	ChA_GPout3	General Purpose Output	50Ω Driver
15	ChA_GPout4	General Purpose Output	50Ω Driver
3	ChA_RTS_CTS_Lo	Hand Shake Differential IO Low	RS 422
16	ChA_RTS_CTS_Hi	Hand Shake Differential IO High	RS 422
4	ChA_GPin1	General Purpose Input	Input
17	ChA_GPin2	General Purpose Input	Input
5	BiDAC_Out	Bipolar DAC Output ±10	DAC 200 mA
18	ChA_WTic1	Wheel Tic	50Ω Driver
6	ChA_WTic2	Wheel Tic	50Ω Driver
19	ChA_WTic3	Wheel Tic	50Ω Driver
7	ChA_WTic4	Wheel Tic	50Ω Driver
20	ChA_DAC_OutA	5V DAC Output	DAC 50 mA
8	DGND	10Analog Ground	N/A
21	ChA_DAC_OutB	5V DAC Output	DAC 50 mA
9	ChA_DAC_OutC	5V DAC Output	DAC 50 mA
22	ChA_DAC_OutD	5V DAC Output	DAC 50 mA
10	ChA_DataLo	Data Differential IO Low	RS 422
23	ChA_DataHi	Data Differential IO High	RS 422
11	AGND	Digital Ground	N/A
24	ChA_ClkLo	Clock Differential IO Low	RS 422
12	ChA_ClkHi	Clock Differential IO High	RS 422
25	ChA_SyncLo	Synchronous Differential IO Low	RS 422
13	ChA_SyncHi	Synchronous Differential IO High	RS 422

Major Changes in Version 3

Item	**New Version 3**	**Old Version 2**
1	New CPLDs (3.3V)	Old CPLDs (5.0V)
2	New Spartan II Xilinx (3.3V)	Old Spartan I (5.0V)
3	Dual Channel SDLC Chip	Single Channel SDLC Chip (discontinue)
4	One 16-Bit DAC (5.0V Output)	One 12-Bit DAC (5.0V Output)
5	One 16-Bit Bipolar DAC (±10V Output)	No Bipolar DAC
6	50Ω Drivers on GPout and WheelTics	Small Drivers on GPout and WheelTics


15
Pin-15
Pin-25
Pin-14
Pin-24
Pin-13
Pin-23
Pin-22
Pin-9
Pin-21
Pin-20
Pin-7
Pin-6
Pin-19
Pin-5
Pin-18
Pin-4
Pin-3
Pin-17
Pin-2
Pin-16
16
1