LM5141-Q1 Wide Input Range Synchronous Buck Controller

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1: –40ºC to +125ºC Ambient Operating Temperature Range
  - Device HBM ESD Classification Level 2
  - Device CDM ESD Classification Level C4B
- VIN 3.8 V to 65 V (70 V Absolute Maximum)
- Output: Fixed 3.3 V, 5 V, or Adjustable From 1.5 V - 15 V with ±0.8% Accuracy
- Fixed 2.2 MHz or 440 kHz Switching Frequency with ±5% Accuracy
- High-Side and Low-Side Gate Drive With Slew Rate Control
- Optional Frequency Shift by Varying an Analog Voltage or RT Resistor
- Optional Synchronization to an External Clock
- Optional Spread Spectrum
- Shutdown Mode I_Q: 10 µA Typical
- Low Standby Mode I_Q: 35 µA Typical
- 75 mV Current Limit Threshold with ±0.9% Accuracy
- External Resistor or DCR Current Sensing
- Output Enable Logic Input
- Hiccup Mode for Sustained Overload
- Power Good Indication Output
- Selectable Diode Emulation or Forced Pulse Width Modulation
- QFN-24 Package with Wettable Flanks

2 Applications

- Automotive Applications Including:
- Infotainment Systems
- Instrumentation Clusters
- Advanced Driver Assistance Systems (ADAS)

3 Description

The LM5141-Q1 is a synchronous buck controller, intended for high voltage wide V_{IN} step-down converter applications. The control method is peak current mode control. Current mode control provides inherent line feed-forward, cycle-by-cycle current limiting, and ease of loop compensation. The LM5141-Q1 features slew rate control to simplify the compliance with CISPR and Automotive EMI requirements.

The LM5141-Q1 has two selectable switching frequencies: 2.2 MHz and 440 kHz. Gate Drivers with Slew Rate Control that can be adjusted to reduce EMI.

In light or no-load conditions, the LM5141-Q1 operates in skip cycle mode for improved low power efficiency. The LM5141-Q1 has a high voltage bias regulator with automatic switch-over to an external bias to reduce the I_Q current from V_{IN}. Additional features include frequency synchronization, cycle-by-cycle current limit, hiccup mode fault protection for sustained overload, and power good output.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM5141-Q1	QFN (24)	4.00 mm × 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic

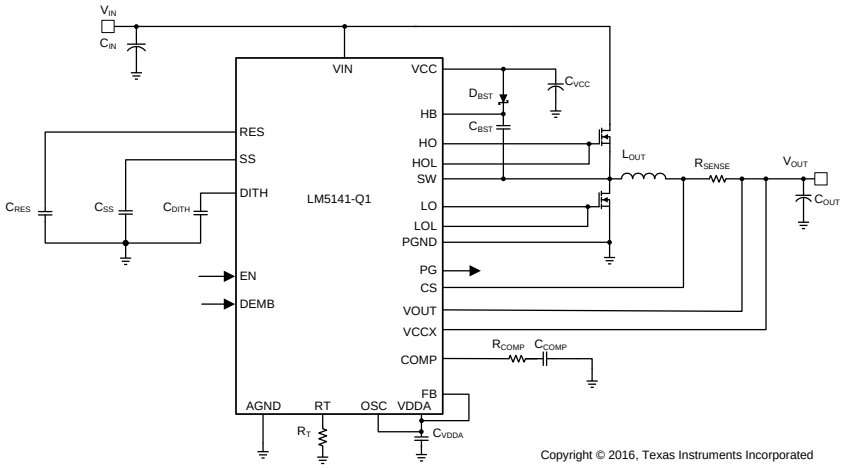


Table of Contents

4 Revision History

Changes from Revision A (July 2016) to Revision B **Page**

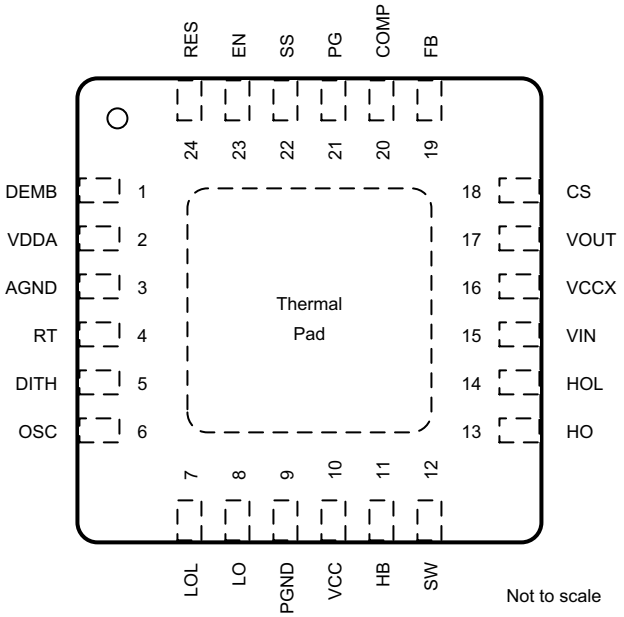
- Added 'Systems' to the ADAS bullet in *Applications* ... 1
- Changed *Description* text From: 'conducted EMI' To: 'EMI' ... 1
- Changed test conditions for RT parameter from: OSC = VDD to: OSC = GND ... 8
- Changed equation unit From: '0.815 Apk' To: '0.815 A' ... 24
- Changed equation unit From: '6.41 Apk' To: '6.41 A' ... 24
- Changed equation unit From: '8.81 Apk' To: ' 8.81 A' ... 24
- Changed equation unit From: '0.235 A_{RMS}' To: '0.235 A' ... 25
- Changed text From: 'a capacitance value greater than filter capacitor C_{IN}' To: 'a capacitance value greater than 5 times the filter capacitor C_{IN}' ... 27
- Changed equation text From: '6^2A' and '105 nc' To: '$(6A)^{2}$' and '105 nC' ... 27
- Added G_{CS} to equation definition list ... 30
- Added Ω and µS symbols to equation text ... 32
- Added Ω symbols to equation text ... 32

Changes from Original (July 2016) to Revision A **Page**

- Changed Product Preview to Production Data Release ... 1

5 Pin Configuration and Functions

RGE Package
24-Pin QFN With Exposed Thermal Pad
Top View



Connect Exposed Pad on bottom to AGND and PGND on the PCB.

Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	DEMB	I	Diode Emulation pin. Connect the DEMB pin to AGND to enable diode emulation. If it is connected to VDDA the LM5141-Q1 operates in Forced PWM (FPWM) mode with continuous conduction at light loads. The DEMB pin can also be used as a synchronization input, to synchronize the internal oscillator to an external clock.
2	VDDA	P	Internal analog bias regulator output. Connect a capacitor from the VDDA pin to AGND.
3	AGND	G	Analog ground connection. Ground return for the internal voltage reference and analog circuits.
4	RT	I	A resistor from the RT pin to ground shifts the oscillator frequency up or down from 2.2 MHz (1.8 MHz to 2.53 MHz), or 440 kHz (300 kHz to 500 kHz). An analog voltage can be applied to the RT pin (through a resistor) to shift the oscillator frequency.
5	DITH	O	A capacitor connected between the DITH pin and AGND is charged and discharged with a 20 µA current source. If Dither is enabled, the voltage on the DITH pin ramps up and down modulating the oscillator frequency between –5% and +5% of the internal oscillator. Connecting DITH to VDDA will disable the dithering feature. DITH is ignored if an external synchronization clock is used.
6	OSC	I	Frequency selection pin. Connecting the OSC pin to VDDA sets the oscillator frequency to 2.2 MHz. Connecting the OSC pin to AGND sets the frequency to 440 kHz.
7	LOL	O	Low-side gate driver turn-off output.
8	LO	O	Low-side gate driver turn-on output.
9	PGND	G	Power ground connection pin for low-side NMOS gate driver.
10	VCC	P	VCC bias supply pin. Connect a capacitor from the VCC pin to PGND.
11	HB	P	High-side driver supply for bootstrap gate drive.
12	SW		Switching node of the buck regulator. Connect to the bootstrap capacitor, the source terminal of the high-side MOSFET and the drain terminal of the low-side MOSFET.
13	HO	O	High-side gate driver turn-on output.
14	HOL	O	High-side gate driver turn-off output.

Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NO.	NAME		
15	VIN	P	Supply voltage input source for the VCC regulator
16	VCCX	P	Optional input for an external bias supply. If VCCX > 4.5 V, VCCX is internally connected to the VCC pin and the internal VCC regulator is disabled. If VCCX is unused, it should be grounded.
17	VOUT	I	Current sense amplifier input. Connect this pin to the output side of the current sense resistor.
18	CS	I	Current sense amplifier input. Make a low current Kelvin connection between this pin and the inductor side of the external current sense resistor.
19	FB	I	Connect the FB pin to VDDA for a fixed 3.3-V output or connect FB to AGND for a fixed 5-V output. Connecting the FB pin to the appropriate output divider network will set the output voltage between 1.5 V and 15 V. The regulation threshold at the FB pin is 1.2 V.
20	COMP	I	Output of the transconductance error amplifier.
21	PG	O	An open collector output which switches low if V_{OUT} is outside of the power good window.
22	SS	I	Soft-start programming pin. An external capacitor and an internal 20-μA current source set the ramp rate of the internal error amplifier reference during soft-start. Pulling SS pin below 80 mV turns-off the gate driver outputs, but all the other functions remain active.
23	EN	I	An active high logic input enables the controller.
24	RES	O	Restart timer pin. An external capacitor configures the hiccup mode current limiting. The capacitor at the RES pin determines the time the controller will remain off before automatically restarting in hiccup mode. The hiccup mode commences when the controller experiences 512 consecutive PWM cycles with cycle-by-cycle current limiting. Connecting the RES pin to VDD during power up disables hiccup mode protection.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage	VIN	–0.3	70	V
	SW to PGND	–0.3	70	V
	SW to PGND (20 ns transient)	–5		V
	HB to SW	–0.3	6.5	V
	HB to SW (20 ns transient)	–5		V
	HO, HOL to SW	–0.3	HB + 0.3	V
	HO, HOL to SW (20 ns transient)	–5		V
	LO, LOL to PGND	–0.3	VCC + 0.3	V
	LO, LOL to PGND (20 ns transient)	–1.5		V
	OSC, SS, COMP, RES, DEMB, RT, DITH	–0.3	VDD + 0.3	V
	EN to PGND	–0.3	70	V
	VCC, VCCX, VDD, PG, FB	–0.3	6.5	V
	VOUT, CS	–0.3	15.5	V
PGND to AGND		–0.3	0.3	V
Operating junction temperature(2)		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002[1]		±2000	V
		Charged-device model (CDM), per AEC Q100-011	All pins except 1,6,7,12,13,18,19, and 24	±500	
			Pins 1,6,7,12,13,18,19, and 24	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	VIN	3.8		65	V
		SW to PGND	–0.3		65	V
		HB to SW	–0.3	5	5.25	V
		HO, HOL to SW	–0.3		HB + 0.3	V
		LO, LOL to PGND	–0.3	5	5.25	V
		FB, PG, OSC, SS, RES, DEMB, VCCX	–0.3		5	V
		EN to PGND	–0.3		65	V
		VCC, VDD	–0.3	5	5.25	V
		VOUT, CS	1.5	5	15	V
	PGND to AGND		–0.3		0.3	V
	Operating junction temperature[2]		–40		150	°C

(1) Recommended Operating Conditions are conditions under which the device is intended to be functional. For specifications and test conditions, see *Electrical Characteristics*.
(2) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

6.4 Thermal Information

THERMAL METRIC[1]		LM5141-Q1 RGE (QFN) 24 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	34.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	36.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	12.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	12.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

T_J = –40°C to +125°C, Typical values T_J = 25°C, VIN = 12 V, VCCX = 5 V, VOUT = 5 V, EN = 5 V, OSC = VDD, F_{SW} = 2.2 MHz, no-load on the Drive Outputs (HO, HOL, LO, and LOL outputs), over operating free-air temperature range (unless otherwise noted)(1)(2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VIN SUPPLY VOLTAGE						
$I_{SHUTDOWN}$	Shutdown mode current	V_{IN} = 8–18 V, EN = 0 V, VCCX = 0 V		10	12.5	µA
$I_{STANDBY}$	Standby current	EN = 5 V, FB = VDD, V_{OUT} in regulation, no-load, not switching, DEMB = GND.		35	45	µA
		EN = 5 V, FB = 0 V, V_{OUT} in regulation, no-load, not switching, VCCX = 5 V, DEMB = GND.		42	55	
VCC REGULATOR						
$VCC_{(REG)}$	VCC regulation voltage	V_{IN} = 6–18 V, 0–75 mA, VCCX = 0 V	4.75	5	5.25	V
$VCC_{(UVLO)}$	VCC under voltage threshold	VCC rising, VCCX = 0 V	3.25	3.4	3.55	V
$VCC_{(HYST)}$	VCC hysteresis voltage	VCCX = 0 V		175		mV
$I_{CC(LIM)}$	VCC sourcing current limit	VCCX = 0 V	85	125		mA
VDDA						
$VDDA_{(REG)}$	Internal bias supply power	VCCX = 0 V	4.75	5	5.25	V
$VDDA_{(UVLO)}$		VCC rising, VCCX = 0 V	3.1	3.2	3.3	V
$VDDA_{(HYST)}$		VCCX = 0 V		125		mV
R_{VDDA}		VCCX = 0 V		55		Ω
VCCX						
$VCCX_{(ON)}$		VCC rising	4.1	4.3	4.4	V
$VCCX_{(HYST)}$				80		mV
$R_{(VCCX)}$		VCCX = 5 V		2		Ω
OSCILLATOR SELECT THRESHOLDS						
	Oscillator select threshold 2.2 MHz	(OSC pin)	2.0			V
	Oscillator select threshold 440 kHz	(OSC pin)			0.8	V
CURENT LIMIT						
$V_{(CS)}$	Current limit threshold	ILSET = VDDA, measure from CS to V_{OUT}	68	75	82	mV
t_{dly}	Current sense delay to output			40		ns
	Current sense amplifier gain		11.4	12	12.6	V/V
$ICS_{(BIAS)}$	Amplifier input bias				10	nA
RES						
$I_{(RES)}$	RES current source			20		µA
$V_{(RES)}$	RES threshold			1.2		V
T_{imer}	Timer hiccup mode fault			512		cycles
$R_{DS(ON)}$	RES pull-down			4		Ω
OUTPUT VOLTAGE REGULATION						
	3.3 V	V_{IN} = 3.8–42 V	3.273	3.3	3.327	V
	5 V	V_{IN} = 5.5–42 V	4.96	5.0	5.04	V
FEEDBACK						
	V_{OUT} select threshold 3.3 V		VDD - 0.3			V
	Regulated feedback voltage		1.193	1.2	1.207	V
$FB_{(LOWRES)}$	Resistance to ground on FB for FB = 0 detection				500	Ω

(1) All minimum and maximum limits are specified by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(2) The junction temperature (T_J in ºC) is calculated from the ambient temperature (T_A in ºC) and power dissipation (P_D in Watts) as follows: $T_J = T_A + (P_D \times R_{\theta JA})$ where $R_{\theta JA}$ (in °C/W) is the package thermal impedance provided in the *Thermal Information* section.

Electrical Characteristics (continued)

T_J = –40°C to +125°C, Typical values T_J = 25°C, VIN = 12 V, VCCX = 5 V, VOUT = 5 V, EN = 5 V, OSC = VDD, F_{SW} = 2.2 MHz, no-load on the Drive Outputs (HO, HOL, LO, and LOL outputs), over operating free-air temperature range (unless otherwise noted)(1)(2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$FB_{(EXTRES)}$	Thevenin equivalent resistance at FB for external regulation detection	FB < 2 V	5			kΩ
TRANSCONDUCTANCE AMPLIFIER						
Gm	Gain	Feedback to COMP	1010	1200		µS
	Input bias current				15	nA
	Transconductance Amplifier source current	COMP = 1 V, FB = 1 V		100		µA
	Transconductance Amplifier sink current	COMP = 1 V, FB = 1.4 V		100		µA
POWER GOOD						
$PG_{(UV)}$	PG under voltage trip levels	Falling with respect to the regulation voltage	90%	92%	94%	
$PG_{(OVP)}$	PG over voltage trip levels	Rising with respect to the regulation voltage	108%	110%	112%	
$PG_{(HYST)}$				3.4%		
$PG_{(VOL)}$	PG	Open collector, Isink = 2 mA			0.4	V
$PG_{(rdly)}$	OV filter time	V_{OUT} rising		25		µs
$PG_{(fdly)}$	UV filter time	V_{OUT} falling		30		µs
HO GATE DRIVER						
V_{OLH}	HO Low-state output voltage	I_{HO} = 100 mA		0.05		V
V_{OHH}	HO High-state output voltage	I_{HO} = –100 mA, $V_{OHH} = V_{HB} - V_{HO}$		0.07		V
t_{rHO}	HO rise time (10% to 90%)	C_{LOAD} = 2700 pf		4		ns
t_{fHO}	HO fall time (90% to 10%)	C_{LOAD} = 2700 pf		3		ns
I_{OHH}	HO peak source current	V_{HO} = 0 V, SW = 0 V, HB = 5 V, VCCX = 5 V		3.25		Apk
I_{OLH}	HO peak sink current	VCCX = 5 V		4.25		Apk
$V_{(BOOT)}$	UVLO	HO falling		2.5		V
	Hysteresis			110		mV
$I_{(BOOT)}$	Quiescent current			3		µA
LO GATE DRIVER						
V_{OLL}	LO Low-state output voltage	I_{LO} = 100 mA		0.05		V
V_{OHL}	LO High-state output voltage	I_{LO} = –100 mA, $V_{OHL} = VCC - V_{LO}$		0.07		V
t_{rLO}	LO rise time (10% to 90%)	C_{LOAD} = 2700 pf		4		ns
t_{fLO}	LO fall time (90% to 10%)	C_{LOAD} = 2700 pf		3		ns
I_{OHL}	LO peak source current	VCCX = 5 V		3.25		Apk
I_{OLL}	LO peak sink current	VCCX = 5 V		4.25		Apk
ADAPTIVE DEAD TIME CONTROL						
$V_{(GS-DET)}$	VGS detection threshold	VGS falling, no-load		2.5		V
tdly1	HO off to LO on dead time			20	40	ns
tdly2	LO off to HO on dead time			20	38	ns
DIODE EMULATION						
V_{IL}	DEMB input low threshold				0.8	V
V_{IH}	FPWM input high threshold		2.0			V
SW	Zero cross threshold			–5		mV

Electrical Characteristics (continued)

T_J = –40°C to +125°C, Typical values T_J = 25°C, VIN = 12 V, VCCX = 5 V, VOUT = 5 V, EN = 5 V, OSC = VDD, F_{SW} = 2.2 MHz, no-load on the Drive Outputs (HO, HOL, LO, and LOL outputs), over operating free-air temperature range (unless otherwise noted)[1][2]

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ENABLE INPUT						
V_{IL}	Enable input low threshold	VCCX = 0 V			0.8	V
V_{IH}	Enable input high threshold	VCCX = 0 V	2.0			V
I_{lkg}	Leakage	EN logic input only		1		µA
SYN INPUT (DEMB pin)						
V_{IL}	DEMB input low threshold				0.8	V
V_{IH}	DEMB input high threshold		2.0			V
	DEMB input low frequency range 440 kHz		350		550	kHz
	DEMB input high frequency range 2.2 MHz		1800		2600	kHz
DITHER						
I_{DITHER}	Dither source/sink current			20		µA
V_{DITHER}	Dither high threshold			1.26		V
	Dither low threshold			1.14		V
SOFT-START						
I_{SS}	Soft-Start current		16	22	28	µA
$R_{DS(ON)}$	Soft-Start pull-down resistance			3		Ω
THERMAL						
	TSD Thermal Shutdown			175		ºC
	Thermal shutdown hysteresis			15		ºC

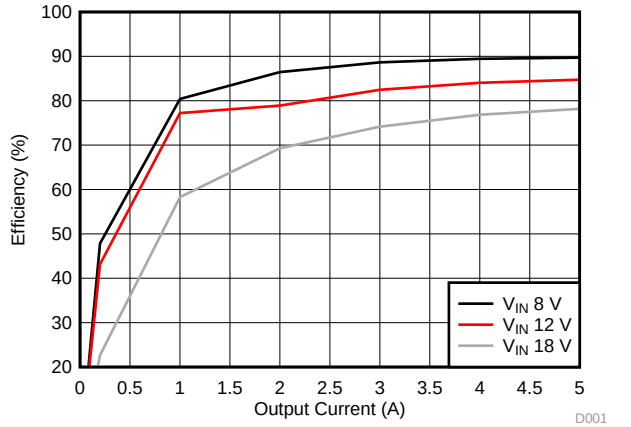
6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Oscillator Frequency 2.2 MHz		OSC = VDDA, V_{IN} = 8–18 V	2100	2200	2300	kHz
	Oscillator Frequency 440 kHz		OSC = GND, V_{IN} = 8–18 V	420	440	460	kHz
RT	Adjustment Range 2.2 MHz	Minimum	OSC = VDD, RT_{MIN} = 61.9 kΩ	1710	1800	1890	kHz
		Typical	OSC = VDD, RT_{TYP} = 49.9 kΩ	2100	2200	2300	kHz
		Maximum	OSC = VDD, RT_{MAX} = 43.2 kΩ	2405	2530	2655	kHz
RT	Adjustment Range 440 kHz	Minimum	OSC = GND, RT_{MIN} = 73.2 k	285	300	315	kHz
		Typical	OSC = GND, RT_{TYP} = 49.9 kΩ	420	440	460	kHz
		Maximum	OSC = GND, RT_{MAX} = 44.2 kΩ	475	500	525	kHz
RT	Response time	RT= 61.9–43.2 kΩ			2		µs
RT	Response time	RT = 43.2–61.9 kΩ			3.5		µs
RT	Response time				16		µs
t_{on}	Minimum on-time				45	66	ns
t_{off}	Minimum off-time					100	ns

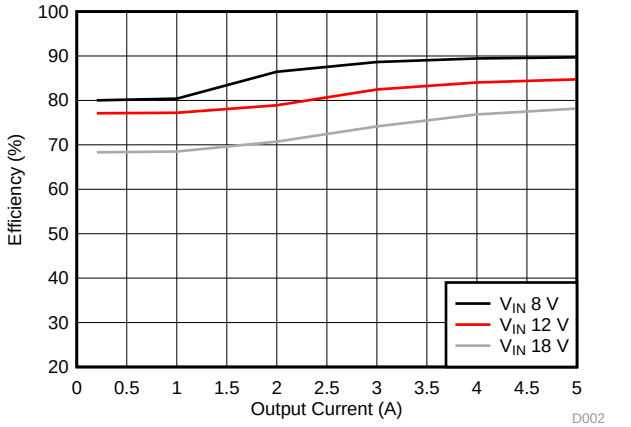
6.7 Typical Characteristics

At T_A = 25ºC, unless otherwise noted



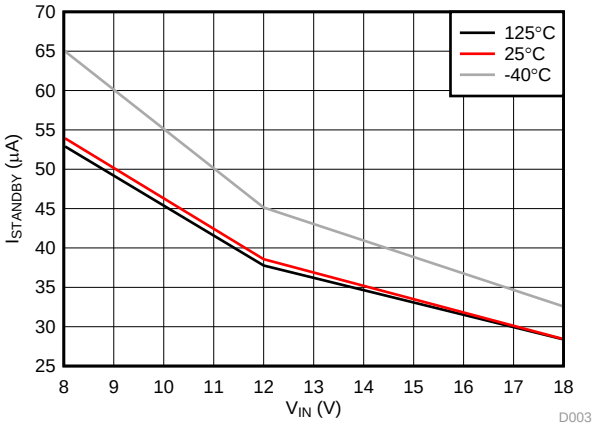
V_{IN} 8–18 V EN = 12 V 2.2 MHz
V_{OUT} 5 V FPWM

Figure 1. Efficiency vs I_{OUT}



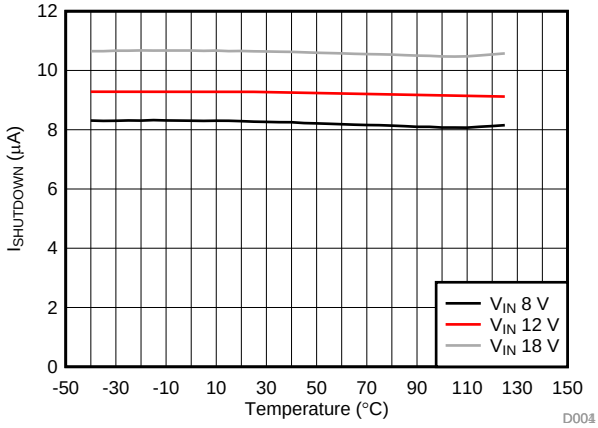
V_{IN} 8–18 V EN = 12 V 2.2 MHz
V_{OUT} 5 V DEMB

Figure 2. Efficiency vs I_{OUT}



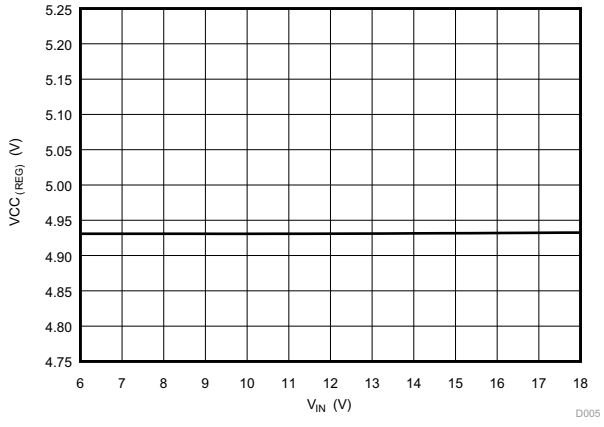
EN = 12 V

Figure 3. $I_{STANDBY}$ vs V_{IN}



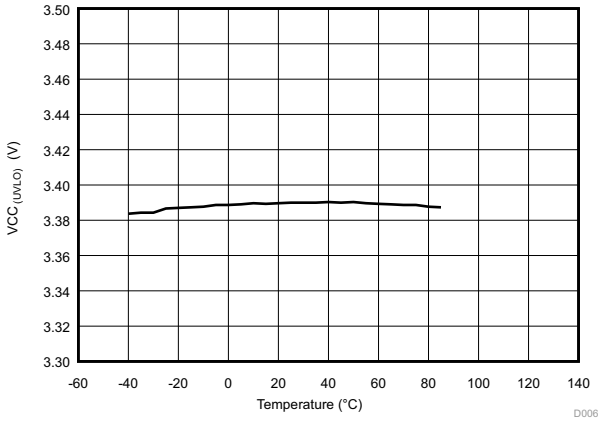
V_{IN} 8–18 V EN = 0 V

Figure 4. $I_{SHUTDOWN}$ vs Temperature



V_{IN} 6-18 V EN = GND

Figure 5. $VCC_{(REG)}$ vs V_{IN}

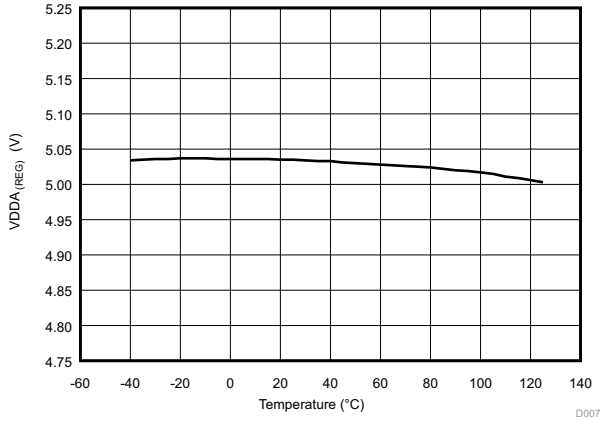


V_{IN} 8–18 V EN = 12 V

Figure 6. $VCC_{(UVLO)}$ vs Temperature

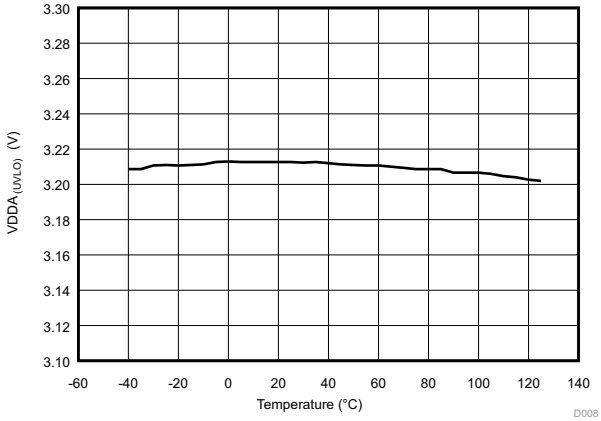
Typical Characteristics (continued)

At T_A = 25ºC, unless otherwise noted



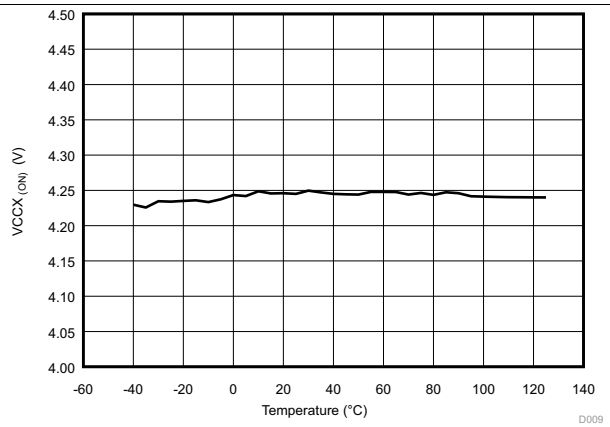
VCC Rising EN = 12 V

Figure 7. $VDD_{(REG)}$ vs Temperature



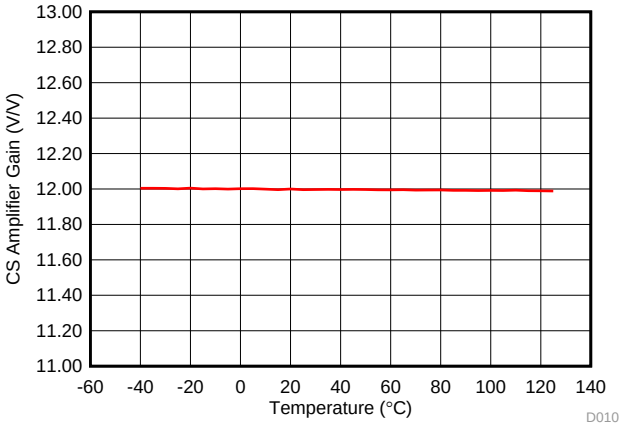
VCC Rising EN = 12 V

Figure 8. $VDD_{(UVLO)}$ vs Temperature



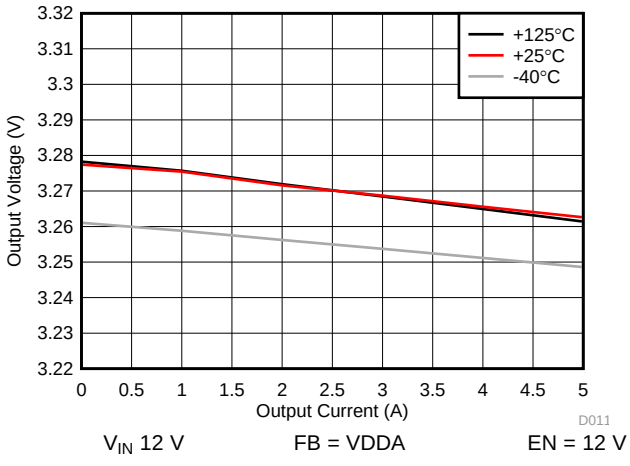
VCC Rising EN = 12 V

Figure 9. $VCCX_{(ON)}$ vs Temperature



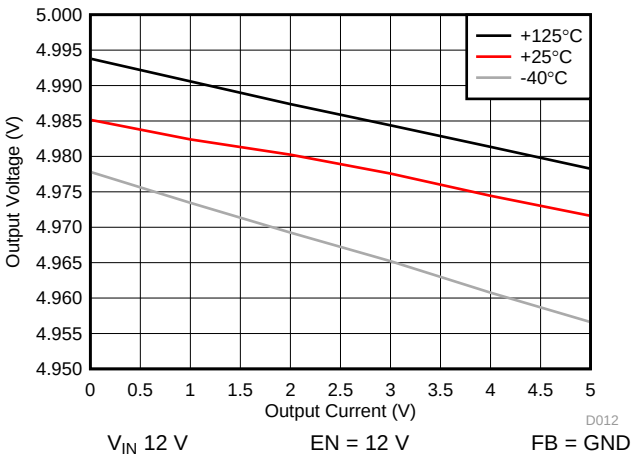
V_{IN} 12 V EN = 12 V

Figure 10. Current Sense Amplifier Gain vs Temperature



V_{IN} 12 V FB = VDDA EN = 12 V

Figure 11. 3.3-V Output Voltage Regulation vs I_{OUT}

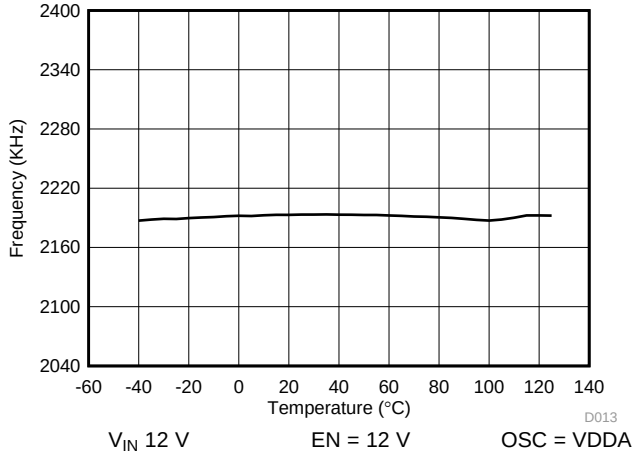


V_{IN} 12 V EN = 12 V FB = GND

Figure 12. 5-V Output Voltage Regulation vs I_{OUT}

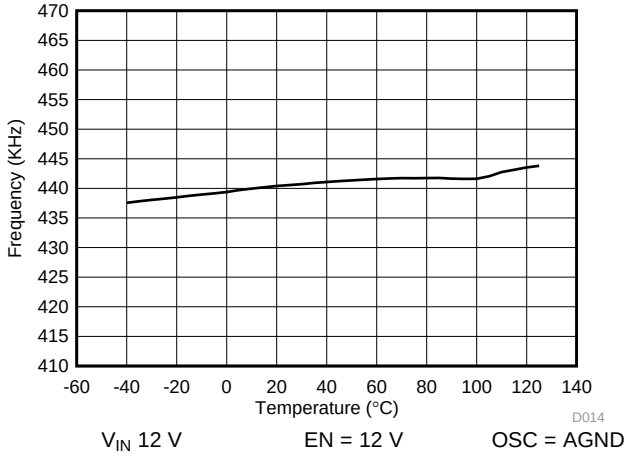
Typical Characteristics (continued)

At T_A = 25ºC, unless otherwise noted



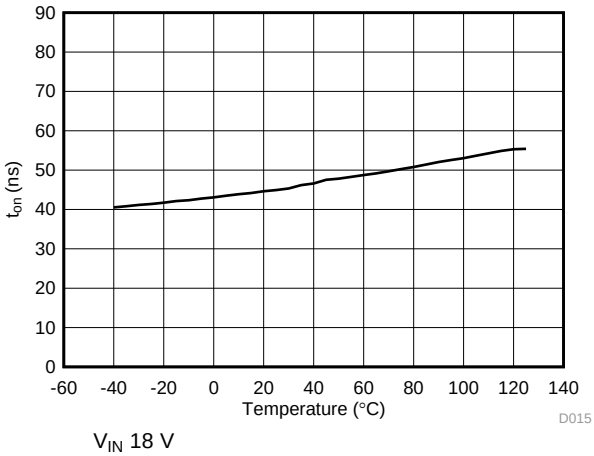
V_{IN} 12 V EN = 12 V OSC = VDDA

Figure 13. 2.2-MHz Oscillator Frequency vs Temperature



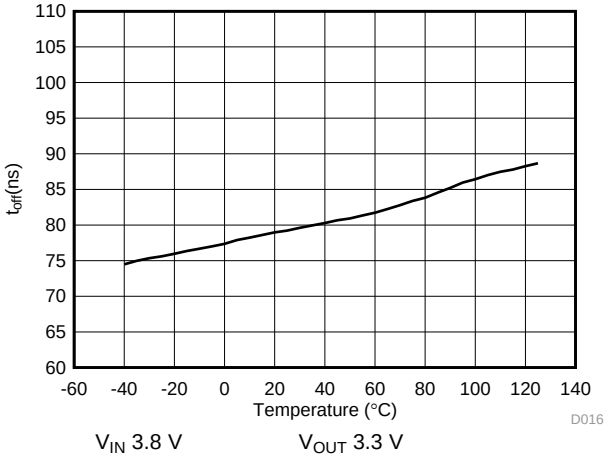
V_{IN} 12 V EN = 12 V OSC = AGND

Figure 14. 440-kHz Oscillator Frequency vs Temperature



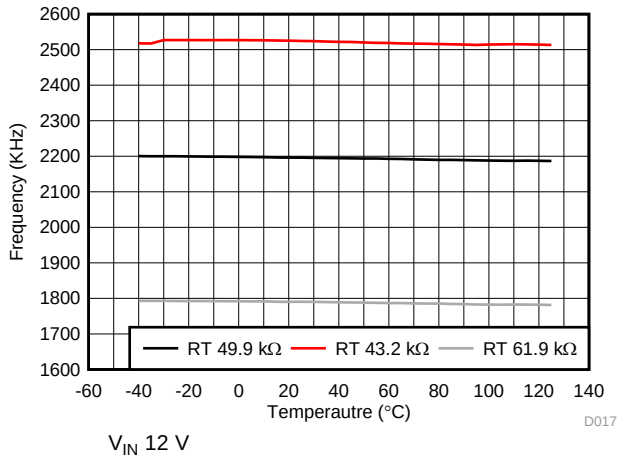
V_{IN} 18 V

Figure 15. t_{on} Minimum vs Temperature



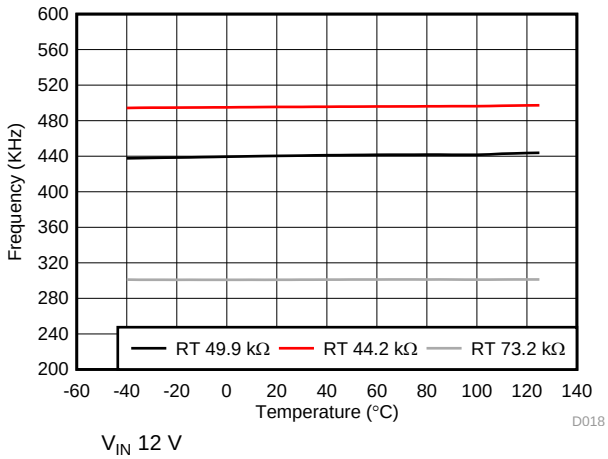
V_{IN} 3.8 V V_{OUT} 3.3 V

Figure 16. t_{off} Minimum vs Temperature



V_{IN} 12 V

Figure 17. RT Frequency vs Temperature (2.2 MHz)



V_{IN} 12 V

Figure 18. RT Frequency vs Temperature (440 kHz)

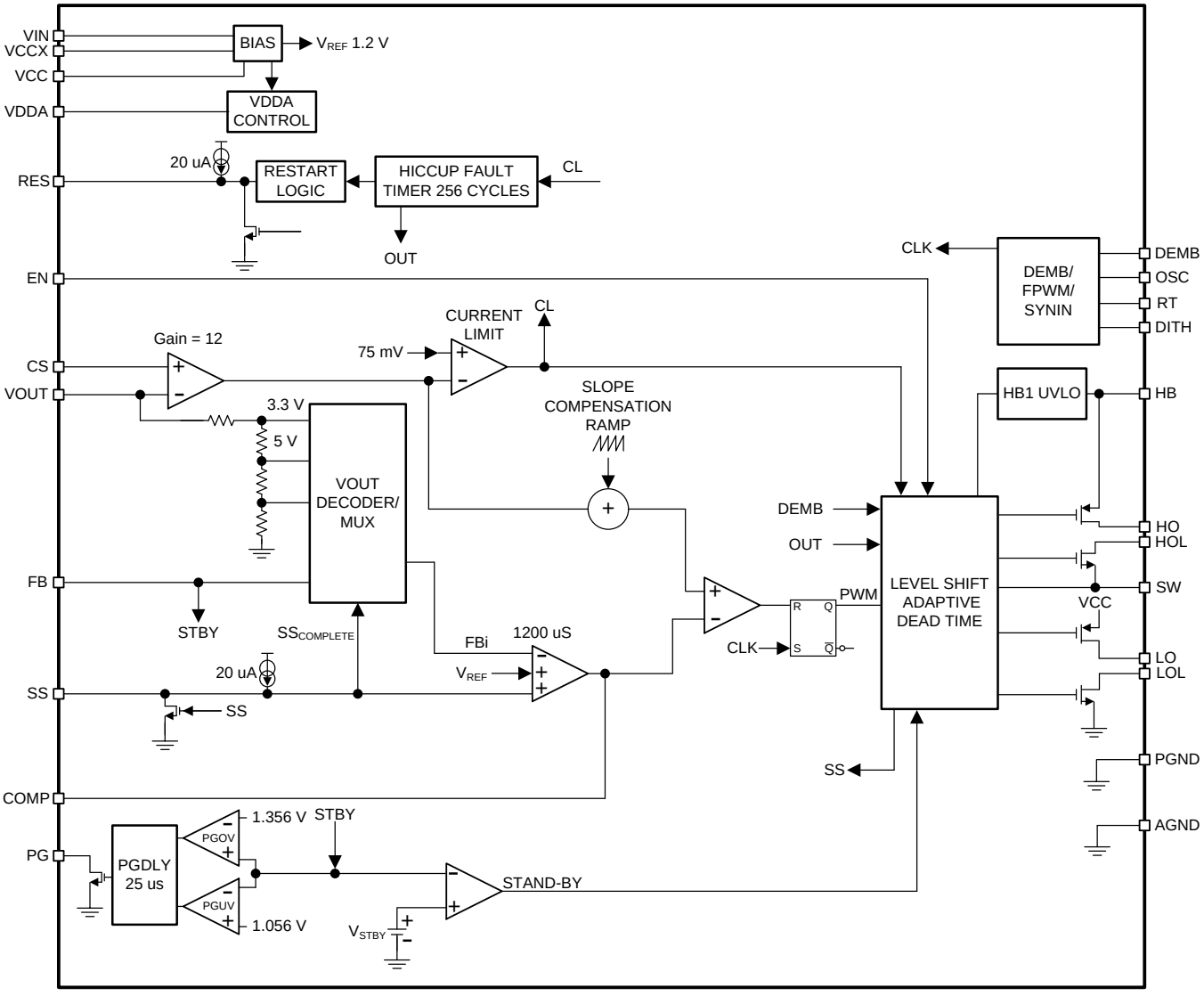
7 Detailed Description

7.1 Overview

The LM5141-Q1 is a switching controller which features all of the functions necessary to implement a high efficiency buck power supply that can operate over a wide input voltage range. The LM5141-Q1 is configured to provide a single fixed 3.3 V, or 5.0 V output, or an adjustable output between 1.5 V to 15 V. This easy to use controller integrates high-side and low-side MOSFET drivers capable of sourcing 3.25 A and sinking 4.25 A peak. The control method is current mode control which provides inherent line feed-forward, cycle-by-cycle current limiting, and ease of loop compensation. With the OSC pin connected to VDD, the default oscillator frequency is 2.2 MHz. With the OSC pin grounded, the oscillator frequency is 440 kHz. The LM5141-Q1 can be synchronized by applying an external clock to the DEMB pin. Fault protection features include current limiting, thermal shutdown, and remote shutdown capability.

The LM5141-Q1 incorporates features that simplify compliance with the CISPR and automotive EMI requirements. The LM5141-Q1 has optional spread spectrum to reduce the peak EMI and gate drivers with slew rate control. The QFN-24 package features an exposed pad to aid in thermal dissipation.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 High Voltage Start-up Regulator

The LM5141-Q1 contains an internal high voltage VCC bias regulator that provides the bias supply for the PWM controller and the gate drivers for the external MOSFETs. The input pin (VIN) can be connected directly to an input voltage source up to 65 V. The output of the VCC regulator is set to 5 V. When the input voltage is below the VCC set-point level, the VCC output will track VIN with a small voltage drop. In high voltage applications extra care should be taken to ensure the VIN pin does not exceed the absolute maximum voltage rating of 70 V including line or load transients. Voltage ringing on the VIN pin that exceeds the Absolute Maximum Ratings can damage the IC. Use a high quality bypass capacitor between VIN and ground to minimize ringing.

7.3.2 VCC Regulator

The VCC regulator output current limit is 75 mA (minimum). At power-up, the regulator sources current into the capacitors connected to the VCC pin. When the voltage on the VCC pin exceeds 3.4 V the output is enabled and the soft-start sequence begins. The output remains active unless the voltage on the VCC pin falls below the $VCC_{(UVLO)}$ threshold of 3.2 V (typical) or the enable pin is switched to a low state. The recommended range for the VCC capacitor is 2.2 µF to 4.7 µF

An internal 5-V linear regulator generates the VDDA bias supply. Bypass VDDA with a 100-nF or greater ceramic capacitor to ensure a low noise internal bias rail. Normally VDDA is 5 V, but there are two operating conditions where it regulates at 3.3 V. The first is in skip cycle mode with VOUT of 3.3 V. The second is when V_{IN} is less than 5 V. Under these conditions both VCC and VDD will drop below 5 V. Internal power dissipation in the VCC Regulator can be minimized by connecting the VCCX pin to a 5 V output or to an external 5 V supply. If VCCX > 4.5 V, VCCX is internally connected to VCC and the internal VCC regulator is disabled. If VCCX is unused, it should be grounded. Never connect the VCCX pin to a voltage greater than 6.5 V.

7.3.3 Oscillator

The LM5141-Q1 has an internal trimmed oscillator with two frequency options: 2.2 MHz, or 440 kHz. With the OSC pin connected to VDDA the oscillator frequency is 2.2 MHz. With the OSC pin grounded, the oscillator frequency is 440 kHz. The state of the OSC pin is read and latched during VCC power-up and cannot be changed until VCC drops below the $VCC_{(UVLO)}$ threshold.

The oscillator frequency can be modulated up or down from the nominal oscillator frequency (2.2 MHz or 440 kHz) on demand by connecting a resistor from the RT pin to ground (refer to Figure 19). To disable the frequency modulation option, the RT pin can be grounded or left open. If the RT pin is connected to ground during power-up the frequency modulation option is latch-off and cannot be changed unless VCC is allowed to drop below the $VCC_{(UVLO)}$ threshold. If the RT pin is left open during power-up the frequency modulation option will be disabled, but it can be enabled at a later time by switching in a valid RT resistor. When the frequency modulation option is disabled, the LM5141-Q1 will operate at the internal oscillator frequency (2.2 MHz or 440 kHz).

On power up, after soft-start is complete and the output voltage is in regulation, a 16 µs timer is initiated. If a valid RT resistor is connected, the LM5141-Q1 will switch to the frequency set by the RT resistor n the completion of the 16 µs time delay.

The modulation range for 2.2 MHz is 1.8 MHz to 2.53 MHz (refer to Table 1). If an RT resistor value > 95 kΩ (typical) is placed on the RT pin, the LM5141-Q1 controller will assume that the RT pin is open, and will use the internal oscillator. If an RT resistor < 27 kΩ (typical) is connected, the controller will use the internal oscillator. To calculate an RT resistor for a specific oscillator frequency, use Equation 1 for the 2.2 MHz frequency range or Equation 2 for the 440 kHz frequency range.

$$RT_{2.2\ MHz} = \frac{\frac{1}{Fsw} - 0.0216}{0.0086} \quad (1)$$

where

- RT is kΩ and Fsw is in MHz

Feature Description (continued)

$$RT_{440\ kHz} = \frac{\frac{1}{Fsw} - 1.38 \times 10^{-5}}{4.5 \times 10^{-5}} \quad (2)$$

where

- RT is in kΩ and Fsw is in kHz

Table 1. RT Resistance vs Oscillator Frequency

S1	S2	RT Resistance (Typical) 2.2 MHz	2.2 MHZ Oscillator Range (Typical)	RT Resistance (Typical) 440 kHz	440 kHz Oscillator Range (Typical)
X	X	> 95 kΩ	Internal Oscillator	> 95 kΩ	Internal Oscillator
OFF	OFF	61.98 kΩTotal	1.8 MHz	73.8 kΩTotal	300 kHz
OFF	ON	50.18 kΩTotal	2.2 MHz	50.1 kΩTotal	440 kHz
ON	OFF	43.2 kΩ	2.53 MHz	44.2 kΩ	500 kHz
X	X	< 27 kΩ	Internal Oscillator	< 27 kΩ	Internal Oscillator

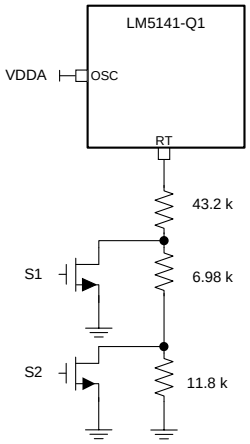


Figure 19. RT Connection Circuit, 2.2 MHz

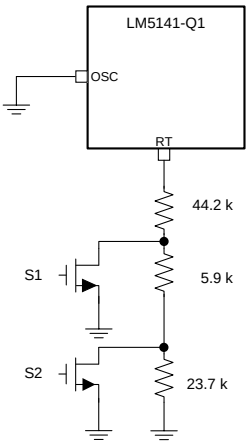


Figure 20. RT Connection Circuit, 440 kHz

An alternative method to modulate the oscillator frequency is to use an analog voltage connected to the RT pin through a resistor. See Figure 21. An analog voltage of 0.0 V to 0.6 V will modulate the oscillator frequency between 1.8 MHz to 2.53 MHz (OSC at 2.2 MHz), or 300 kHz to 500 kHz (OSC at 440 kHz). The analog voltage source must be able to sink current.

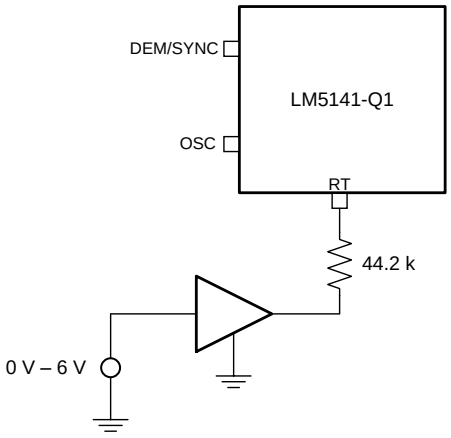


Figure 21. Analog Voltage Control of the Oscillator Frequency

When the LM5141-Q1 is in the low I_Q standby mode, the controller will set the RT pin to a high impedance state and ignore the RT resistor. After coming out of standby mode, the controller will monitor the RT pin. If a valid resistor is connected, and there have been 16 µs of continuous switching without a zero-crossing event, the LM5141-Q1 will switch to the frequency set by the RT resistor.

7.3.4 Synchronization

To synchronize the LM5141-Q1 to an external source, apply a logic level clock signal to the DEMB pin. The synchronization range is 350 kHz to 550 kHz when the internal oscillator is set to 440 kHz. When the internal oscillator is set to 2.2 MHz, the synchronization range is 1.8 MHz to 2.6 MHz. If there is a valid RT resistor and a synchronization signal, the LM5141-Q1 with ignore the RT resistor and synchronize the controller to the external clock. Under low V_{IN} conditions, when the minimum toff time is reached (100ns), the synchronization clock will be ignored to allow the frequency to drop to maintain output voltage regulation.

7.3.5 Frequency Dithering (Spread Spectrum)

The LM5141-Q1 provides a frequency dithering option that is enabled by connecting a capacitor from the DITH pin to AGND. A triangular waveform centered at 1.2 V is generated across the C_{DITH} capacitor. Refer to Figure 22. The triangular waveform modulates the oscillator frequency by ±5% of the nominal frequency set by the OSC pin or by an RT resistor. The C_{DITH} capacitance value sets the rate of the low frequency modulation. A lower C_{DITH} capacitance will modulate the oscillator frequency at a faster rate than a higher capacitance. For the dithering circuit to effectively reduce the peak EMI, the modulation rate must be less than the oscillator frequency (Fsw). Equation 3 calculates the DITH pin capacitance required to set the modulation frequency, FMOD.

$$C_{DITH} = \frac{20\ \mu A}{2 \times F_{MOD} \times 0.12\,V} \tag{3}$$

If the DITH pin is connected to VDDA during power-up the Dither feature is latch-off and cannot be changed unless VCC is allowed to drop below the $VCC_{(UVLO)}$ threshold. If the DITH pin is connected to ground on power up, Dither will be disabled, but it can be enabled by raising the DITH pin voltage above ground and connecting it to C_{DITH}. When the LM5141 is synchronized to an external clock, Dither is disabled.

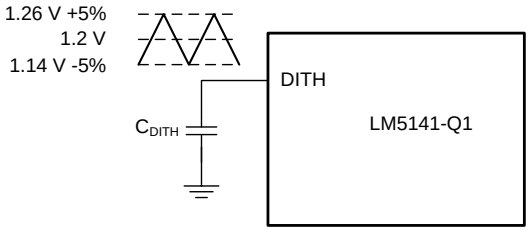


Figure 22. Dither Operation

7.3.6 Enable

The LM5141-Q1 has an enable input EN for start-up and shutdown control of the output. The EN pin can be connected to a voltage as high as 70 V. If the enable input is greater than 2.0 V the output is enabled. If the enable pin is pulled below 0.8 V, the output will be in shutdown, and the LM5141-Q1 is switched to a low I_Q shutdown mode, with a 10-µA typical current drawn from the VIN pin. It is not recommended to leave the EN pin left floating.

7.3.7 Power Good

The LM5141-Q1 includes an output voltage monitoring function to simplify sequencing and supervision. The power good function can be used to enable circuits that are supplied by the output voltage rail or to turn-on sequenced supplies. The PG pin switches to a high impedance state when the output voltage is in regulation. The PG signal switches low when the output voltage drops below the lower power good threshold (92% typical) or rises above the upper power good threshold (110% typical). A 25 µs deglitch filter prevents any false tripping of the power good signal due to transients. A pull-up resistor of 10 kΩ is recommended from the PG pin to the relevant logic rail. Power good is asserted low during soft-start and when the buck converter is disabled by EN.

7.3.8 Output Voltage

The LM5141-Q1 output can be configured for one of the two fixed output voltages with no external feedback resistors, or the output can be adjusted to the desired voltage using an external resistor divider. V_{OUT} can be configured as a 3.3-V output by connecting the FB pin to VDDA, or a 5-V output by connecting the FB pin to ground with a maximum resistance of 500 Ω. The FB connections (either VDDA or GND) are detected during power up.

The configuration setting is latched and cannot be changed until the LM5141-Q1 is powered down with VCC falling below $VCC_{(UVLO)}$ (3.4 V typical) and then powered up again.

Alternatively the output voltage can be set using an external resistive dividers from the output to the FB pin. The output voltage adjustment range is between 1.5 V and 15 V. The regulation threshold at the FB pin is 1.2 V (V_{REF}). To calculate R_{FB1} and R_{FB2} use Equation 4. Refer to Figure 23:

$$R_{FB2} = \left(\frac{V_{OUT}}{V_{REF}} - 1 \right) \times R_{FB1} \tag{4}$$

The recommend starting point is to select R_{FB1} between 10 kΩ to 20 kΩ.

The Thevenin equivalent impedance of the resistive divider connected to the FB pin must be greater than 5 kΩ for the LM5141-Q1 to detect the divider and set the controller to the adjustable output mode. Refer to Equation 5.

$$R_{TH} = \frac{R_{FB1} \times R_{FB2}}{R_{FB1} + R_{FB2}} > 5k\Omega \tag{5}$$

If a low I_Q mode is required, take care when selecting the external resistors. The extra current drawn from the external divider is added to the LM5141-Q1 $I_{STANDBY}$ current (35 μA typical). The divider current reflected to VIN is divided down by the ratio of V_{OUT}/V_{IN}. For example, if V_{IN} is 12V and V_{OUT} is set to 5.5 V with R_{FB1} 10 kΩ, and R_{FB2} = 35.7 kΩ, the input current at VIN required to supply the current in the feedback resistors is:

$$I_{DIVIDER} = \frac{V_{OUT}}{R_{FB1} + R_{FB2}} \times \frac{V_{OUT}}{V_{IN}} = \frac{5.5\,V}{10k + 35.7k} \times \frac{5.5\,V}{12\,V} = 55.16\,\mu A$$

where

- V_{IN} = 12 V

(6)

The total input current in this condition will be:

$$I_{VIN} \approx I_{STANDBY} + I_{DIVIDER} \approx 35\,\mu A + 55.16\,\mu \approx 90.16\,\mu A \quad (7)$$

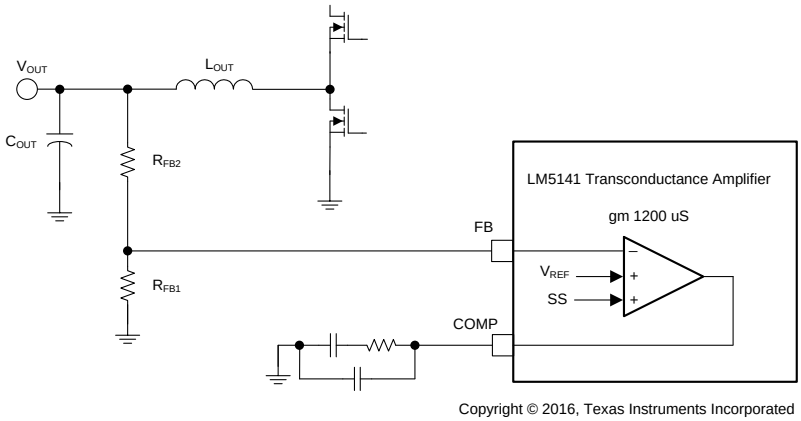


Figure 23. Voltage Feedback

7.3.8.1 Minimum Output Voltage Adjustment

There are two limitations to the minimum output voltage adjustment range: the LM5141-Q1 voltage reference of 1.2 V and the minimum switch node pulse width, t_{SW}.

The minimum controllable on-time at the switch node (t_{SW}) limits the voltage conversion ratio (V_{OUT}/V_{IN}). For fixed-frequency PWM operation, the voltage conversion ratio should meet the following condition:

$$\frac{V_{OUT}}{V_{IN}} > t_{sw} \times Fsw \quad (8)$$

Where t_{SW} is 70 ns (typical) and Fsw is the switching frequency. If the desired voltage conversion ratio does not meet the above condition, the controller transitions from fixed frequency operation into a pulse skipping mode to maintain regulation of the output voltage.

For example if the desired output voltage is 3.3 V with a V_{IN} of 20 V and operating at 2.2 MHz, the voltage conversion ratio test is satisfied:

$$\frac{3.3\,V}{20\,V} > 70ns \times 2.2MHz \quad (9)$$

0.165> 0.154

For wide V_{IN} applications and lower output voltages, an alternative is to use the LM5141-Q1 with a 440-kHz oscillator frequency. Operating at 440 kHz, the limitation of the minimum t_{SW} time is less significant. For example, if a 1.8-V output is required with a V_{IN} of 50 V:

$$\frac{1.8\,V}{50\,V} > 70ns \times 440kHz \quad (10)$$

0.036> 0.0308

7.3.9 Current Sense

There are two methods to sense the inductor current of the buck converter. The first is using current sense resistor in series with the inductor and the second is to use the dc resistance of the inductor (DCR sensing). Figure 24 illustrates inductor current sensing using a current sense resistor. This configuration continuously monitors the inductor current providing accurate current-limit protection. For the best current-sense accuracy and over current protection, use a low inductance ±1% tolerance current-sense resistor between the inductor and output, with a Kelvin connection to the LM5141-Q1 sense amplifier.

If the peak differential current signal sensed from CS to VOUT exceeds 75 mV, the current limit comparator immediately terminates the HO output for cycle-by-cycle current limiting.

$$R_{SENSE} = \frac{V_{(CS)}}{\left(I_{OUT(MAX)} + \frac{\Delta I}{2}\right)}$$

where

- $V_{(CS)}$ = 75 mV (11)

$I_{OUT(MAX)}$ is the over current set point which is set higher than the maximum load current to avoid tripping the over current comparator during load transients. ΔI is the peak-peak inductor ripple current.

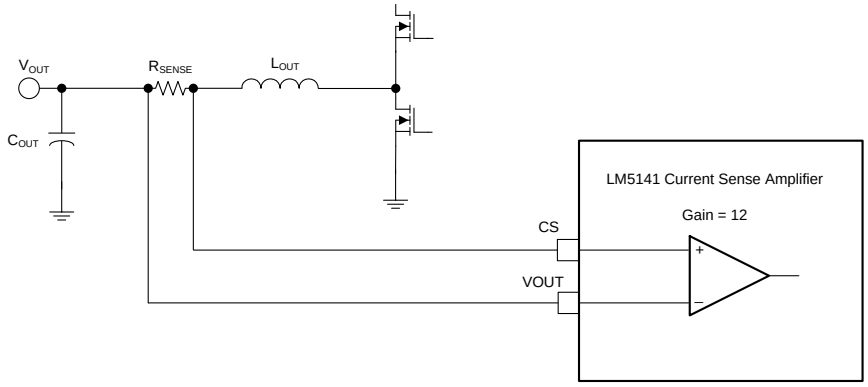


Figure 24. Current Sense

7.3.10 DCR Current Sensing

For high-power applications which do not require high accuracy current-limit protection, DCR sensing may be preferable. This technique provides lossless and continuous monitoring of the output current using an RC sense network in parallel with the inductor. Using an inductor with a low DCR tolerance, the user can achieve a typical current limit accuracy within the range of ±10% to ±15% at room temperature.

Components R_{CS} and C_{CS} in Figure 25 create a low-pass filter across the inductor to enable differential sensing of the voltage drop across inductor DCR. When $R_{CS} \times C_{CS}$ is equal to L_{OUT}/R_{DCR}, the voltage developed across the sense capacitor, C_{CS}, is a replica of the inductor DCR voltage waveform. Choose the capacitance of C_{CS} to be greater than 0.1 µF to maintain a low impedance sensing network, thus reducing the susceptibility of noise pickup from the switch node. Carefully observe the PCB layout guidelines to ensure the noise and DC errors do not corrupt the differential current-sense signals applied across the CS and VOUT pins.

The voltage drop across C_{CS}:

$$V_{CS}(s) = \frac{1 + \frac{sL_{OUT}}{R_{DCR}}}{1 + sR_{CS}C_{CS}} Ipk \times R_{DCR} \quad (12)$$

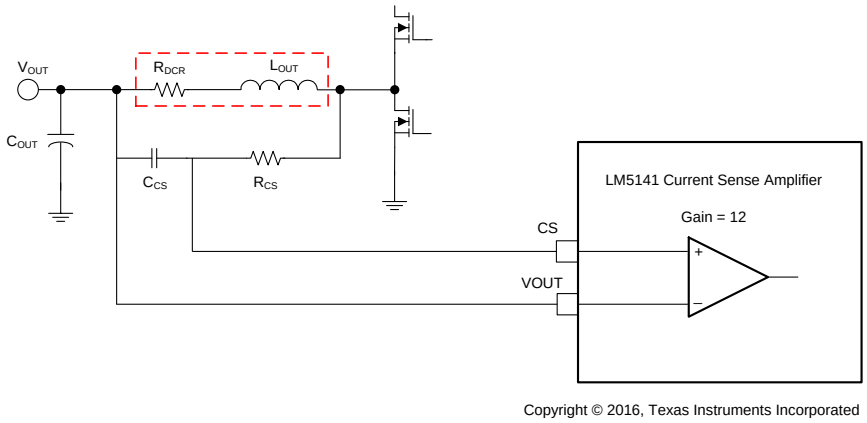


Figure 25. DCR Current Sensing

$R_{CS}C_{CS} = L_{OUT}/R_{DCR} \rightarrow$ accurate DC and AC current sensing

If the RC time constant is not equal to the L_{OUT}/L_{DRC} time constant there will be an error

$R_{CS}C_{CS} > L_{OUT}/R_{DCR} \rightarrow$ DC level still correct, the AC amplitude will be attenuated

$R_{CS}C_{CS} < L_{OUT}/R_{DCR} \rightarrow$ DC level still correct, the AC amplitude will be amplified

7.3.11 Error Amplifier and PWM Comparator

The LM5141-Q1 has a high-gain transconductance amplifier which generates an error current proportional to the difference between the feedback voltage and an internal precision reference (1.2 V). The output of the transconductance amplifier is connected to the COMP pin allowing the user to provide external control loop compensation. Generally for current mode control a type II network is recommended.

7.3.12 Slope Compensation

The LM5141-Q1 provides internal slope compensation to ensure stable operation with a duty cycle greater than 50%. To correctly use the internal slope compensation, the inductor value must be calculated based on the following guidelines (Equation 12 assumes an inductor ripple current of 30%):

$$L_{OUT} \geq \frac{V_{OUT}}{Fsw \times (0.3 \times I_{OUT})} \tag{13}$$

- Lower inductor values increase the peak-to-peak inductor current, which minimizes size and cost and improves transient response at the cost of reduced efficiency due to higher peak currents.
- Higher inductance values decrease the peak-to-peak inductor current typically increases efficiency by reducing the RMS current at the cost of requiring larger output capacitors to meet load-transient specifications.

7.3.13 Hiccup Mode Current Limiting

The LM5141-Q1 includes an optional hiccup mode protection function that is enabled when a capacitor is connected to the RES pin. In normal operation the RES capacitor is discharged to ground. If 512 consecutive cycles of cycle-by-cycle current limiting occur, the SS pin capacitor is pulled low and the HO and LO outputs are disabled (refer to Figure 26). A 20-μA current source begins to charge the RES capacitor.

When the RES pin charges to 1.2 V, the RES pin is pulled low and the SS capacitor begins to charge. The 512 cycle hiccup counter is reset if 4 consecutive switching cycles occur without exceeding the current limit threshold. The controller is in forced PWM (FPWM) continuous conduction mode when the DEMB pin is connected to VDDA. In this mode the SS pin is clamped to a level 200 mV above the feedback voltage to the internal error amplifier. This ensures that SS can be pulled low quickly during a brief overcurrent event and prevent overshoot of VOUT when the overcurrent condition is removed.

If DEMB=0 V, the controller operates in diode emulation with light loads (discontinuous conduction mode) and the SS pin is allowed to charge to VDDA. This reduces the quiescent current of the LM5141-Q1. If 32 or more cycle-by-cycle current limit events occur, the SS pin is clamped to 200 mV above the feedback voltage to the internal error amplifier until the hiccup counter is reset. Thus, if a momentary overload occurs that causes at least 32 cycles of current limiting, the SS capacitor voltage will be slightly higher than the FB voltage and will control VOUT during overload recovery.

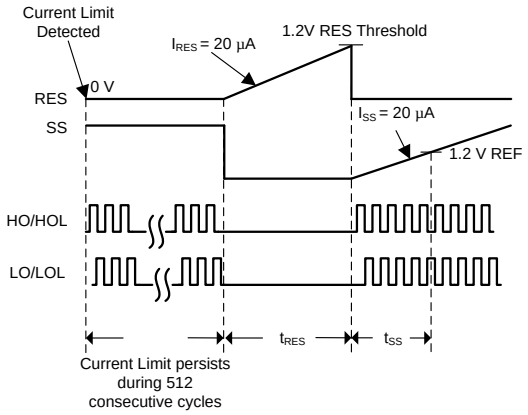


Figure 26. Hiccup Mode

7.3.14 Standby Mode

The LM5141-Q1 operates with peak current mode control such that the compensation voltage is proportional to the peak inductor current. During no-load or light load conditions, the output capacitor will discharge very slowly. As a result the compensation voltage will not demand a driver output pulses on a cycle-by-cycle basis. When the LM5141-Q1 controller detects that there have been 16 missing switching cycles, it enters Standby Mode and switches to a low IQ state to reduce the current drawn from VIN. For the LM5141-Q1 to go into a Standby Mode, the controller must be programmed for diode emulation (DEMB pin < 0.4 V). The typical IQ in Standby Mode is 35 µA with VOUT regulating at 3.3 V.

7.3.15 Soft-Start

The soft-start feature allows the controller to gradually reach the steady state operating point, thus reducing Start-up stresses and surges. The LM5141-Q1 regulates the FB pin to the SS pin voltage or the internal 1.2-V reference, whichever is lower. At the beginning of the soft-start sequence when SS = 0 V, the internal 20 µA soft-start current source gradually increases the voltage on an external soft-start capacitor connected to the SS pin, resulting in a gradual rise of the FB and output voltages. The controller is in the forced PWM (FPWM) mode when the DEMB pin is connected to VDDA. In this mode, the SS pin is clamped at 200 mV above the feedback voltage. This ensures that SS will be pulled low quickly when FB falls during brief over-current events to prevent overshoot of VOUT during recovery. SS can be pulled low with an external circuit to stop switching, but this is not recommended. Pulling SS low will result in COMP being pulled down internally as well. If the controller is operating in FPWM mode (DEMB = VDDA), LO will remain on and the low-side MOSFET will discharge the VOUT capacitor resulting in large negative inductor current. In contrast when the LM5141-Q1 pulls SS low internally due to a fault condition, the LO gate driver is disabled.

7.3.16 Diode Emulation

A fully synchronous buck controller implemented with a free-wheel MOSFET rather than a diode has the capability to sink negative current from the output in certain conditions such as light load, over-voltage, and pre-bias start-up. The LM5141-Q1 provides a diode emulation feature that can be enabled to prevent reverse (drain to source) current flow in the low-side free-wheel MOSFET. The diode emulation feature is configured with the DEMB pin. To enable diode emulation, connect the DEMB pin to ground. When configured for diode emulation, the low-side MOSFET is disabled when reverse current flow is detected. The benefit of this configuration is lower power loss at no load or light load conditions and the ability to turn on into a pre-biased output without discharging the output. The negative effect of diode emulation is degraded light load transient response times. Enabling the diode emulation feature is recommended to allow discontinuous conduction operation. If continuous conduction operation is desired, the DEMB pin should be tied to VDDA.

Table 2. DEMB Pin Modes

DEMB Pin	MODE
1	FPWM
0	DEMB
CLK	FPWM

7.3.17 High and Low Side Drivers

The LM5141-Q1 contains N-channel MOSFET gate drivers and an associated high-side level shifter to drive the external N-channel MOSFETs. The high-side gate driver works in conjunction with an external bootstrap diode D_{BST}, and bootstrap capacitor C_{BST} (refer to Figure 27). During the on-time of the low-side MOSFET, the SW pin voltage is approximately 0 V and C_{BST} is charged from VCC through the D_{BST}. A 0.1-µF or larger ceramic capacitor, connected with short traces between the HB and SW pin is recommended.

The LO and HO outputs are controlled with an adaptive dead-time methodology which ensures that both outputs (HO and LO) are never enabled at the same time, preventing cross conduction. When the controller commands LO to be enabled, the adaptive dead-time logic first disables HO and waits for the HO-SW voltage to drop below 2.5 V typical. LO is then enabled after a small delay (HO falling to LO rising delay). Similarly, the HO turn-on is delayed until the LO voltage has dropped below 2.5 V. HO is then enabled after a small delay (LO falling to HO rising delay). This technique ensures adequate dead-time for any size N-channel MOSFET device or parallel MOSFET configurations. Caution is advised when adding series gate resistors, as this may decrease the effective dead-time. Each of the high and low-side drivers have independent driver source and sink output pins. This allows the user to adjust drive strength to optimize the switching losses for maximum efficiency and to control the slew rate for reduced EMI. The selected N-channel high-side MOSFET determines the appropriate boost capacitance values C_{BST} in the Figure 27 according to Equation 13.

$$C_{BST} = \frac{Q_G}{\Delta V_{BST}} \tag{14}$$

Where Q_G is the total gate charge of the high-side MOSFET and ΔV_{BST} is the voltage variation allowed on the high-side MOSFET driver after turn-on. Choose ΔV_{BST} such that the available gate-drive voltage is not significantly degraded when determining C_{BST}. A typical range of ΔV_{BST} is 100 mV to 300 mV. The bootstrap capacitor should be a low-ESR ceramic capacitor. A minimum value of 0.1 µF to 0.47 µF is best in most cases. The gate threshold of the high-side and low-side MOSFETs should be a logic level variety approporiate for 5-V gate drive.

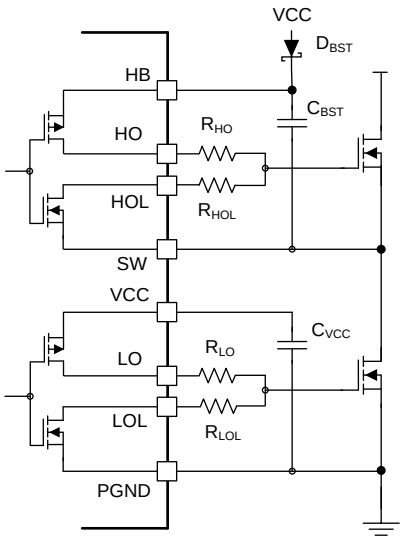


Figure 27. Drivers

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LM5141-Q1 is a synchronous buck controller used to convert a higher input voltage to a lower output voltage. The following design procedure can be used to select external component values. Alternately, the WEBENCH® software may be used to generate a complete design. The WEBENCH software uses an iterative design procedure and accesses a comprehensive database of components when generating a design. This section presents a simplified design process. In addition to the WEBENCH software the LM5141ADESIGN-CALC.xls quick start Excel calculator is available at www.ti.com.

8.2 Typical Application

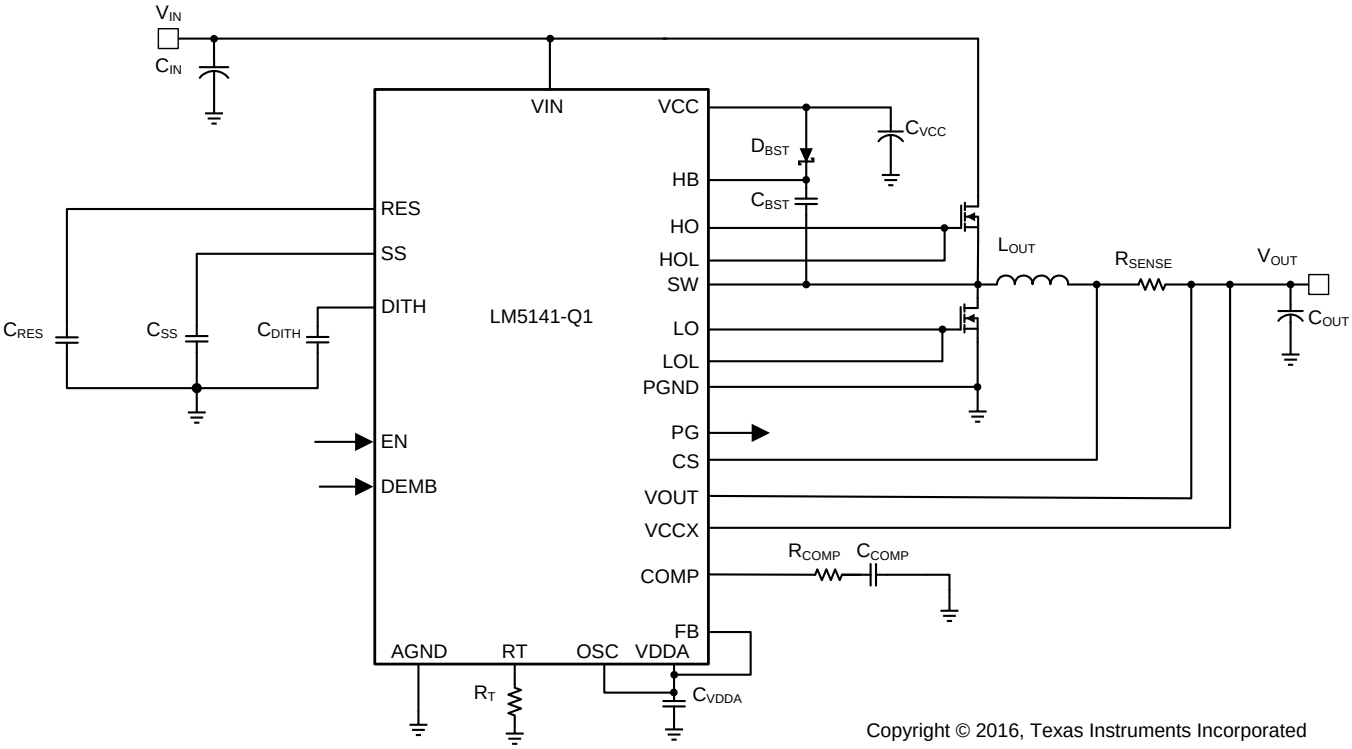


Figure 28. Typical Application Schematic

Typical Application (continued)

8.2.1 Design Requirements

For this design example, the intended input, output, and performance parameters are shown in Table 2.

Table 3. Design Requirements

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range (Steady State)	8 V to 18 V
V_{IN} maximum (Transient)	42 V
V_{IN} minimum (Cold Crank)	3.8 V
Output voltage	3.3 V
Output current	6 A
Operating frequency	2.2 MHz
Output voltage regulation	±1%
Standby current, one output enabled, no-load	< 35 µA
Shutdown Current	10 µA

8.2.2 Detailed Design Procedure

- Buck Inductor value
- Calculate the peak inductor current
- Current Sense resistor value
- Output capacitor value
- Input filter
- MOSFET selection
- Control Loop design

8.2.3 Inductor Calculation

For peak current mode control, sub-harmonic oscillation occurs with a duty cycle greater than 50% and is characterized by alternating wide and narrow pulses at the SW pin. By adding a slope compensating ramp equal to at least one-half the inductor current down-slope, any tendency toward sub-harmonic oscillation is damped within one switching cycle. For design simplification, the LM5141-Q1 has an internal slope compensation ramp added to the current sense signal.

For the slope compensation ramp to dampen sub-harmonic oscillation, the inductor value should be calculated based on the following guidelines (equation 15 assumes an inductor ripple current 30%):

$$L_{OUT} \geq \frac{V_{OUT}}{Fsw \times (0.3 \times I_{OUT})} \tag{15}$$

- Lower inductor values increase the peak-to-peak inductor current, which minimizes size and cost and improves transient response at the expense of reduced efficiency due to higher peak currents.
- Higher inductance values decrease the peak-to-peak inductor current, which typically increases efficiency by reducing the RMS current but requires larger output capacitors to meet load-transient specifications.

$$L_{OUT} \geq \frac{3.3\,V}{2.2MHz \times (0.3 \times 6\,A)}$$
$$L_{OUT} \geq 0.833\mu H \tag{16}$$

A standard inductor value of 1.5 µH was selected

$$D_{MAX} = \frac{V_{OUT}}{V_{IN(MIN)}} = \frac{3.3\,V}{8\,V} = 0.413 \tag{17}$$

$$D_{MIN} = \frac{V_{OUT}}{V_{IN(MAX)}} = \frac{3.3\,V}{18\,V} = 0.183 \quad (18)$$

The peak-to-peak inductor current is:

$$\Delta I = \frac{V_{IN(MAX)} - V_{OUT}}{L_{OUT}} \times \frac{D_{MIN}}{Fsw} \quad (19)$$

$$\Delta I = \frac{18\,V - 3.3\,V}{1.5\,\mu H} \times \frac{0.183}{2.2MHz} = 0.815\,A \quad (20)$$

$$Ipk = I_{OUT} + \frac{\Delta I}{2} \quad (21)$$

$$Ipk = 6\,A + \frac{0.815}{2} = 6.41A \quad (22)$$

8.2.4 Current Sense Resistor

When calculating the current sense resistor, the maximum output current capability ($I_{OUT(MAX)}$) should be at least 20% higher than the required full load current to account for tolerances, ripple current, and load transients. For this example, 120% of the 6.41 A peak inductor current calculated in the previous section (Ipk) is 7.69 A. The current sense resistor value can be calculated using:

$$R_{SENSE} = \frac{V_{(CS)}}{I_{OUT(MAX)}} \quad (23)$$

$$R_{SENSE} = \frac{75\,mV}{7.69\,A} = 0.00975\,\Omega$$

where

- $V_{(CS)}$ is the 75 mV current limit threshold (24)

The R_{SENSE} value selected is 9 mΩ

Carefully observe the PCB layout guidelines to ensure that noise and DC errors do not corrupt the differential current sense signals between the CS and VOUT pins. Place the sense resistor close to the devices with short, direct traces, creating Kelvin-sense connections between the current-sense resistor and the LM5141-Q1.

The propagation delays through the current limit comparator, logic, and external MOSFET gate drivers allow the peak current to increase above the calculated current limit threshold. For a propagation delay of t_{dly}, the worst case peak current through the inductor with the output shorted can be calculated from:

$$Ipk_{SCKT} = \frac{V_{(CS)}}{R_{SENSE}} + \frac{V_{IN(MAX)} \times t_{dly}}{L_{OUT}} \quad (25)$$

From the Electrical Characterization Table, t_{dly} is typically 40 ns.

$$Ipk_{SCKT} = \frac{75\,mV}{0.009\Omega} + \frac{18\,V \times 40\,ns}{1.5\,\mu H} = 8.81A \quad (26)$$

Once the peak current and the inductance parameters are known, the inductor can be chosen. An inductor with a saturation current greater than Ipk_{SCKT} (8.81 Apk) should be selected.

8.2.5 Output Capacitor

In a switch mode power supply, the minimum output capacitance is typically selected based on the capacitor ripple current rating and the load transient requirements. The output capacitor must be large enough to absorb the inductor energy and limit over voltage when transitioning from full-load to no-load, and to limit the output voltage undershoot during no-load to full load transients. The worst-case load transient from zero to full load occurs when the input voltage is at the maximum value and a current switching cycle has just finished. The total output voltage drop ΔV_{OUT} is the sum of the voltage drop while the inductor is ramping up to support the full load and the voltage drop before the next pulse can occur.

The output capacitance required to maintain the minimum output voltage drop (ΔV_{OUT}) can be calculated as follows:

$$C_{OUT(MIN)} = \frac{L_{OUT} \times I_{STEP}^2}{2 \times \Delta V_{OUT} \times D_{MAX} \times \left(V_{IN(MIN)} - V_{OUT}\right)} \quad (27)$$

$$C_{OUT(MIN)} = \frac{1.5\,\mu H \times 4\,A^2}{2 \times 33\,mV \times 0.413 \times \left(8\,V - 3.3\,V\right)} = 186\,\mu F$$

where

- I_{STEP} = 4 A
- ΔV_{OUT} = 1% of 3.3 V, or 33 mV (28)

For this example a total of 211 µF of capacitance is used, two 82-µF aluminum capacitors for energy storage and one 47 µF low ESR ceramic capacitor to reduce high frequency noise.

Generally, when sufficient capacitance is used to satisfy the undershoot requirement, the overshoot during a full-load to no-load transient will also be satisfactory. After the output capacitance has been selected, calculate the output ripple current and verify that the ripple current is within the capacitor ripple current ratings.

$$I_{OUT(RMS)} = \frac{\Delta I}{\sqrt{12}} \quad (29)$$

$$I_{OUT(RMS)} = \frac{0.815\,A}{\sqrt{12}} = 0.235\,A \quad (30)$$

8.2.6 Input Filter

A power supply input typically has a relatively high source impedance at the switching frequency. Good quality input capacitors are necessary to limit the ripple voltage at the VIN pin while supplying most of the switch current during the buck switch on-time. When the buck switch turns on, the current drawn from the input capacitor steps from zero to the valley of the inductor current waveform, then ramps up to the peak value, and then drops to the zero at turn-off.

Average input current can be calculated from the total input power required to support the load at V_{OUT}:

$$P_{IN} = \frac{V_{OUT} \times I_{OUT}}{\eta} \quad (31)$$

The efficiency (η) is assumed to be 83% for this design example, yielding a total input power:

$$P_{IN} = \frac{3.3\ V \times 6\,A}{0.83} = 23.86\,W \quad (32)$$

$$I_{avg} = \frac{P_{IN}}{V_{IN(MIN)}} \quad (33)$$

$$I_{avg} = \frac{28.6\,W}{8\,V} = 3.58\,A \quad (34)$$

The input capacitors should be selected with sufficient RMS current rating and the maximum voltage rating.

$$I_{IN(RMS)} = \sqrt{\left[\left(Ipk - I_{avg}\right)^2 + \frac{\Delta I^2}{12}\right] x D_{MAX} + \left(I_{avg}^2 \times \left(1 - D_{MAX}\right)\right)} \quad (35)$$

$$I_{IN(RMS)} = \sqrt{\left(6.41A - 3.58\,A\right)^2 + \frac{0.815^2}{12} \times 0.413 + \left(3.58\,A^2 \times \left(1 - 0.413\right)\right)} = 2.93\,A \quad (36)$$

8.2.6.1 EMI Filter Design

EMI Filter Design Steps:

- Calculate the required attenuation
- Capacitor C_{IN} represents the existing capacitor at the input of the switching converter (10 µF was used for this application)
- Inductor LF is usually selected between 1 µH and 10 µH (1.8 µH was used for this application), but can be smaller to reduce losses in a high current design
- Calculate capacitor C_F

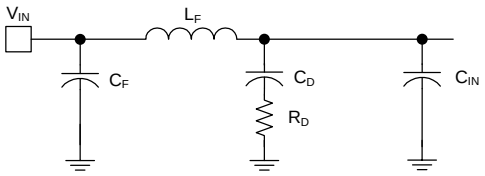


Figure 29. Input EMI Filter

By calculating the first harmonic current from the Fourier series of the input current waveform and multiplying it by the input impedance (the impedance is defined by the existing input capacitor C_{IN}), a formula can be derived to obtain the required attenuation:

$$\left|Attn\right| = 20 \times \log\left[\frac{\frac{Ipk}{\pi^2 \times F_{SW} \times C_{IN}} \times \sin\left(\pi \times D_{MAX}\right)}{1\,\mu V}\right] - V_{MAX} \tag{37}$$

$$\left|Attn\right| = 20\log\left[\frac{\frac{6.41A}{\pi^2 \times 2.2MHz \times 10\,\mu F} \times \sin\left(\pi \times 0.413\right)}{1\mu V}\right] - 45\ dB\mu V = 44.07\,dB \tag{38}$$

V_{MAX} is the allowed dBµV noise level for the particular EMI standard. C_{IN} is the existing input capacitors of the Buck converter, for this application 10 µF was selected. D_{MAX} is the maximum duty cycle, Ipk is the inductor current, the current at the input can be modeled as a square wave, F_{SW} is the switching frequency.

$$C_F = \frac{1}{L_F}\left[\frac{10^{\frac{|Attn|}{40}}}{2 \times \pi \times F_{SW}}\right]^2 \tag{39}$$

$$C_F = \frac{1}{1.8\,\mu H}\left(\frac{10^{\frac{44.07}{40}}}{2 \times \pi \times 2.2MHz}\right)^2 = 0.47\,\mu F \tag{40}$$

For this application, C_F was chosen to be 1 µF. Adding an input filter to a switching regulator modifies the control-to output transfer function. The output impedance of the filter must be sufficiently small such that the input filter does not significantly affect the loop gain of the buck converter. The impedance of the filter peaks at the filter resonant frequency.

$$F_R = \frac{1}{2 \times \pi \sqrt{L_F C_{IN}}} \tag{41}$$

$$F_R = \frac{1}{2 \times \pi \sqrt{1.8\,\mu H \times 10\,\mu F}} = 37.53\,kHz \tag{42}$$

Referring to Figure 29, the purpose of R_D is to reduce the peak output impedance of the filter at the cutoff frequency. The capacitor C_D blocks the dc component of the input voltage, and avoids excessive power dissipation on R_D. The capacitor C_D should have lower impedance than R_D at the resonant frequency, with a capacitance value greater than 5 times the filter capacitor C_{IN}. This will prevent it from interfering with the cutoff frequency of the main filter. Added damping is needed when the output impedance is high at the resonant frequency (Q) of filter formed by C_{IN} and L_F is too high):

An electrolytic cap C_D can be used as damping device, with value:

$$R_D = \sqrt{\frac{L_F}{C_{IN}}} \tag{43}$$

For this design C_D = 47 µF was selected

$$R_D = \sqrt{\frac{1.8\,\mu H}{10\,\mu F}} = 0.424\,\Omega \tag{44}$$

8.2.6.2 MOSFET Selection

The LM5141-Q1 gate drivers are powered by the internal 5-V VCC bias regulator. To reduce power dissipation in the controller and improve efficiency, the VCCX pin should be connected to the 5-V output or an external 5 V bias supply. The MOSFETs used with the LM5141-Q1 require a logic-level gate threshold with $R_{DS(ON)}$ specified with V_{GS} = 4.5 V or lower.

The MOSFETs must be chosen with a V_{DS} rating to withstand the maximum V_{IN} voltage plus supply voltage transients and spikes (ringing). For automotive applications, the maximum V_{IN} occurs during a load dump and the voltage can surge up to 42 V under some conditions. A MOSFET with a V_{DS} rating of 60 V would meet most application requirements. The N-channel MOSFETs must be capable of delivering the load current plus peak ripple current during switching.

The high-side MOSFET losses are associated with the $R_{DS(ON)}$ of the MOSFET and the switching losses.

$$P_{D(HS)} = \left(I_{OUT}{}^2 \times R_{DS(ON)} \times D_{MAX}\right) + \frac{1}{2} \times V_{IN} \times \left(t_r + t_f\right) \times I_{OUT} \times F_{SW} \tag{45}$$

$$P_{D(HS)} = \left((6\,A)^2 \times 0.026\,\Omega \times 0.413\right) + \frac{1}{2} \times 12\,V \times \left(17\,ns + 17\,ns\right) \times 6\,A \times 2.2\,MHz = 2.69\,W$$

where

- tr = ts = 17 ns (46)

The losses in the low side MOSFET include: $R_{DS(ON)}$ losses, dead time losses, and losses in the MOSFETs internal body diode. The body diode conducts the inductor current during the dead time before the rising edge of the switch node; minority carriers are injected into and stored in the diode PN junction when forward biased. As the high side FET starts to turn-on, a negative current must first flow through the diode to remove the stored charge before the diode can block a reverse voltage. During this time, the high side drain-source voltage remains at V_{IN} until all the diode minority carriers are removed. Then, the diode begins to block negative voltage and the reverse current continues to flow to charge the body diode depletion capacitance. The total charge involved in this period is called reverse-recovery charge Qrr.

$$P_{D(LO)} = \left(I_{OUT}{}^2 \times R_{DS(ON)} \times (1 - D_{MAX})\right) + \left(I_{OUT} \times (t_{dr} + t_{df})\right) \times F_{SW} \times V_{D(FET)} + \left(D_{Qrr} \times F_{SW} \times V_{IN}\right) \tag{47}$$

$$P_{D(LO)} = \left((6A)^2 \times 26\,m\Omega \times (1 - 0.413)\right) + \left(6\,A \times (20\,ns + 20\,ns)\right) \times 2.2\,MHz \times 0.8\,V + (105\,nC \times 2.2\,MHz \times 12\,V) = 3.744\,W$$

where

- t_{dr} and t_{df} are the switch node voltage rise and fall times (20 ns)
- $V_{D(FET)}$ is the forward voltage drop across the low-side MOSFET internal body diode (0.8 V)
- D_{Qrr} is the internal body diodes reverse recovery charge (105 nC)
- $R_{DS(ON)}$ is the on resistance of the MOSFETs (26 mΩ at T_J = 125ºC) (48)

Table 4 provides parameters for several MOSFETs that have tested in the LM5141-Q1 evaluation module.

Table 4. EVM MOSFETs

Manufacture	Part Number	V_{DS} (V)	I_D (A)	$Q_{g(MAX)}$ (nC) V_{GS} = 4.5 V	$R_{DS(ON)}$ V_{GS} = 4.5 V (Ω)	$C_{OSS(MAX)}$ (pF)	Application
VISHAY	SQJ850EP	60	24	30	32	215	Automotive High Power
VISHAY	SQ7414EN	60	5.6	25	36	175	Automotive Low Power
Texas Instruments	CDS18534Q5A	60	13	11.1	12.4	217	Industrial

8.2.6.3 Driver Slew Rate Control

Figure 30 shows the high current driver outputs with independent source and current sink pins for slew rate control. Slew rate control enables the user to adjust the switch node rise and fall times which can reduce the conducted EMI in the FM radio band (30 MHz to 108 MHz). Using the LM5141-Q1 EVM, conducted emissions were measured in accordance with CISPR 25 Class 5. Figure 31 shows the measured results without slew rate control.

The conducted EMI results with slew rate control are shown in Figure 32, a 10-dB reduction in conduction emissions in the FM band is attained by using slew rate control. This can help reduce the size and cost of the EMI filters.

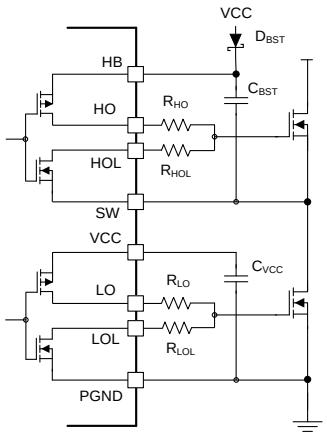


Figure 30. Drivers with Slew Rate Control

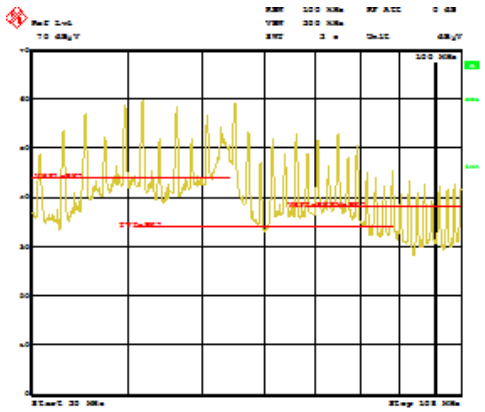


Figure 31. EMI Measurements CISPR 25 Class 5, Without Slew Rate Control

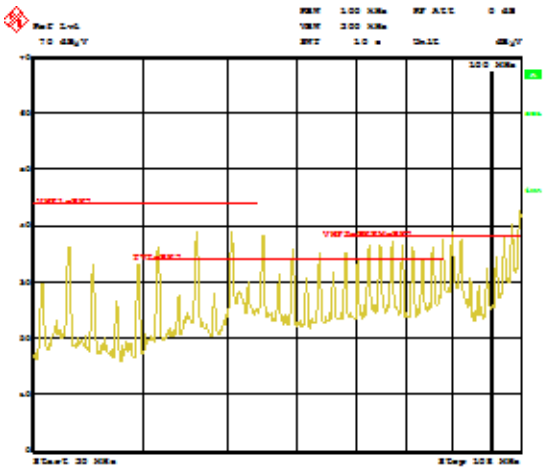


Figure 32. EMI Measurements CISPR 25 With Slew Rate Control

8.2.6.4 Frequency Dithering

Figure 33 shows the CISPR 25 Class 5 conducted emission test run on the LM5141-Q1EVM, without the Dither feature enabled. The first harmonic (peak measurement) is 48 dBµV, Figure 34 shows the conducted emissions test results with the Dither feature enabled. With the Dither featured enabled, the first harmonic (peak measurement) was lowered to 40 dBµV, an 8 dB reduction.

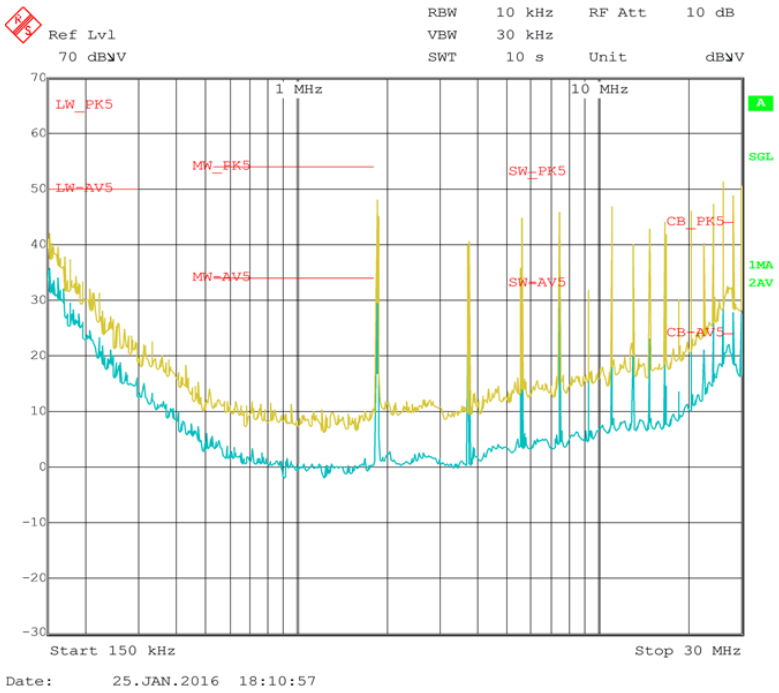


Figure 33. CISPR 25 Class 5 Conducted EMI, Without Dither

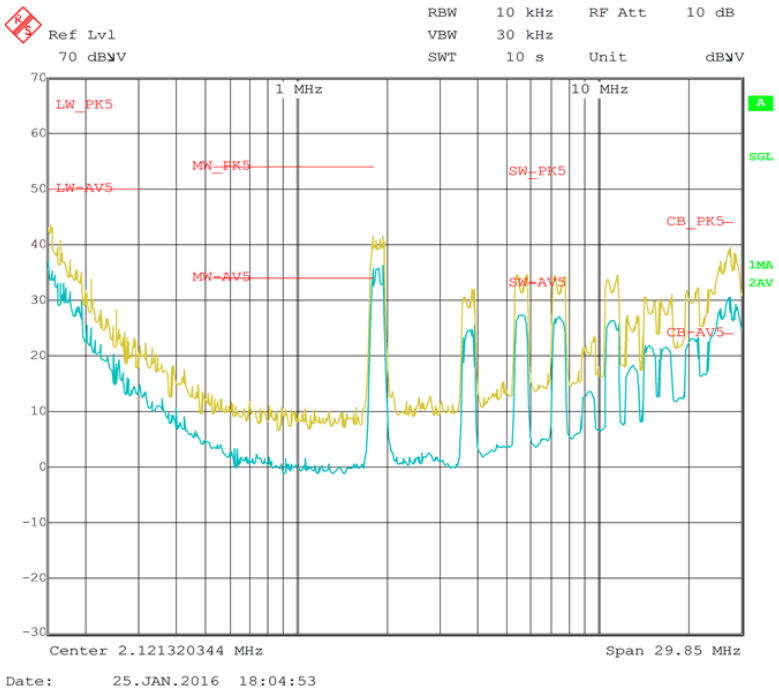


Figure 34. CISPR 25 Class 5 With Dither

8.2.7 8.9 Control Loop

The open loop gain is defined as the product of modulator transfer function and feedback transfer function. When plotted on a dB scale, the open loop gain is shown as the sum of modulator gain and feedback gain.

DC modulator gain is:

$$AM = \frac{R_{LOAD}}{(R_{SENSE} + R_{DCR}) \times G_{CS}} \tag{49}$$

The modulator gain plus power stage transfer function with an embedded current loop is show in Equation 50. The equation includes the sample gain at F_{SW} /2 (ω_n), which is caused by sampling effect of current mode control.

$$\frac{\hat{V}_{OUT}}{\hat{V}_C(s)} = AM \times \frac{\left(1 + \frac{s}{\omega_Z}\right)}{\left(1 + \frac{s}{\omega_P}\right) \times \left(1 + \frac{s}{\omega_n Q} + \frac{s^2}{\omega_n^2}\right)}$$

where

- $s = 2 \times \pi \times F_{SW}$
- $Q = \frac{1}{\pi(K - 0.5)}$
- $\omega_Z = \frac{1}{C_{ESR} \times C_{OUT}}$
- $\omega_p = \frac{1}{R_{LOAD} \times C_{OUT}}$
  $\omega_n = \pi \times F_{SW}$
- K = 1
- G_{CS} is the current sense amplifier gain which is 12 (50)

Because the loop cross over frequency is well below sample gain effects, Equation 50 can be simplified as one pole and a one zero system as shown in Equation 51.

$$\frac{\hat{V}_{OUT}(s)}{\hat{V}_C(s)} = AM \times \frac{\left(1+\frac{s}{\omega_Z}\right)}{\left(1+\frac{s}{\omega_p}\right)} \tag{51}$$

R_{LOAD} is the load resistance

R_{DCR} is the dc resistance on the output inductor which is 8.1 mΩ

R_{SENSE} is the current sense resistance which is 9 mΩ

8.2.7.1 Feedback Compensator

A type II compensator using an transconductance error amplifier (EA), Gm, is shown in Figure 35. The dominant pole of the EA open-loop gain is set by the EA output resistance, R_{AMP}, and effective bandwidth-limiting capacitance, C_O, as follows:

$$G_{EA(openloop)}(s) = -\frac{GmR_{AMP}}{1+sR_{AMP}C_O} \tag{52}$$

The EA high frequency pole is neglected in the above expression. The compensator transfer function from output voltage to COMP, including the gain contribution from the feedback resistor divider network is:

$$G_C(s) = \frac{\hat{V}_C(s)}{\hat{V}_{OUT}(s)} = -\frac{V_{REF}}{V_{OUT}} \times Gm \times Z_{EAOUT}(s) \tag{53}$$

$$\frac{R_{LOWER}}{R_{LOWER}+R_{UPPER}} = \frac{V_{REF}}{V_{OUT}} \tag{54}$$

where

$$Z_{EAOUT}(s) = Gm \times \left(R_{AMP} \left\| \left(R_{COMP} + \frac{1}{sC_{COMP}}\right) \right\| \frac{1}{sC_{HF}} \right\| \frac{1}{sC_O}\right) \tag{55}$$

Which simplifies to:

$$Z_{EAOUT}(s) = R_{AMP} \frac{1+\frac{s}{\omega_{zEA}}}{\left(1+\frac{s}{\omega_{pEA1}}\right)+\left(1+\frac{s}{\omega_{pEA2}}\right)} \tag{56}$$

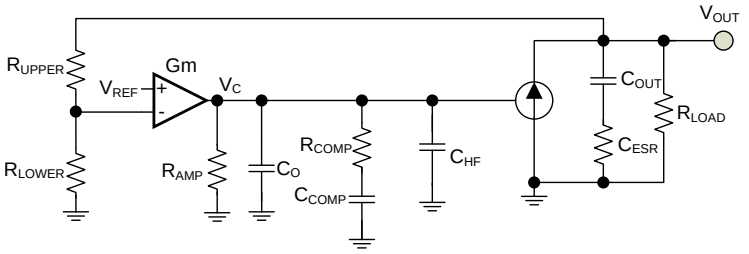


Figure 35. Transconductance Amplifier

$$\omega_{zEA} = \frac{1}{R_{COMP} \times C_{COMP}} \quad (57)$$

$$\omega_{pEA1} = \frac{1}{(R_{AMP} + R_{COMP})(C_{COMP} + C_{HF} + C_O)} \cong \frac{1}{R_{AMP} \times C_{COMP}} \quad (58)$$

$$\omega_{pEA2} = \frac{1}{R_{COMP}\left(C_{COMP} \| (C_{HF} + C_O)\right)} \cong \frac{1}{R_{COMP} \times C_{HF}} \quad (59)$$

Typically R_{COMP} << R_{AMP} and C_{COMP} >> (C_{HF} + C_O) so the approximations are valid.

where

V_{REF} is the feedback voltage reference (1.2 V)

G_m is the error amplifier gain transconductance (1200 µS)

R_{AMP} is the error amplifier output impedance (2.5 MΩ)

The error amplifier compensation components create a pole at the origin, a zero, and a high frequency pole.

The procedure for choosing compensation components for a stable closed loop is:

- Select the desired open loop gain crossover frequency (fc); for this application 30 kHz was chosen
- Calculate the R_{COMP} resistor for the gain crossover frequency at 30 kHz

$$R_{COMP} = fc \frac{V_{OUT}}{V_{REF}} \times \frac{2 \times \pi \times C_{OUT} \times (R_{SENSE} + R_{DCR}) \times G_{CS}}{Gm} \quad (60)$$

$$R_{COMP} = 30KHz \times \frac{3.3V}{1.2V} \times \frac{2 \times \pi \times 293\mu F \times (0.009\Omega + 0.0081\Omega) \times 12}{1200 \times 10^{-6} \mu S} = 25927\Omega \quad (61)$$

  The value selected for R_{COMP} is 22.6 kΩ.

  where

  R_{DCR} = 0.0081 Ω

- Calculate the C_{COMP} capacitor value to create a zero that cancels the pole ω_p (ω_p = 1/R_{LOAD} × C_{OUT})

$$C_{COMP} = \frac{R_{LOAD} \times C_{OUT}}{R_{COMP}} \quad (62)$$

$$C_{COMP} = \frac{0.477\Omega \times 290\mu F}{22.6k\Omega} = 6nF \quad (63)$$

  The value selected for C_{COMP} is 10nF.

8.2.8 Application Curves

The Bode Plots of the modulator and plus power stage are shown in refer to Figure 36. The results of the total loop gain crossover frequency are 40 kHz with 112º of phase margin, (see Figure 37).

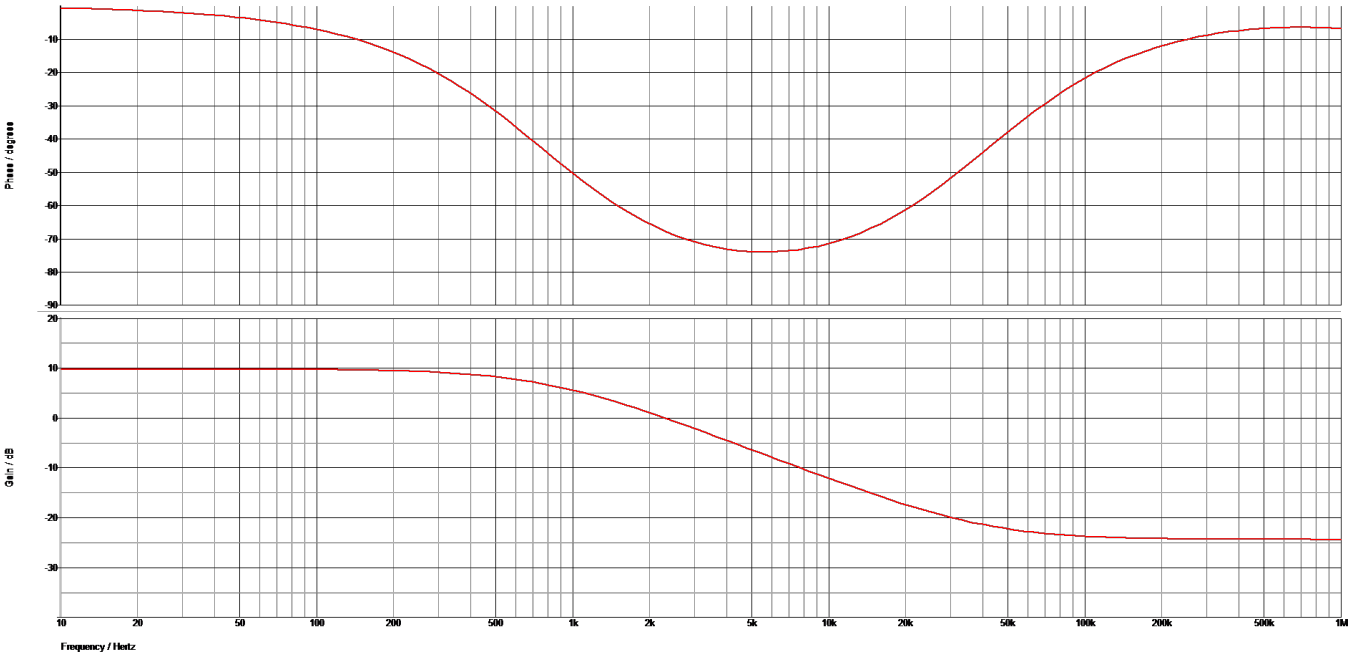


Figure 36. (V_{OUT}/V_C) Modulator Gain and Phase

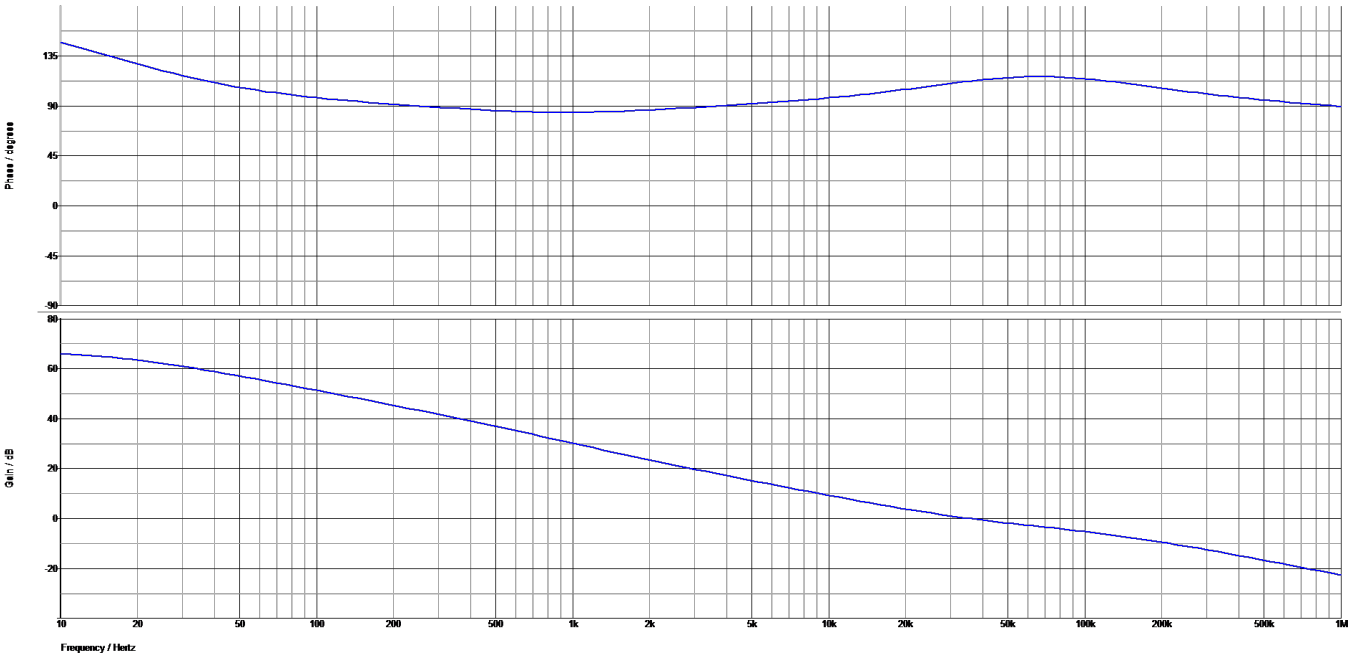


Figure 37. Loop Gain and Phase

9 Power Supply Recommendations

The LM5141-Q1EVM was designed to operate over an input voltage supply range between 5.5 V and 42 V. The input supply must be well regulated. If the power source is located more than a few inches from the LM5141-Q1 EVM, additional bulk capacitance and ceramic bypass capacitors may be required at the power supply input. An electrolytic capacitor with a value of 47 μF is typically a good choice.

10 Layout

10.1 Layout Guidelines

Careful PCB layout is critical to achieve low EMI and stable power supply operation. Make the high frequency current loops as small as possible, and follow these guidelines of good layout practices:

1. Keep the high-current paths short. This is essential for stable, jitter-free operation.
2. Keep the power traces and load connections short. This is essential for high efficiency. Using 2 oz or thicker copper can enhance full load efficiency.
3. Minimize current-sensing errors by routing CS and VOUT using a kelvin sensing directly across the current sense resistor (R_{SENSE}).
4. Route high-speed switching nodes (HB, HO, LO, and SW) away from sensitive analog signals (FB, CS, and VOUT).

10.1.1 Layout Procedure

Place the power components first, with ground terminals adjacent to the low-side FET.

- Mount the controller IC as close as possible to the high and low-side MOSFETs. Make the grounds and high and low-sided drive gate drive lines as short and wide as possible. Place the series gate drive resistor as close to the MOSFET as possible to minimize gate ringing.
- Locate the gate drive components (D1 and C12) together and near the controller IC; refer to Figure 38. Be aware that peak gate drive currents can be as high as 4 A. Average current up to 75 mA can flow from the VCC pin to the V_{CC} capacitor through the bootstrap diode to the bootstrap capacitor. Size the traces accordingly.
- Figure 39 shows the high frequency loops of the synchronous buck converter. The high frequency current flows through Q1 and Q2, through the power ground plane and back to V_{IN} through the ceramic capacitors C6, C7, and C8. This loop must be as small as possible to minimize EMI. Refer to Figure 41 and Figure 42 for the recommended PCB layout.
- Make the PGND and AGND connections to the LM5141-Q1 controller as shown in Figure 40. Create a power grounds directly connected to all high-power components and an analog ground plane for sensitive analog components. The analog ground plane (AGND) and power ground plane (PGND) must be connected at a single point directly under the IC (at the die attach pad or DAP).

10.2 Layout Examples

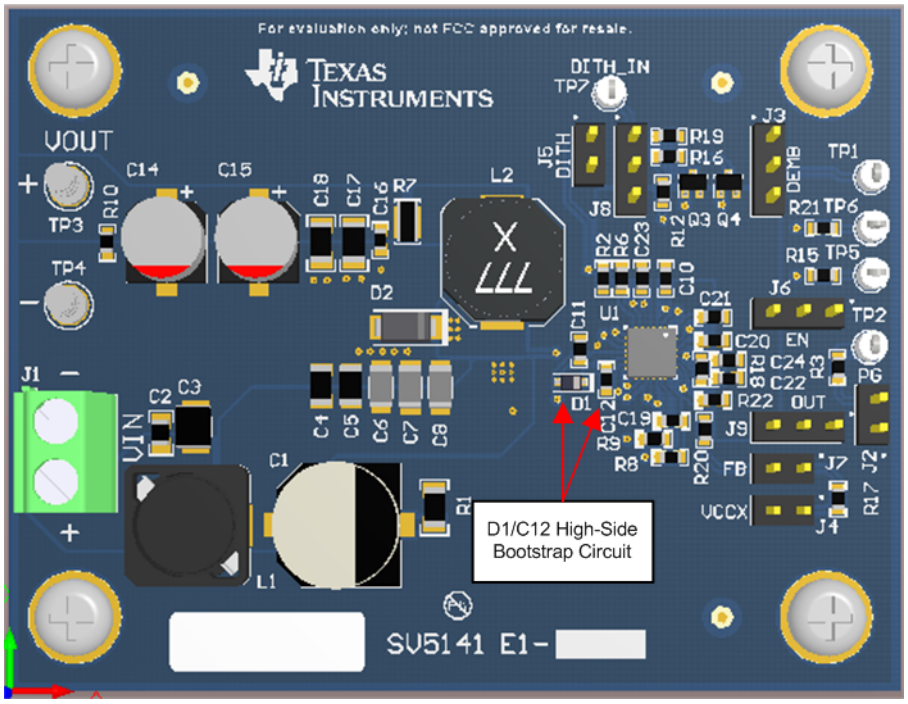


Figure 38. EVM Top Side

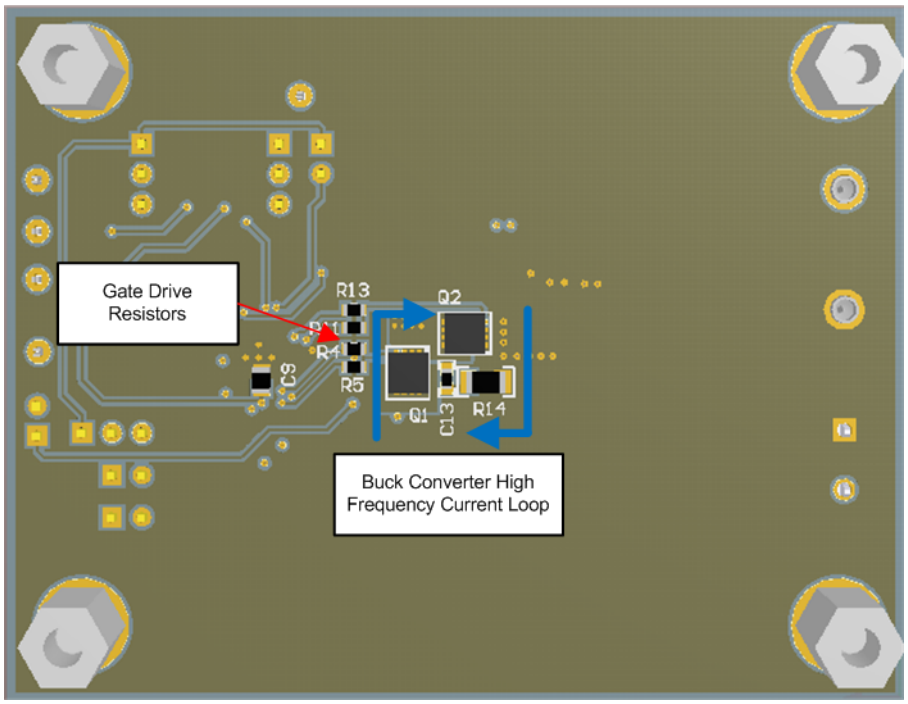


Figure 39. EVM Bottom Layer, High Frequency Current Loop

Layout Examples (continued)

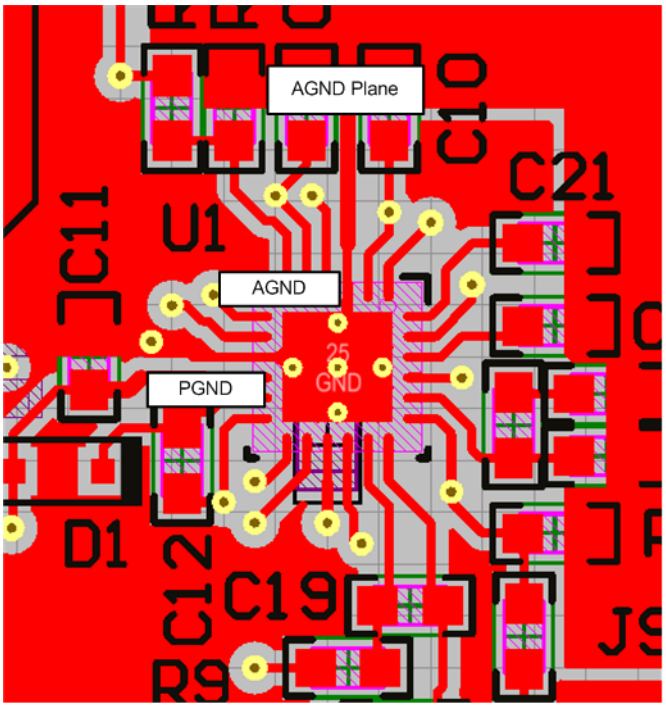


Figure 40. AGND and PGND Connections

Figure 41 and Figure 42 show the Top and Bottom layer of the LM5141-Q1 EVM.

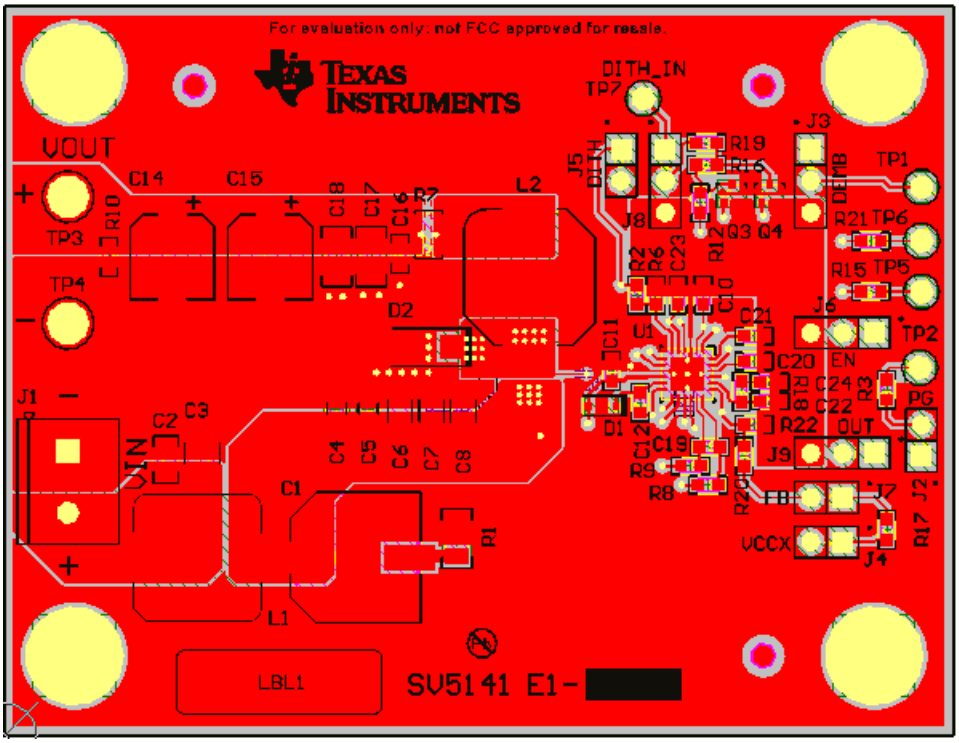


Figure 41. EVM Top Layer

Layout Examples (continued)

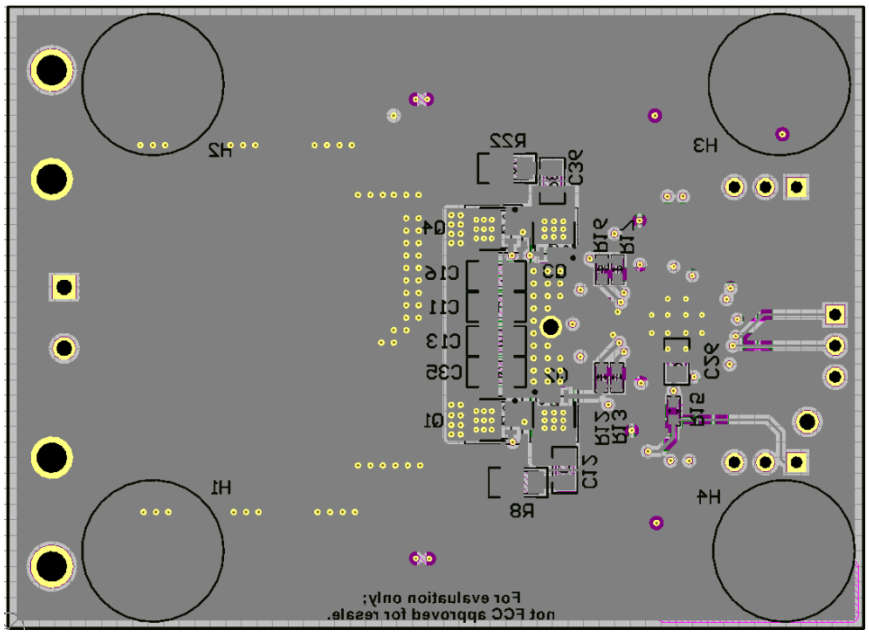


Figure 42. EVM Bottom Layer

11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

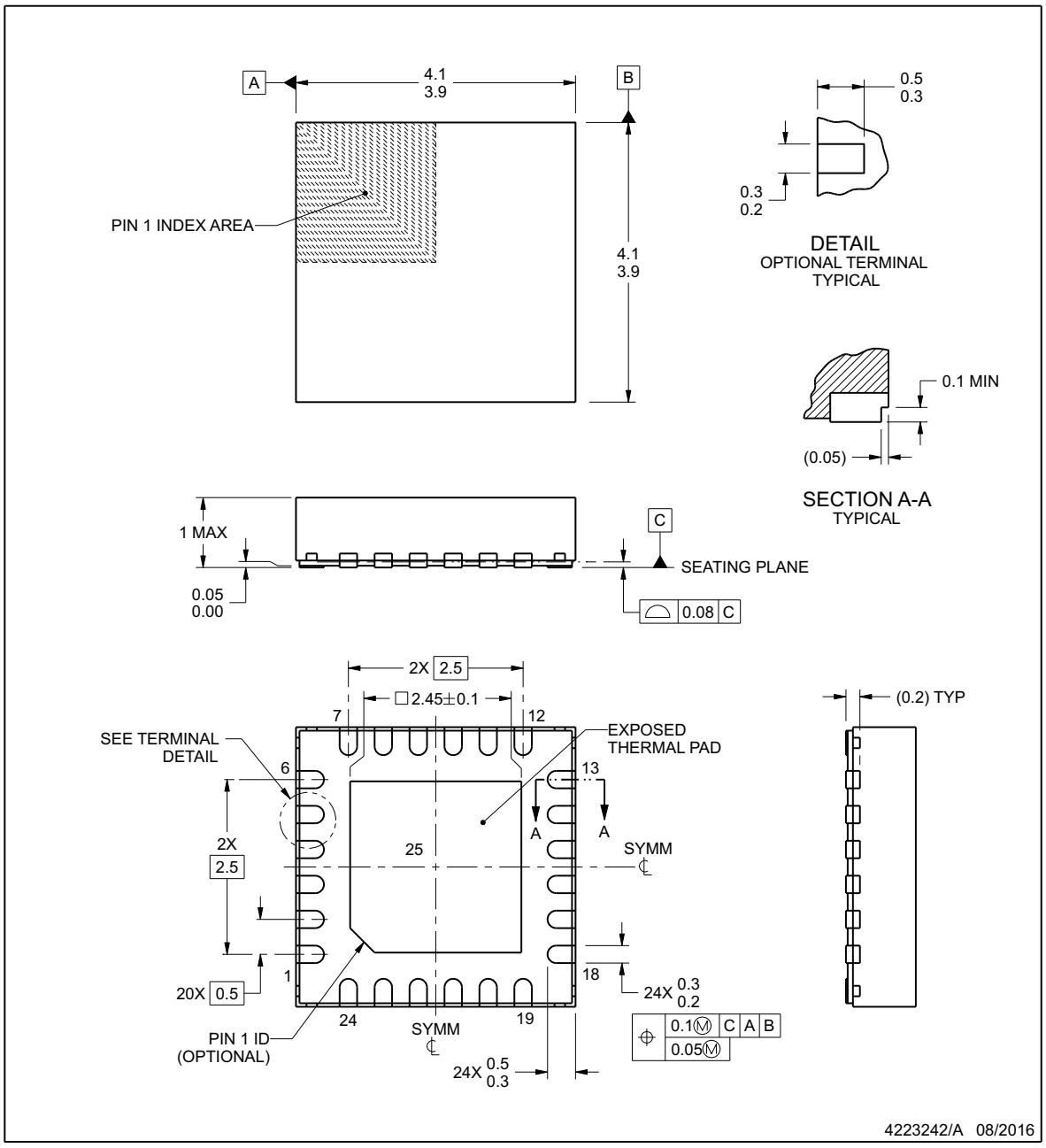
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OUTLINE

RGE0024J

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



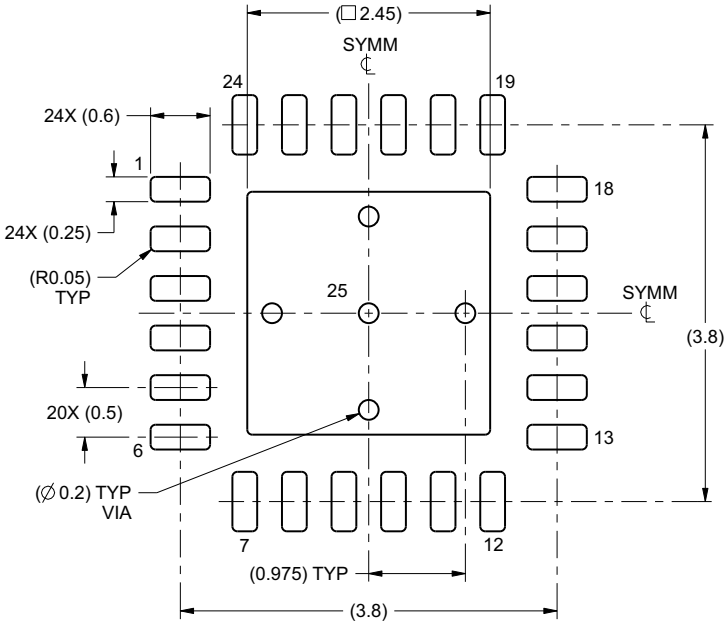
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

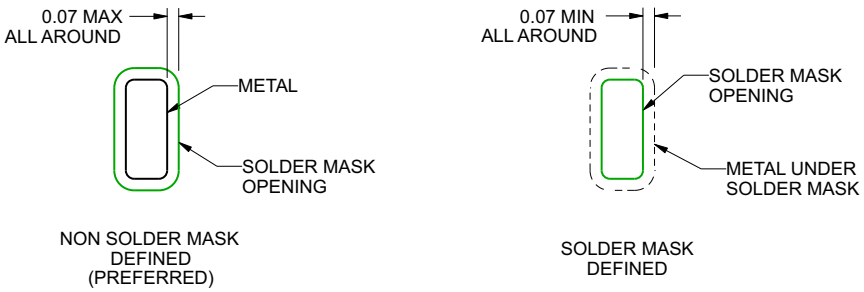
EXAMPLE BOARD LAYOUT

RGE0024J — **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SCALE:15X



SOLDER MASK DETAILS

4223242/A 08/2016

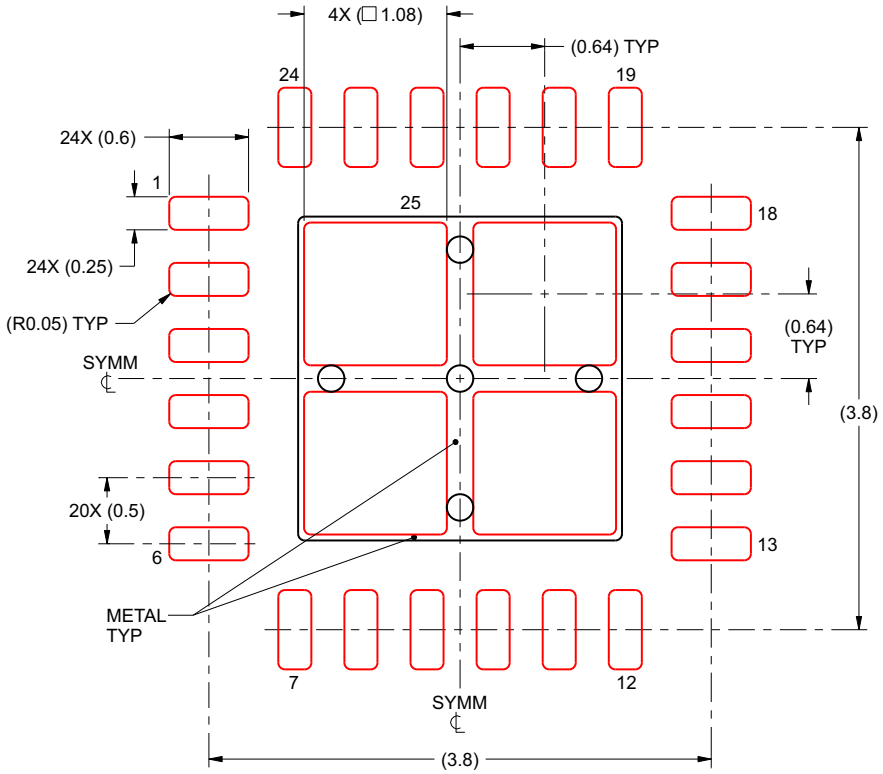
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RGE0024J **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 25
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4223242/A 08/2016

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM5141QRGERQ1	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 150	LM5141 RGEQ1	Samples
LM5141QRGETQ1	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 150	LM5141 RGEQ1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

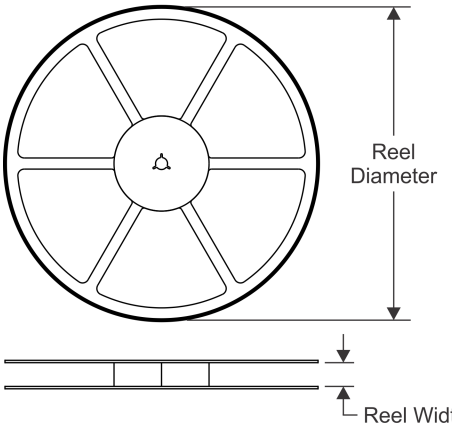
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

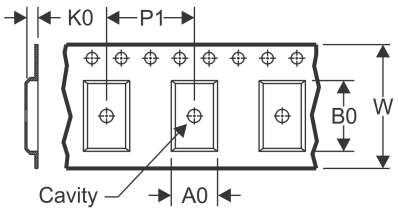
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

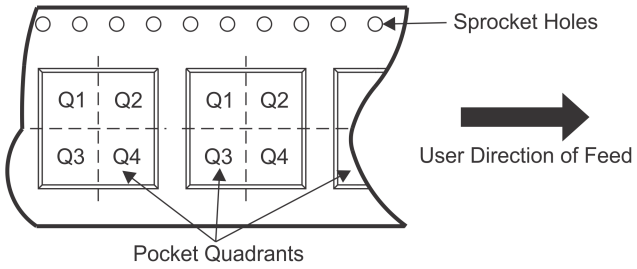


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

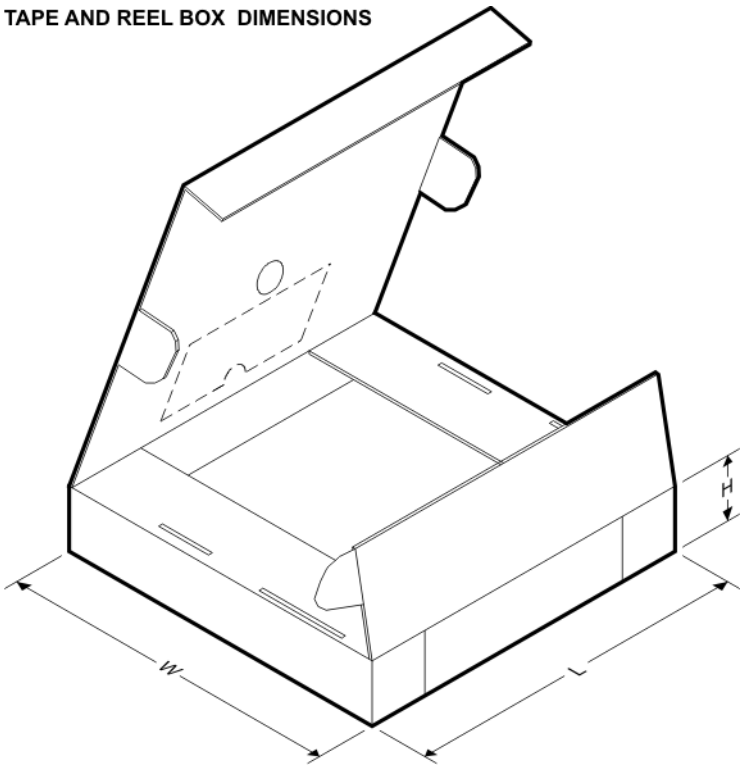
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM5141QRGERQ1	VQFN	RGE	24	3000	330.0	12.4	4.3	4.3	1.1	8.0	12.0	Q2
LM5141QRGETQ1	VQFN	RGE	24	250	180.0	12.4	4.3	4.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM5141QRGERQ1	VQFN	RGE	24	3000	370.0	355.0	55.0
LM5141QRGETQ1	VQFN	RGE	24	250	195.0	200.0	45.0

IMPORTANT NOTICE FOR TI DESIGN INFORMATION AND RESOURCES

Texas Instruments Incorporated ('TI") technical, application or other design advice, services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using any particular TI Resource in any way, you (individually or, if you are acting on behalf of a company, your company) agree to use it solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources.

You understand and agree that you remain responsible for using your independent analysis, evaluation and judgment in designing your applications and that you have full and exclusive responsibility to assure the safety of your applications and compliance of your applications (and of all TI products used in or for your applications) with all applicable regulations, laws and other applicable requirements. You represent that, with respect to your applications, you have all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. You agree that prior to using or distributing any applications that include TI products, you will thoroughly test such applications and the functionality of such TI products as used in such applications. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

You are authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING TI RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY YOU AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

You agree to fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of your non-compliance with the terms and provisions of this Notice.

This Notice applies to TI Resources. Additional terms apply to the use and purchase of certain types of materials, TI products and services. These include; without limitation, TI's standard terms for semiconductor products http://www.ti.com/sc/docs/stdterms.htm), evaluation modules, and samples (http://www.ti.com/sc/docs/sampterms.htm).

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265