# V4100 Controller Board

**Document Revision: 006** 

**Technical Reference** 





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## **Revision history**

Revision	Description	Date		
001	Preliminary	07.05.2010		
002	Board Revision B (Measures)	06.07.2010		
003	Board Revision B (Connections)	11.10.2010		
004	J3	25.11.2010		
005	Multi-Purpose I/O: Gated Synch Pins	27.08.2012		
	Note regarding hot-plugging			
006	Multi-Purpose I/O: PWM Pin	30.04.2013		
	Add note regarding ALP_DEV_DMD_MODE			
	Add section DMD Mechanical Assembly			

## **General**

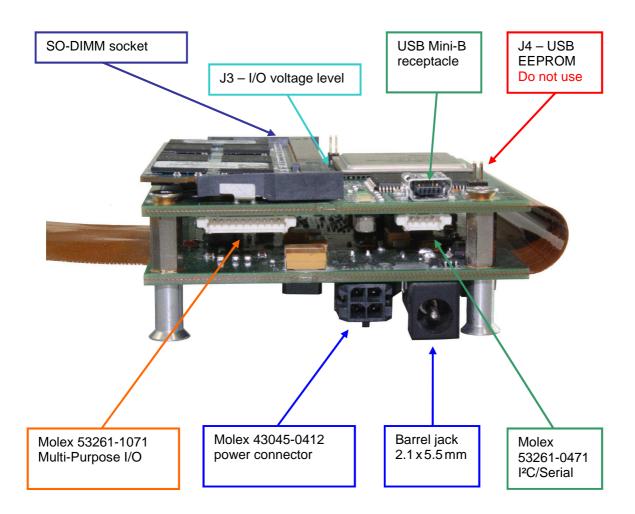
This document describes the functionality of the DLP® V-Module V4100 Board.

The DLP® V4100 Controller Board provides control logic and power supply for driving a 0.7 XGA 2xLVDS DMD by using the Texas Instruments DMD Discovery<sup>™</sup> 4100 chipset.

Key feature of the V4100 are two flexible sections. The 90 mm long flexible part allows high freedom in positioning the DMD part. The 20 mm long flexible part makes it possible to fold the Controller Board (see Figure 1). Please see Chapter "Flexible connection" for reliability issues.

## **Connectors**

Figure 1 - V4100 connectors



#### **SO-DIMM** socket

A standard DDR2 SO-DIMM (small outline dual-inline memory module) is used for image storage. Please use the module specified and supplied by ViALUX. Always switch off the device before removal or insertion of the memory module.

#### **Power connectors**

A 4-pin Molex DC power jack or, alternatively, a Barrel Receptacle is provided on the V4100 to connect to a power supply unit. Please do <u>not</u> use both power connectors simultaneously.

#### Molex Micro Fit 3.0™



This is a Molex Micro Fit 3.0<sup>™</sup> dual row header, part number 43045-0412. It mates with receptacle 43025-04xx.

Pin Number	Signal Name	Power Consumption		
3 – 4	5 V	4 A		
1 – 2 (lower on drawing)	GND	_		

#### **Barrel DC Power Jack**



Center pin diameter 2.1 mm, outside diameter 5.5 mm, Insertion Depth 9 mm

Pin	Signal Name	Power Consumption	
Inside	5 V	4 A	
Outside	GND	_	

#### **USB Mini-B connector**



This is the connector for USB connection to the PC. Use the supplied USB cable to connect the board.

Pin Number	Signal Name	
1 (left on drawing)	USB VCC	
2	USB D-	
3	USB D+	
4	not connected	
5	GND	

## Multi-Purpose I/O (Synchronization) connector



The synchronization connector is a Molex header, part number 53261-1071. It mates with Molex part number 51021-1000. Use crimp contacts 50058-8000 or 50079-8000.

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This connector is not hot-plug capable. Only attach a plug while the device is off in order to avoid damage. Always apply a common GND when connecting devices.

Pin Number	Signal Name	Direction	Purpose
1 (left on drawing)	VCC_GPIO	IN/OUT	Power (see configuration of jumper J3)
2	SYNCH_OUT1 _GATE	OUT <sup>2</sup>	Dynamic Gate Synch Output 1, refer to the ALP-4 <i>high-speed</i> API description, ALP_DEV_DYN_SYNCH_OUT1_GATE
3	SYNCH_OUT2 _GATE	OUT <sup>2</sup>	ALP_DEV_DYN_SYNCH_OUT2_GATE
4	SYNCH_OUT3 _GATE	OUT <sup>2</sup>	ALP_DEV_DYN_SYNCH_OUT3_GATE
5		OUT	Reserved for future use
6		IN	Reserved for future use
7	TRIGGER_IN	IN <sup>1</sup>	Trigger Input
8	SYNCH_OUT	OUT <sup>2</sup>	Frame Synchronization Output
9	PWM	OUT <sup>2</sup>	ALP_PWM_LEVEL: output a pulse-width modulated value
10	GND	_	Power ground

## I2C and Serial I/O connector



This connector is a Molex header, part number 53261-0471. It mates with Molex part number 51021-0400, use crimp contacts 50058-8000 or 50079-8000.

This connector is not hot-plug capable. Only attach a plug while the device is off in order to avoid damage. Always apply a common GND when connecting devices.

Pin Number	Signal Name	Direction	Purpose
1 (left on drawing)	GND RxD	- IN	Power ground Reserved for future use
2	VCC_USB TxD	OUT OUT	Power (3.1 V) Reserved for future use
3	SDA	IN/OUT	Serial Data
4	SCL	OUT	Serial Clock

Please contact ViALUX before using this connector.

<sup>&</sup>lt;sup>1</sup> Input: SN74LVC2G14 <sup>2</sup> Output: SN74LVC2T45

## **Jumper configuration**

All jumpers used in this board layout are 1.27 mm pitch.

## J3 – I/O voltage selection

This jumper is used to select either 2.5 V or 5.0 V voltage supplies for the Multi-Purpose I/O connector.

The attached hardware can supply the voltage level, when the jumper is left open.

Position	I/O voltage	VCC_GPIO source	
open	2.5 V to 5.0 V	extern	
1 – 2	2.5 V	intern	
3 – 4	5.0 V	intern	

## J4 – USB EEPROM programming

This jumper allows to temporally disconnect the USB EEPROM or to disable its write protection feature. Please contact ViALUX before using this jumper.

## **LED** description

Table 1 lists the on board LEDs with a functional description.

Table 1 – Description of LEDs

LED	Color	Status	Description
LD1	Blue	Steady	USB high-speed port acknowledged
		Blink	Bulk data traffic (image download)
LD2	Green	Steady	FPGA configured
LD3	Yellow	Steady	Firmware running, USB active
		Blink	Generic USB traffic (projection control, etc.)
LD4	Red	Steady	USB Power Input
LD5	Red	Steady	5 V power supply is connected
LD6	Red	Steady	On-board 3.3 V power regulator output, supply for USB
LD7	Red	Steady	On-board 3.3 V power regulator output, supply for DMD CMOS logic
LD8	Red	Steady	On-board 2.5 V power regulator output
LD9	Red	Steady	On-board 1.8 V power regulator output
LD10	Red	Steady	On-board 1.0 V power regulator output
LD12	Red	Steady	On-board 12 V power regulator output
LD13	Green	Steady	DDC finished
LD14	Red	Steady	DDC done
LD15	Green	Steady	System "heartbeat" signal (VLED0)
LD16	Green	Steady	Denotes initialization complete (VLED1)

## **Protection features**

The V4100 board provides protection logic control for the DMD.

#### **Power float**

In the event of power failure or if the 5 V power supply is shut down, the DMD will be issued a FLOAT command that places all mirrors in a non-deflected position. The threshold is below 4.5 V. The ALP-4 *high-speed* API implements ALP\_DEV\_DMD\_MODE for checking this state.

## **Operating conditions**

Operating Temperature: 25 ... 45 ℃

Storage Temperature: -40 ... 80 ℃

Relative Humidity: 0 ... 95 % (non-condensing)

## Flexible connection

The flexible connection of the V4100 is designed to satisfy applications where space is limited. The flexible connection is <u>not</u> designed for dynamic mechanical bending. The number of bending cycles that lead to a damage of the flexible connection depends on the bending radius, the smaller the bending radius the higher the fatigue of the flexible connection. See Table 2 for details.

Furthermore, it is recommended to keep the tensile forces as small as possible. ViALUX also recommends that the user pays attention to the handling and uses the wrapping delivered with the V4100 Board.

Table 2 – Bending radius versus bending cycles that lead to a damage

Radius	Cycles
1 mm	> 1
2 mm	> 10
40 mm	> 10000

## **DMD Mechanical Assembly**

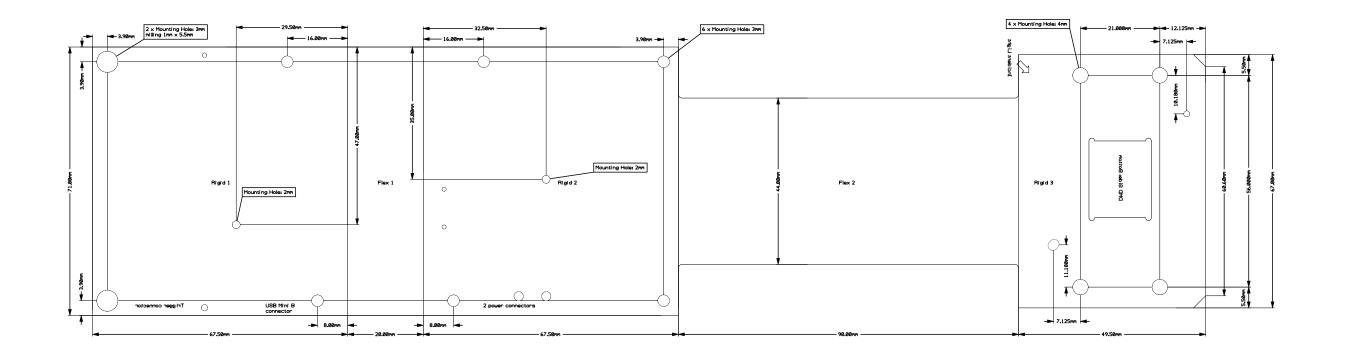
Please observe the following Torque Specification for the four M3 screws of the standard ViALUX DMD mounting set:  $3.0 \pm 1.0$  IN·LB (i.e.  $0.34 \pm 0.11$  N·m)

## **Mounting Instructions**

Observe ESD requirements strictly!

Please be aware that there is an on-board battery that supports the key memory for FPGA encryption. Avoid short-circuits when mounting the board in order to not lose the encryption key.

The V4100 Board is designed to work in any mounting position. Good air circulation is recommended.



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DESIGN TITLE: V4100	REVISION	: В	
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