

Ultra-Low Offset/Drift, Low-Noise, Precision SOT23 Amplifiers

ABSOLUTE MAXIMUM RATINGS

Power-Supply Voltage (V_{CC} to GND).....6V
 All Other Pins(GND - 0.3V) to (V_{CC} + 0.3V)
 Output Short-Circuit Duration
 (OUT shorted to V_{CC} or GND)Continuous
 Continuous Power Dissipation ($T_A = +70^\circ\text{C}$)
 6-Pin Plastic SOT23 (derate 9.1mW/ $^\circ\text{C}$ above $+70^\circ\text{C}$).....727mW
 8-Pin Plastic SO (derate 5.88mW/ $^\circ\text{C}$ above $+70^\circ\text{C}$).....471mW

Operating Temperature Range -40°C to $+125^\circ\text{C}$
 Junction Temperature $+150^\circ\text{C}$
 Storage Temperature Range..... -65°C to $+150^\circ\text{C}$
 Lead Temperature (soldering, 10s) $+300^\circ\text{C}$

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

($2.7\text{V} \leq V_{CC} \leq 5.5\text{V}$, $V_{CM} = \text{GND} = 0\text{V}$, $V_{OUT} = V_{CC}/2$, $R_L = 10\text{k}\Omega$ connected to $V_{CC}/2$, $\overline{\text{SHDN}} = V_{CC}$, $T_A = +25^\circ\text{C}$, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	(Note 1)		0.1	2	μV
Long-Term Offset Drift				50		nV/1000hr
Input Bias Current	I_B	(Note 2)		1		pA
Input Offset Current	I_{OS}	(Note 2)		2		pA
Input Noise Voltage	e_{nP-P}	$R_S = 100\Omega$, 0.01Hz to 10Hz		1.5		$\mu\text{Vp-p}$
Common-Mode Input Voltage Range	V_{CM}	Inferred from CMRR test	GND - 0.1		$V_{CC} - 1.3$	V
Common-Mode Rejection Ratio	CMRR	$-0.1\text{V} \leq V_{CM} \leq V_{CC} - 1.3\text{V}$ (Note 1)	120	140		dB
Power-Supply Rejection Ratio	PSRR	$2.7\text{V} \leq V_{CC} \leq 5.5\text{V}$ (Note 1)	120	140		dB
Large-Signal Voltage Gain	A_{VOL}	$0.05\text{V} \leq V_{OUT} \leq V_{CC} - 0.05\text{V}$ (Note 1) $R_L = 10\text{k}\Omega$	125	150		dB
		$0.1\text{V} \leq V_{OUT} \leq V_{CC} - 0.1\text{V}$ (Note 1) $R_L = 1\text{k}\Omega$	125	145		
Output Voltage Swing	V_{OH}/V_{OL}	$R_L = 10\text{k}\Omega$ $V_{CC} - V_{OH}$		4	10	mV
		V_{OL}		4	10	
		$R_L = 1\text{k}\Omega$ $V_{CC} - V_{OH}$		35	50	
		V_{OL}		35	50	
Output Short-Circuit Current		To either supply		40		mA
Output Leakage Current		$0 \leq V_{OUT} \leq V_{CC}$, $\overline{\text{SHDN}} = \text{GND}$ (Note 2)		0.01	1	μA
Slew Rate		$V_{CC} = 5\text{V}$, $C_L = 100\text{pF}$, $V_{OUT} = 2\text{V}$ step		0.35		V/ μs
				1.6		
Gain-Bandwidth Product	GBWP	$R_L = 10\text{k}\Omega$, $C_L = 100\text{pF}$, measured at $f = 100\text{kHz}$		1		MHz
				6.5		
Minimum Stable Closed-Loop Gain		$R_L = 10\text{k}\Omega$, $C_L = 100\text{pF}$, phase margin = 60°		1		V/V
				10		

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ELECTRICAL CHARACTERISTICS (continued)

($2.7V \leq V_{CC} \leq 5.5V$, $V_{CM} = GND = 0V$, $V_{OUT} = V_{CC}/2$, $R_L = 10k\Omega$ connected to $V_{CC}/2$, $\overline{SHDN} = V_{CC}$, $T_A = +25^\circ C$, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Maximum Closed-Loop Gain		$R_L = 10k\Omega$, $C_L = 100pF$, phase margin = 60°	MAX4238	1000		V/V
			MAX4239	6700		
Settling Time		-1V step	0.1% (10 bit)	0.5		ms
			0.025% (12 bit)	1.0		
			0.006% (14 bit)	1.7		
			0.0015% (16)	2.3		
Overload Recovery Time		$A_V = 10$ (Note 4)	0.1% (10 bit)	3.3		ms
			0.025% (12 bit)	4.1		
			0.006% (14 bit)	4.9		
			0.0015% (16)	5.7		
Startup Time		$A_V = 10$	0.1% (10 bit)	1.8		ms
			0.025% (12 bit)	2.6		
			0.006% (14 bit)	3.4		
			0.0015% (16)	4.3		
Supply Voltage Range	V_{CC}	Inferred by PSRR test	2.7		5.5	V
Supply Current	I_{CC}	$\overline{SHDN} = V_{CC}$, no load, $V_{CC} = 5.5V$		600	850	μA
		$\overline{SHDN} = GND$, $V_{CC} = 5.5V$		0.1	1	
Shutdown Logic High	V_{IH}		2.2			V
Shutdown Logic Low	V_{IL}				0.8	V
Shutdown Input Current		$0V \leq \overline{SHDN} \leq V_{CC}$		0.1	1	μA

MAX4238/MAX4239

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ELECTRICAL CHARACTERISTICS

($2.7V \leq V_{CC} \leq 5.5V$, $V_{CM} = GND = 0V$, $V_{OUT} = V_{CC}/2$, $R_L = 10k\Omega$ connected to $V_{CC}/2$, $\overline{SHDN} = V_{CC}$, $T_A = -40^\circ C$ to $+125^\circ C$, unless otherwise noted.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	(Note 1)	$T_A = -40^\circ C$ to $+85^\circ C$			2.5	μV
			$T_A = -40^\circ C$ to $+125^\circ C$			3.5	
Input Offset Drift	TCV_{OS}	(Note 1)			10		$nV/^\circ C$
Common-Mode Input Voltage Range	V_{CM}	Inferred from CMRR test		GND - 0.05		$V_{CC} - 1.4$	V
Common-Mode Rejection Ratio	CMRR	$GND - 0.05V \leq V_{CM} \leq V_{CC} - 1.4V$ (Note 1)	$T_A = -40^\circ C$ to $+85^\circ C$	115			dB
			$T_A = -40^\circ C$ to $+125^\circ C$	90			
Power-Supply Rejection Ratio	PSRR	$2.7V \leq V_{CC} \leq 5.5V$ (Note 1)		120			dB
Large-Signal Voltage Gain	A_{VOL}	$R_L = 10k\Omega$, $0.1V \leq V_{OUT} \leq V_{CC} - 0.1V$ (Note 1)	$T_A = -40^\circ C$ to $+85^\circ C$	125			dB
			$T_A = -40^\circ C$ to $+125^\circ C$	95			
		$R_L = 1k\Omega$ (Note 1)	$0.1V \leq V_{OUT} \leq V_{CC} - 0.1V$, $T_A = -40^\circ C$ to $+85^\circ C$	120			dB
			$0.2V \leq V_{OUT} \leq V_{CC} - 0.2V$, $T_A = -40^\circ C$ to $+125^\circ C$	80			
Output Voltage Swing	V_{OH}/V_{OL}	$R_L = 10k\Omega$	$V_{CC} - V_{OH}$			20	mV
			V_{OL}			20	
		$R_L = 1k\Omega$	$V_{CC} - V_{OH}$			100	
			V_{OL}			100	
Output Leakage Current		$0V \leq V_{OUT} \leq V_{CC}$, $\overline{SHDN} = GND$ (Note				2	μA
Supply Voltage Range	V_{CC}	Inferred by PSRR test		2.7		5.5	V
Supply Current	I_{CC}	$\overline{SHDN} = V_{CC}$, no load, $V_{CC} = 5.5V$				900	μA
		$\overline{SHDN} = GND$, $V_{CC} = 5.5V$				2	
Shutdown Logic High	V_{IH}			2.2			V
Shutdown Logic Low	V_{IL}					0.7	V
Shutdown Input Current		$0V \leq V_{\overline{SHDN}} \leq V_{CC}$				2	μA

Note 1: Guaranteed by design. Thermocouple and leakage effects preclude measurement of this parameter during production testing. Devices are screened during production testing to eliminate defective units.

Note 2: $IN+$ and $IN-$ are gates to CMOS transistors with typical input bias current of 1pA. CMOS leakage is so small that it is impractical to test and guarantee in production. Devices are screened during production testing to eliminate defective units.

Note 3: Leakage does not include leakage through feedback resistors.

Note 4: Overload recovery time is the time required for the device to recover from saturation when the output has been driven to either rail.

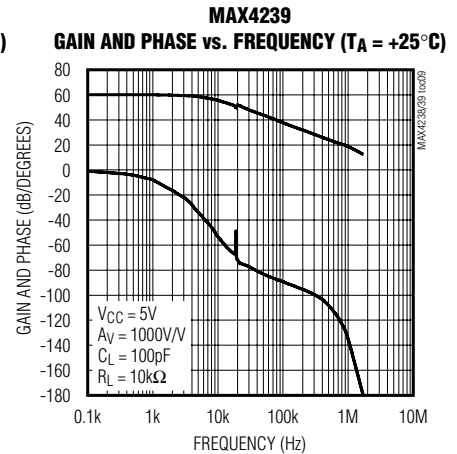
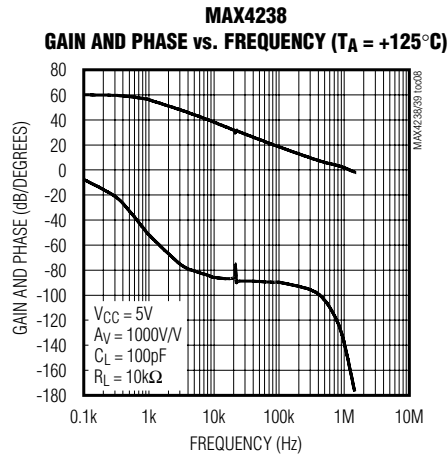
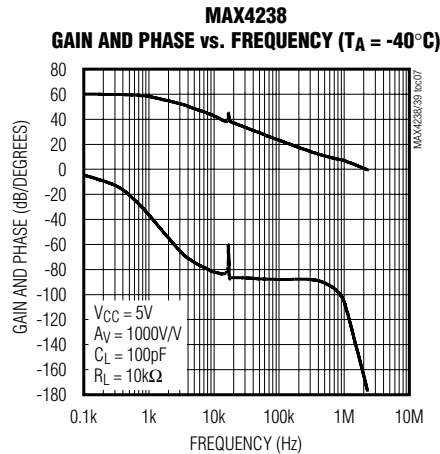
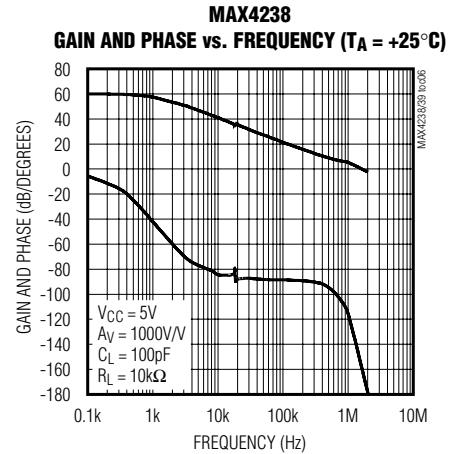
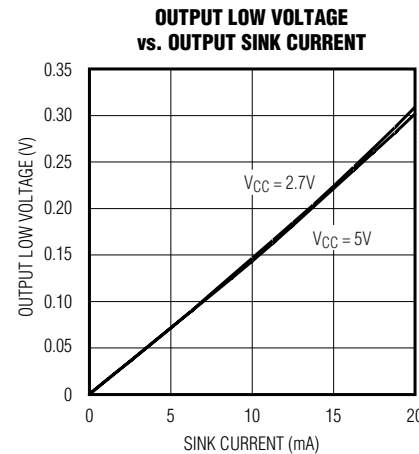
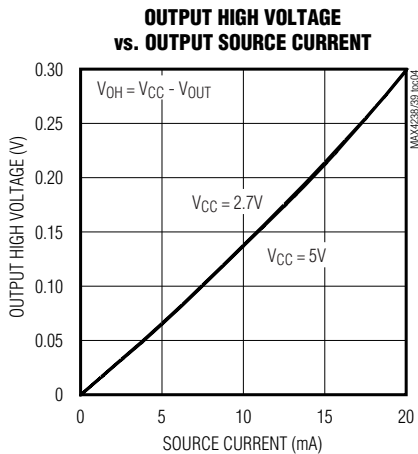
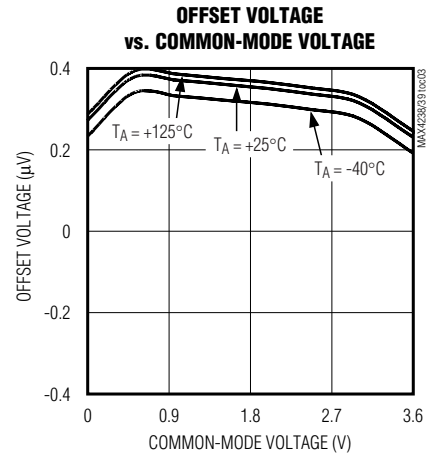
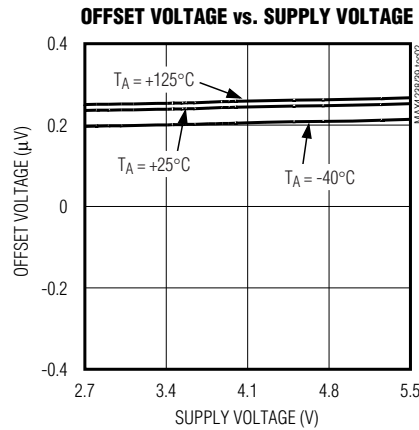
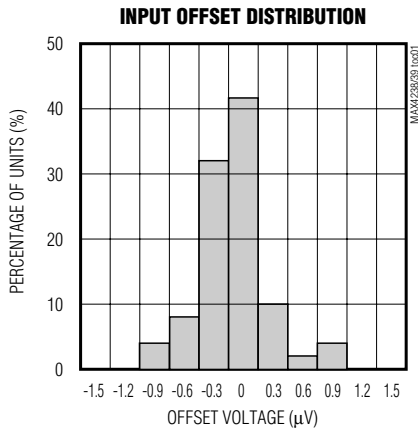
Note 5: Specifications are 100% tested at $T_A = +25^\circ C$, unless otherwise noted. Limits over temperature are guaranteed by design.

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Typical Operating Characteristics

($V_{CC} = 5V$, $V_{CM} = 0V$, $R_L = 10k\Omega$ connected to $V_{CC}/2$, $\overline{SHDN} = V_{CC}$, $T_A = +25^\circ C$, unless otherwise noted.)

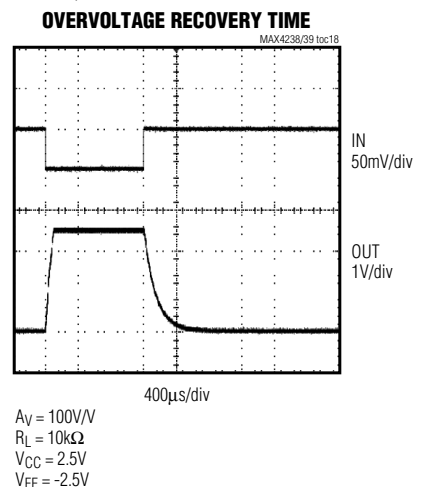
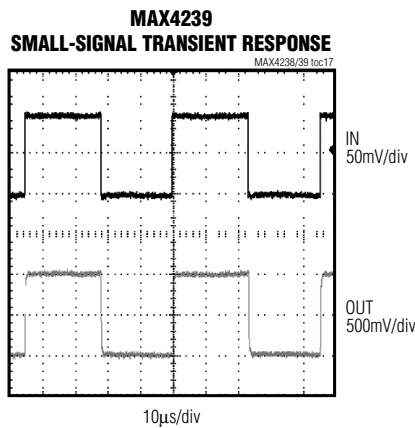
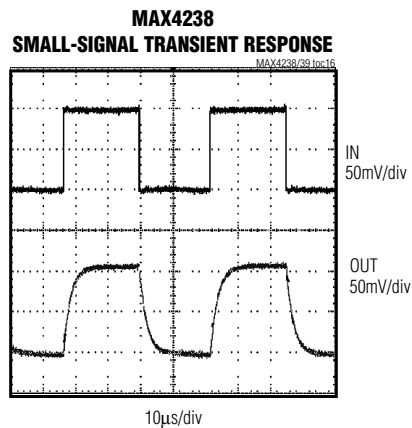
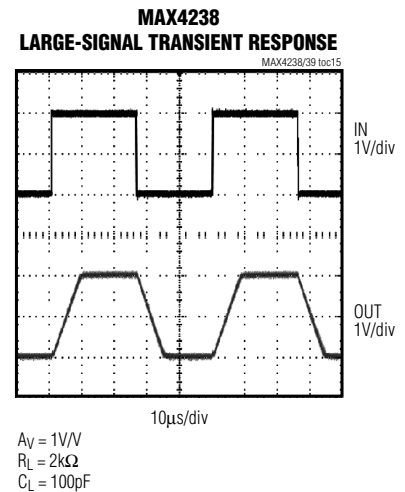
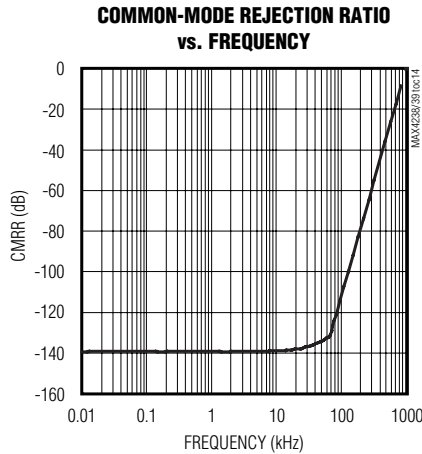
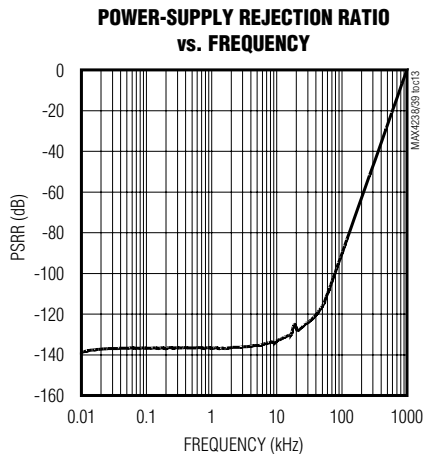
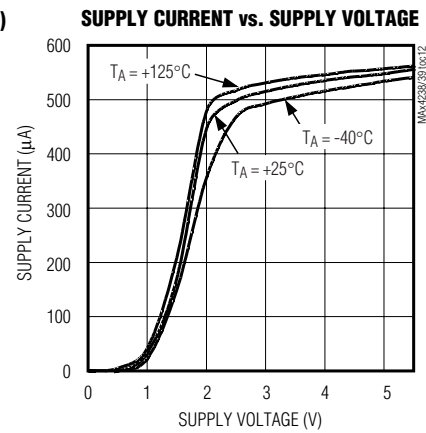
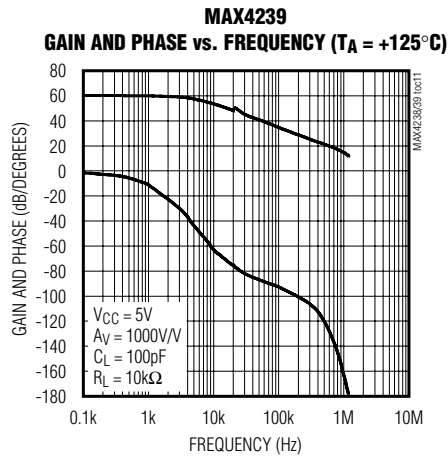
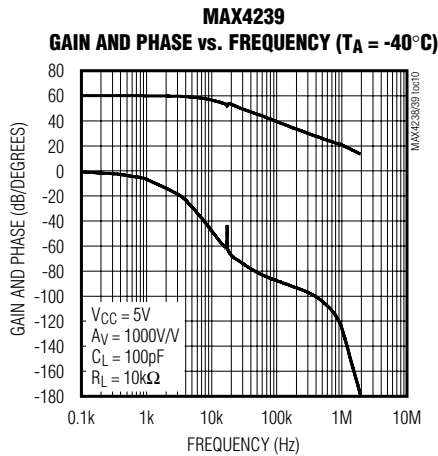
MAX4238/MAX4239



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Typical Operating Characteristics (continued)

($V_{CC} = 5V$, $V_{CM} = 0V$, $R_L = 10k\Omega$ connected to $V_{CC}/2$, $\overline{SHDN} = V_{CC}$, $T_A = +25^\circ C$, unless otherwise noted.)

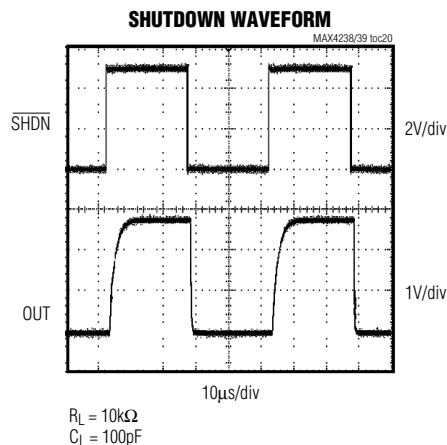
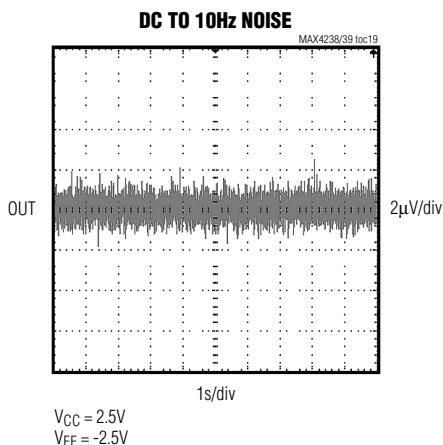


Ultra-Low Offset/Drift, Low-Noise, Precision SOT23 Amplifiers

MAX4238/MAX4239

Typical Operating Characteristics (continued)

($V_{CC} = 5V$, $V_{CM} = 0V$, $R_L = 10k\Omega$ connected to $V_{CC}/2$, $\overline{SHDN} = V_{CC}$, $T_A = +25^\circ C$, unless otherwise noted.)



Pin Description

PIN		NAME	FUNCTION
SOT23	SO		
1	6	OUT	Amplifier Output
2	4	GND	Ground
3	3	IN+	Noninverting Input
4	2	IN-	Inverting Input
5	1	\overline{SHDN}	Shutdown Input. Active low shutdown, connect to V_{CC} for normal operation.
6	7	V_{CC}	Positive Power Supply
—	5, 8	N.C.	No Connection. Not internally connected.

Detailed Description

The MAX4238/MAX4239 are high-precision amplifiers that have less than $2.5\mu V$ of input-referred offset and low $1/f$ noise. These characteristics are achieved through a patented autozeroing technique that samples and cancels the input offset and noise of the amplifier. The pseudorandom clock frequency varies from 10kHz to 15kHz, reducing intermodulation distortion present in chopper-stabilized amplifiers.

Offset Error Sources

To achieve very low offset, several sources of error common to autozero-type amplifiers need to be considered. The first contributor is the settling of the sampling

capacitor. This type of error is independent of input-source impedance, or the size of the external gain-setting resistors. Maxim uses a patented design technique to avoid large changes in the voltage on the sampling capacitor to reduce settling time errors.

The second error contributor, which is present in both autozero and chopper-type amplifiers, is the charge injection from the switches. The charge injection appears as current spikes at the input, and combined with the impedance seen at the amplifier's input, contributes to input offset voltage. Minimize this feedthrough by reducing the size of the gain-setting resistors and the input-source impedance. A capacitor in parallel with the feedback resistor reduces the amount of clock feedthrough to the output by limiting the closed-loop bandwidth of the device.

The design of the MAX4238/MAX4239 minimizes the effects of settling and charge injection to allow specification of an input offset voltage of $0.1\mu V$ (typ) and less than $2.5\mu V$ over temperature ($-40^\circ C$ to $+85^\circ C$).

1/f Noise

$1/f$ noise, inherent in all semiconductor devices, is inversely proportional to frequency. $1/f$ noise increases 3dB/octave and dominates amplifier noise at lower frequencies. This noise appears as a constantly changing voltage in series with any signal being measured. The MAX4238/MAX4239 treat $1/f$ noise as a slow varying offset error, inherently canceling the $1/f$ noise.

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Output Overload Recovery

Autozeroing amplifiers typically require a substantial amount of time to recover from an output overload. This is due to the time it takes for the null amplifier to correct the main amplifier to a valid output. The MAX4238/MAX4239 require only 3.3ms to recover from an output overload (see *Electrical Characteristics* and *Typical Operating Characteristics*).

Shutdown

The MAX4238/MAX4239 feature a low-power (0.1μA) shutdown mode. When $\overline{\text{SHDN}}$ is pulled low, the clock stops and the device output enters a high-impedance state. Connect $\overline{\text{SHDN}}$ to V_{CC} for normal operation.

Applications Information

Minimum and Maximum Gain Configurations

The MAX4238 is a unity-gain stable amplifier with a gain-bandwidth product (GBWP) of 1MHz. The MAX4239 is decompensated for a GBWP of 6.5MHz and is stable with a gain of 10V/V. Unlike conventional operational amplifiers, the MAX4238/MAX4239 have a maximum gain specification. To maintain stability, set the gain of the MAX4238 between $A_V = 1000\text{V/V}$ to 1V/V, and set the gain of the MAX4239 between $A_V = 6700\text{V/V}$ and 10V/V.

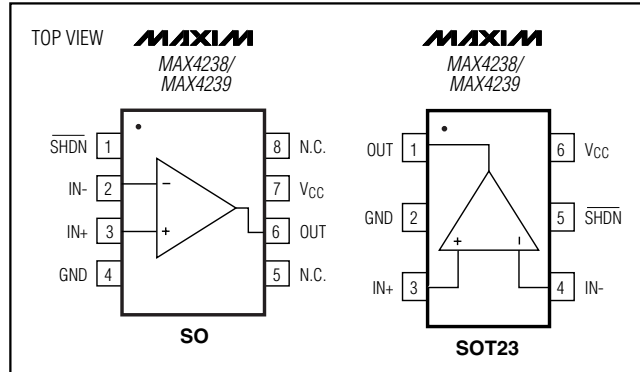
ADC Buffer Amplifier

The low offset, fast settling time, and 1/f noise cancellation of the MAX4238/MAX4239 make these devices ideal for ADC buffers. The MAX4238/MAX4239 are well suited for low-speed, high-accuracy applications such as strain gauges (see *Typical Application Circuit*).

Error Budget Example

When using the MAX4238/MAX4239 as an ADC buffer, the temperature drift should be taken into account when determining the maximum input signal. With a typical offset drift of 10nV/°C, the drift over a 10°C range is 100nV. Setting this equal to 1/2LSB in a 16-bit system yields a full-scale range of 13mV. With a single 2.7V supply, an acceptable closed-loop gain is $A_V = 200$. This provides sufficient gain while maintaining headroom.

Pin Configurations



Chip Information

TRANSISTOR COUNT: 821

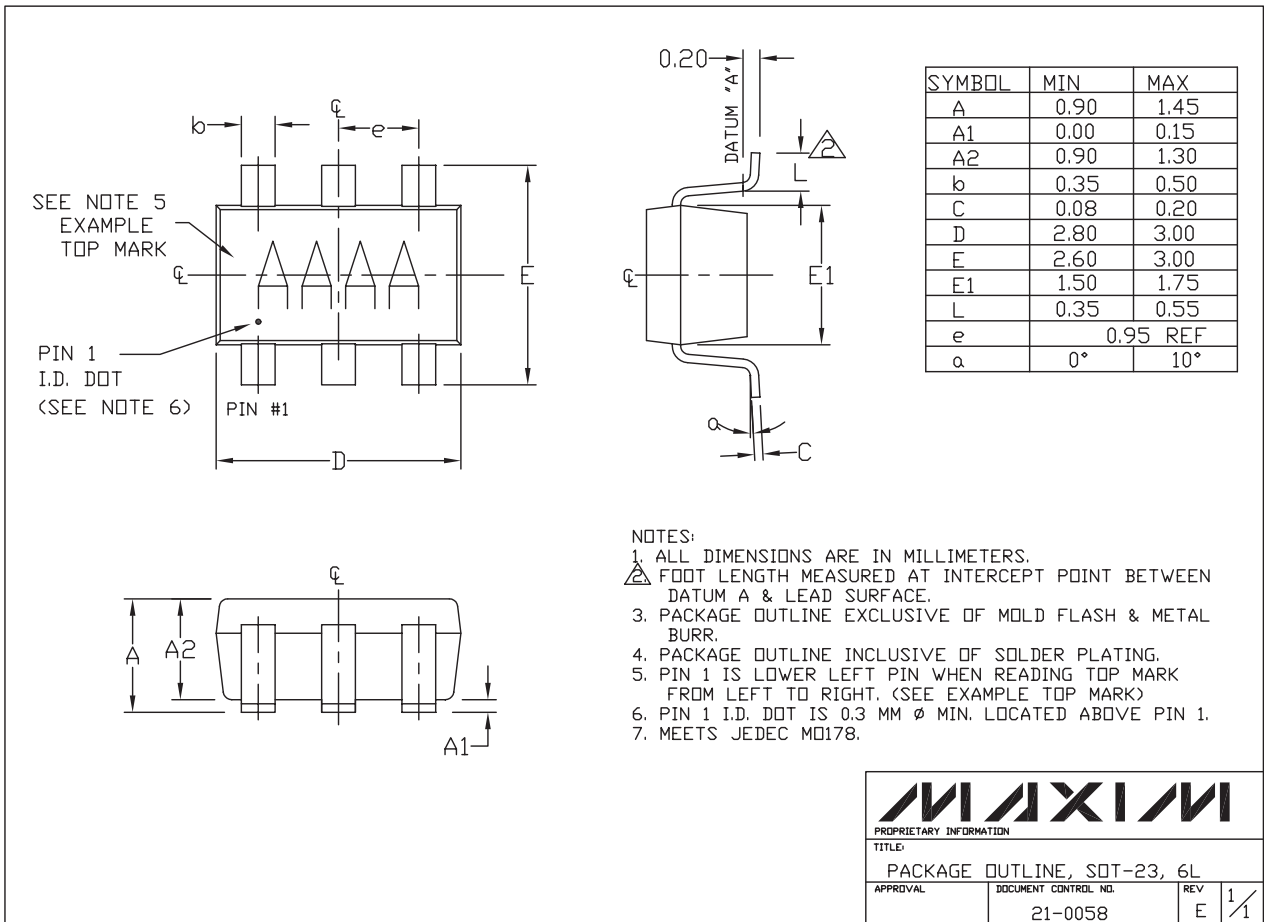
PROCESS: BiCMOS

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Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)

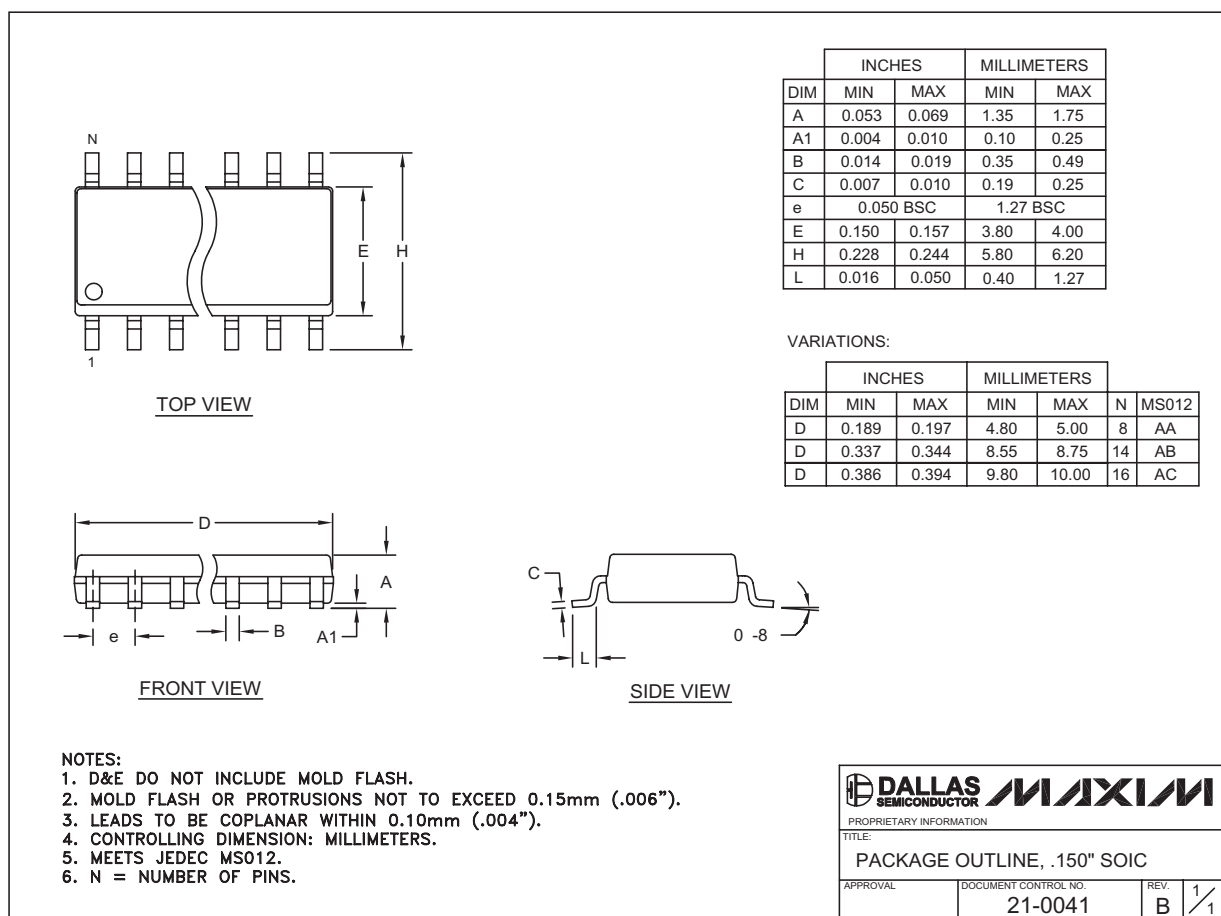
MAX4238/MAX4239



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Package Information (continued)

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