Lecture and Hands-on Workshop on Design for Test (DFT)

Laboratory:
Importing Modules, Pin Assignment via QSF, and Signal Verification in Simulation and on the DE10-Standard FPGA

Electronics Engineering Department, Costa Rica Institute of Technology

Intel, Costa Rica

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General Lecture and Workshop Content

Module 1	Module 2	Module 3
Semiconductor fabrication and assembly of integrated circuits	High volume manufacturing test approaches	Hands-on labs on testing
Testing of integrated circuits	Structural and automated test approaches	DFT CAD Tools
Automated test equipment	Automated test pattern generation and standardization	FPGA-based DFT implementation
Introduction to high volume manufacturing flow	Functional content	

Outline

- **Laboratory**

Create project

1. Create new LabFPGA2 project
2. Import **LabFPGA2.sv** module

```
module LabFPGA2 #(
    parameter int WIDTH = 24,
    parameter int DIVIDER = 20e6
)(
    input       logic               clk_i,
                                    rst_i,
                                    en_reg_i,
                                    sw_reg_b_i,
                                    slct_op_i,
                                    slct_byte_i,
                                    slct_sb_i,
    input       logic   [3:0]       cntrl_alu_i,
    input       logic   [3:0]       op_i,
    output      logic   [3:0]       flag_o,
    output      logic   [41:0]      display_o,
    output      logic   [1:0]       counter_slct_op_o,
                                    counter_slct_byte_o,
    output      logic               sb_op_o

);
```


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Pin Assignment via QSF

1. Open **LabFPGA2_pinout.qsf**
2. Assign the signals to the corresponding pins
3. Import the **LabFPGA2_pinout.qsf**

No signal assigned

Signal assigned

```
# ------------------------------------------------------------------------- #
# Clock
#   set_location_assignment PIN_AF14 -to clk
# ------------------------------------------------------------------------- #
# ------------------------------------------------------------------------- #
# Clock
    set_location_assignment PIN_AF14 -to clk_i
# ------------------------------------------------------------------------- #
```

```
# Slide Switches

#SW[0]
    set_location_assignment PIN_AB30 -to op_i[0]
#SW[1]
    set_location_assignment PIN_Y27 -to op_i[1]
#SW[2]
    set_location_assignment PIN_AB28 -to op_i[2]
#SW[3]
    set_location_assignment PIN_AC30 -to op_i[3]
#SW[4]
    set_location_assignment PIN_W25 -to sw_reg_b_i
#SW[5]
    set_location_assignment PIN_V25 -to cntrl_alu_i[0]
#SW[6]
    set_location_assignment PIN_AC28 -to cntrl_alu_i[1]
#SW[7]
    set_location_assignment PIN_AD30 -to cntrl_alu_i[2]
#SW[8]
    set_location_assignment PIN_AC29 -to cntrl_alu_i[3]
#SW[9]
    set_location_assignment PIN_AA30 -to rst_i
```

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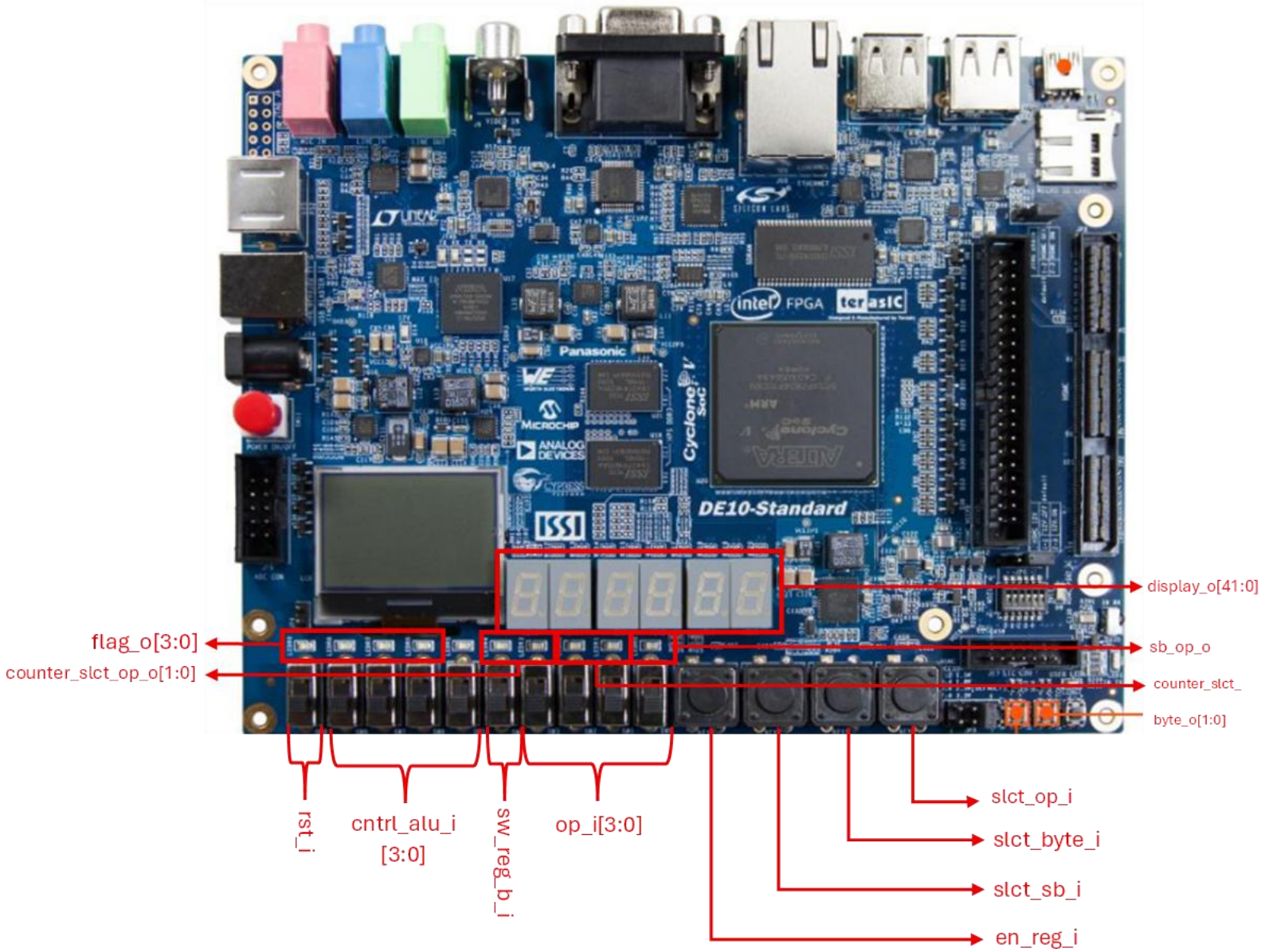
Peripherals



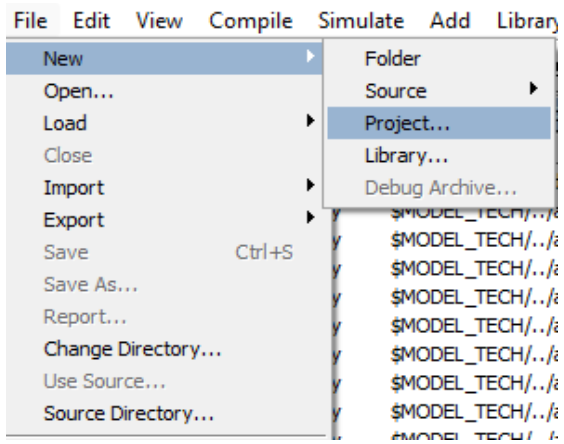
ModelSim Simulation

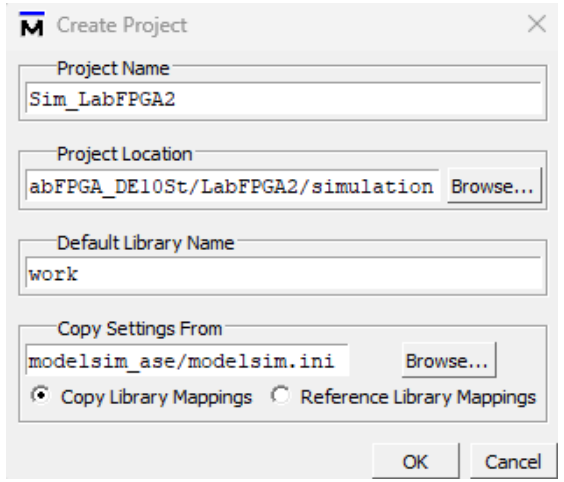
- Modify the testbench

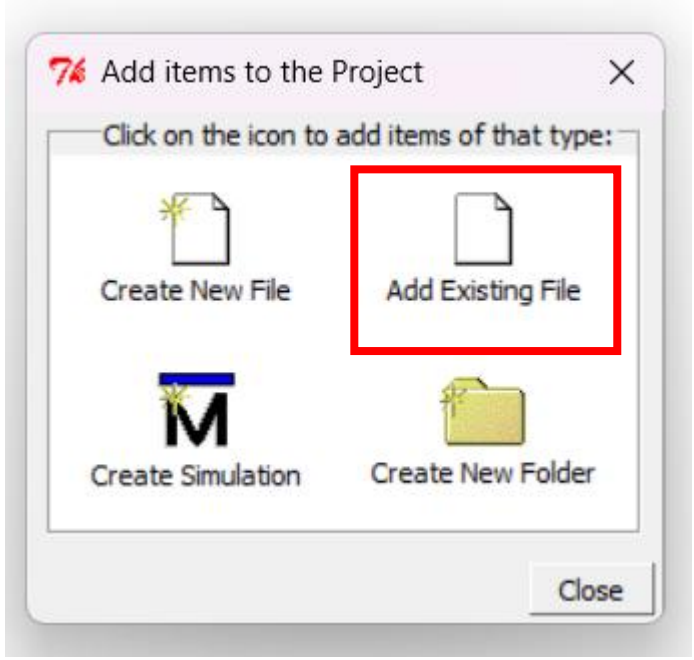
```
// === Main test sequence ===
initial begin

    // Initialize all control signals
    rst = 1;
    en_reg_i = 1;
    sw_reg_b_i = 0;
    slct_op_i = 1;
    slct_byte_i = 1;
    slct_sb_i = 1;
    cntrl_alu_i = 0;
    op_i = 0;
    #10;

    // Apply reset pulse
    rst = 0;
    #20;
    rst = 1;
    #30;

    // Test case 1: A = 0x005A5, B = 0x00A5A, operation = ADD (0)
    calc(4'd0, 24'h5A5, 24'hA5A);

    // Continue your code here....

    // Test case 2: A = 0x00xxx, B = 0x00xxx, operation = ? (x)
    // calc(4'dx, 24'hxxx, 24'hxxx);


    $finish;
end
```

ModelSim Simulation

- Create a new Project
- Import **LabFPGA2_sim.sv** and **tb_LabFPGA2.sv**

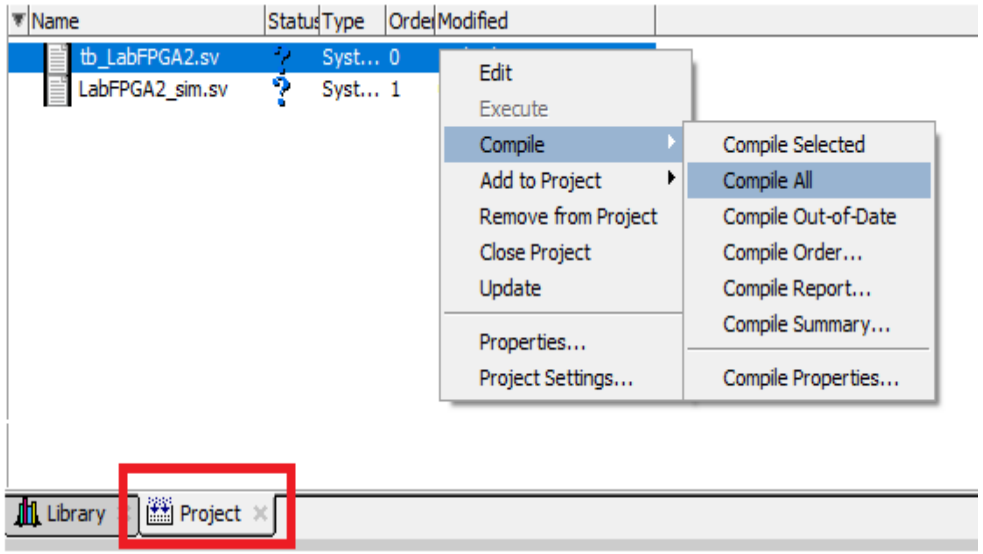


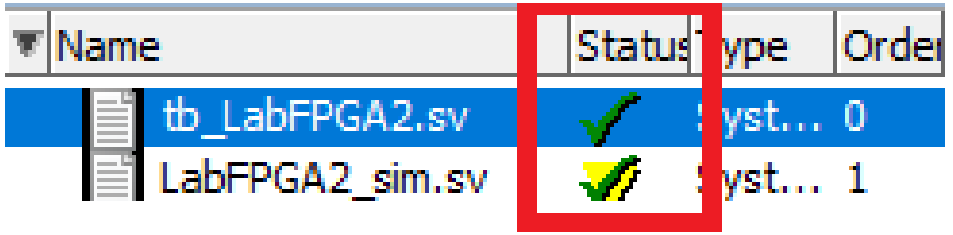




ModelSim Simulation

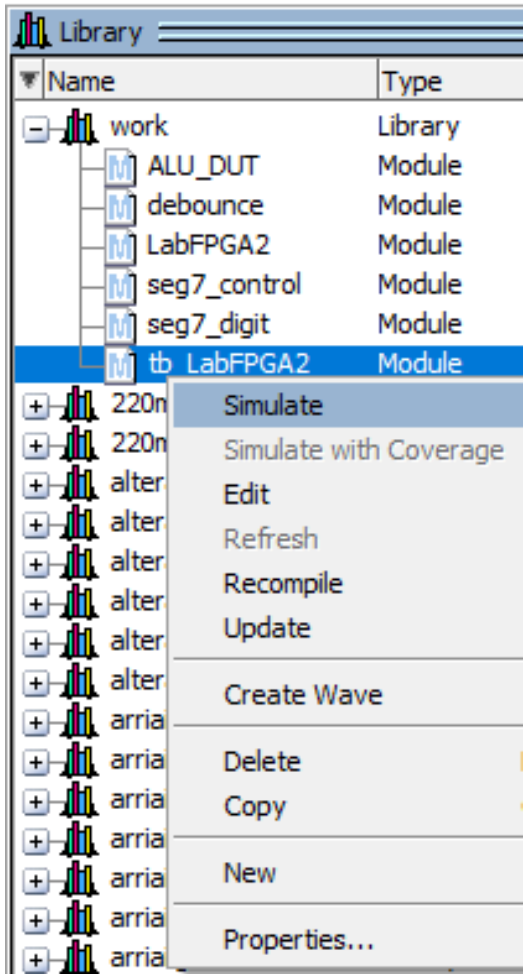
- ***Compile*** Project

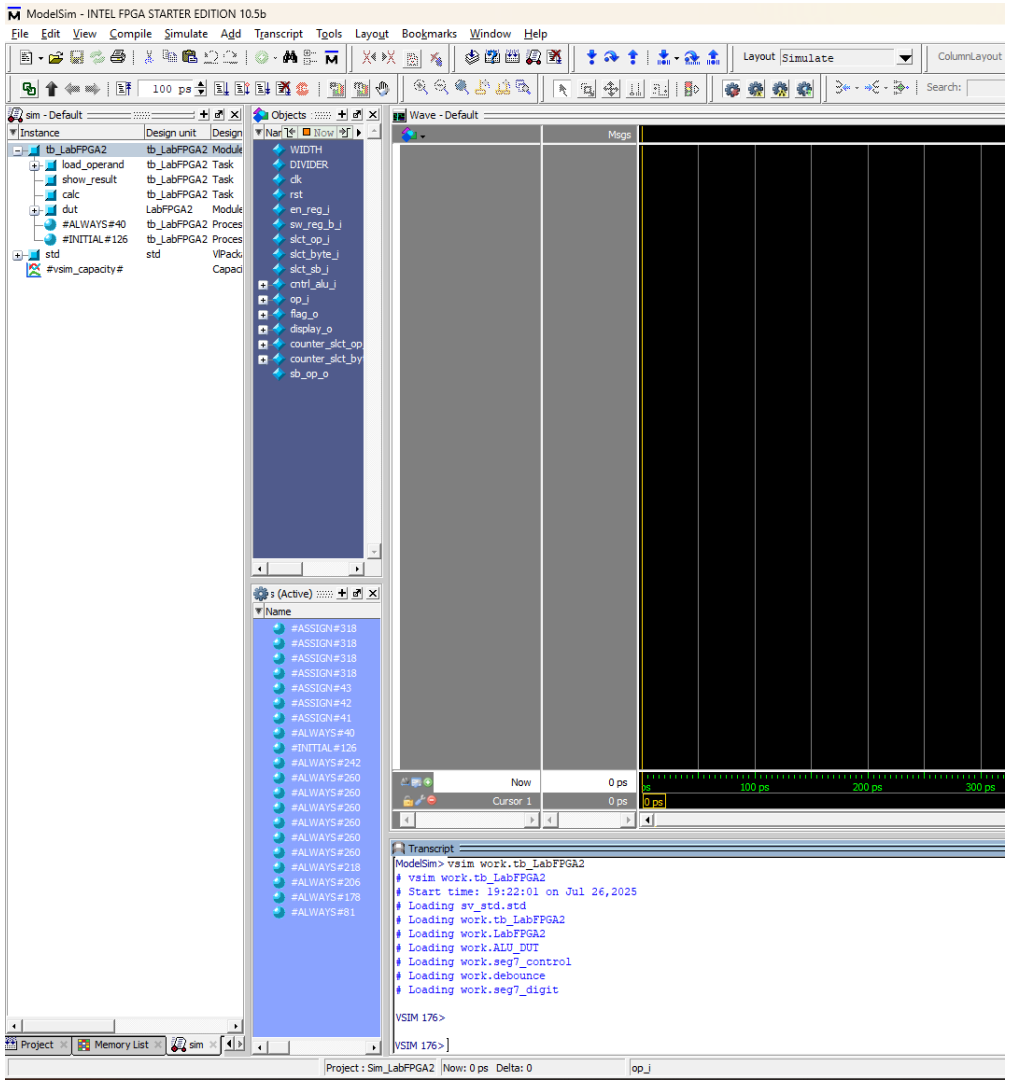




ModelSim Simulation

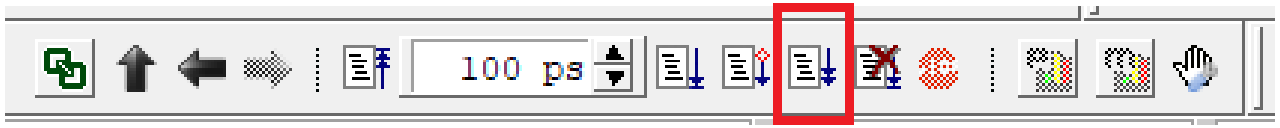
- ***Simulate*** Project

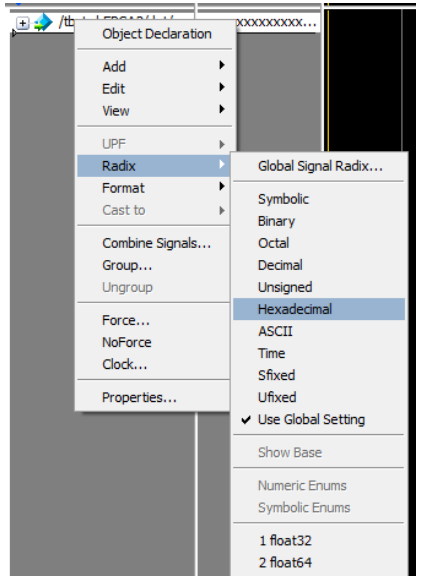


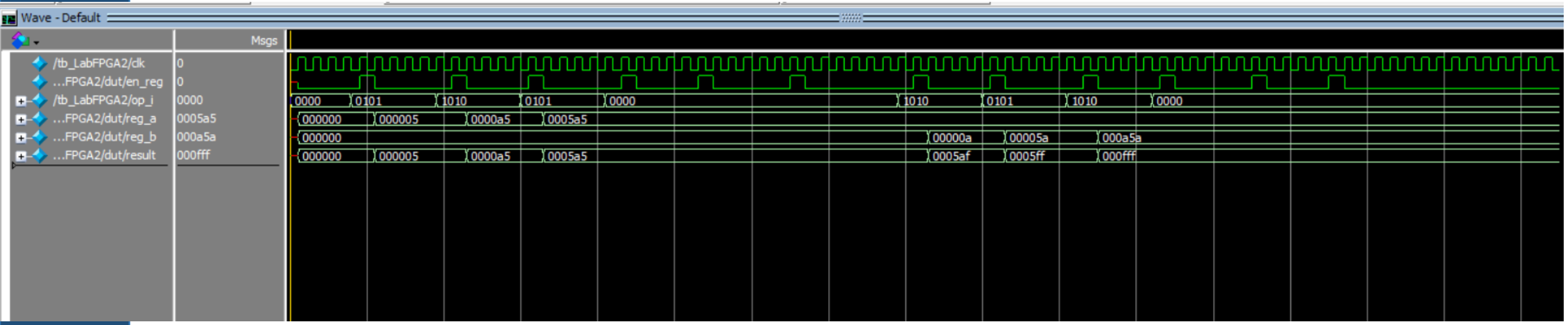


ModelSim Simulation

- ***Run*** *simulation*





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