Lecture and Hands-on Workshop on Design for Test (DFT)

Module 1
Fundamentals of Design for Testability (DFT)
Session 5, part 1:
BSCAN and JTAG

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General Lecture and Workshop Content

Module 1	Module 2	Module 3
Semiconductor fabrication and assembly of integrated circuits	High volume manufacturing test approaches	Hands-on labs on testing
Testing of integrated circuits	Structural and automated test approaches	DFT CAD Tools
Automated test equipment	Automated test pattern generation and standardization	FPGA-based DFT implementation
Introduction to high volume manufacturing flow	Functional content	

Outline

- JTAG and Boundary SCAN

JTAG - IEEE 1149.x

JTAG (Joint Test Action Group) emerged in the 1980s as a solution to testing challenges in modern PCBs, as the number of pins of systems was increasing for:

- Surface-mount devices (SMDs)
- Multi-chip modules (MCMs)
- Limited physical access for probing

Current applications

- Structural & Functional Testing
  - Scan chains allow testing internal logic without physical probes.
- Debugging and Diagnostics
  - Real-time access to internal registers, buses, and I/O pins.
- Embedded System Control
  - Used for firmware updates, clock and power management, and SoC control.
- Device Programming
  - Enables in-system programming (ISP) of FPGAs, CPLDs, Flash, etc.
- Post-Production Maintenance
  - Remote failure diagnosis and reconfiguration in the field.

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JTAG 1149.x

Family Overview

Number	Main Objetives	Status
1149.1	Testing of digital chips and interconnects between chips	Std. 1149.1-1990 Std. 1149.1a-1993 Std. 1149.1b-1994 (BSDL) Std. 1149.1-2001
1149.2	Extended digital serial interface	Discontinued
1149.3	Direct access testability interface	Discontinued
1149.4	Mixed-signal test bus	Std. 1149.4-1999
1149.5	Standard module test and maintenance (MTM) bus	Std. 1149.5-1995 (not endorsed by IEEE since 2003)
1149.6	High-speed network interface protocol	Std. 1149.6-2003

- IEEE 1149.x addresses testing from **chip level** to **system level**.
- Most focus today is on **1149.1 (core boundary scan)** and 1149.6 (high-speed I/O).
- Other standards were discontinued due to overlap or lack of adoption.

Techovedas. 2023. "How Does a Mixed-Signal Device Work?" *Techovedas*. https://techovedas.com/how-does-a-mixed-signal-device-work/.

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IEEE 1149.1

IEEE 1149.1 defines a test architecture and protocol for digital ICs and the digital sections of mixed-signal ICs.

Why IEEE 1149.1?

- Traditional PCB testing (e.g. flying probes, in-circuit testers) relied on **direct physical access** to test points and component pins.
- As digital ICs became **smaller**, **denser**, and **more complex**—with SMDs, BGAs, and multilayer PCBs—physical access became impractical or impossible.
- While testing ICs in isolation was feasible, testing them after PCB assembly became increasingly difficult and unreliable.

BGA: bolitas debajo del chip

IEEE 1149.1

IEEE 1149.1 defines a test architecture and protocol for digital ICs and the digital sections of mixed-signal ICs.

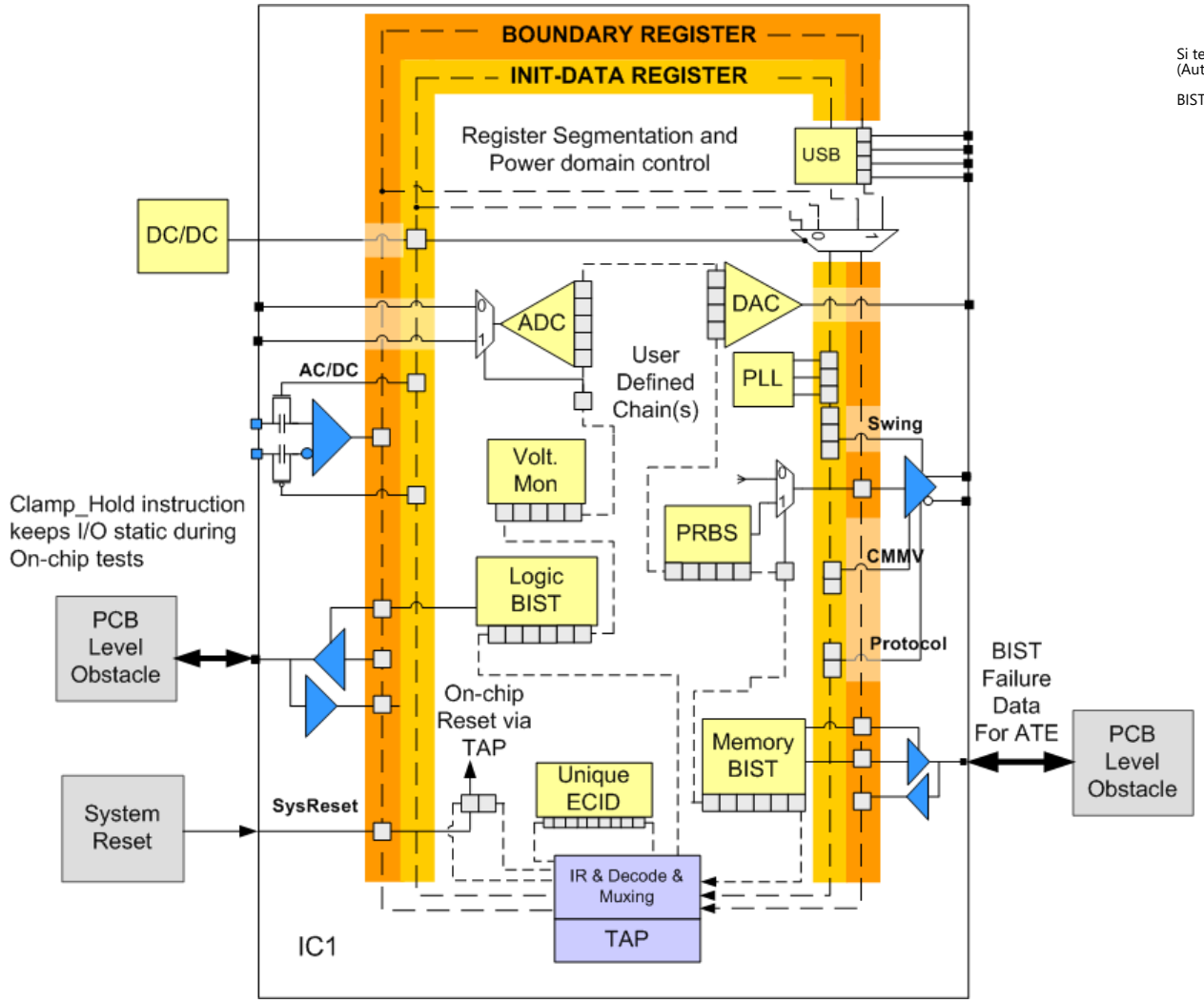
Solution: Digital Boundary Scan

- IEEE Std. 1149.1, also known as **JTAG Boundary Scan**, was officially approved in 1990 to solve test access problems.
- It defines a **standardized serial scan path** placed around the digital I/O boundary of compliant integrated circuits.
- This allows:
  - Access to internal logic and I/Os without physical probing
  - Testing of interconnects between multiple devices
  - A scalable, non-intrusive method suitable for modern electronic systems

Uso serial, digamos en la FPGA cuando digitamos el valor de una entrada con switches digitamos ya sea 4 en paralelo. En cambio este literalmente si es serial seria un bit por flanco de reloj. Osea si el registro es 24 bits mínimo hay 24 flancos reloj para leerlo.

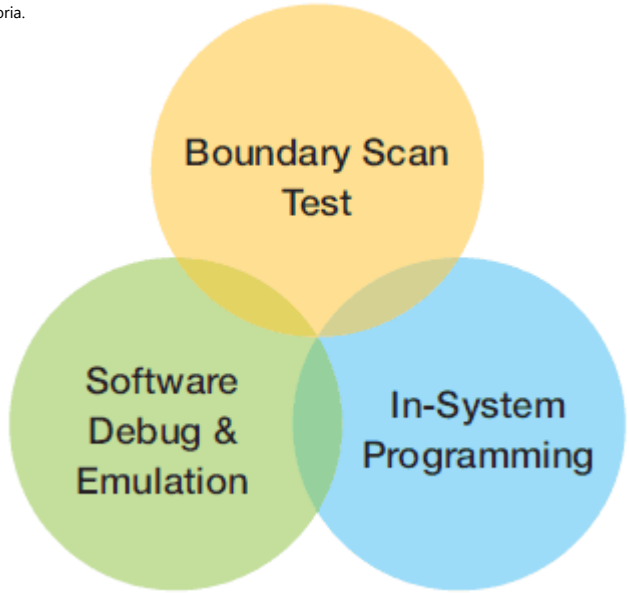
Este no es método intrusivo, trabaja alrededor del circuito.

JTAG 1149.x



Si tengo BIST (Buillt in self testing) no le tengo meter ATE (Automted Testing Equipment).

BIST recuerda que es para memoria.



https://www.xjtag.com/about-jtag/what-is-jtag/

boundary-scan register and other building blocks accessed through a Test Access Port (TAP).

https://grouper.ieee.org/groups/1149/1/

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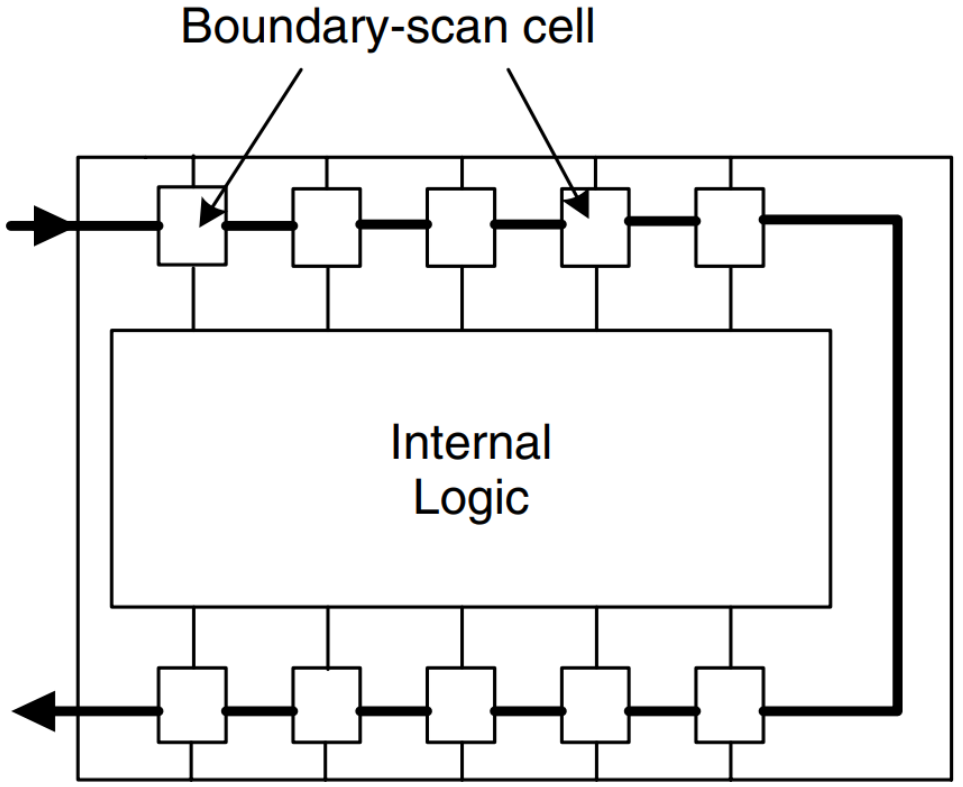
Boundary Scan

- A Boundary-Scan Cell (BSC) is inserted in each I/O pin of the chip.
- These cells are connected in series forming the Boundary-Scan Register (BSR).
- This structure allows signals to be captured, modified and observed without the need for direct physical access to the pins and without interferinq with the normal operation of the chip.

El va recorre todo los pines y sale.



- During normal operation, data flows directly between pins and internal logic.
- In test mode, the cells allow signals to be captured, switched or monitored.

L.-T. Wang, C.-W. Wu, and X. Wen, *VLSI Test Principles and Architectures: Design for Testability*, San Francisco, CA, USA: Morgan Kaufmann, 2006.

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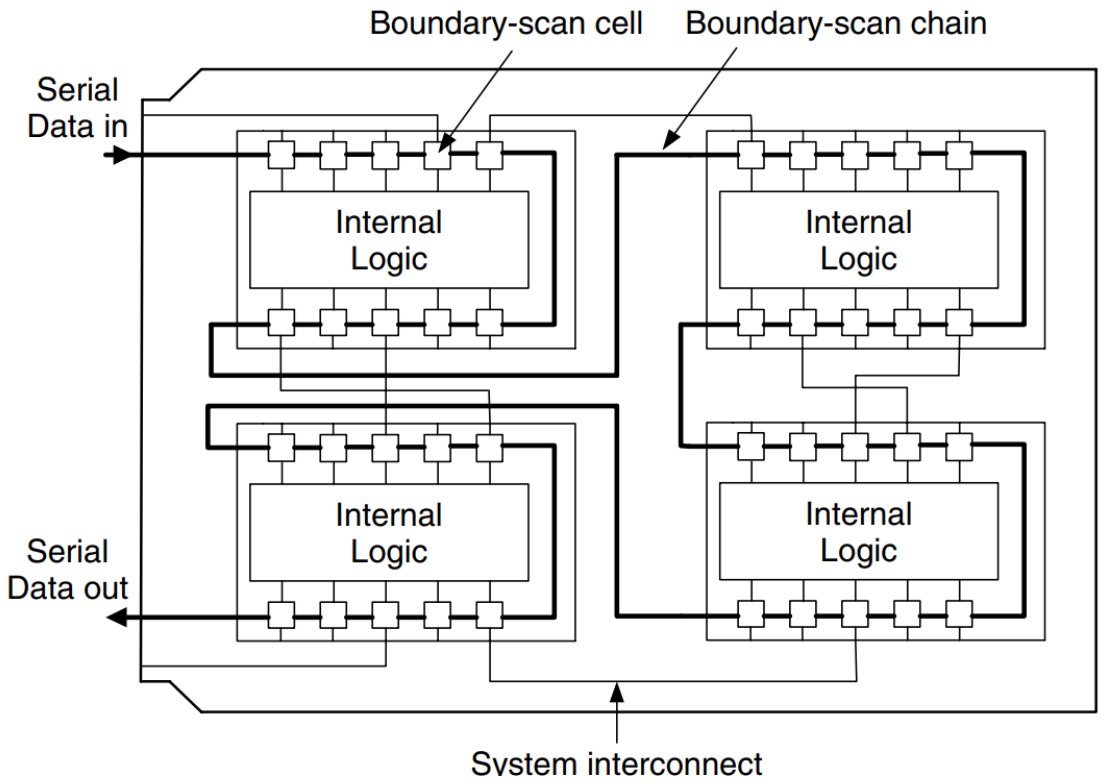
Boundary Scan in Multiple Chip Systems

When multiple ICs are IEEE 1149.1 compliant, their scan cells can be connected in series forming a global test chain on the PCB.

Advantages

- Serial access to all pins of multiple ICs.
- Allows testing:
  - Internal logic of each chip.
  - Physical connections between chips (PCB tracks).
- Scanning and capture does not interfere with normal system operation.

Los prueba todos en un mismo ensayo.



L.-T. Wang, C.-W. Wu, and X. Wen, *VLSI Test Principles and Architectures: Design for Testability*, San Francisco, CA, USA: Morgan Kaufmann, 2006.

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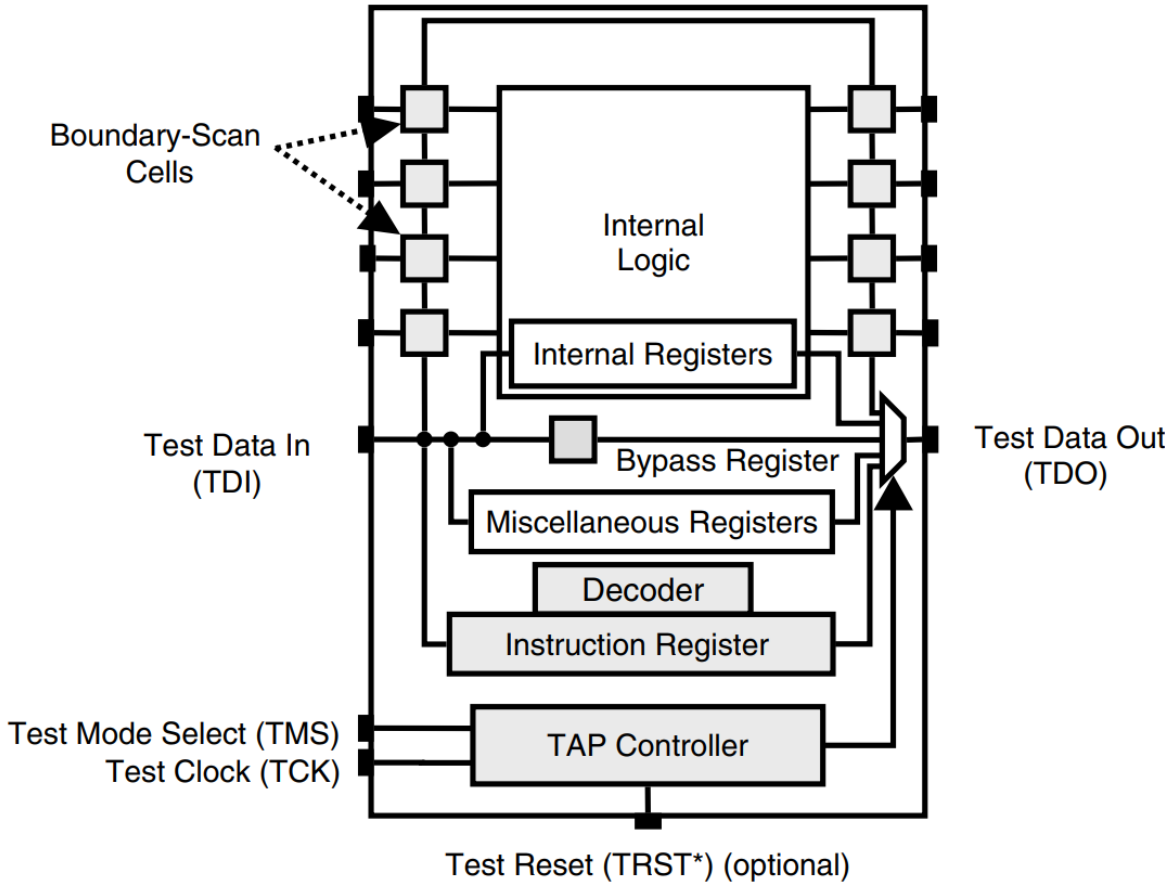
Boundary Scan Architecture

Main hardware components

1. **Test access port** (TAP)
   - Test data input (TDI)
   - Test data output (TDO)
   - Test clock (TCK)
   - Test mode select (TMS)
   - Test reset (TRST)
2. **TAP controller** (TAPC)
3. **Instruction register** (IR) and its associated decoder
4. **Several test data registers**, including the mandatory boundary-scan register and bypass register, and some optional miscellaneous registers, such as the device-ID register, and some design-specific test data registers

Tiene reloj para probar dentro, es del JTAG no del sistema.

Vea la semejanza del un procesador con JTAG vea que tiene registros, tiene registros de instruciones, decodificador, un controller, ...



L.-T. Wang, C.-W. Wu, and X. Wen, *VLSI Test Principles and Architectures: Design for Testability*, San Francisco, CA, USA: Morgan Kaufmann, 2006.

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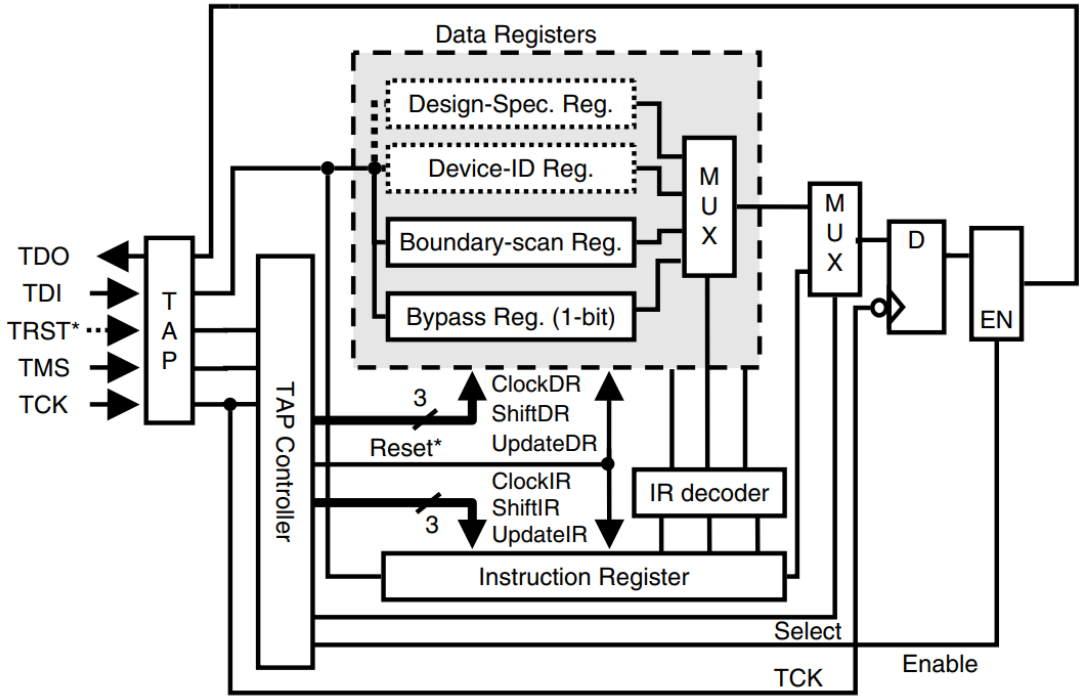
Test Access Port (TAP)

The TAP of 1149.1 contains four mandatory pins and one optional pin:

1. Test Data Input (TDI):

- Serial **input** for:
  - Test **instructions:** loaded into the Instruction Register (IR).
  - Test **data:** loaded into Data Registers (e.g., BSR).
- Data is **clocked** in on the rising edge of TCK.
- Expected to change on the **falling edge** of TCK (controlled by the test master).
- If left undriven, should default to **logic '1'** (fail-safe behavior).



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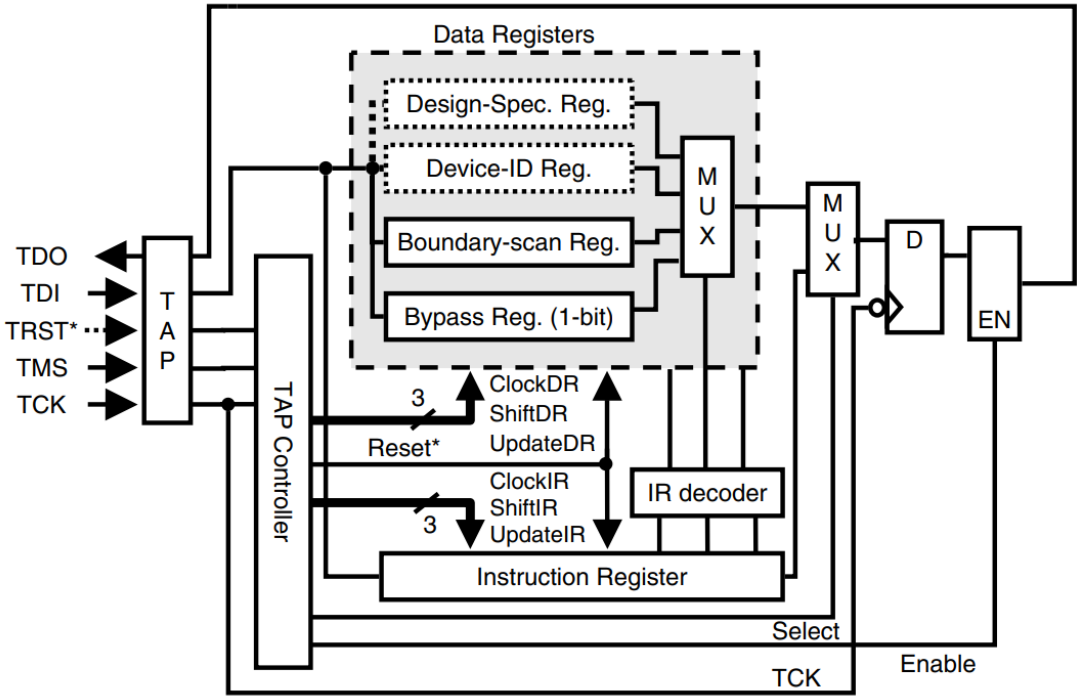
Test Access Port (TAP)

The TAP of 1149.1 contains four mandatory pins and one optional pin:

2. Test data output (TDO):

- Serial **output** for test data from the chip.
- Data is **updated** on the falling edge of TCK.
- Driver is **inactive** unless a scan operation is active.
- **No data inversion**: what goes into TDI is shifted out through TDO as-is.
- Controlled by an internal **Enable** signal to tri-state the output when not used.

Normalemente un O en el nombre implica alta impedancia.



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Test Access Port (TAP)

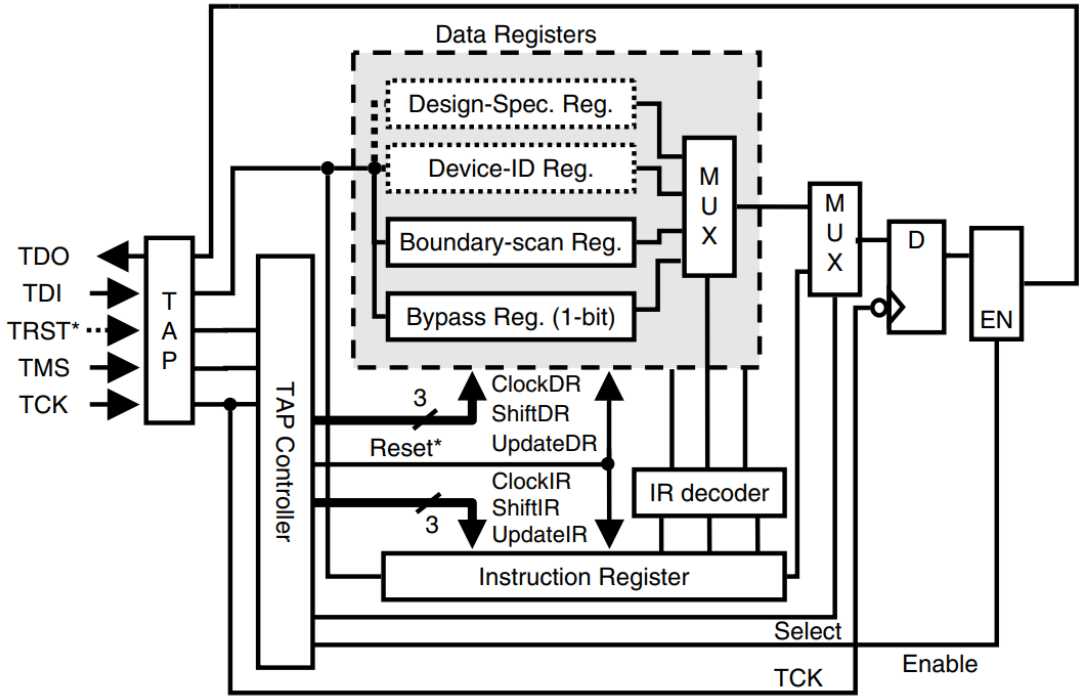
The TAP of 1149.1 contains four mandatory pins and one optional pin:

3. Test clock (TCK)

- Provides the **clock signal** for all test operations (shift, capture, update).
- **Independent** from system clock, ensuring that test operations do not interfere with system functionality.
- Enables **synchronous shifting** and **capturing** across different chips or modules even if their internal clocks differ.

Ese tiene el mismo periodo?, que se refiere con sync shifting.

Shifting = al corrimiento que sucede en el scan que le pasa un dato al siguiente y así sucesivamente.



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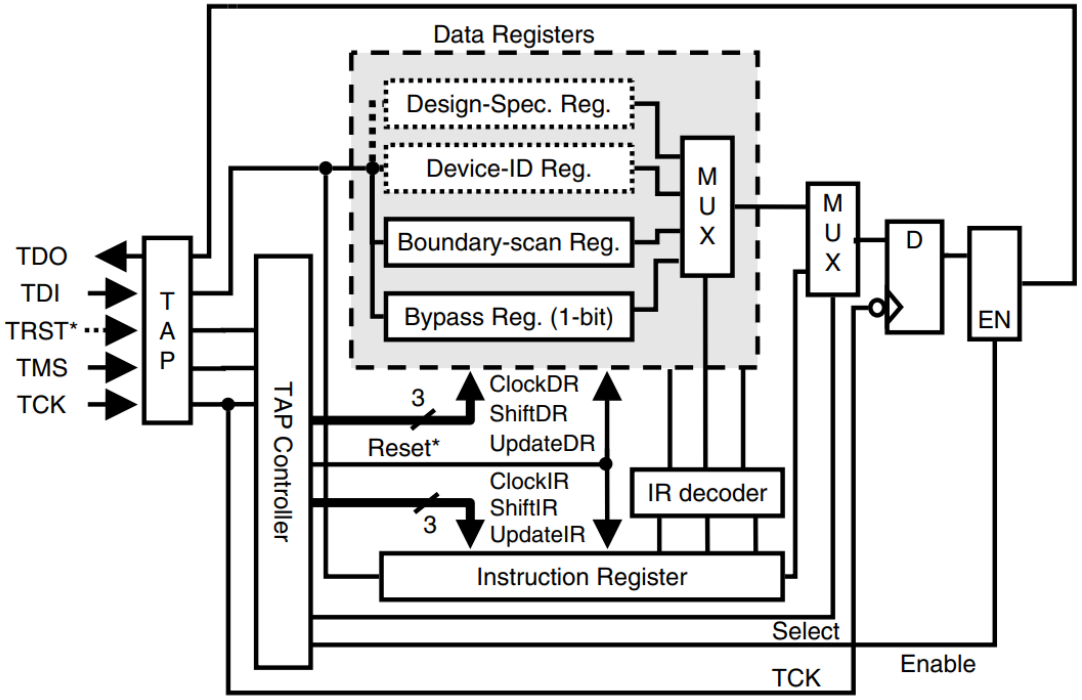
Test Access Port (TAP)

The TAP of 1149.1 contains four mandatory pins and one optional pin:

4. Test mode select (TMS)

- **Main control** input for the TAP Controller (16-state FSM).
- Dictates boundary-scan operations: Capture, Shift, Pause, Update, etc.
- Sampled on the **rising edge** of TCK.
- Expected to be modified on the **falling edge** of TCK.
- Should be driven to **logic '1'** when inactive (ensures safe FSM state transitions).



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Data Registers and Boundary-Scan Cells

Mandatory Registers in Every JTAG-Compliant Chip

1. **Boundary-Scan Register (BSR)**
   - Composed of **Boundary-Scan Cells (BSCs)** inserted at each I/O pin.
   - Each BSC can function as **input**, **output**, or **bidirectional**.
   - Implements a **shift register chain** from TDI to TDO.
2. **Bypass Register**
   - A **single-bit register** used to bypass a device during scan operations.
   - Helps **reduce total shift time**, especially in large scan chains.

Yo me puedo saltar boundary-scan cells, haciendo bypass porque pasa si probe un 48 registros y solo 2 ultimos me dieron un problema. Yo puedo hacer un bypass de los primeros 46 para ver que sucede en los últimos.

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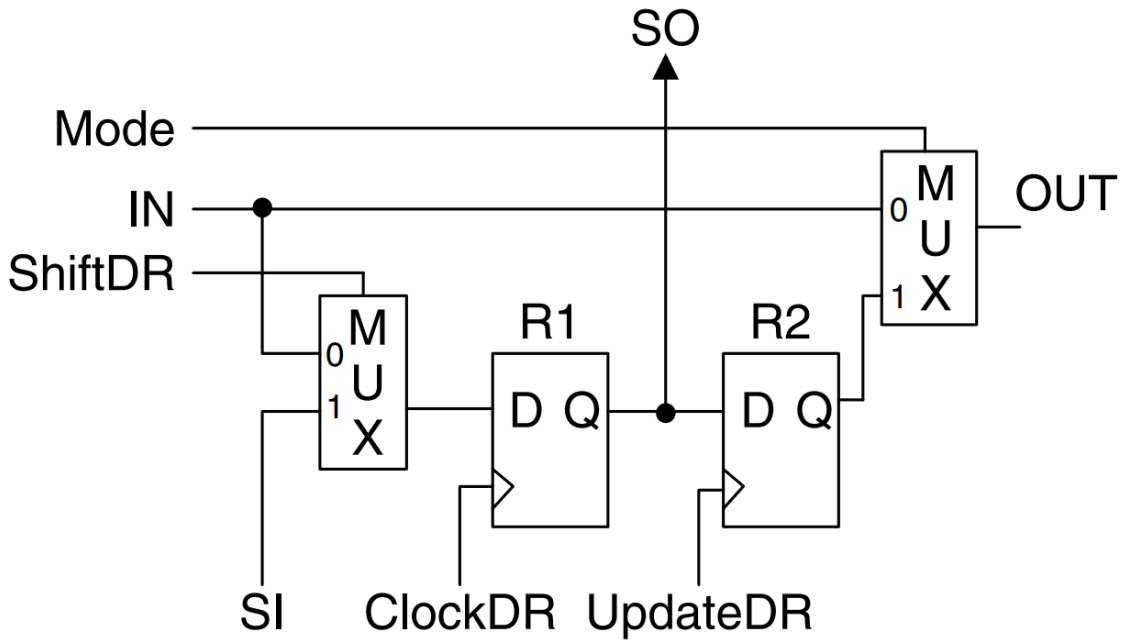
Typical Boundary-Scan Cell

BSC Operating Modes (based on the Mode signal)

- **Mode = 0 (Normal):** IN ⟶ OUT (cell is transparent).
- **Mode = 1 (Test):** R2 (test data) ⟶ OUT (via multiplexer).

Controlled by TAP Signals

TAP Signal	Function
ClockDR	Clock pulse for capturing or shifting
ShiftDR	Enables shift mode
UpdateDR	Updates R2 (the output latch) from R1



Ese IN es la entrada del PIN y SI es la entrada del JTAG.

Si habilito el IN obtengo obversabilidad
Mientras si habilito SI obtengo controllabilidad.

SO es la salida del JTAG que está encantado con las de mas Boundary-Scan Cells

ClockDR es el reloj del JTAG osea este siempre va con el JTAG.

Mientras UpdateDR es que eralmente setea el valor en la salida.

L.-T. Wang, C.-W. Wu, and X. Wen, *VLSI Test Principles and Architectures: Design for Testability*, San Francisco, CA, USA: Morgan Kaufmann, 2006.

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Optional Registers and Boundary Scan Cell Operations

Main BSC Operations

- **Capture:** ShiftDR = 0, one ClockDR pulse ⟶ input (IN) is latched into R1.
- **Shift:** ShiftDR = 1, multiple ClockDR pulses ⟶ data shifts SI ⟶ SO through the BSR chain.
- **Update**: UpdateDR pulse ⟶ R1 content is latched into R2 (can drive OUT if Mode = 1)

These operations can happen **even while the circuit is in normal mode**, enabling flexible testing and data latching.

Optional Registers

- **Device ID Register**:
  - Stores manufacturer ID, part number, and version.
  - Useful for chip identification, debugging, and traceability.
  - Data can be scanned out after mounting on a board.
- **Design-Specific Registers**: Used for custom scan paths, BIST, or test data compression.

TAP Controller

The **TAP Controller** is a **16-state finite-state machine (FSM)** that orchestrates all boundary scan operations defined in IEEE 1149.1.

How it works

- State transitions occur on the rising edge of TCK (Test Clock).
- The **value of TMS** (Test Mode Select) determines the **next state**.
- It controls all activities: instruction loading, data capture, shifting, and updating.

Main functions

- Resetting the boundary-scan architecture
- Providing control signals to load instructions into the instruction register
- Providing signals to perform test functions such as Capture and Update (application) of test data
- Providing control signals to shift test data from TDI to TDO

State diagram of TAP controller

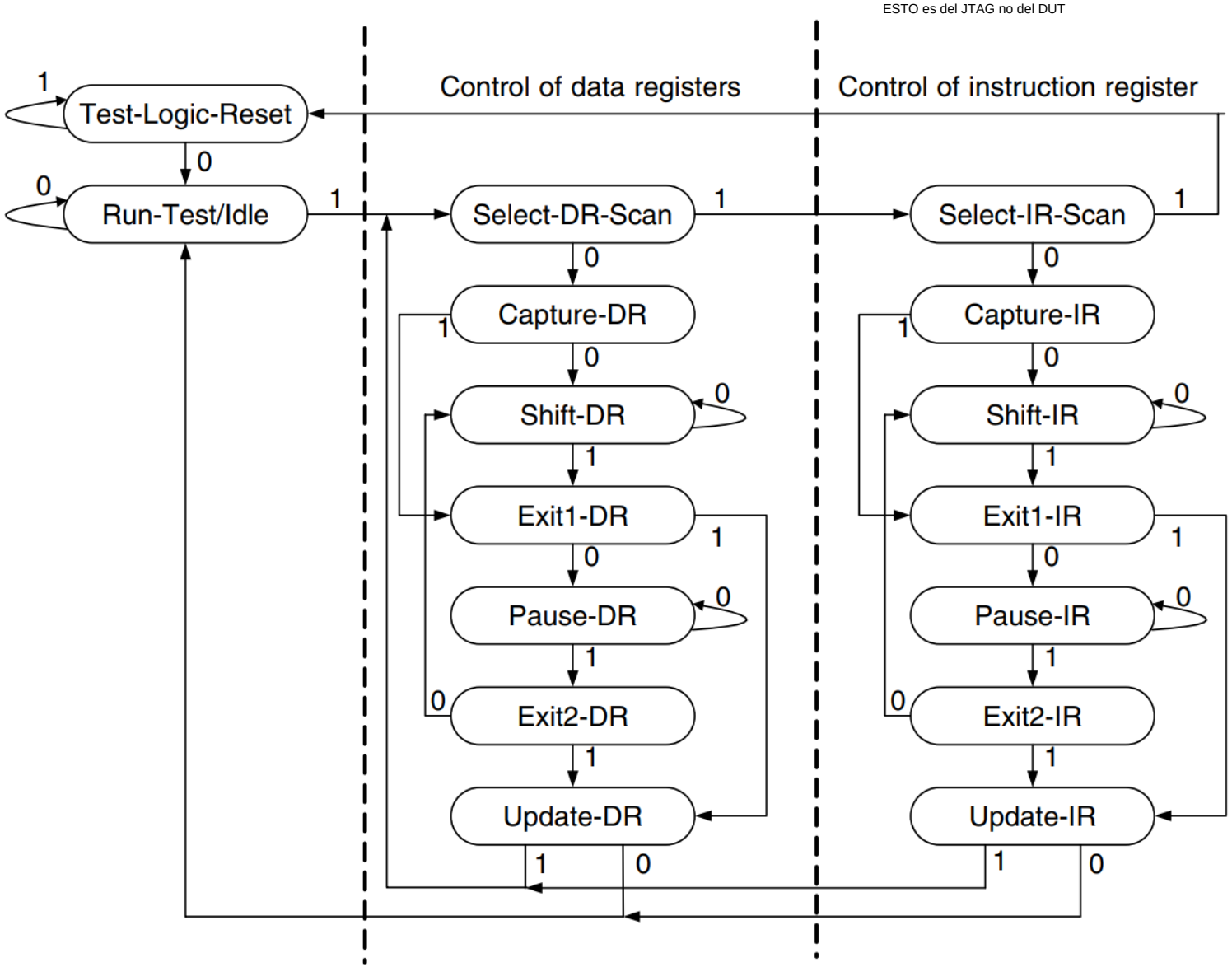
TMS
Note que 1 normalmente significa que no haga nada al inicio..

Capture-DR captura el dato y lo guarda en el Boundry-scan cell

Shift-DR hace los corrimientos necesearios para que pase atraves de los Boundrys-scan cells

Los Exit1-DR es una pausa que hace para esperar que el sistema sete bien los datos.

ESTO es del JTAG no del DUT



L.-T. Wang, C.-W. Wu, and X. Wen, *VLSI Test Principles and Architectures: Design for Testability*, San Francisco, CA, USA: Morgan Kaufmann, 2006.

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State diagram of TAP controller

State	Main Purpose	Transition Event	Associated Actions
Test–Logic–Reset	Resets all boundary-scan logic.	TRST*=0 or TMS=1 for 5 consecutive TCK rising edges	TAP enters safe reset state. Normal chip operation resumes.
Run-Test/Idle	Idle state or executes background operations (e.g., BIST).	TMS=0 from Reset or Update	Allows test logic to run while scan paths are idle.
Select-DR-Scan	Prepares to access data registers (DR).	TMS=1 from Run-Test/Idle	Routes to data register control flow.
Capture-DR	Captures current data into the selected data register.	TMS=0 from Select-DR-Scan	Loads test inputs or circuit values into R1. Shift-DR
Shift-DR	Shifts data through the selected data register (e.g., BSR).	TMS=0 from Capture-DR or Exit2-DR	Enables serial shift between TDI and TDO.
Exit1-DR	Intermediate state; transition to Pause or Update.	TMS=1 from Shift-DR	Allows path change based on TMS.
Pause-DR	Temporarily halts shifting; waits for external input.	TMS=0 from Exit1-DR	Holds register content. Useful during long shift operations.
Exit2-DR	Exits Pause-DR or loops back to Shift-DR.	TMS=1 from Pause-DR	Chooses to return to Shift-DR or proceed to Update-DR.
Update-DR	Loads captured data from R1 to R2; applies it to circuit if needed.	TMS=1 from Exit1-DR or Exit2-DR	Applies new data to output pins or internal logic.

State diagram of TAP controller

State	Main Purpose	Transition Event	Associated Actions
Select-IR-Scan	Prepares to access the instruction register (IR).	TMS=1 from Select-DR-Scan	Switches from DR control flow to IR control flow.
Capture-IR	Captures current instruction into the IR shift register.	TMS=0 from Select-IR-Scan	Loads default or test-specific value into IR.
Shift-IR	Shifts instruction bits into the IR.	TMS=0 from Capture-IR or Exit2-IR	Serially loads new instruction via TDI.
Exit1-IR	Intermediate state; transition to Pause or Update for IR.	TMS=1 from Shift-IR	Allows selection of next path.
Pause-IR	Temporarily halts IR shifting.	TMS=0 from Exit1-IR	Suspends IR shift operation (e.g., for timing control).
Exit2-IR	Exits Pause-IR or loops back to Shift-IR.	TMS=1 from Pause-IR	Moves back to Shift-IR or on to Update-IR.
Update-IR	Loads instruction from shift path into IR output latch.	TMS=1 from Exit1-IR or Exit2-IR	Executes new instruction (e.g., EXTEST, SAMPLE).

Instruction Register and Instruction Set

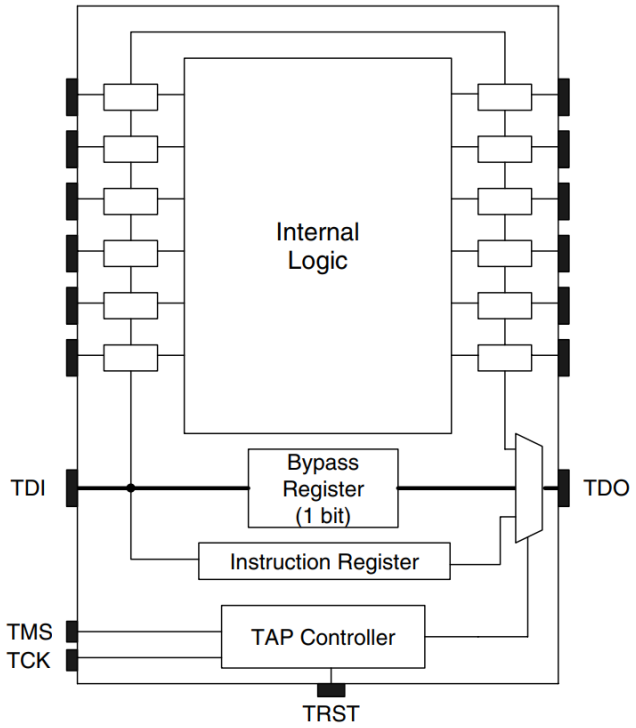
- The instruction register is used to store the instruction to be executed.
- According to the standard, the register must have a two-stage design.
  - So that when a new instruction is entered, the current instruction can be latched on the parallel output of the IR to avoid the possibility of having an indeterminate state on the IR output.

Mandatory Boundary-Scan Instructions (IEEE 1149.1)

Instruction	Purpose	Main Behavior	Notes
BYPASS	Skip unused devices	Connects TDI directly to TDO through 1-bit bypass register	Reduces scan time; loaded by default after TAP reset (unless IDCODE is present)
SAMPLE	Observe normal operation	Captures system signals into boundary-scan registers (during Capture-DR)	No effect on logic or I/O; useful for debugging
PRELOAD	Load test pattern	Shifts data into BSR before switching to another instruction (e.g., EXTEST)	Ensures safe values at outputs before test begins
EXTEST	Test external interconnects	Drives outputs and captures responses at other devices	Works together with PRELOAD for seamless transition
(Recommended) **INTEST**	Test internal logic	Drives internal inputs via BSR and captures responses	Often used to test internal logic blocks using scan

Instruction Register and Instruction Set

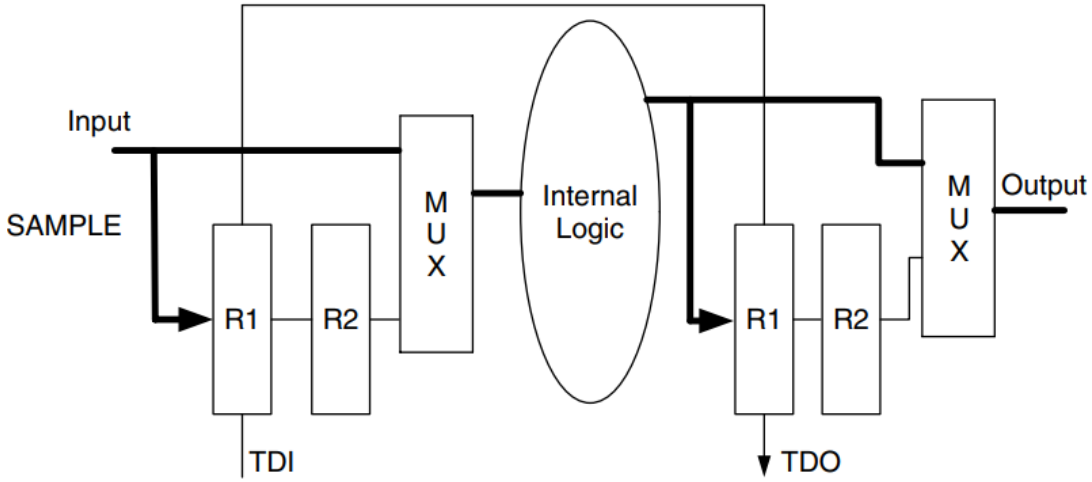
Execution of the BYPASS instruction



El bypass literealmente no pasa por ningun Boundry-scan cell. Pasa por el regitro y ala salida. Litrealmente no pasa el DUT

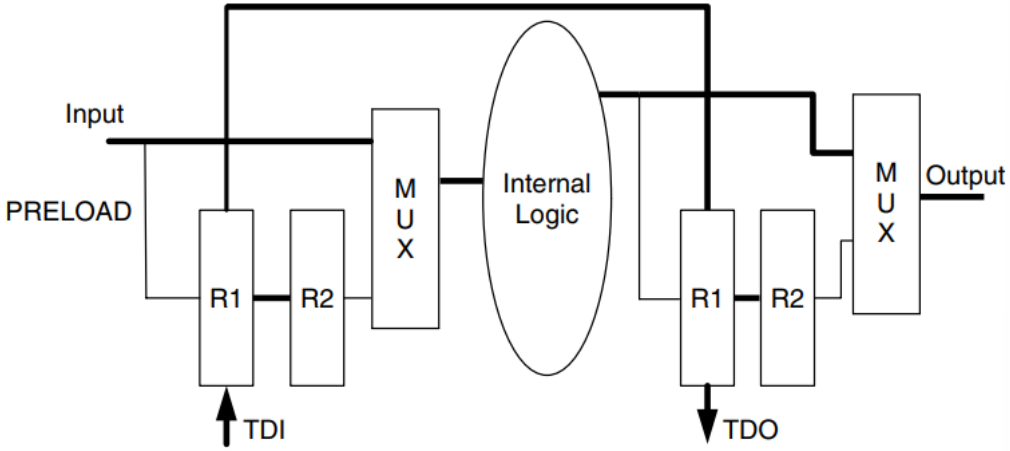
Literalmente pura observabilidad. Solo le metodo los IN al DUT

Execution of SAMPLE instruction.



Aqui si hago la controbilidad atraves de la entradas del Boundry-scan cells. Hacia aufera

Execution of PRELOAD instruction.



L.-T. Wang, C.-W. Wu, and X. Wen, *VLSI Test Principles and Architectures: Design for Testability*, San Francisco, CA, USA: Morgan Kaufmann, 2006.

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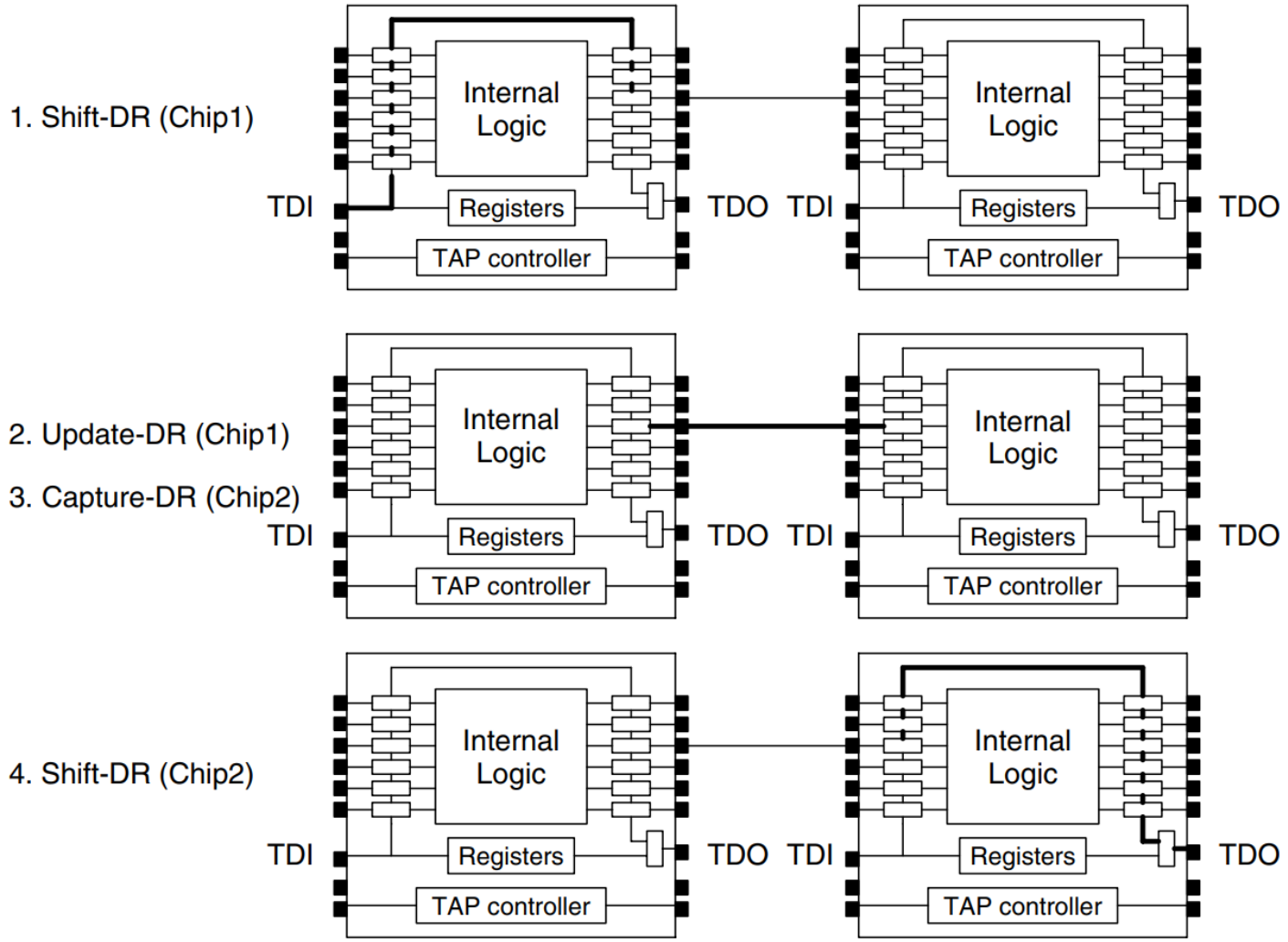
Instruction Register and Instruction Set

Execution of EXTEST instruction (connect TDI and TDO to the BSCAN Register)



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Instruction Register and Instruction Set

Optional Instructions (Commonly Supported in IEEE 1149.1)

Instruction	Purpose	Main Behavior	Notes
RUNBIST	Run built-in self-test (BIST)	Activates user-defined BIST logic internally	Must be supported by design-specific logic
CLAMP	Hold safe output values	Drives outputs with PRELOADed data; no further shifting	Similar to BYPASS in chain behavior (short path)
IDCODE	Read chip identity	Loads manufacturer ID, part number, version into Device ID Register	Default after reset if implemented; useful for inventory/debugging
USERCODE	Read user-programmed ID	Loads a user-defined 32-bit code from a programmable chip	Used especially in FPGAs or programmable devices
HIGHZ	Disable all outputs	Places all output pins in high-impedance state	Useful in multi-device testing to avoid conflicts

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Typical Test Procedure Using Boundary Scan

1. A boundary-scan test instruction is shifted into the IR through the TDI.
2. The instruction is decoded by the decoder associated with the IR to generate the required control signals so as to properly configure the test logic.
3. A test pattern is shifted into the selected data register through the TDI and then applied to the logic to be tested.
4. The test response is captured into some data register.
5. The captured response is shifted out through the TDO for observation, and, at the same time, a new test pattern can be scanned in through the TDI.
6. Steps 3 to 5 are repeated until all test patterns are shifted in and applied, and all test responses are shifted out.

On-Chip Test Support with Boundary Scan

Although IEEE 1149.1 focuses on test circuitry at the chip boundary, it can be extended to control internal **DFT** logic (e.g., BIST, scan chains) by:

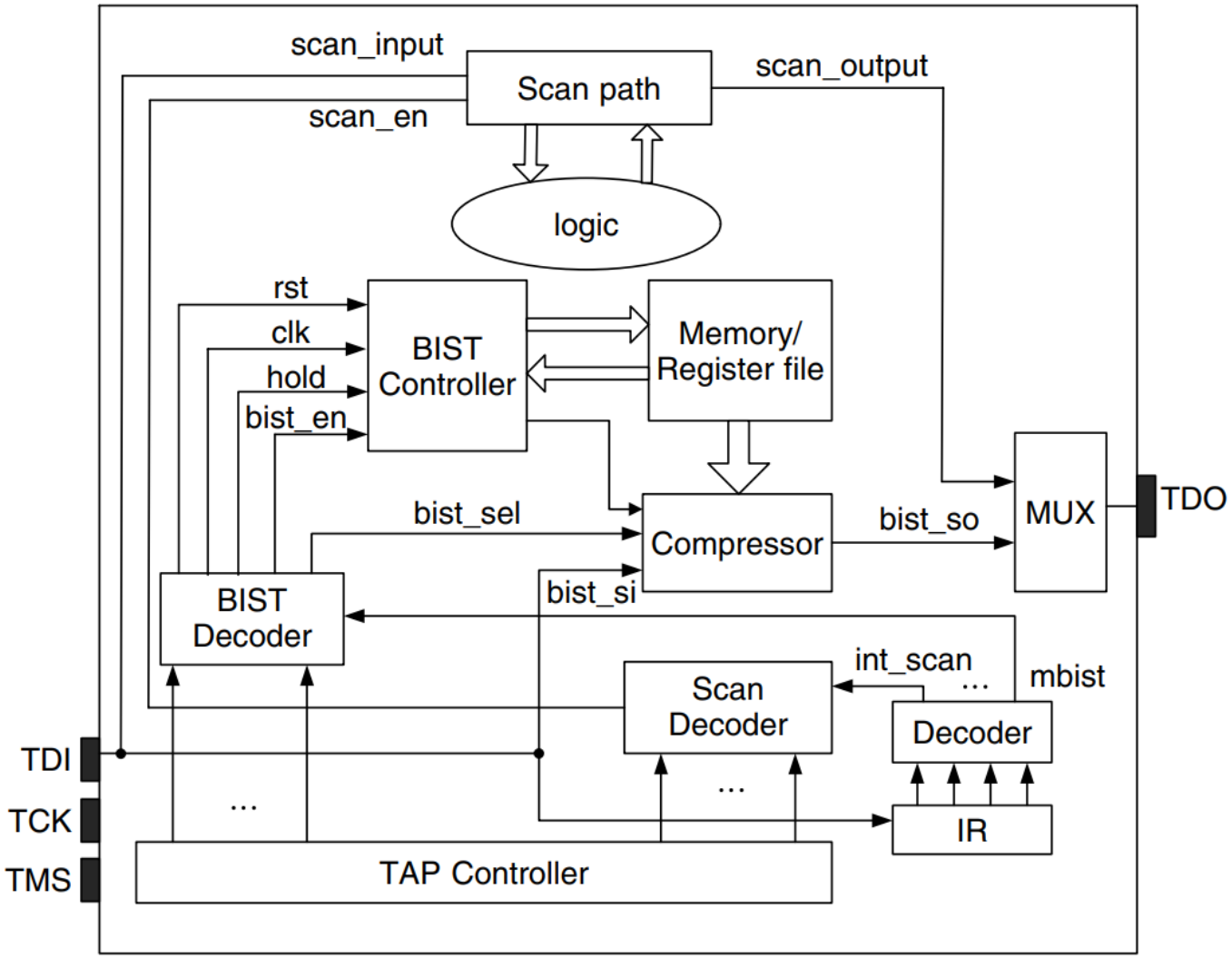
- Adding custom instructions (e.g., RUNBIST, RUNSCAN)
- Designing the IR decoder to activate control lines based on the loaded instruction
- Routing TAPC control outputs to internal DFT logic via custom decoders

Example Flow for BIST Activation

1. **RUNBIST** instruction is loaded into the IR ⟶ activates mbist control line.
2. **TAPC enters Test–Logic–Reset** ⟶ resets the BIST controller (rst signal).
3. (Optional) Initialize compressor via bist-sel using TDI input.
4. **TAPC enters Run-Test/Idle** ⟶ enables BIST controller (bist_en).
5. Upon BIST completion, **TAPC switches to shift mode** to scan out results via TDO.
6. Use hold signal to pause BIST controller if needed (e.g., waiting for TAP state).

On-Chip Test Support with Boundary Scan

Example Flow for BIST Activation



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IEEE 1150

What is IEEE 1500?

A mechanism for the test of core designs within a system on chip (SoC) that defines a hardware architecture and leverages the core test language (CTL) to facilitate communication between core designers and core integrators.

Key Problem Addressed

- Modern SoCs contain multiple reusable IP cores.
- Each core may have different test requirements.
- Need standardized way to access and test embedded cores

Hardware Architecture

- **Test Wrapper**: Isolates individual cores for testing
- **Wrapper Interface**: Standardized test access points
- **Test Data Routing**: Manages test signals between cores

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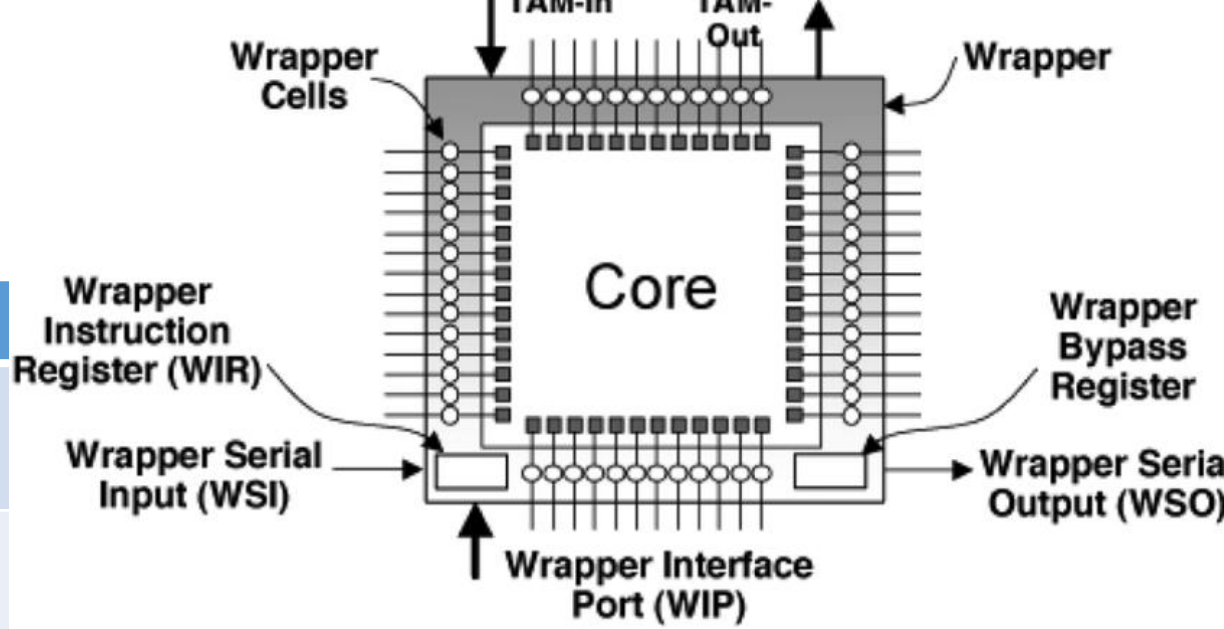
IEEE 1150

Detailed Wrapper Components

Component	Detail
Test Access Mechanism input (**TAM-In**)	Data path into the wrapper.
Test Access Mechanism output (**TAM-Out**)	Data path out of the wrapper.
Wrapper Cells	Interface cells that control signals between core and wrapper.
Wrapper	Complete test isolation structure around the core.
Wrapper Instruction Register (**WSI**)	Controls wrapper operation modes.
Wrapper Bypass Register	Allows bypassing of wrapper when not in test mode.
Wrapper Serial Input (**WIR**)	Serial data input to wrapper boundary.
Wrapper Serial Output (**WSO**)	Serial data output from wrapper boundary.
Wrapper Interface Port (**WIP**)	Standardized connection points.



Es como un wrapper el CTL es para que digamos que tengo un RISC-V y un ARM entonces generalizo el comportamiento de los cores.

Taken from: https://www.researchgate.net/figure/EEE-1500-core-test-wrapper-architecture_fig1_3338144

IEEE 1150

Core Test Language (CTL)

- Describes implemented wrapper functionalities in a standard format
- Enables communication between core designers and integrators
- Facilitates automated test generation for core-based designs

Benefits

- **Modular Testing**: Test individual cores independently
- **IP Reuse**: Standard test interface for all cores
- **Scalability**: Works with complex multi-core SoCs
- **Automation**: Enables automated test pattern generation

IEEE 1687 (iJTAG): Internal JTAG Standard

Description Languages

- Instrument Connectivity Language (ICL): Describes the behavior of the instrumentation network within a chip in a standard way.
- **Procedure Description Language (PDL):** Defines test procedures and transformations.

Applications

- **Built-in Instruments**: Oscilloscopes, counters, monitors
- **Debug Features**: On-chip debugging capabilities
- **Parametric Testing**: Embedded measurement instruments
- **Field Testing**: Post-deployment diagnostics

iJTAG

i es internal

significa que cambia el DUT este si es invasivo.

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IEEE 1687 (iJTAG): Internal JTAG Standard

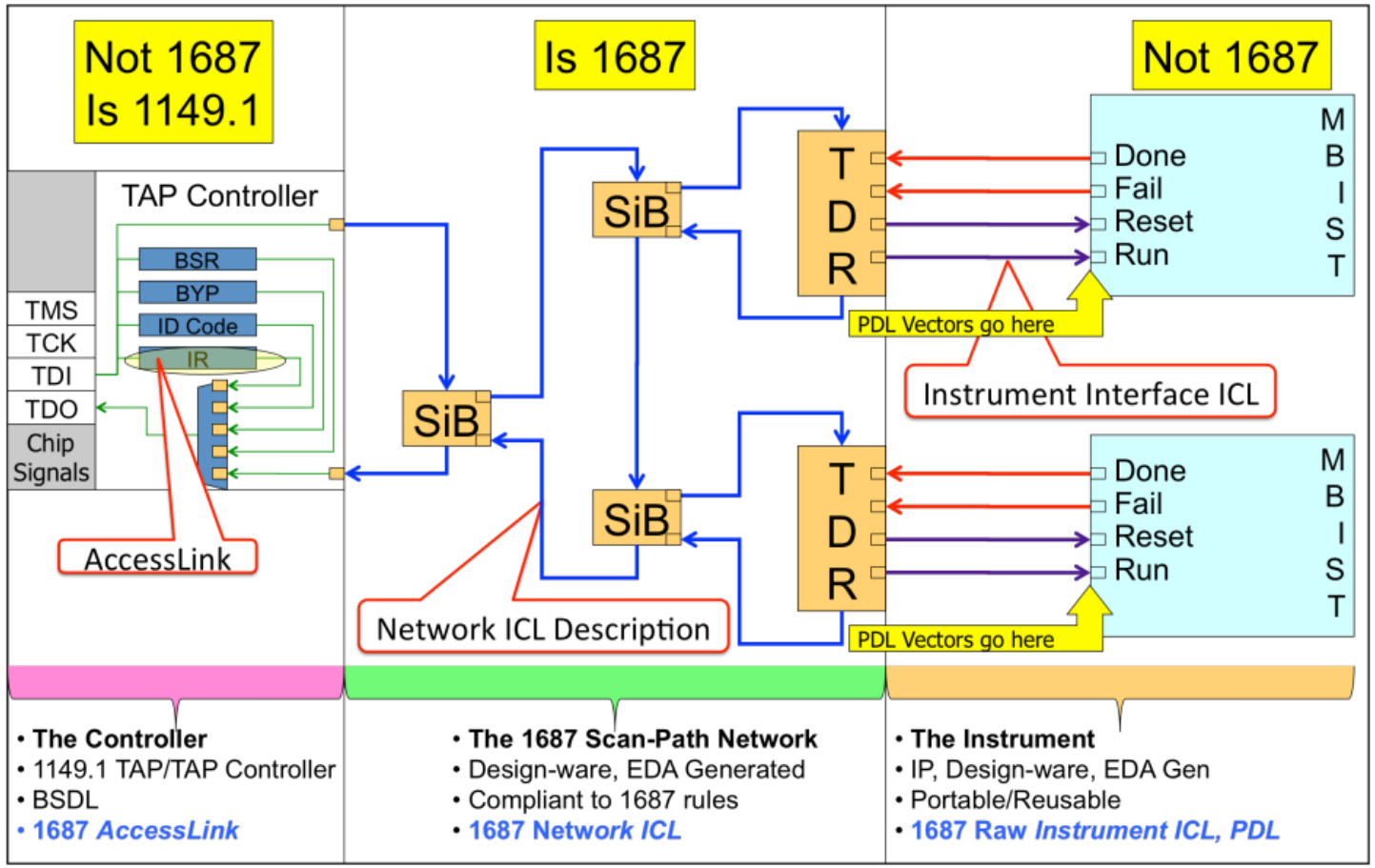

Figure 2: IEEE 1687 IJTAG basic architecture

https://www.asset-intertech.com/wp-content/uploads/2023/01/IJTAG-Tutorial-third-edition.pdf

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Comparison of standards

Aspect	IEEE 1500	IEEE 1149.1 (JTAG)	IEEE 1687 (iJTAG)
Primary Focus	Core-based SoC testing	Board-level interconnect testing	Embedded instrumentation access
Target Level	Individual IP cores within SoC	Chip-to-chip connections	On-chip embedded instruments
Interface	Test wrapper architecture	4-5 pin TAP (TMS, TCK, TDI, TDO, TRST)	Extended JTAG TAP + internal network
Key Architecture	Core test wrapper	Boundary scan chain	Instrumentation network
Description Language	CTL (Core Test Language)	BSDL (Boundary Scan Description Language)	ICL + PDL (Instrument Connectivity + Procedure Description)
Test Access	Internal core isolation	External pins only	Internal instruments and features
Reconfiguration	Static per core	Static chain	Dynamic network reconfiguration
Typical Applications	IP core structural testing	Pin/interconnect testing	Debug, parametric test, field diagnostics
Test Patterns	Core-specific ATPG patterns	Simple I/O control	Instrument control sequences
Scalability	Scales with number of cores	Limited by pin count	Highly scalable instrument network
Industry Adoption	Wide SoC adoption	Universal (mandatory for most chips)	Growing in advanced designs
Cost Impact	Low (wrapper overhead)	Minimal (4-5 pins)	Variable (depends on instruments)


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