Lecture and Hands-on Workshop on Design for Test (DFT)

Laboratory 1: Getting Started with DE10-Standard FPGA

Electronics Engineering Department, Costa Rica Institute of Technology

Intel, Costa Rica

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Scope

- **Purpose:** Introduce students to the complete FPGA development flow, from project creation to physical device programming.
- **Approach:** Practical implementation of an ALU (Arithmetic Logic Unit) that performs basic operations and displays results on physical peripherals.

Main Goal

Become familiar with Quartus Prime and the process of implementation on real hardware.

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Laboratory Objectives

1. Configuration

Create and configure a Quartus Prime project for the DE10-Standard.

2. Implementation

Develop a combinational ALU module and a sequential Top module in SystemVerilog.

3. Synthesis

Develop a combinational ALU module and a sequential Top module in SystemVerilog.

4. Validation

Program the FPGA and validate functionality using switches and LEDs.

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Tools and Materials

Software

Quartus Prime 24.1

Standard Edition

Simulation

ModelSim Intel FPGA

Starter Edition 10.5b

Hardware

DE10-Standard

FPGA Board

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Laboratory Objectives

1. **New Project**
   Initial configuration and FPGA device selection
2. **Create Modules**
   ALU implementation and Top module in SystemVerilog
3. **Compile**
   Synthesis, analysis, and design verification
4. **Assign Pins**
   Synthesis, analysis, and design verification
5. **Program**
   Load the design onto the FPGA and validate

Technical Specifications

FPGA: 5CSXFC6D6F31C6

Clock: 50 MHz (PIN_AF14)

Language: SystemVerilog HDL

LALU: Combinational logic

Top Module: Sequential logic

I/O: Switches, Buttons, LEDs

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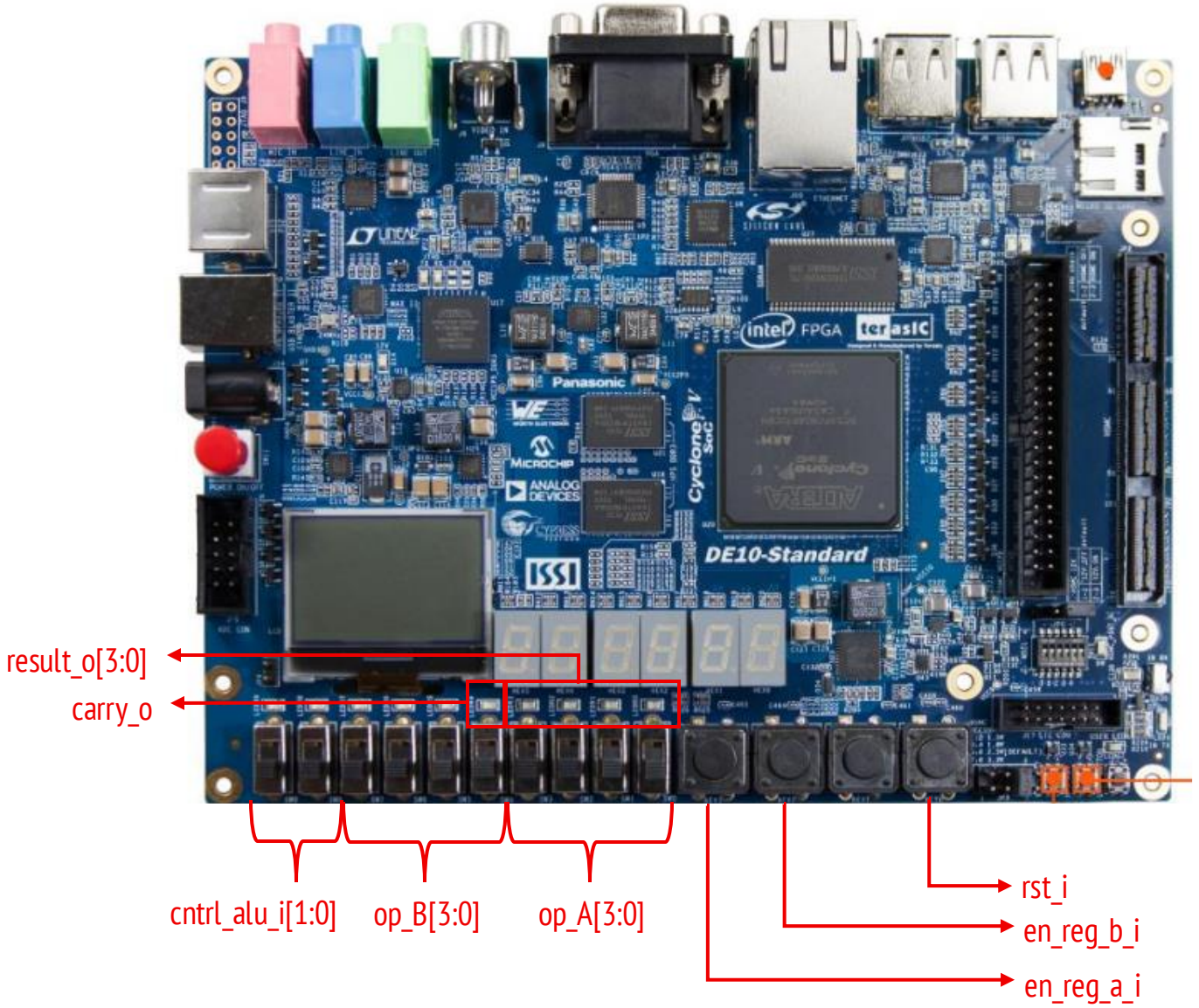
Full User Interface



System Functionality

Reset:
Initializes internal registers

Load Operand A:
Key 2 captures switches 3–0

Load Operand B:
Key 3 captures switches 7–4

ALU Control:
Switches 9–8 select the operation

Result:
LEDs 3–0 display the output

Carry:
LED 4 indicates carry-out

Expected Results

Upon completing this laboratory, students will have:

- ✓ Mastered the Quartus Prime flow
- ✓ Implemented SystemVerilog modules
- ✓ Configured physical pins
- ✓ Compiled the design without errors
- ✓ Successfully programmed the FPGA
- ✓ Validated functionality on hardware

Outcome: A functional ALU operating on real hardware with a user interface through physical peripherals.

Installation Links

Quartus Prime 24.1 Standard Edition:
https://www.intel.com/content/www/us/en/software-kit/849770/intel-quartus-prime-lite-edition-design-software-version-24-1-for-windows.html

ModelSim Intel FPGA Starter Edition 10.5b
ModelSim-Intel® FPGAs Standard Edition Software Version 20.1.1

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