Simulation Procedures for Hspice

How to Define FinFET Transistors

Fig 1. Shows an example of the typical structure of a FinFet. In this technology, the designer has freedom to control the sizes of transistors by means of the channel length (parameter l), the number of fins (parameter nfin), and the number of fingers (parameter nf).

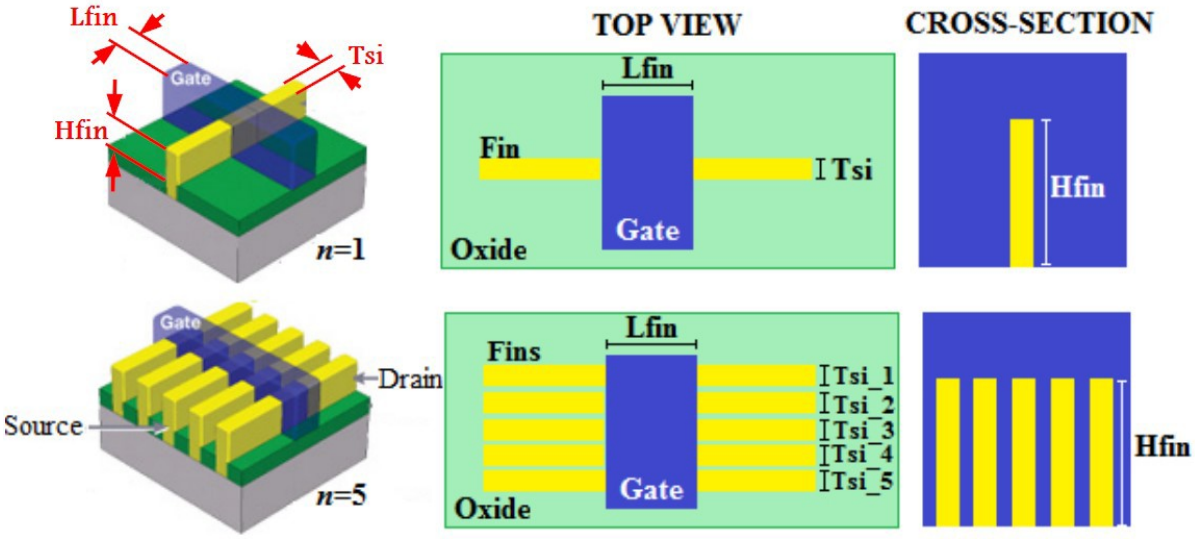


*Figure 1. FinFet Structure, **source**: Zimpeck, et al. "FinFET cells with different transistor sizing techniques against PVT variations". ISCAS 2016.*

An example Hspice netlist for the inverter in Fig.2 is shown:
M1 Q A Vdd Vdd pmos_lvt (nfin = 4 l = 16n nf=2)
M2 Q A Vdd Vdd nmos_lvt (nfin = 4 l = 16n nf=2)

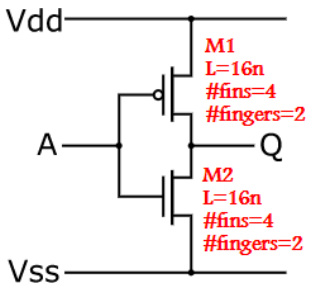


Figure 2 Inverter Example

How to Run Hspice

1) Un-compress the models and save them in your <simulation folder>
2) In text editor, create a netlist and save it in the <simulator folder> with extension .sp or .cir (in this example Comparator.sp)

********** START EXAMPLE COMPARATOR NETLIST **********
.option post runlvl=6
.include '<PATH>/<TT MODELFILE>.inc'
.TEMP 80
m1 p clk 0 0 nmos_lvt (nfin = 4 l = 16n nf=2) m2a xn inp p 0 nmos_lvt(nfin = 4 l = 16n nf=2) m2b xp inn p 0 nmos_lvt(nfin = 4 l = 16n nf=2)

```
m3a outn outp xn 0 nmos_lvt (nfin = 4 l = 16n nf=2 ) m3b outp
outn xp 0 nmos_lvt (nfin = 4 l = 16n nf=2 ) m4a outn outp 1 1
pmos_lvt (nfin = 4 l = 16n nf=2 ) m4b outp outn 1 1 pmos_lvt
(nfin = 4 l = 16n nf=2 ) m5a outn clk 1 1 pmos_lvt (nfin = 4 l =
16n nf=2 ) m5b outp clk 1 1 pmos_lvt (nfin = 4 l = 16n nf=2 )
m6a xn clk 1 1 pmos_lvt (nfin = 4 l = 16n nf=2 )
m6b xp clk 1 1 pmos_lvt (nfin = 4 l = 16n nf=2 ) C1 outp 0
25f
C2 outn 0 25f

vdd 1 0 dc 0.9
vinn inn 0 0.6
vinp inp 0 0.61
************************************
Vclk clk 0 pulse (0 'pvdda' '0.4*per' '0.1*per' '0.1*per' '0.4*per' 'per')
.param freq=250Meg per='1/freq' pvdda=0.9
.tran 'per/50' '20*per'
.probe TRAN V(*)

.alter
.include '<PATH>/<FF MODELFILE>.inc'
.alter
.include '<PATH>/<SS MODELFILE>.inc'

.end
********** END COMPARATOR NETLIST ***********
```

3) set any environment variables required to access your Hspice license and add Hspice executables folder to your path. (This part is dependent on your particular installation and environment.)
4) run the netlist by entering:

hspice Comparator.sp > Comparator.out

```
jsalinas@anubis.eecg[~/Desktop/ECE1352/2020/PTM-MG/tests]> hspice Comparator.sp > Comparator.out
>info:          ***** hspice job concluded
>info:          ***** hspice job concluded
>info:          ***** hspice job concluded
```

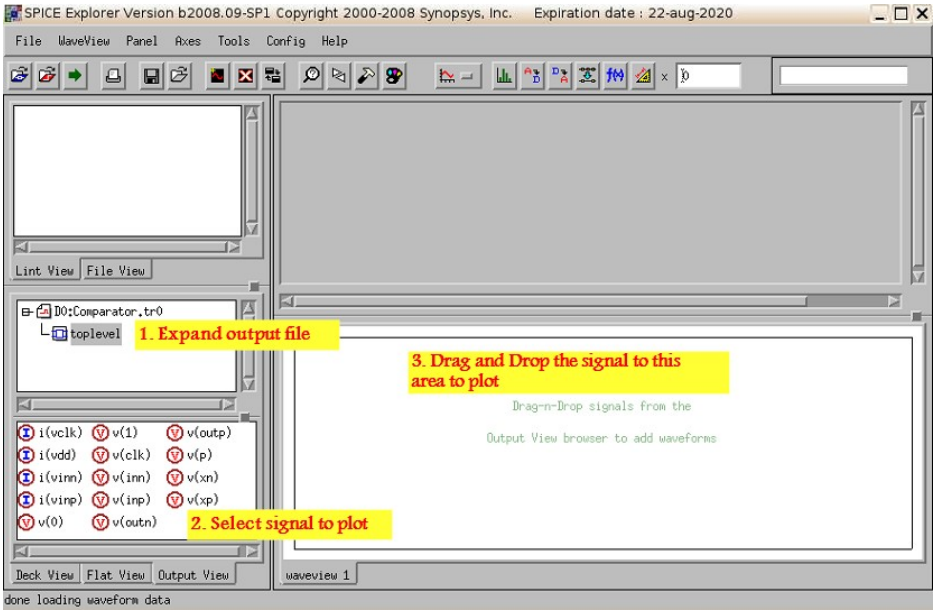
5) Notice how some files with the initials Comparator.* are created (Advice: study what each file is)

```
Comparator.ic0      Comparator.ic2      Comparator.sp       Comparator.tr0      Comparator.tr2
Comparator.ic1      Comparator.out      Comparator.st0      Comparator.tr1
```

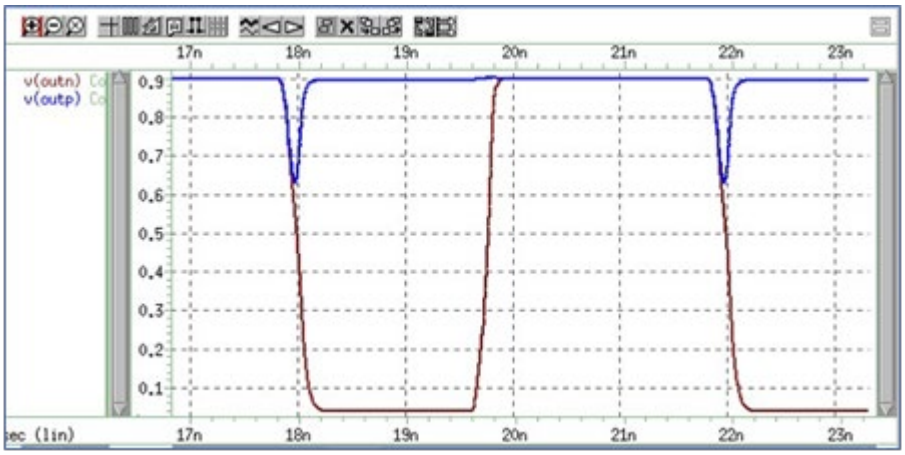
6) Open the waveform viewer (in this case spice explorer)
   a. sx <output file we want to plot>

```
jsalinas@anubis.eecg[~/Desktop/ECE1352/2020/PTM-MG/tests]> sx Comparator.tr0
```

7) plot your results



For example, these are the outputs of the comparator:



- Or you can export the data and plot in other external tools

How To Setup Process Corner Simulation in Hspice

The model may include models for Typical, Slow PMOS/Slow NMOS (SS) and Fast PMOS/Fast NMOS (FF).
In Hspice, with the .include command, we can point to the model file for each corner. For example for TT corner, the command is:
.include './ece1352_models/hp_model_finfet16_TT.inc'

In the example netlist (Comparator.sp), the command ".alter" is used to modify the netlist to point to SS and FF corner models
.alter
After simulating this netlist, three output files are created, each output file corresponds to each process corner.

```
jsalinas@anubis.eecg[~/Desktop/ECE1352/2020/PTM-MG/tests]> sw Com
Comparator.ic0       Comparator.ic2       Comparator.sp       Comparator.tr0       Comparator.tr2
Comparator.ic1       Comparator.out       Comparator.st0      Comparator.tr1
```