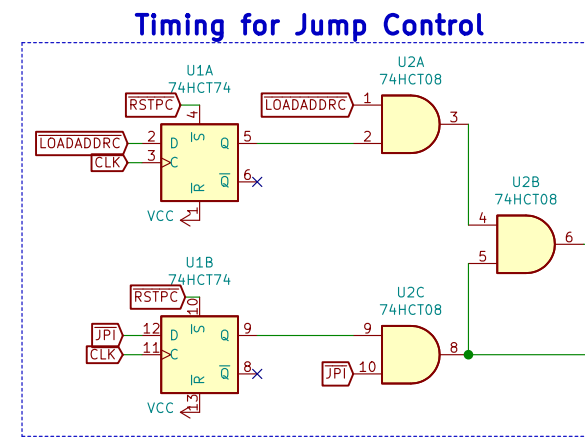


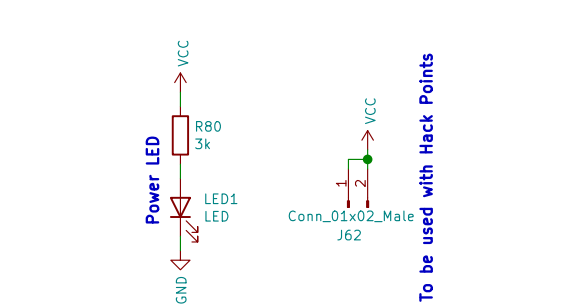
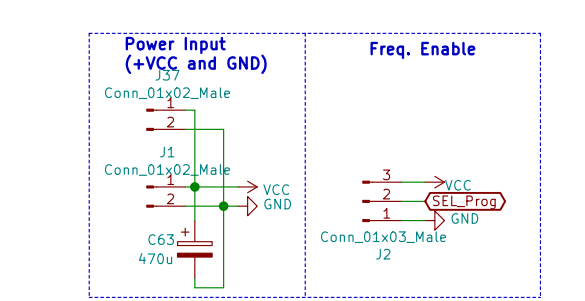
It allows the LD signal to be kept active for a longer time in the jump instructions so that the data containing the address can be loaded. After loading, the LOADADDR or JPI signal (stored in D-type FF 7474) returns to 1. Data loading is synchronized with the clock signal.

Note: 7474 must be started with Q=1.



Conditional jump (short JPC and JPZ):  
PC <= MA[7:4]:A[3:0]  
PCH = PCH (is not modified)  
(Jumps only to addresses in the current memory page)

Unconditional jump (long JPI):  
PC = RC:MA[7:4]:A[3:0]  
PCH <= RC  
(all memory addresses)

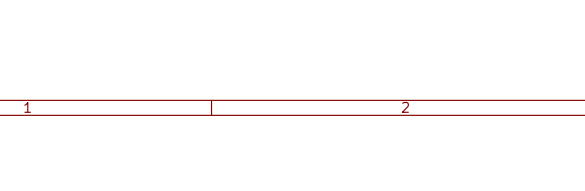
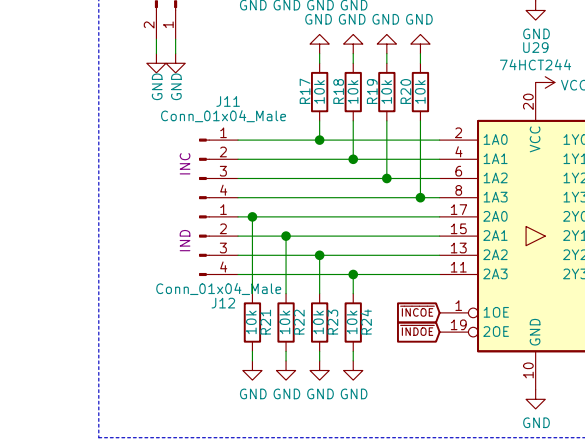
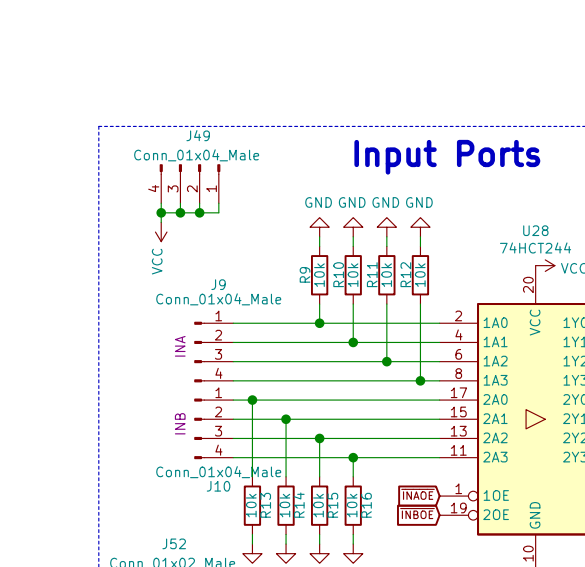
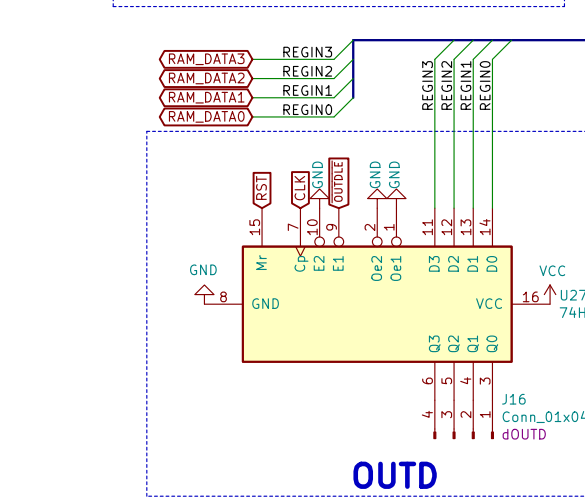
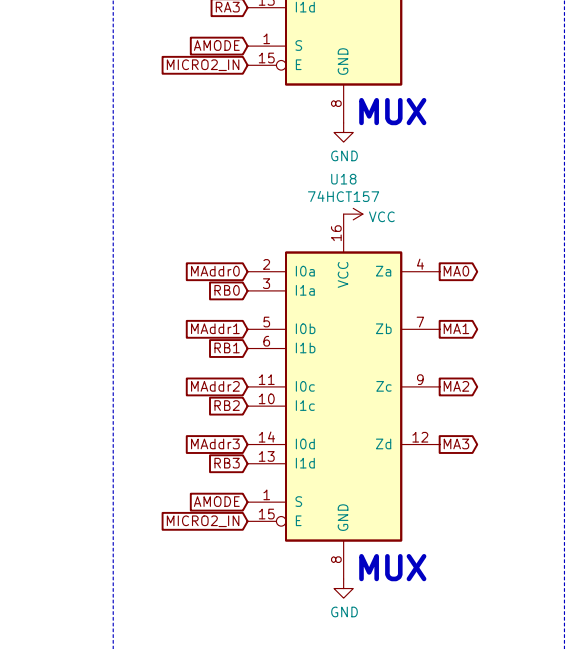
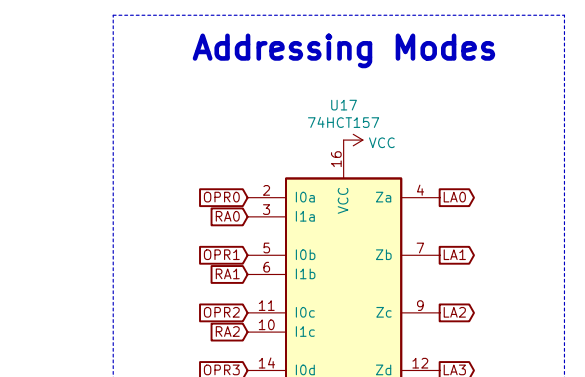


The 8-bit ANDC selects the Addressing Mode. The addressing modes are used for data addressing and jumps.

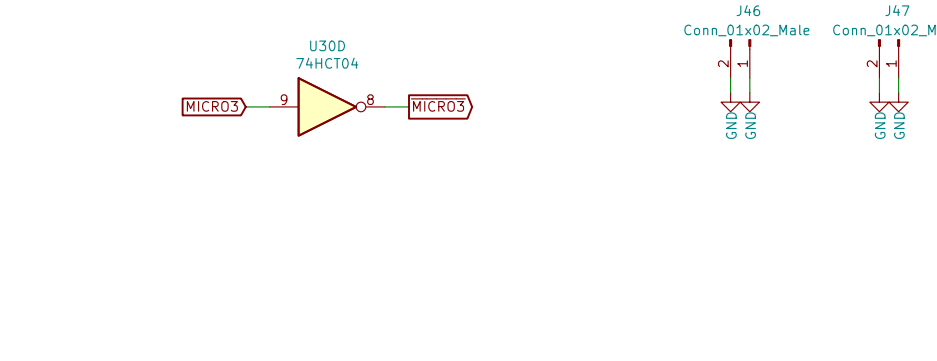
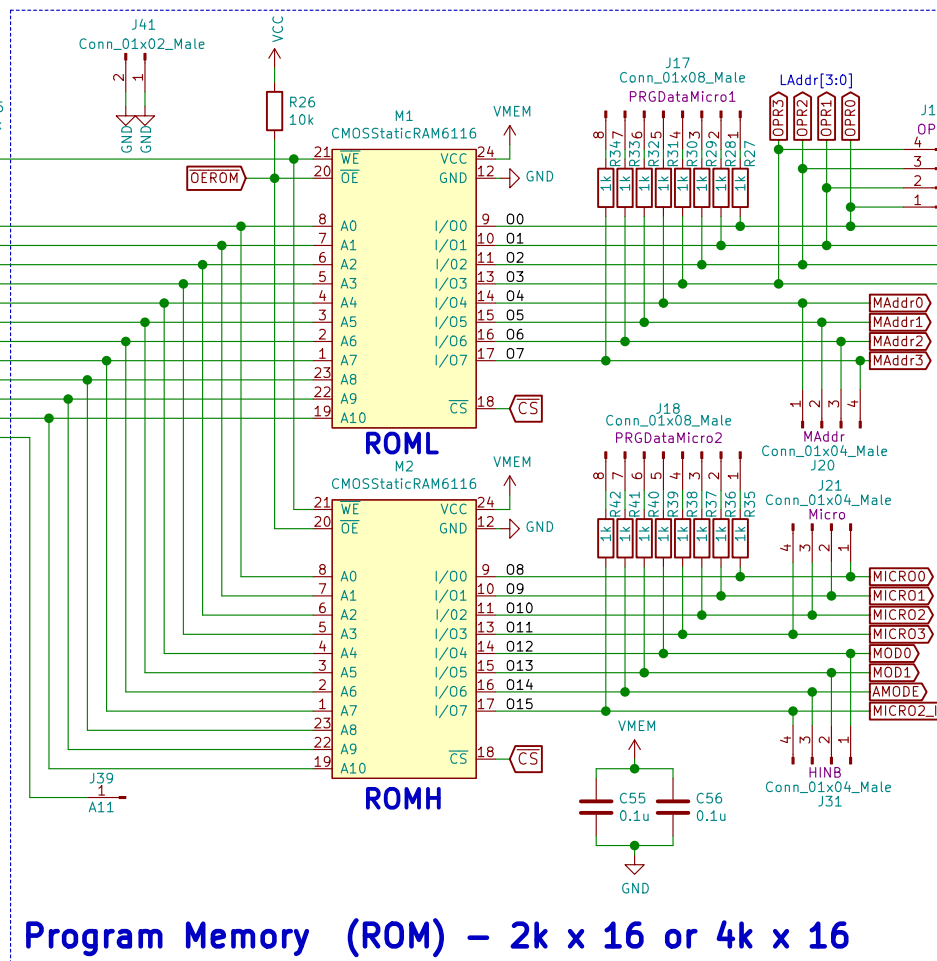
If ANDC=0, Register indirect + immediate addressing mode  
If ANDC=1, Register indirect addressing mode

Register indirect + immediate (R[7:4]:A[3:0])  
Register indirect + Address (R[7:4]:A[3:0])

Note: LDR (Low Address) = DFR (Operand), so the names are interchangeable. Sometimes it can be called LDR and other times DFR.

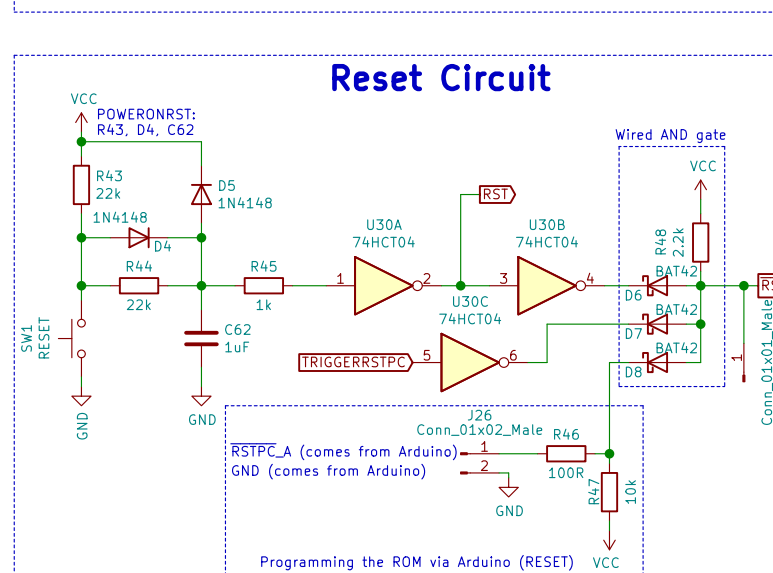
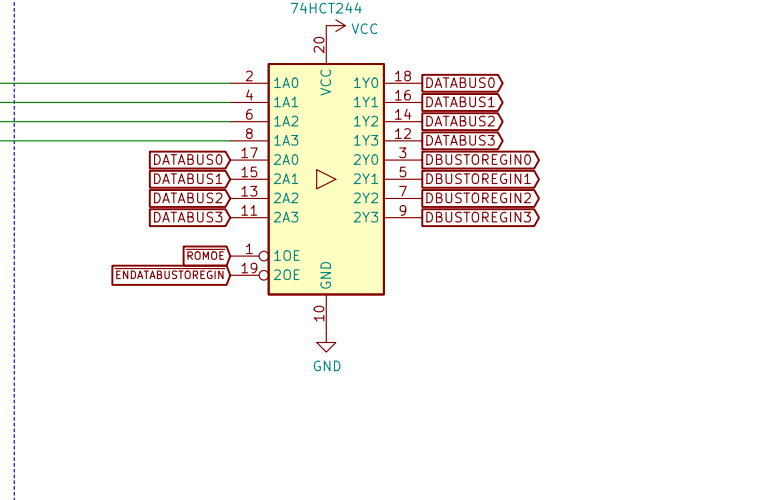


The Program memory is implemented with two RAM memories to facilitate programming. In this way, it is possible to use a manual programmer or an Arduino Mega 2560 board connected directly to MikroLeo.



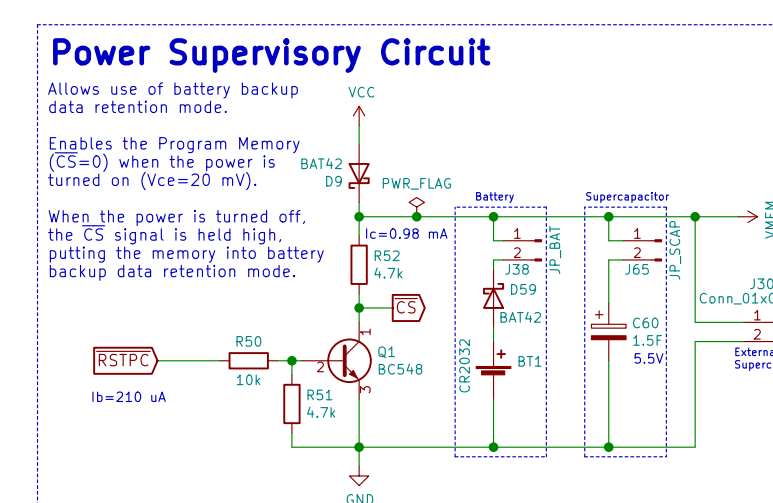
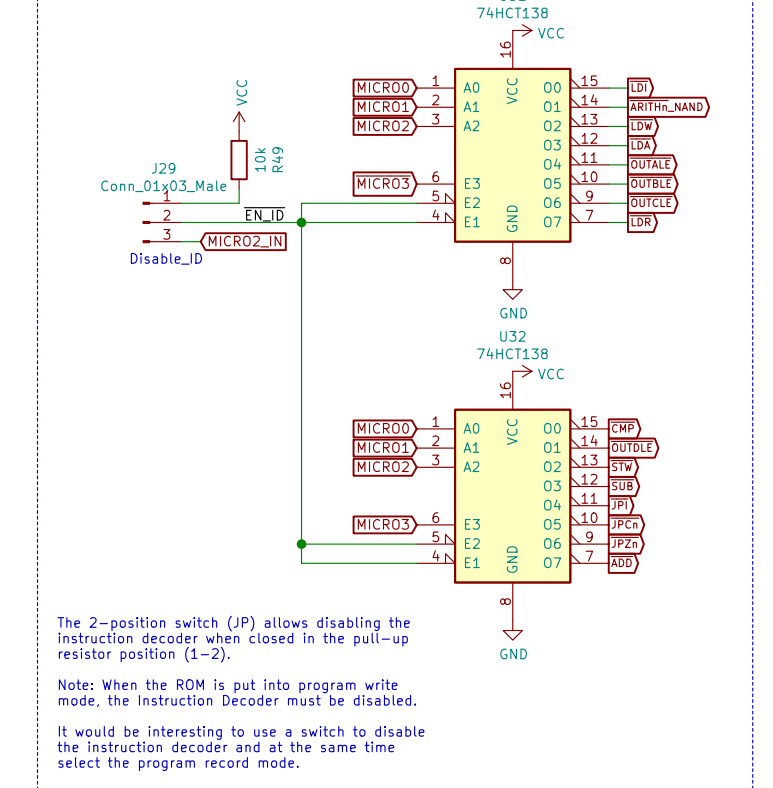
The PC (74161) is incremented in the transition from 0 to 1.  
The LD input works synchronously with the clock input.

**Buffer ROM to DataBus / DataBus to REGIN**



Note: when establishing the power supply, the RSTPC signal must briefly go low level to perform the reset. (POWERONRST)

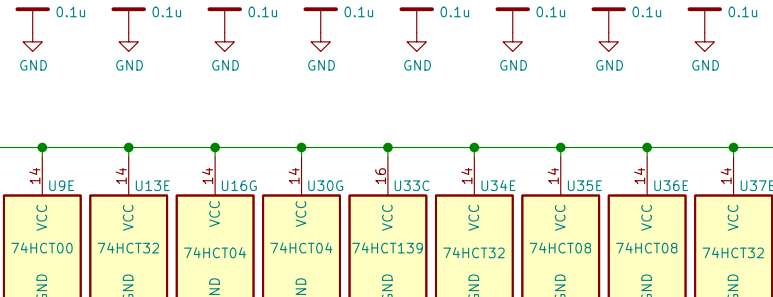
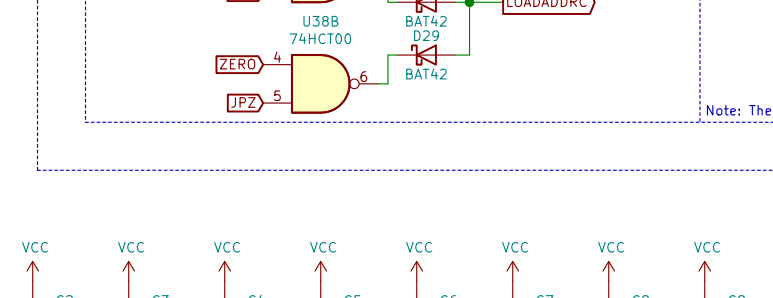
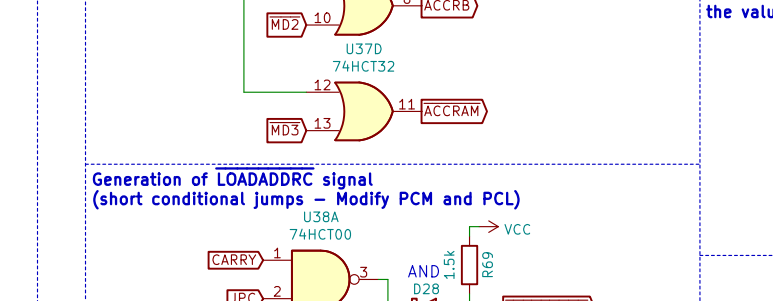
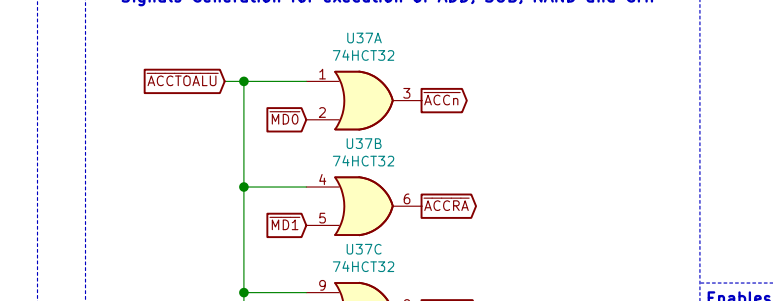
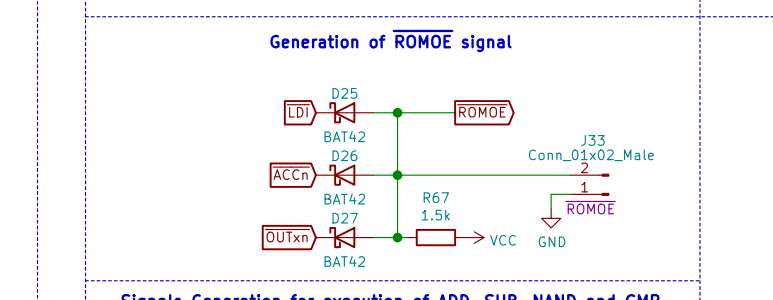
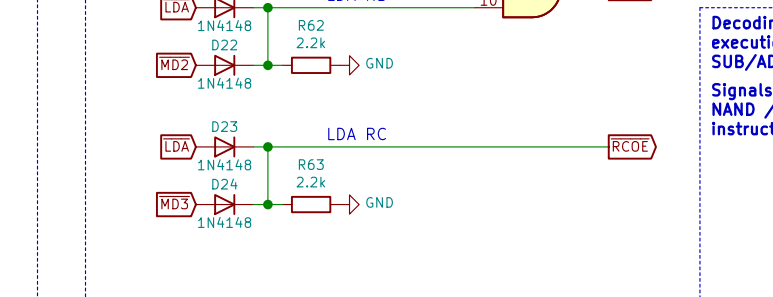
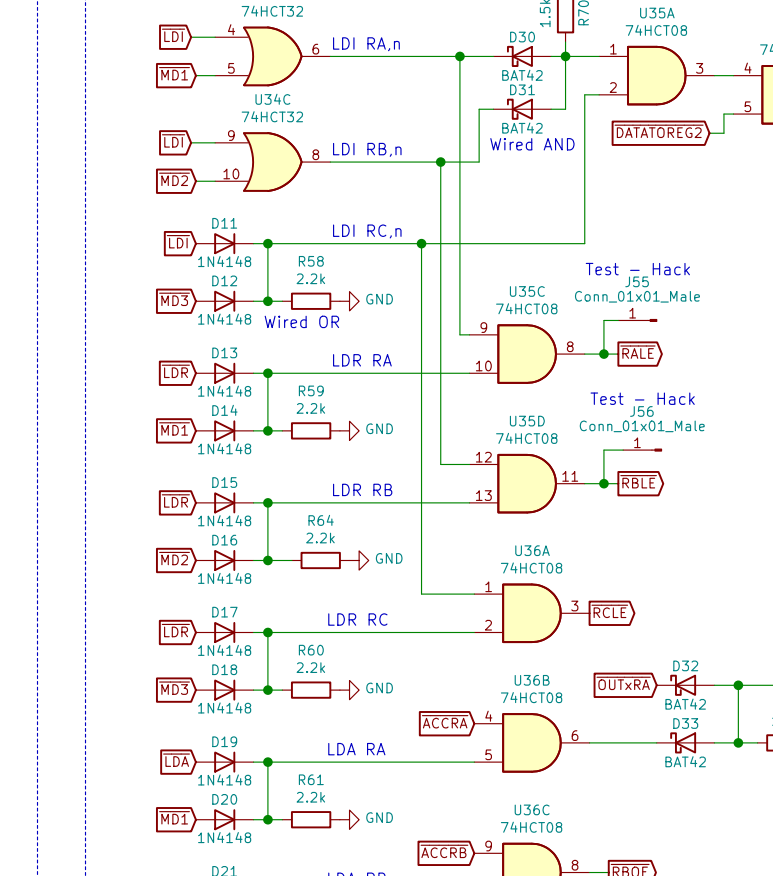
**Instruction Decoder (ID)**



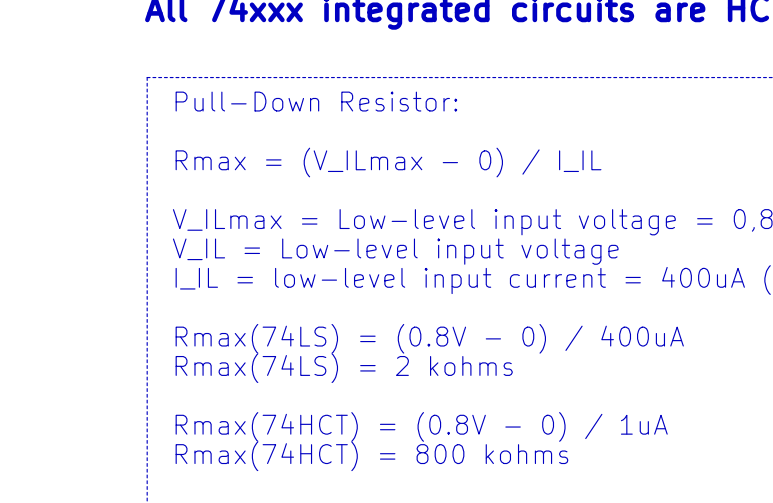
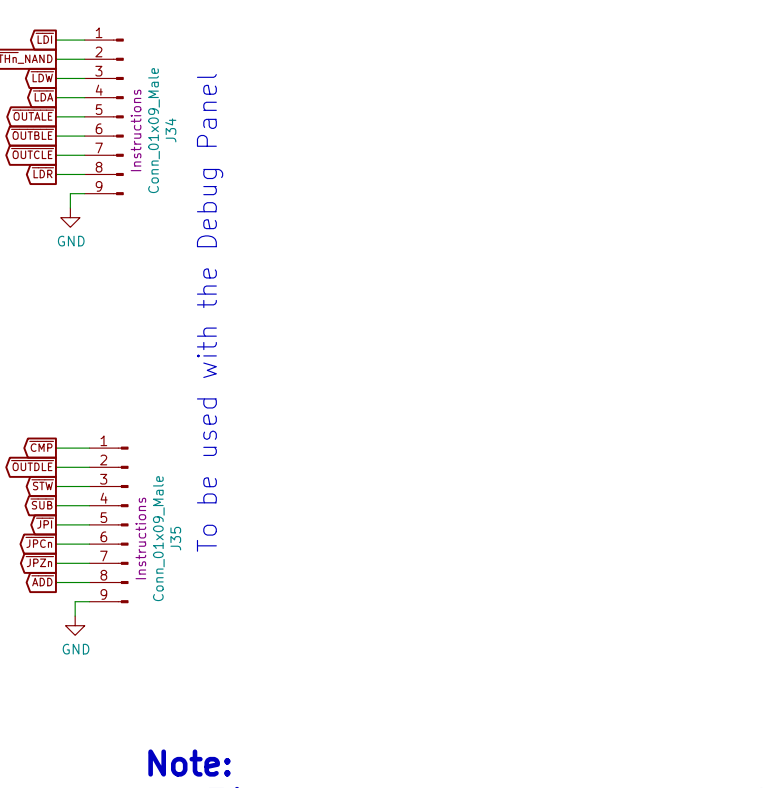
Note: 74xx integrated circuits are HCT

All 74xx integrated circuits are HCT

It generates the signals for the execution of the LDI, LDR and LDA

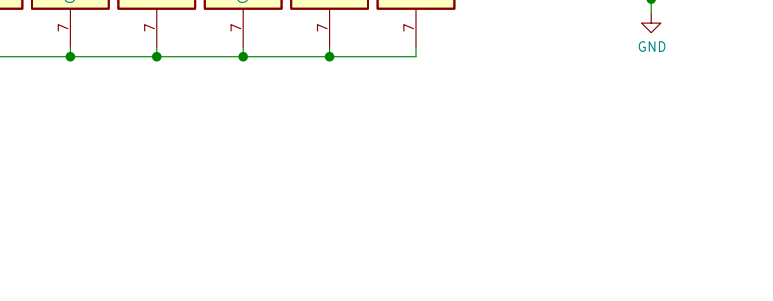
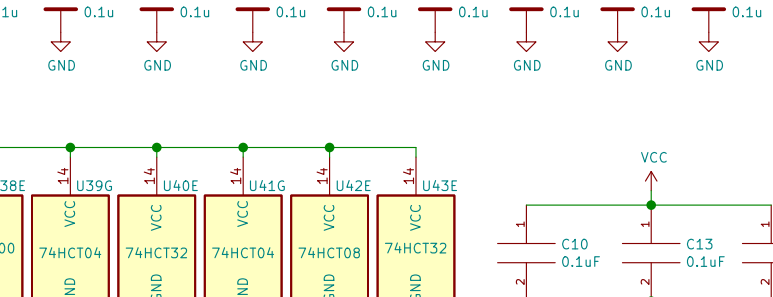
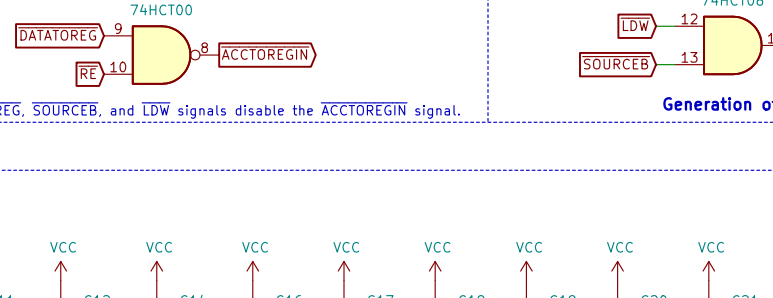
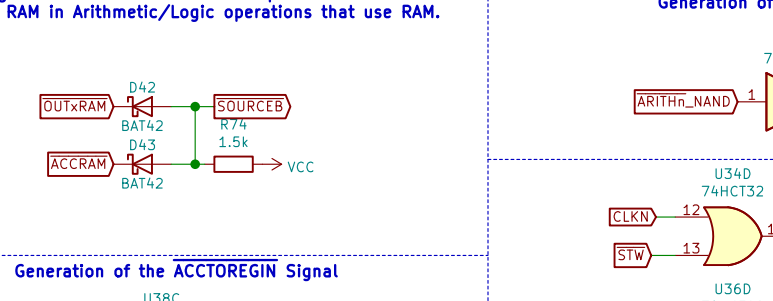
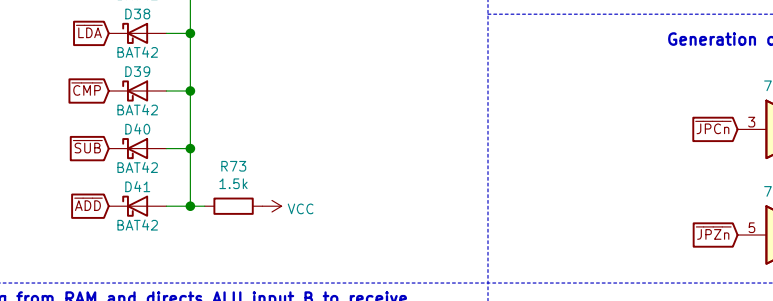
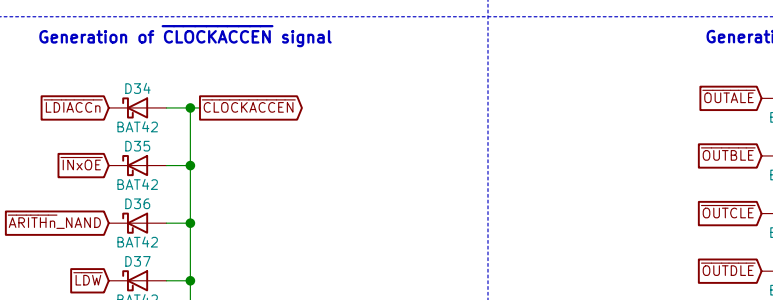
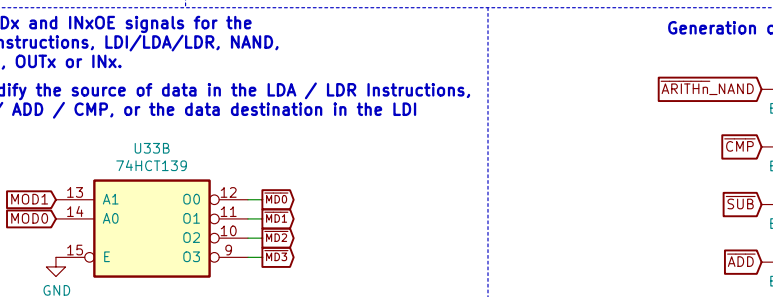
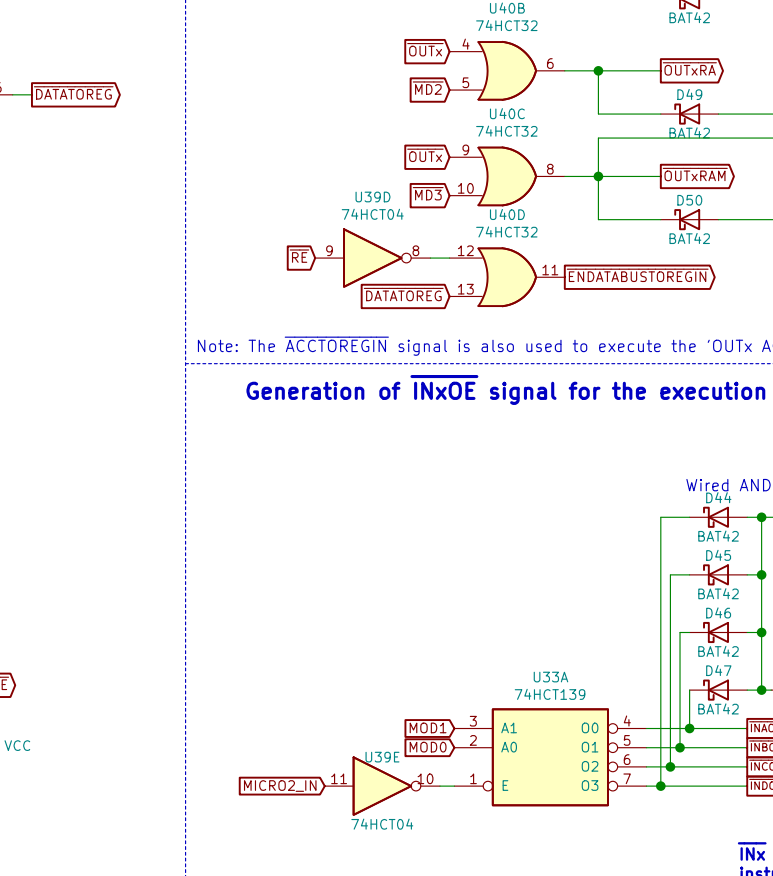


**Control Unit (UC)**



Note: The RDONE signal is also used to execute the OUTC instruction.

Generation of INDOE signal for the execution of INB, INC, and IND



It is initially assumed that the CLK clock signal is in logic 0 state. In this state, the code to be executed is read from program memory and all control signals are generated.

It is important that all control signals are generated before the clock pulse transition occurs.

In addition, it is important that all the data needed to execute the instruction is also available before the clock pulse occurs.

The program counter (PC) must be the last to be incremented. The PC (74161) is incremented on the falling edge of the clock signal. Therefore, the Clock signal used on the PC is CLKN. So, only after executing the first instruction the PC will be incremented.

CPU Phases:



Phase 1 (ph1): the word code (HINB, Opcode, MAddr and operand) is read from the program memory and the respective control signals are generated.

Phase 2 (ph2): On the rising edge of the CLK clock signal the instruction is executed.

Phase 3 (ph3): On the falling edge of the CLK clock signal the program counter is incremented.

CLKN => Fetch of Instruction/decode  
CLK => execute

For AND logic gates (with DRL Technology), it is better to use the BAT42/1N60P diode with a pull-up of 1.5k. Schottky diodes are best for AND logic gates (DRL) because they are low forward voltage.

For OR logic gates (with DRL Technology), it is better to use the 1N4148 diode with a pull-down of 2.2k. The 1N4148 has a reverse recovery time of around 4ns!

