MikroLeo Instruction Set

Encoding of MikroLeo Instruction Word (16-bits)						Instructions with all possibilities		Operation	Flags affected
ROMH (8-bit)				ROML (8-bit)					
High Nibble (HiNB)			Decoder Address	MAddr	Operand/ LAddr				
MICRO2_IN	AMODE	MOD	MICRO						
b15	b14	b13:12	b11:b8	b7:b4	b3:b0				
0	x	0	0	x	n	LDI	LDI ACC,n	ACC ← n	Carry, Zero
		1					LDI RA,n	RA ← n	-
		2					LDI RB,n	RB ← n	
		3					LDI RC,n	RC ← n	
	x	0	1	x	n	NAND	NAND ACC,n	ACC ← ACC NAND n	Carry, Zero
		1			x		NAND ACC,RA	ACC ← ACC NAND RA	
		2					NAND ACC,RB	ACC ← ACC NAND RB	
	0, 1	3		MAddr	LAddr		NAND ACC,RAM[Addr]	ACC ← ACC NAND RAM[RC:MA:LA]	
	0, 1	0	2	MAddr	LAddr	LDW	LDW ACC,RAM[Addr]	ACC ← RAM[RC:MA:LA]	Carry, Zero
	x	1	3	x	x	LDA	LDA RA	ACC ← RA	Carry, Zero
		2					LDA RB	ACC ← RB	
		3					LDA RC	ACC ← RC	
	x	0	4	x	n	OUTA	OUTA n	OUTA ← n	-
		1			x		OUTA ACC	OUTA ← ACC	
		2					OUTA RA	OUTA ← n	
	0, 1	3		MAddr	LAddr		OUTA RAM[Addr]	OUTA ← RAM[RC:MA:LA]	
	x	0	5	x	n	OUTB	OUTB n	OUTB ← n	-
		1			x		OUTB ACC	OUTB ← ACC	
		2					OUTB RA	OUTB ← n	
	0, 1	3		MAddr	LAddr		OUTB RAM[Addr]	OUTB ← RAM[RC:MA:LA]	
	x	0	6	x	n	OUTC	OUTC n	OUTC ← n	-
		1			x		OUTC ACC	OUTC ← ACC	
		2					OUTC RA	OUTC ← n	
	0, 1	3		MAddr	LAddr		OUTC RAM[Addr]	OUTC ← RAM[RC:MA:LA]	
	x	1	7	x	x	LDR	LDR RA	RA ← ACC	-
		2					LDR RB	RB ← ACC	
		3					LDR RC	RC ← ACC	
	x	0	8	x	n	CMP	CMP ACC,n	ACC - n	Carry, Zero
		1			x		CMP ACC,RA	ACC - RA	
		2					CMP ACC,RB	ACC - RB	
	0, 1	3		MAddr	LAddr		CMP ACC,RAM[Addr]	ACC - RAM[RC:MA:LA]	
	x	0	9	x	n	OUTD	OUTD n	OUTD ← n	-
		1			x		OUTD ACC	OUTD ← ACC	
		2					OUTD RA	OUTD ← n	
	0, 1	3		MAddr	LAddr		OUTD RAM[Addr]	OUTD ← RAM[RC:MA:LA]	
	0, 1	0	Ah	MAddr	LAddr	STW	STW RAM[Addr],ACC	RAM[RC:MA:LA] ← ACC	
	x	0	Bh	x	n	SUB	SUB ACC,n	ACC ← ACC - n	Carry, Zero
		1			x		SUB ACC,RA	ACC ← ACC - RA	
		2					SUB ACC,RB	ACC ← ACC - RB	
	0, 1	3		MAddr	LAddr		SUB ACC,RAM[Addr]	ACC ← ACC - RAM[RC:MA:LA]	
	0, 1	0	Ch	MAddr	LAddr	JPI	JPI RC:MA[7:4]:LA[3:0]	PC ← [RC:MA:LA]	-
	0, 1	0	Dh	MAddr	LAddr	JPC	JPC MA[7:4]:LA[3:0]	If CARRY=1, PC ← [MA:LA]	
	0, 1	0	Eh	MAddr	LAddr	JPZ	JPZ MA[7:4]:LA[3:0]	If ZERO=1, PC ← [MA:LA]	
	x	0	Fh	x	n	ADD	ADD ACC,n	ACC ← ACC + n	Carry, Zero
		1			x		ADD ACC,RA	ACC ← ACC + RA	
		2					ADD ACC,RB	ACC ← ACC + RB	
	0, 1	3		MAddr	LAddr		ADD ACC,RAM[Addr]	ACC ← ACC + RAM[RC:MA:LA]	
1	x	8	x			INA	INA	ACC ← INA	Carry, Zero
		9				INB	INB	ACC ← INB	
		A				INC	INC	ACC ← INC	
		B				IND	IND	ACC ← IND	

LA[3:0] => can be RA or OPR (LAddr), depends on the AMODE bit.
MA[7:4] => can be RB or MAddr, depends on the AMODE bit.
Address = Addr => RC:MA[7:4]:LA[3:0]
If AMODE=0, Addr=RC:Maddr:LAddr
If AMODE=1, Addr=RC:RB:RA
x = don't care

AMODE = Addresing mode
MOD = Modifier
MAddr = Mediam Address
LAddr = Low Address