
It allows the LD signal to be kept active for a longer time in the jump instructions so that the data containing the address can be loaded. After loading, the LOADADDRC or JPI signal (stored in D-type FF 7474) returns to "1". Data loading is synchronized with the clock signal.
Note: 7474 must be started with Q=1.
Timing for Jump Control
Conditional jump (short, JPC and JPZ): Modify only PCM and PCL
PC <= MA[7:4]:LA[3:0]
PCH = PCH (is not modified)
(Jumps only to addresses in the current memory page)
Unconditional jump (long, JPI):
PC = RC:MA[7:4]:LA[3:0]
PCH <= RC
(all memory addresses)
Power Input (+VCC and GND)
Freq. Enable
Program Counter (PC)
PCL
PCM
PCH
Program Memory (ROM) - 2k x 16 or 4k x 16
ROML
ROMH
The PC (74161) is incremented in the transition from 0 to 1.
The LD input works synchronously with the clock input.
Buffer ROM to DataBus / DataBus to REGIN
Reset Circuit
Instruction Decoder (ID)
Power Supervisory Circuit
Note:
All 74xxx integrated circuits are HCT
Pull-Down Resistor:
Rmax = (V_ILmax - 0) / I_IL
V_ILmax = Low-level input voltage = 0,8 V
V_IL = Low-level input voltage
I_IL = low-level input current = 400uA (for 74LS), 1uA (for 74HCT)
Rmax(74LS) = (0.8V - 0) / 400uA
Rmax(74LS) = 2 kohms
Rmax(74HCT) = (0.8V - 0) / 1uA
Rmax(74HCT) = 800 kohms
It is initially assumed that the CLK clock signal is in logic 0 state.
In this state, the code to be executed is read from program memory and all control signals are generated.
It is important that all control signals are generated before the clock pulse transition occurs.
In addition, it is important that all the data needed to execute the instruction is also available before the clock pulse occurs.
The program counter (PC) must be the last to be incremented.
The PC (74161) is incremented on the falling edge of the clock signal.
Therefore, the Clock signal used on the PC is CLKN.
So, only after executing the first instruction the PC will be incremented.
CPU Phases:
CLK
ph1 ph2 ph3
Phase 1 (ph1): the word code (HiNB, Opcode, MAddr and operand) is read from the program memory and the respective control signals are generated.
Phase 2 (ph2): On the rising edge of the CLK clock signal the instruction is executed.
Phase 3 (ph3): On the falling edge of the CLK clock signal the program counter is incremented.
CLKN => Fetch of Instruction/decode
CLK => execute
For AND logic gates (with DRL Technology), it is better to use the BAT42/1N60P diode with a pull-up of 1.5k.
Schottky diodes are best for AND logic gates (DRL) because they are low forward voltage.
For OR logic gates (with DRL Technology), it is better to use the 1N4148 diode with a pull-down of 2.2k.
The 1N4148 has a reverse recovery time of around 4ns!
Arithmetic and Logic Unit (ALU)
Detector of ZERO
Complement of B Input
ADDER
MUX
ACC
BUFFER
FLAGS Register
Addressing Modes
Control Unit (UC)
It generates the signals for the execution of the LDI, LDR and LDA
Generation of signals for execution of instructions OUTA, OUTB, OUTC e OUTD
Clock Control Circuit
Clock Generator
OUTD
OUTC
OUTB
OUTA
RA
RB
RC
Input Ports
Register Buffer
Debug LED
RAM 2k X 4
RAM memory
Decoupling Capacitors (ceramic)
MikroLeo v0.1901 | 2020-2022
https://github.com/edson-acordi/4bit-microcomputer
Visit the project repository and support this project!
Schematic drawing in Kicad: Matheus Fernando Tasso and Carlos Daniel de Souza Nunes
Design: Edson Junior Acordi / Licensed under CERN-OHL-S v2 or any later version
Sheet: /
File: MikroLeo_v0.1901_Rev1.01A.sch
Title: MikroLeo: 4-bit Didactic Microcomputer
Size: A0
Date: 2021-04-16
Rev: R1.01A
KiCad E.D.A. kicad (5.1.9)-1
Id: 1/1