Instruction Code (14-bits)				Instructions with all possibilities	
Micro2 (ROMH)		Micro1 (ROML)			
Decoder Address		MAddr	Operand/ LAddr		
MOD	Opcode				

0
1
2
3
	0	-	n	LDI	LDI ACC,n ok
					LDI RA,n ok
					LDI RB,n
					LDI RD,n

0 1 2 3	1	- MAddr	n LAddr	NAND	NAND ACC,n ok NAND ACC,RA ok NAND ACC,RB NAND ACC,RAM[Addr] ok
0	2	MAddr	LAddr	LDW	LDW ACC,RAM[Addr] ok
1 2 3	3	-	-	LDA	LDA RA ok LDA RB LDA RD
0 1 2 3	4	- MAddr	n - LAddr	OUTA	OUTA n ok OUTA ACC ok OUTA RA ok OUTA RAM[Addr] ok
0 1 2 3	5	- MAddr	n - LAddr	OUTB	OUTB n OUTB ACC OUTB RA OUTB RAM[Addr]
0 1 2 3	6	- MAddr	n - LAddr	OUTC	OUTC n OUTC ACC OUTC RA OUTC RAM[Addr]
1 2 3	7	-	-	LDR	LDR RA ok LDR RB LDR RD

0
1
2
3
	8	-
		
		MAddr
			n
			
			-
			LAddr
				CMP	CMP ACC,n ok
					CMP ACC,RA ok
					CMP ACC,RB
					CMP ACC,RAM[Addr]

0 1 2 3	9	- MAddr	n - LAddr	OUTD	OUTD n OUTD ACC OUTD RA OUTD RAM[Addr]
0	Ah	MAddr	LAddr	STW	STW RAM[Addr],ACC ok
0 1 2 3	Bh	- MAddr	n - LAddr	SUB	SUB ACC,n ok SUB ACC,RA ok SUB ACC,RB SUB ACC,RAM[Addr] ok
0	Ch	MAddr	LAddr	JPI	JPI RD:MA[7:4]:LA[3:0] ok
0	Dh	MAddr	LAddr	JPC	JPC MA[7:4]:LA[3:0] ok
0	Eh	MAddr	LAddr	JPZ	JPZ MA[7:4]:LA[3:0] ok

0
1
2
3
	Fh	-
		
		MAddr
			n
			
			-
			LAddr
				ADD	ADD ACC,n ok
					ADD ACC,RA ok
					ADD ACC,RB
					ADD ACC,RAM[Addr]

8 9 A B	MICRO2/IN = 1			INA INB INC IND	INA INB INC IND

LA[3:0] => can be RA or OPR (LAddr), depends on the AMODE bit.
MA[7:4] = can be RB or MAddr, depends on the AMODE bit.