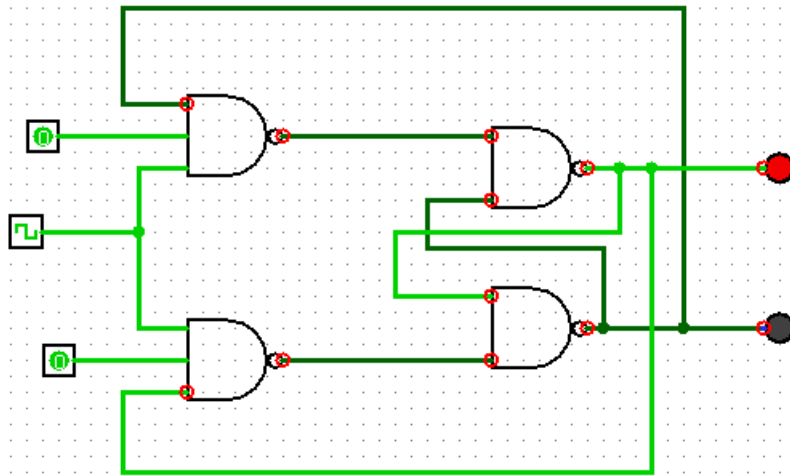
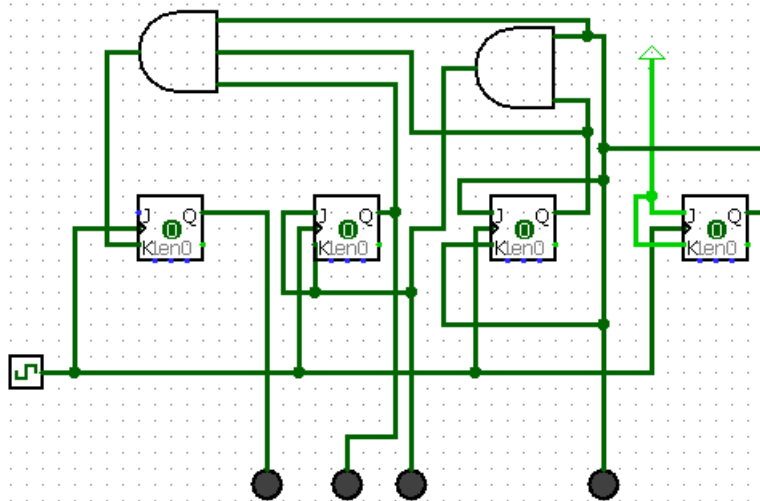


DISEÑO DE FLIP FLOP JK CON COMPUERTAS LÓGICAS



DISEÑO DE CONTADOR SINCRONO DE 4 BITS CON FLIP FLOPS JK

The diagram illustrates a 4-bit synchronous counter implemented with four JK flip-flops. A common square-wave clock signal is connected to the clock input of every flip-flop. The output of the first flip-flop (Q0) is connected to the J input of the second flip-flop and the K input of the first flip-flop. The output of the second flip-flop (Q1) is connected to the J input of the third flip-flop and the K input of the second flip-flop. The output of the third flip-flop (Q2) is connected to the J input of the fourth flip-flop and the K input of the third flip-flop. The output of the fourth flip-flop (Q3) is connected to the J input of the first flip-flop and the K input of the fourth flip-flop. The outputs Q0, Q1, Q2, and Q3 are shown as digital signals at the bottom of the diagram.



Contador síncrono de décadas up/down

