IC Design Lab

HW 2 Verilog Testbench

- Due on 03/03/2022, 23:59, 10% penalty for each day of delay
- If you have any questions, please contact r10943003@ntu.edu.tw , and specify [ICDLab] before your title

I. Objectives

In this homework, you will practice verifying a design by using a testbench.

II. Design Files

Copy files from your HW1：

1. HW1_alu.v

III. Specifications

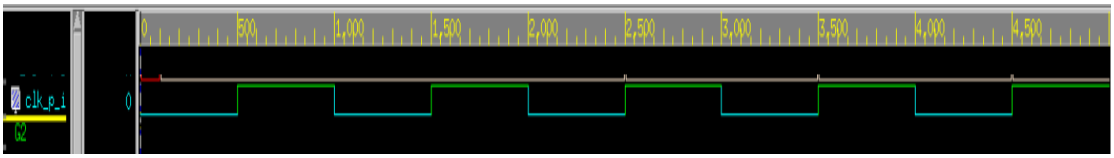
In this homework, Please write a testbench for this design and generate waveforms in the following table:

Time	reset_n_i	data_a_i	data_b_i	inst_i	data_o
0	1'b1	8'd0	8'd0	3'b0	x
1	1'b0	8'd0	8'd0	3'b0	16'd0
6	1'b1	8'd0	8'd0	3'b0	16'd0
10	1'b1	8'd25	8'd35	3'b011	16'd0
20	1'b1	8'd37	8'd128	3'b100	16'd0
25	1'b1	8'd37	8'd128	3'b100	16'd12
30	1'b1	8'd50	8'd60	3'b110	16'd12
35	1'b1	8'd50	8'd60	3'b110	16'd18
40	1'b1	8'd65	8'd100	3'b110	16'd18
45	1'b1	8'd65	8'd100	3'b111	16'd10
50 finish					

Time unit: ns

At t=0, clk_p_i=0. Clock period: 10ns

Clock waveform:



After successfully generating the waveforms, use print screen to capture these waveforms and put the figures in your report. Write some explanations of the waveform.

Attention

1. Plagiarism is not allowed.
2. Design file: HW2_alu_tb.v
3. In your testbench, please follow the port name and port order as used in the given ALU RTL code. Otherwise your design may fail our test for grading.

IV. Grading

1. HW2_alu_tb.v using Verilog (80%)
2. Report (StudentID.pdf)
   - 2.1 nWave output result (15%) : Show every part of required waveform.
   - 2.2 Discussion (5%) : Discuss about your design. For example, introduce how you wrote the testbench.

VI. Notification

1. You should compress your design files into a single ZIP file, and then upload your ZIP file to ceiba before 2022/03/03 23:59
   - 1.1 Files should be compressed as follows:

     ICDLAB_HW2_ StudentID.zip
     - ICDLAB_HW2_StudentID
       - HW2_alu_tb.v
       - StudentID_HW2.pdf

     Examples:

     ICDLAB_HW2_r10943003.zip
     - ICDLAB_HW2_r10943003
       - HW2_alu_tb.v
       - r10943003_HW2.pdf