



### IC Design Lab1 NC-Verilog

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#### **Outline**

- Connect to workstations
  - MobaXterm
- Lab1 NC-Verilog
  - ALU
- Reminder





#### Connect to Workstations

MobaXterm

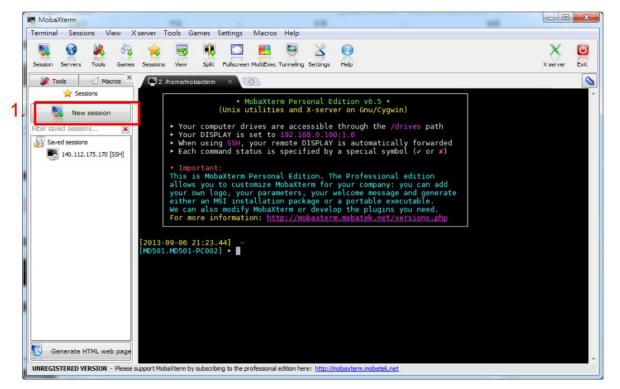


#### MobaXterm

Download the install program of MobaXterm

Download: http://mobaxterm.mobatek.net/

Workstation list: http://cad.ee.ntu.edu.tw/ws\_list.htm





## Log-In(1/2)

SSH T	elnet	Rsh	Xdmcp	RDP	VNC	FTP	SFTP	Serial	File/Url	Sh
Basic SSH	settings	IP:	140.1	12.2	0.XX	(			ро	rt:
Remote ho	st * 140	0.112.20	.70		Specify use	ername	1		Port 22	G
X11-Forw	mand		npression			ot exit after	command e			
	mand TP brows te key	ser	Automatio			ot exit after folder path	command e		<u>}-</u> G	
Execute com  Display Sf  Use priva  Enable Go	mand TP brows te key	ser ep auther	Automation		Do no current SSH Extra	ot exit after folder path	command e	ntal)	<u>}-</u> G	
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Host list: http://cad.ee.ntu.edu.tw/htdocs\_new/ws\_list.htm

Source list: http://cad.ee.ntu.edu.tw/htdocs\_new/software.htm



# Log-In(2/2)

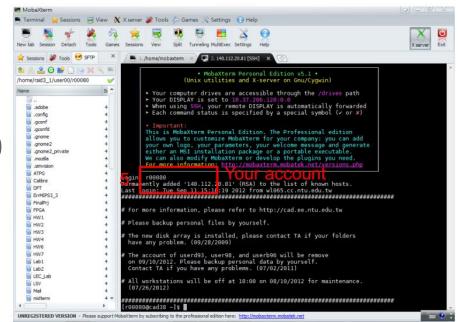
#### User Name

- Ex: <u>r98</u>943<u>032</u> -> r98032

<u>b97</u>901<u>020</u> -> b97020

- Ex: b96502040 -> b6502040

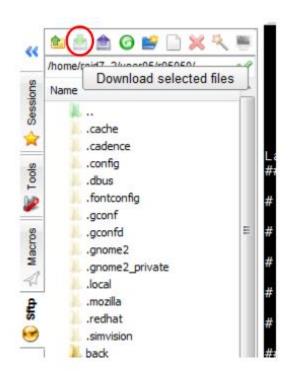
Password

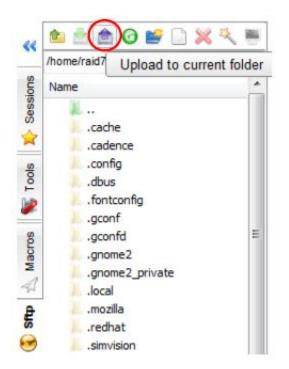


or enter "ssh r02XXX@140.112.20.72" to connect



### Download and upload files







## Simple Linux command

- Source the setting file
  - source
  - Change your password
    - passwd
  - Document management
    - cd [directory name/..]
    - ls [-a/-l]
    - mkdir [directory name]
    - cp [options] [source] [destination]
    - rm [-fir] [file/directory]
    - mv [-fiu] [source] [destination]
  - View Ref[1] for more detail!





### Lab1 NC-Verilog

**ALU** 



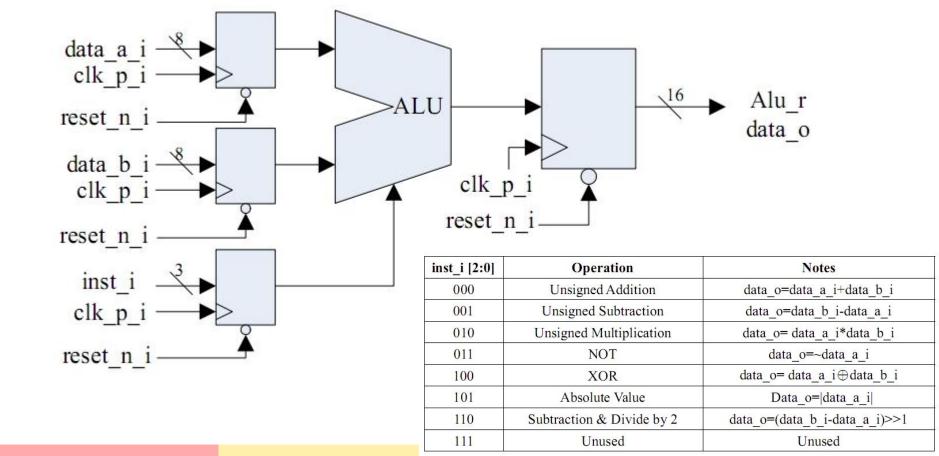
### Objectives

- In this lab, you will learn
  - How to verify your Verilog HDL
  - How to run the NC-Verilog simulator with test-bench
- Copy files from course web
  - Lab1.zip
- Check if you have these files
  - Lab1\_alu.v
  - Lab1\_alu\_tb.v



#### Case: An 8-bit ALU

Posedge clk\_p\_i, negedge reset\_n\_i





### Check Verilog Code via NC-Verilog



- Source the cshrc file (both work)
  - source /usr/cadence/cshrc
  - source /usr/cad/cadence/cshrc
- Check Verilog Code via NC-Verilog
  - ncverilog Lab1\_alu.v
  - NC-Verilog will report your RTL code
  - Ensure that no errors here
- Run simulation with a test bench via NC-Verilog
  - ncverilog +access+r Lab1\_alu\_tb.v Lab1\_alu.v
  - Check the simulation result be no errors now



#### nWave: Source file and execute

- Source
  - source /usr/spring\_soft/CIC/verdi.cshrc
- Execute nWave
  - nWave &



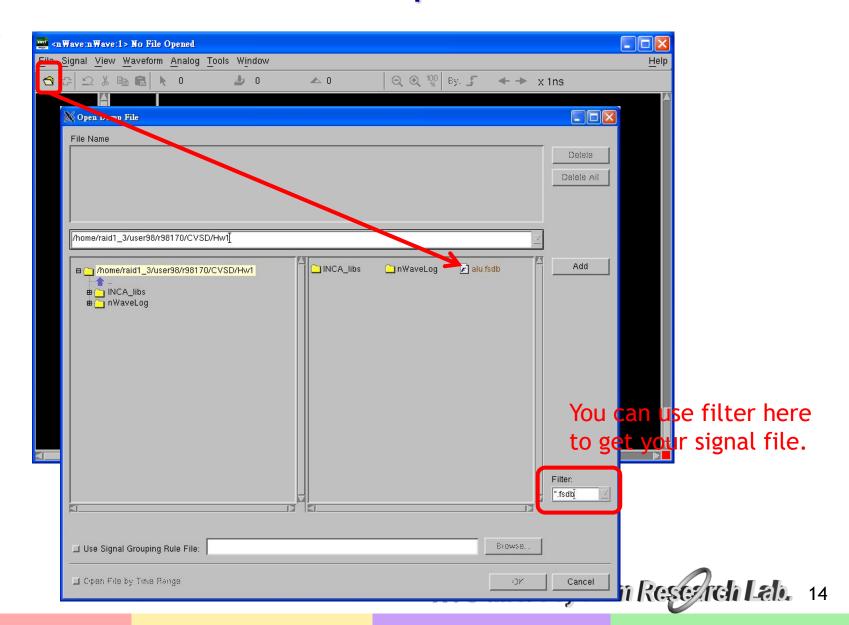
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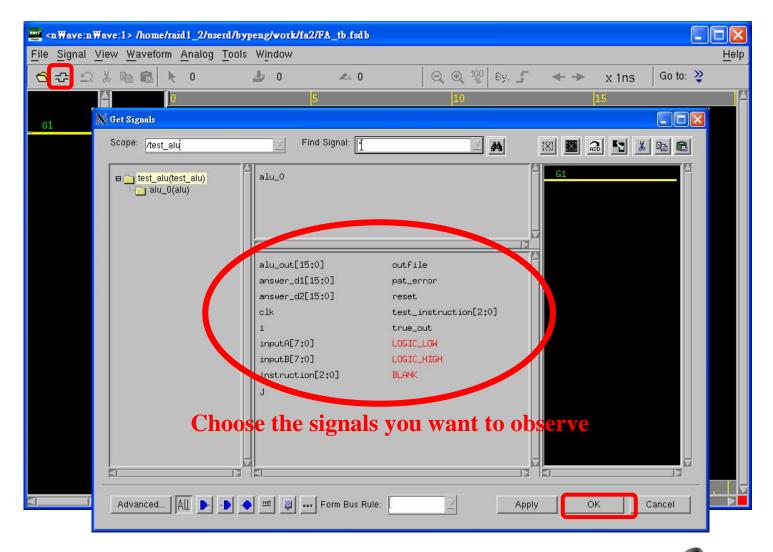


#### Select output file



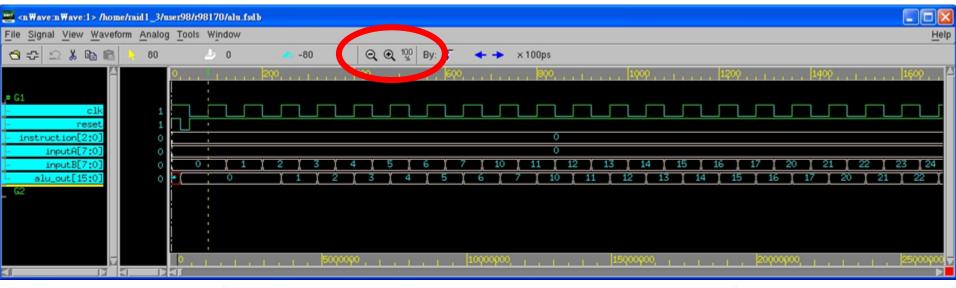


### Select desired signals





### Check your output waveform



inst_i [2:0]	Operation	Notes		
000	Unsigned Addition	data_o=data_a_i+data_b_i		
001	Unsigned Subtraction	data_o=data_b_i-data_a_i		
010	Unsigned Multiplication	data_o= data_a_i*data_b_i		
011	NOT	data_o=~data_a_i		
100	XOR	data_o= data_a_i⊕data_b_i		
101	Absolute Value	Data_o= data_a_i		
110	Subtraction & Divide by 2	data_o=(data_b_i-data_a_i)>>1		
111	Unused	Unused		



#### **Practice**

- Follow the steps to check the Lab1\_alu.v yourself
- Use the nWave to see the output result



#### Reminder

Be patient and careful about each step!

- References
  - [1] "鳥哥的Linux 私房菜" http://linux.vbird.org/
- If you have any questions, please contact...
  - R09943018@ntu.edu.tw
  - Specify [ICDLab] before your title