IC Design Lab1 NC-Verilog

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Derived from slides by Lu-Kuo Chang

Outline

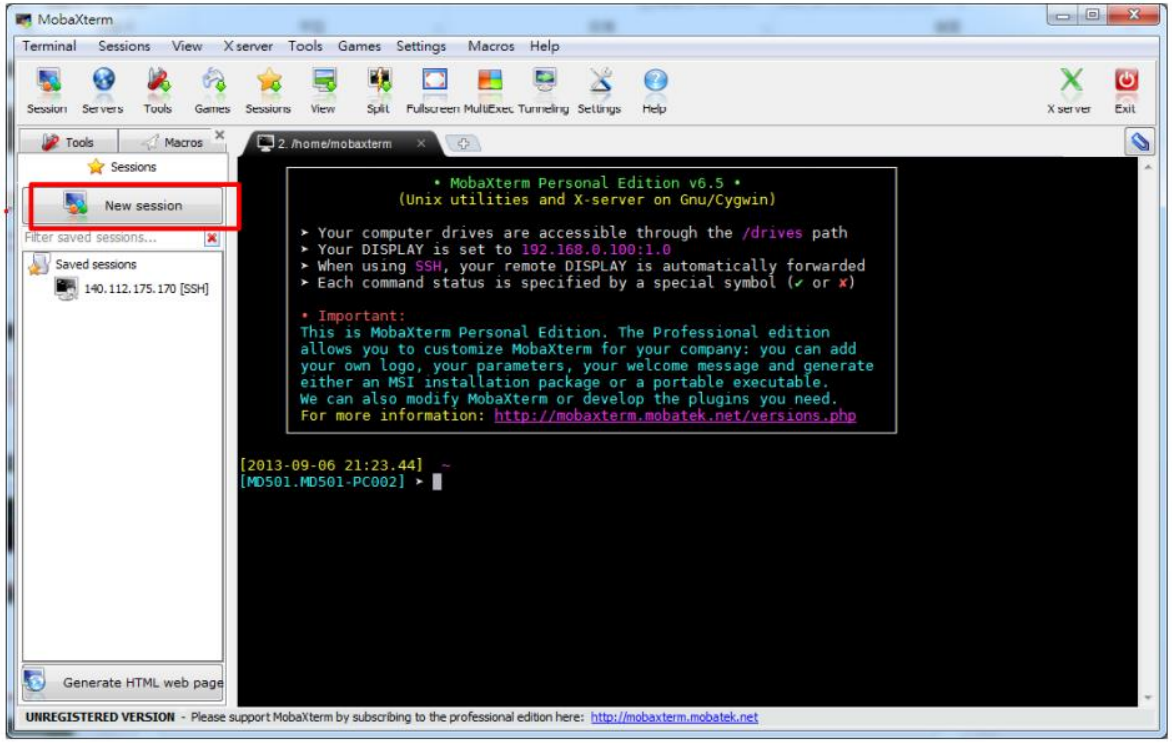
- Connect to workstations
  - MobaXterm
- Lab1 NC-Verilog
  - ALU
- Reminder

Connect to Workstations

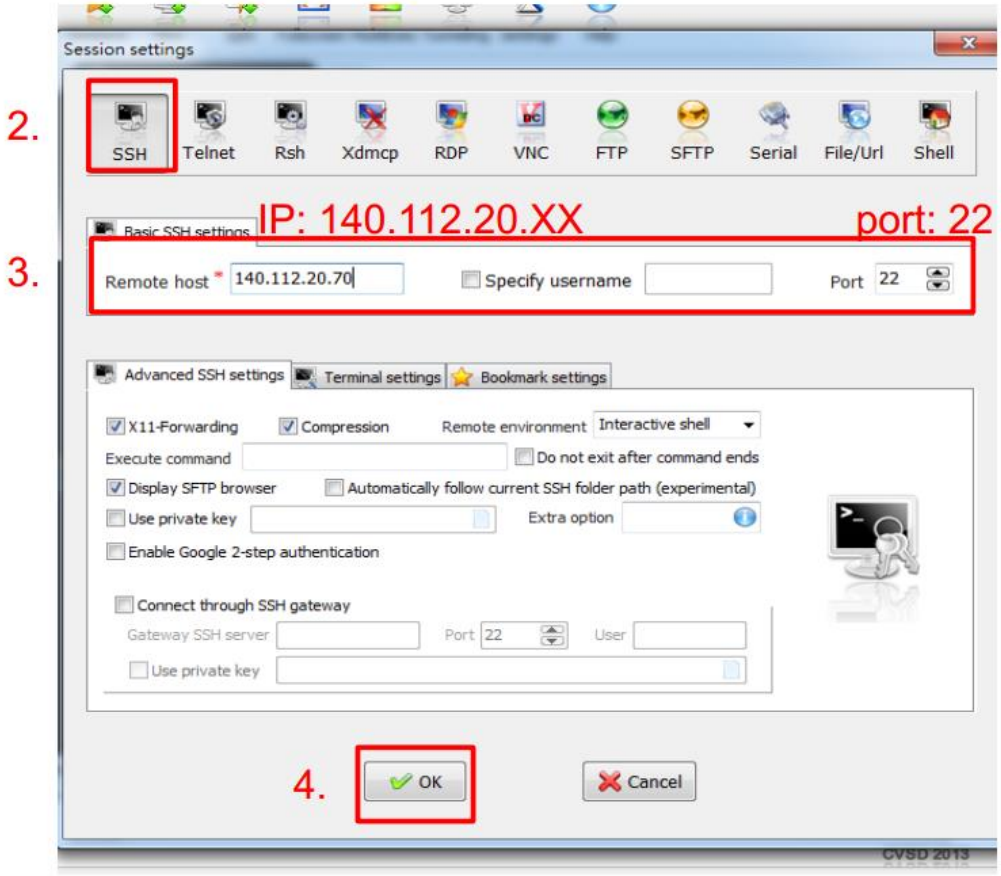
MobaXterm

MobaXterm

- Download the install program of MobaXterm
  - Download: *http://mobaxterm.mobatek.net/*
  - Workstation list: *http://cad.ee.ntu.edu.tw/ws_list.htm*



Log-In(1/2)

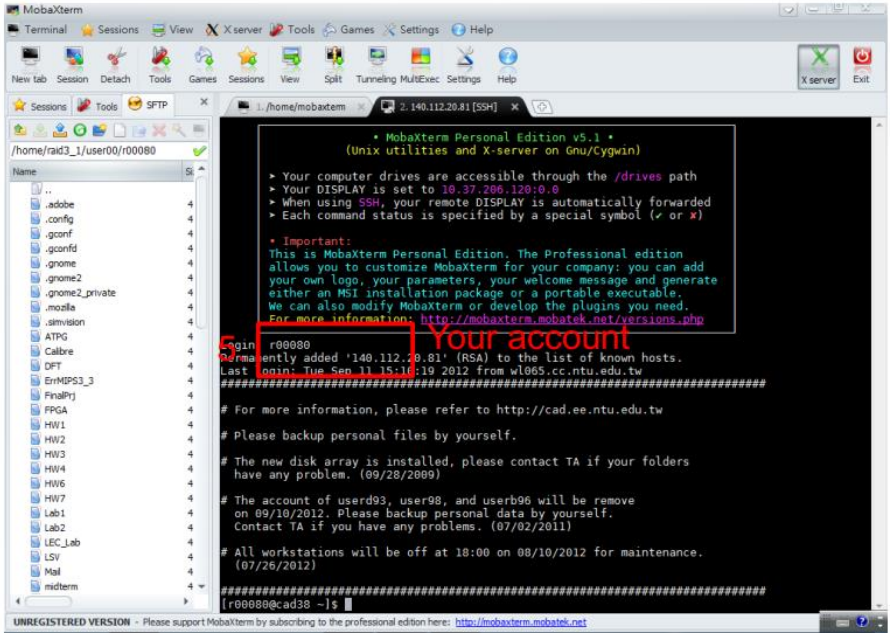


Host list: http://cad.ee.ntu.edu.tw/htdocs_new/ws_list.htm

Source list: http://cad.ee.ntu.edu.tw/htdocs_new/software.htm

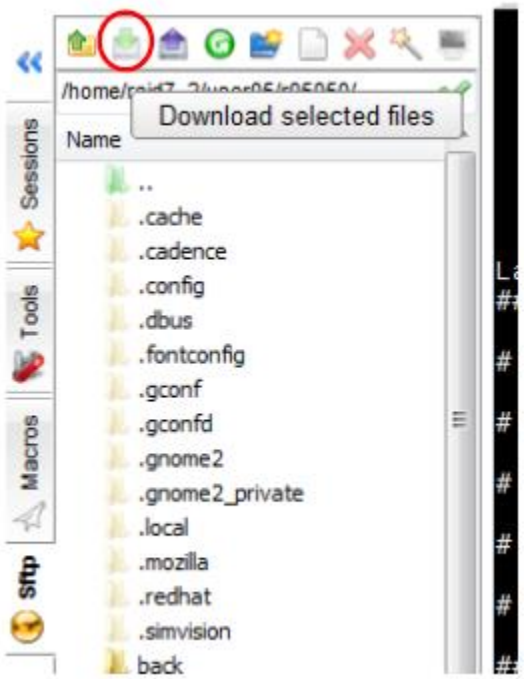
Log-In(2/2)

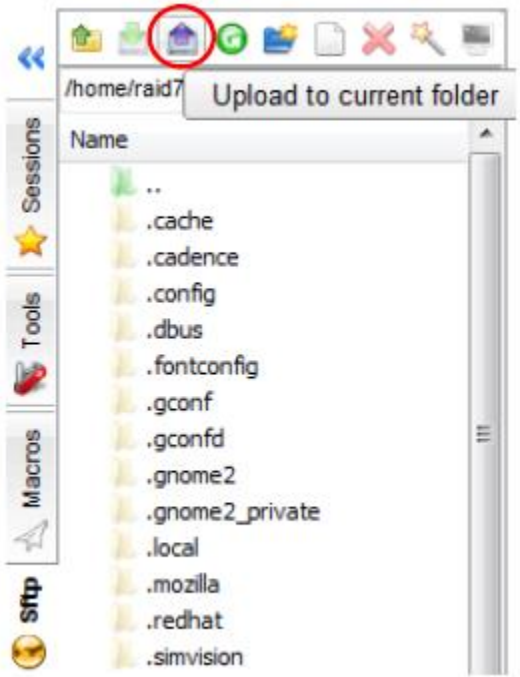
- User Name
  - Ex: r98943032 -> r98032
    b97901020 -> b97020
  - Ex: b96502040 -> b6502040
- Password



- or enter “ ssh r02XXX@140.112.20.72 ” to connect

Download and upload files





Simple Linux command

- Source the setting file
  - source
- Change your password
  - passwd
- Document management
  - cd [directory name/..]
  - ls [-a/-l]
  - mkdir [directory name]
  - cp [options] [source] [destination]
  - rm [-fir] [file/directory]
  - mv [-fiu] [source] [destination]
- View Ref[1] for more detail!

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Lab1 NC-Verilog

ALU

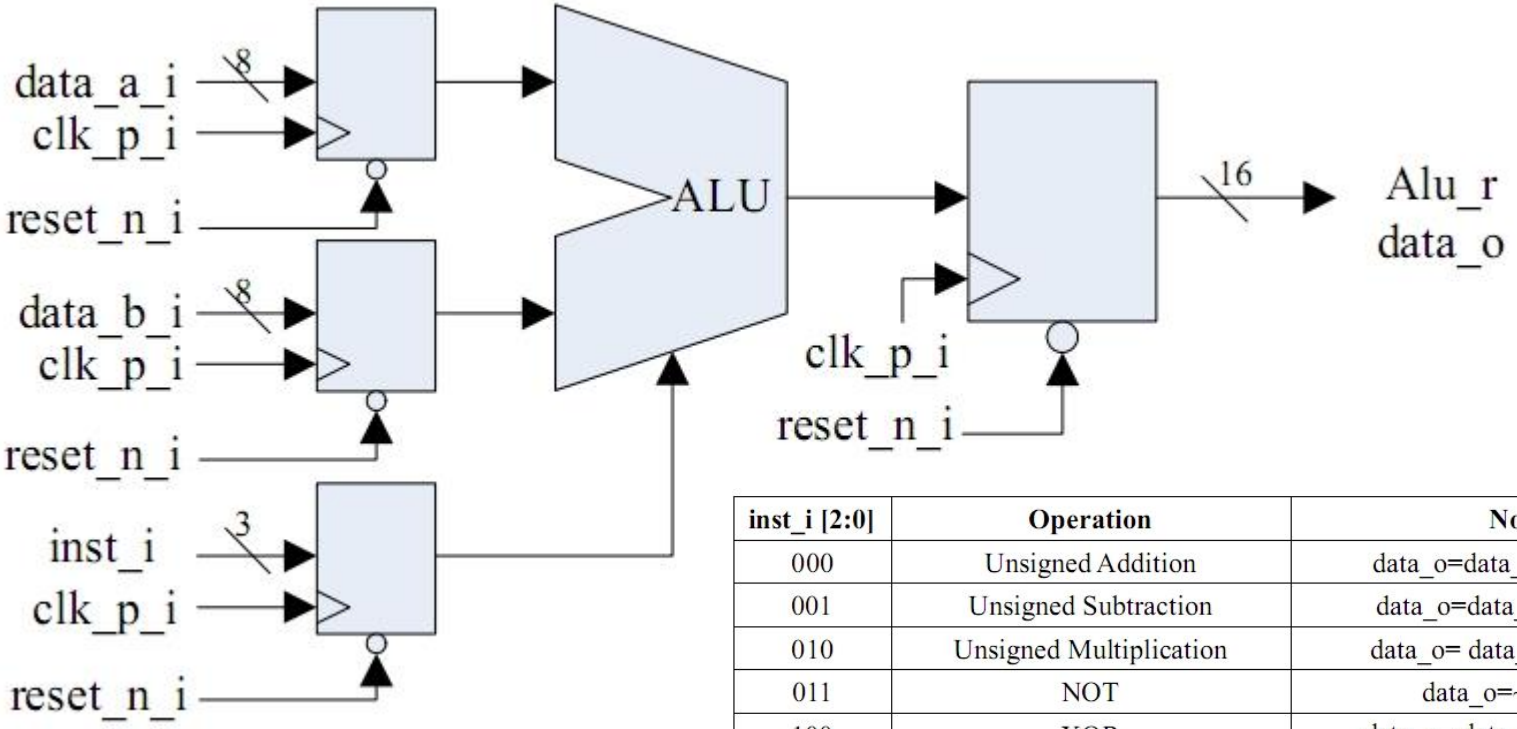
NTU MicroSystem Research Lab.

Objectives

- In this lab, you will learn
  - How to verify your Verilog HDL
  - How to run the NC-Verilog simulator with test-bench
- Copy files from course web
  - Lab1.zip
- Check if you have these files
  - Lab1_alu.v
  - Lab1_alu_tb.v

Case : An 8-bit ALU

- Posedge clk_p_i, negedge reset_n_i



inst_i [2:0]	Operation	Notes
000	Unsigned Addition	data_o=data_a_i+data_b_i
001	Unsigned Subtraction	data_o=data_b_i-data_a_i
010	Unsigned Multiplication	data_o= data_a_i*data_b_i
011	NOT	data_o=~data_a_i
100	XOR	data_o= data_a_i⊕data_b_i
101	Absolute Value	Data_o=|data_a_i|
110	Subtraction & Divide by 2	data_o=(data_b_i-data_a_i)>>1
111	Unused	Unused

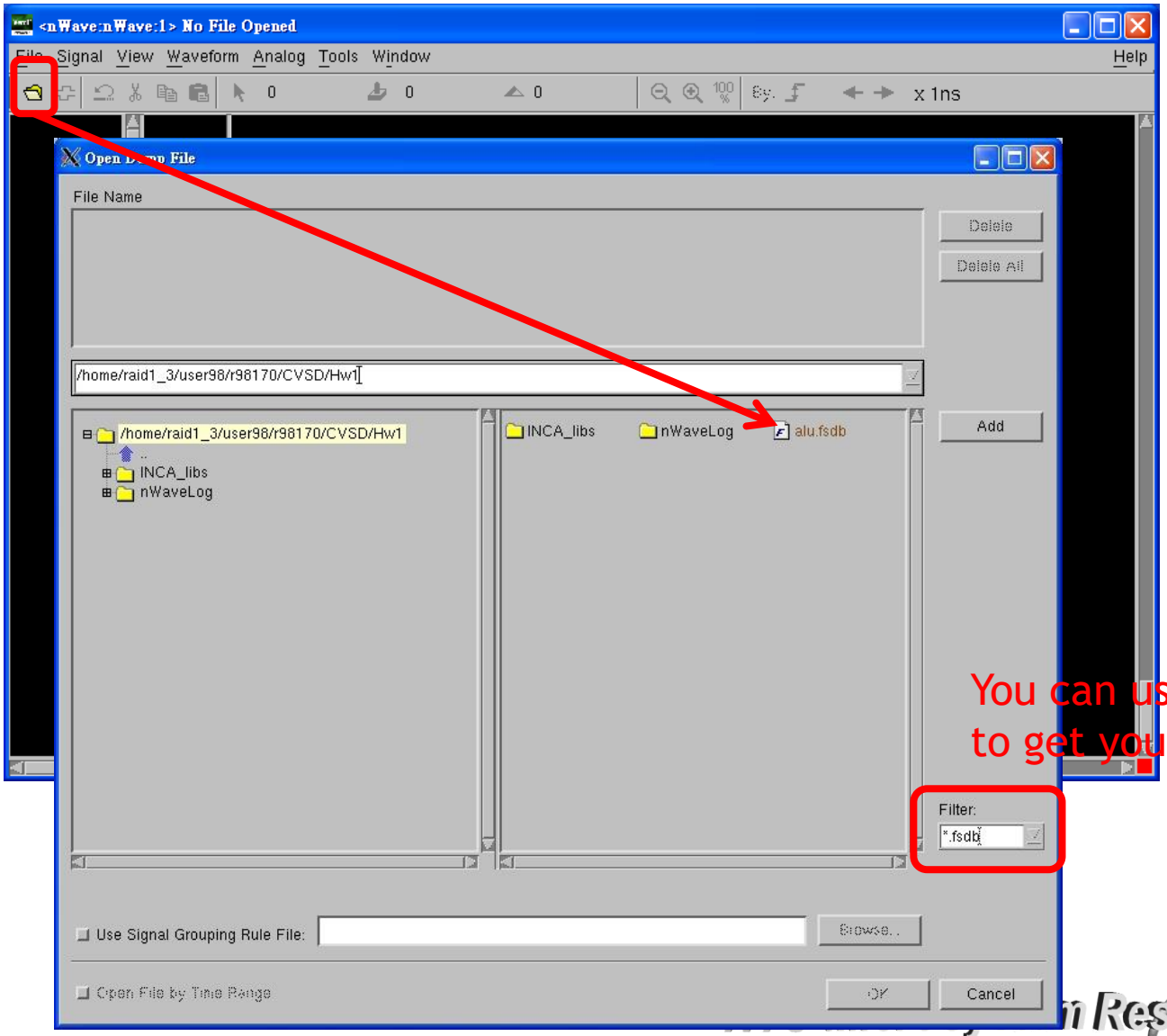
Check Verilog Code via NC-Verilog

- Source the cshrc file (both work)
  - source /usr/cadence/cshrc
  - source /usr/cad/cadence/cshrc
- Check Verilog Code via NC-Verilog
  - ncverilog Lab1_alu.v
  - NC-Verilog will report your RTL code
  - Ensure that no errors here
- Run simulation with a test bench via NC-Verilog
  - ncverilog +access+r Lab1_alu_tb.v Lab1_alu.v
  - Check the simulation result be no errors now

nWave: Source file and execute

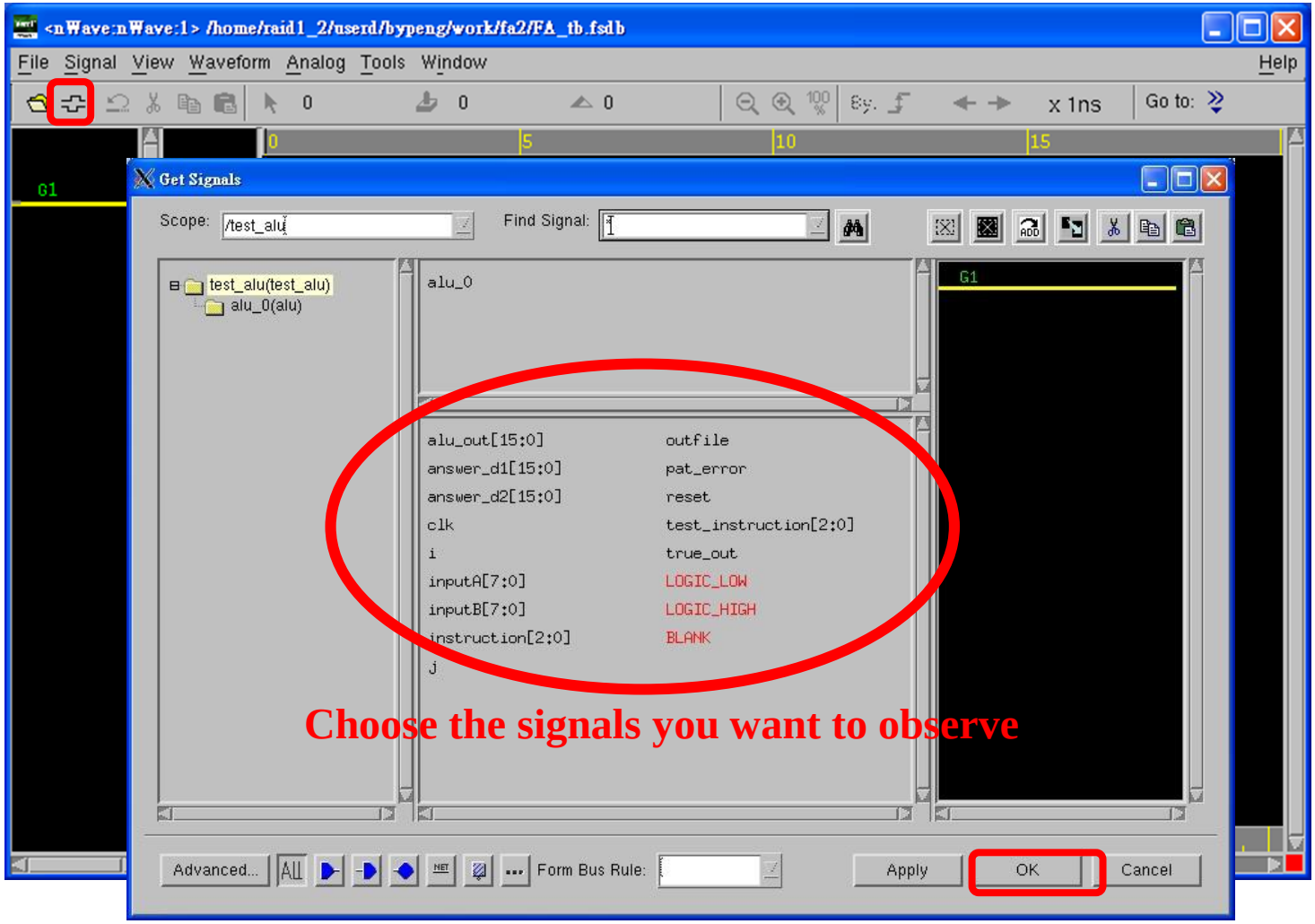
- Source
  - source /usr/spring_soft/CIC/verdi.cshrc
- Execute nWave
  - nWave &

Select output file



You can use filter here to get your signal file.

Select desired signals



Check your output waveform

inst_i [2:0]	Operation	Notes
000	Unsigned Addition	data_o=data_a_i+data_b_i
001	Unsigned Subtraction	data_o=data_b_i-data_a_i
010	Unsigned Multiplication	data_o= data_a_i*data_b_i
011	NOT	data_o=~data_a_i
100	XOR	data_o= data_a_i⊕data_b_i
101	Absolute Value	Data_o=|data_a_i|
110	Subtraction & Divide by 2	data_o=(data_b_i-data_a_i)>>1
111	Unused	Unused

Practice

- Follow the steps to check the Lab1_alu.v yourself
- Use the nWave to see the output result

Reminder

- Be patient and careful about each step!
- References
  - [1] “鳥哥的Linux 私房菜” http://linux.vbird.org/
- If you have any questions, please contact…
  - R09943018@ntu.edu.tw
  - Specify [ICDLab] before your title