My Recent Experience Developing Open Hardware using KiCAD

A newcome's journey from an ideia to a layout

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University of São Paulo - São Carlos

August 24, 2024

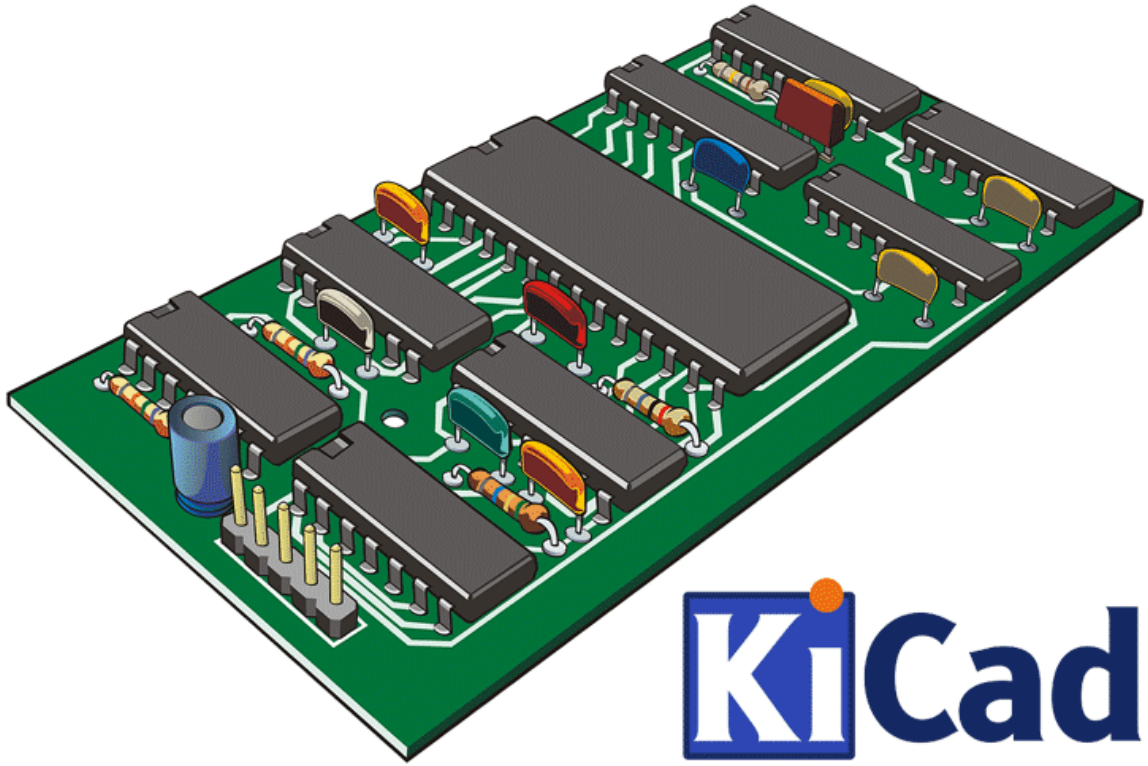
Who am I?

- Carlos Henrique Craveiro Aquino Veras
- Computer Engineering Undergrad Student
- FOSS Herald and Advocate
- Curious guy that loves to learn new things

Open Source Hardware

And many many more...

Focus of the presentation



How it can be used to create amazing things!

The inspiration

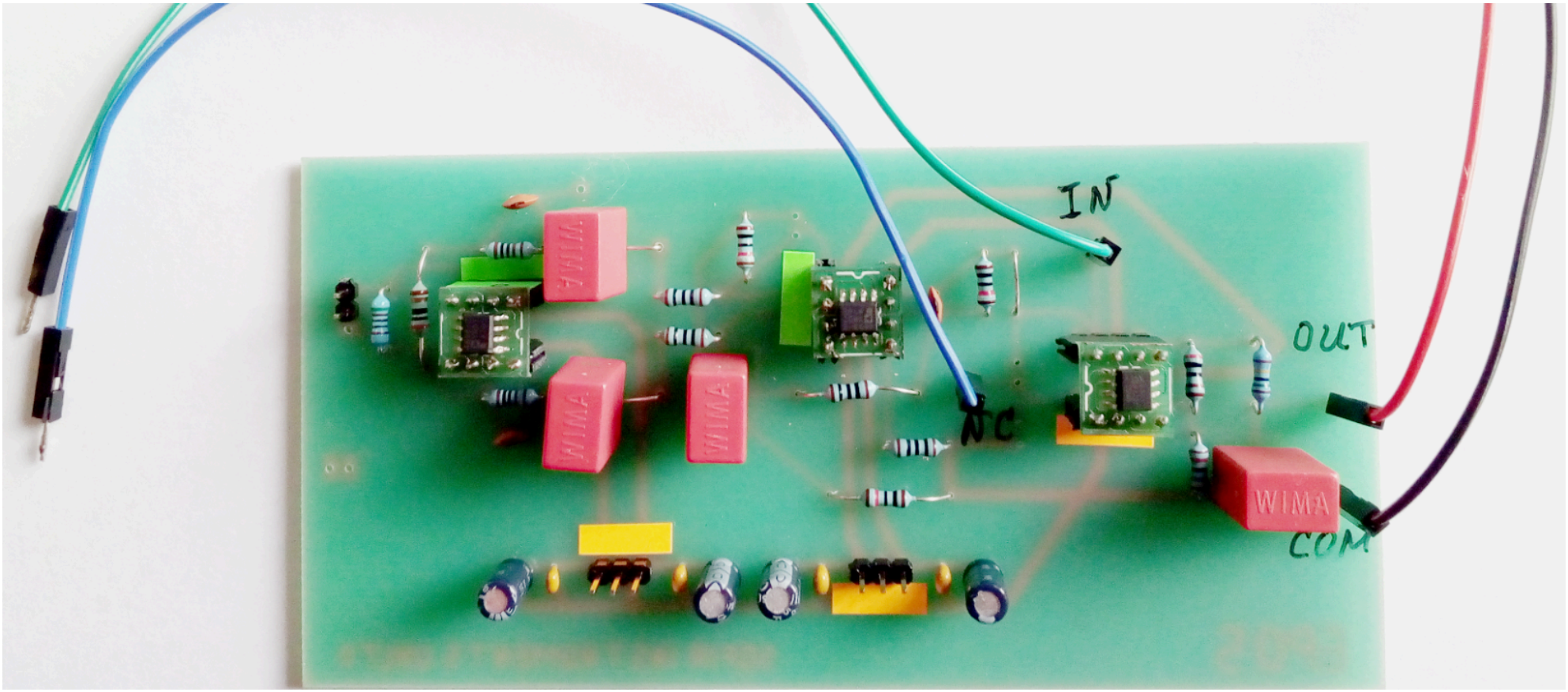
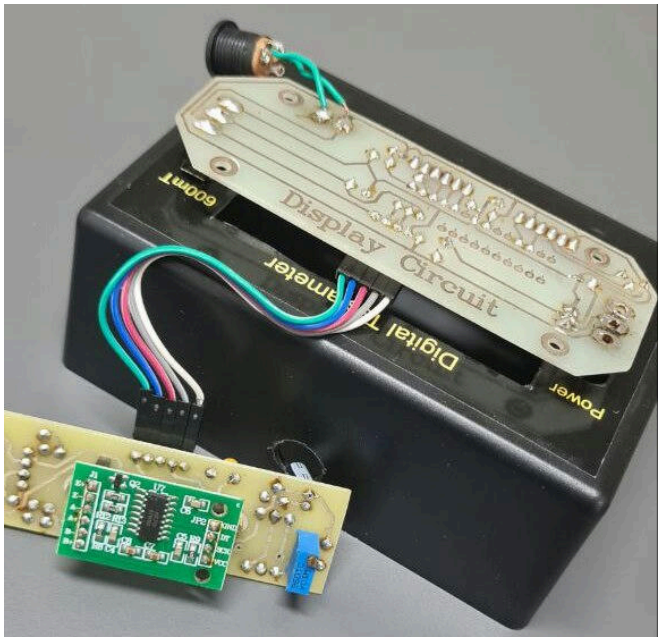
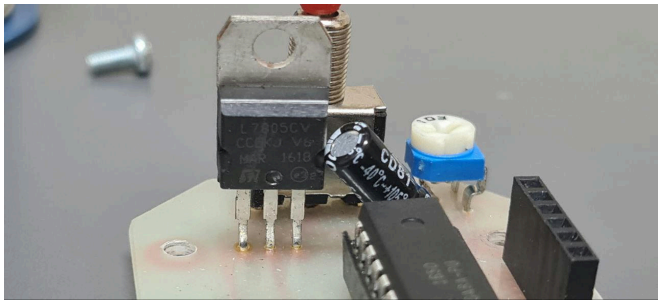


Figure 11: The Original board[1]

When it all started?





48TH IPhO 2017
YOGYAKARTA- INDONESIA
16 - 24 JULY 2017

Original Work

Measurement of the Boltzmann constant by Einstein. Problem of the 5-th Experimental Physics Olympiad. Sofia 9 December 2017

Todor M. Mishonov, Emil G. Petkov, Aleksander A. Stefanov, Aleksander P. Petkov*
Physics Faculty,
St. Clement of Ohrid University at Sofia,
5 James Bourchier blvd, BG-1164 Sofia

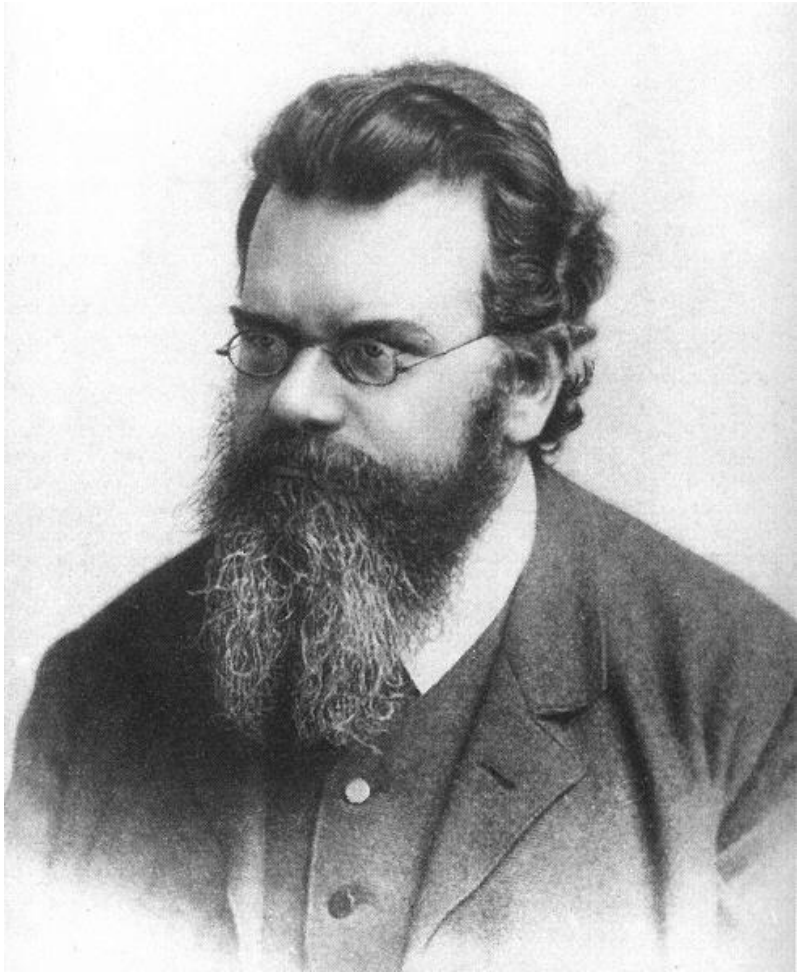
Iglika M. Dimitrova
Faculty of Chemical Technologies,
Department of Physical Chemistry,
University of Chemical Technology and Metallurgy,
8, Kliment Ohridski blvd, BG-1756 Sofia

Stojan G. Manolev†
Middle school Goce Delchev,
Purvomaiska str. 3,
MKD-2460 Valandovo, R. Macedonia

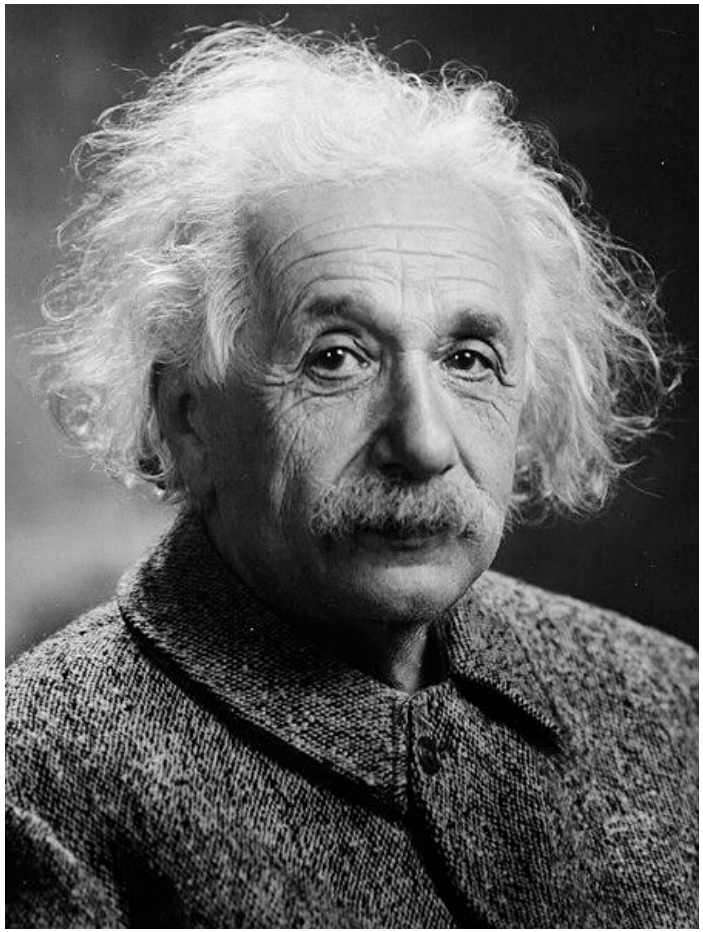
And other authors...

The Boltzmann Constant

$$k_B = 1.380650 \cdot 10^{-23} J.K^{-1}$$



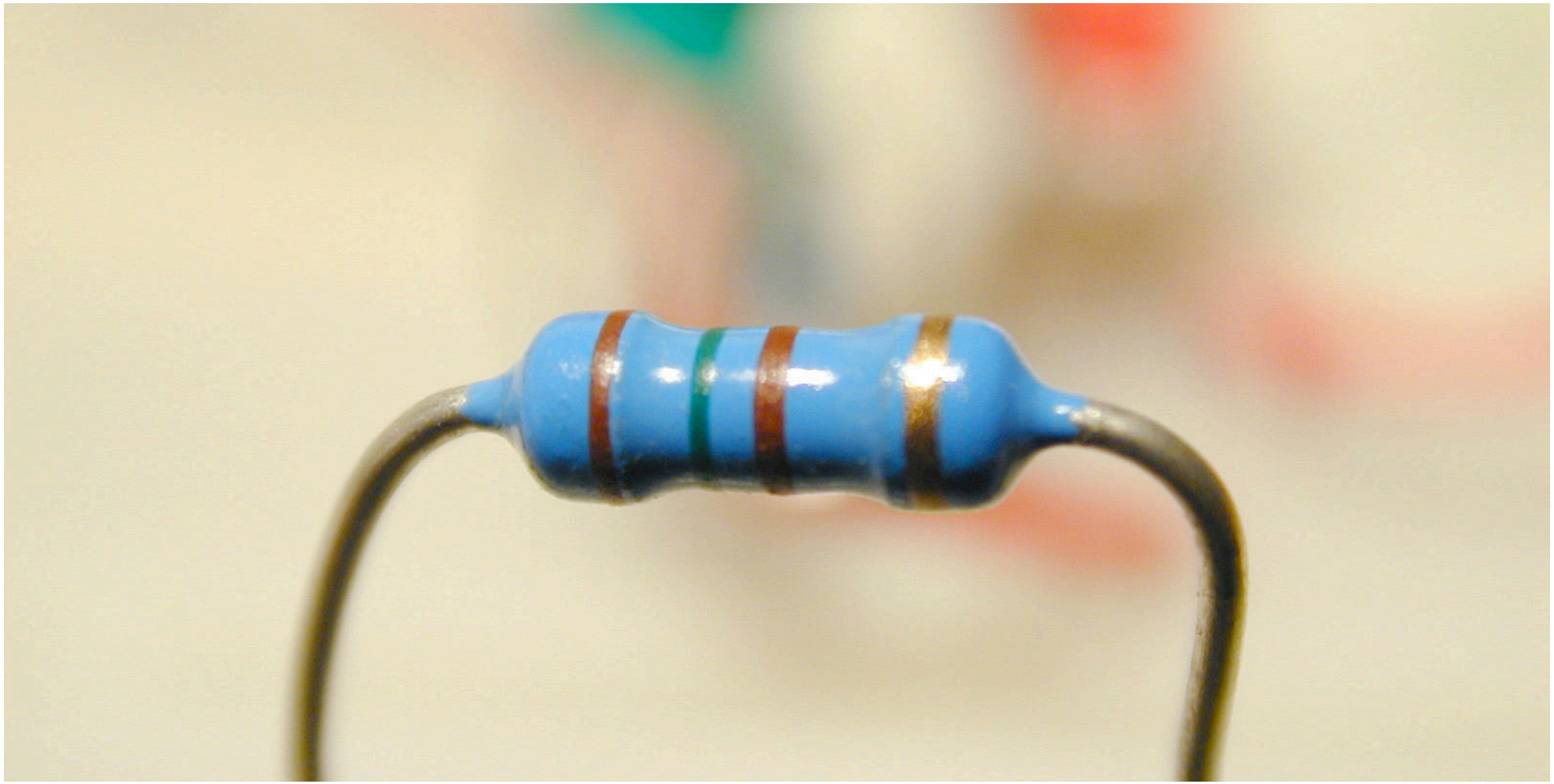
Einstein's Idea



Find k_B by examination of the mean

Thermal Energy[1]!

The Noisy Element



Thermal Noise

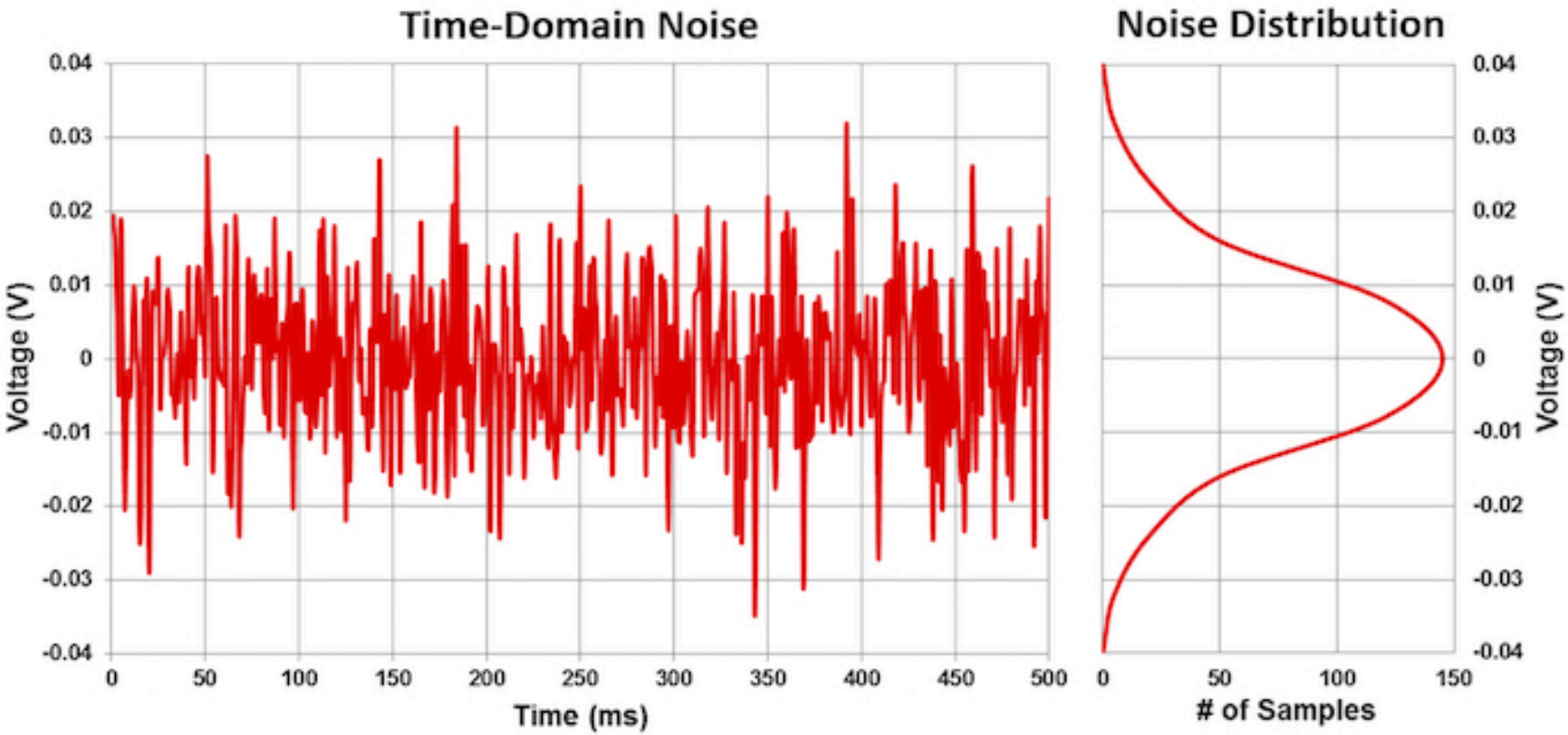
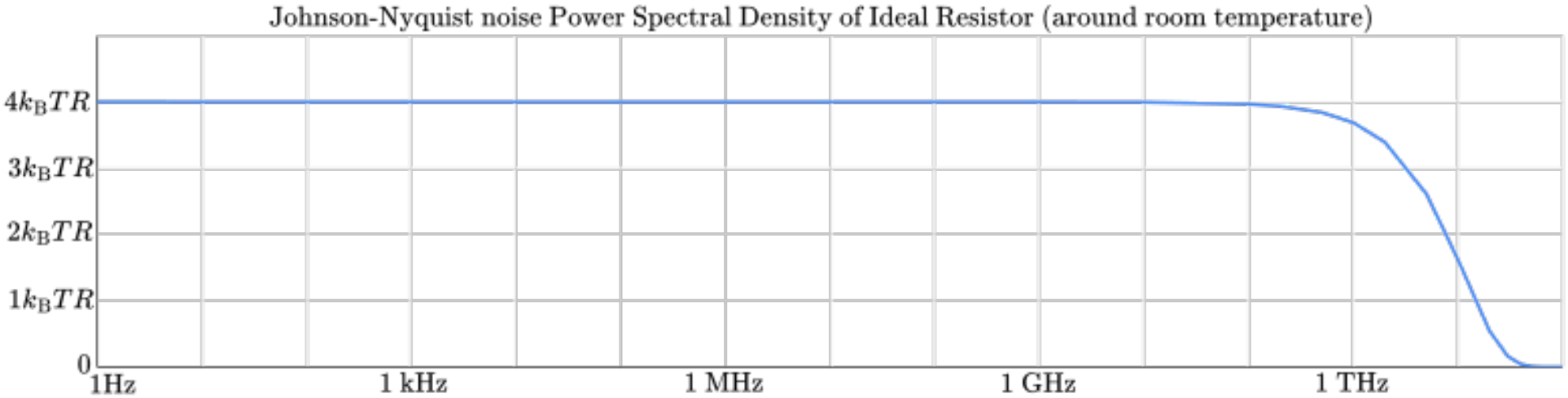


Figure 21: https://www.nwengineeringllc.com/article/thermal-noise-in-communication-and-optical-systems.php

Power Spectral Density

$$S_n(\omega)$$

Thermal Noise Source

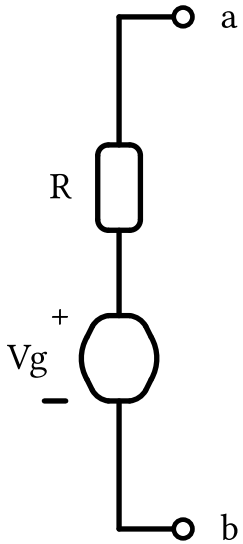


$$\overline{V_n}^2 = 4k_BTR\Delta f$$

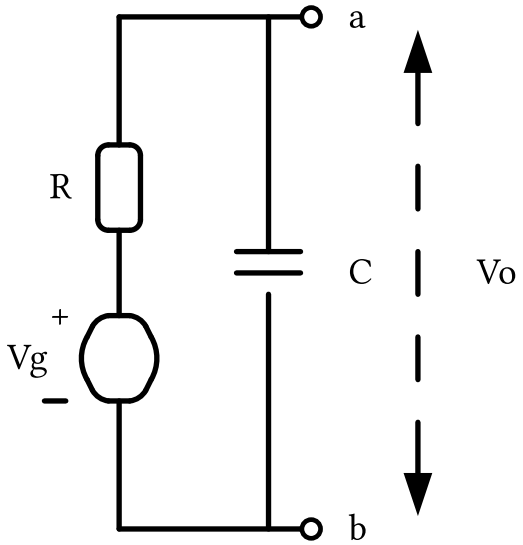
So V_n^2 depends of Δf and R ? What a Drama!

Signal Source[2]

$$S_n(\omega) = 4k_BTR$$

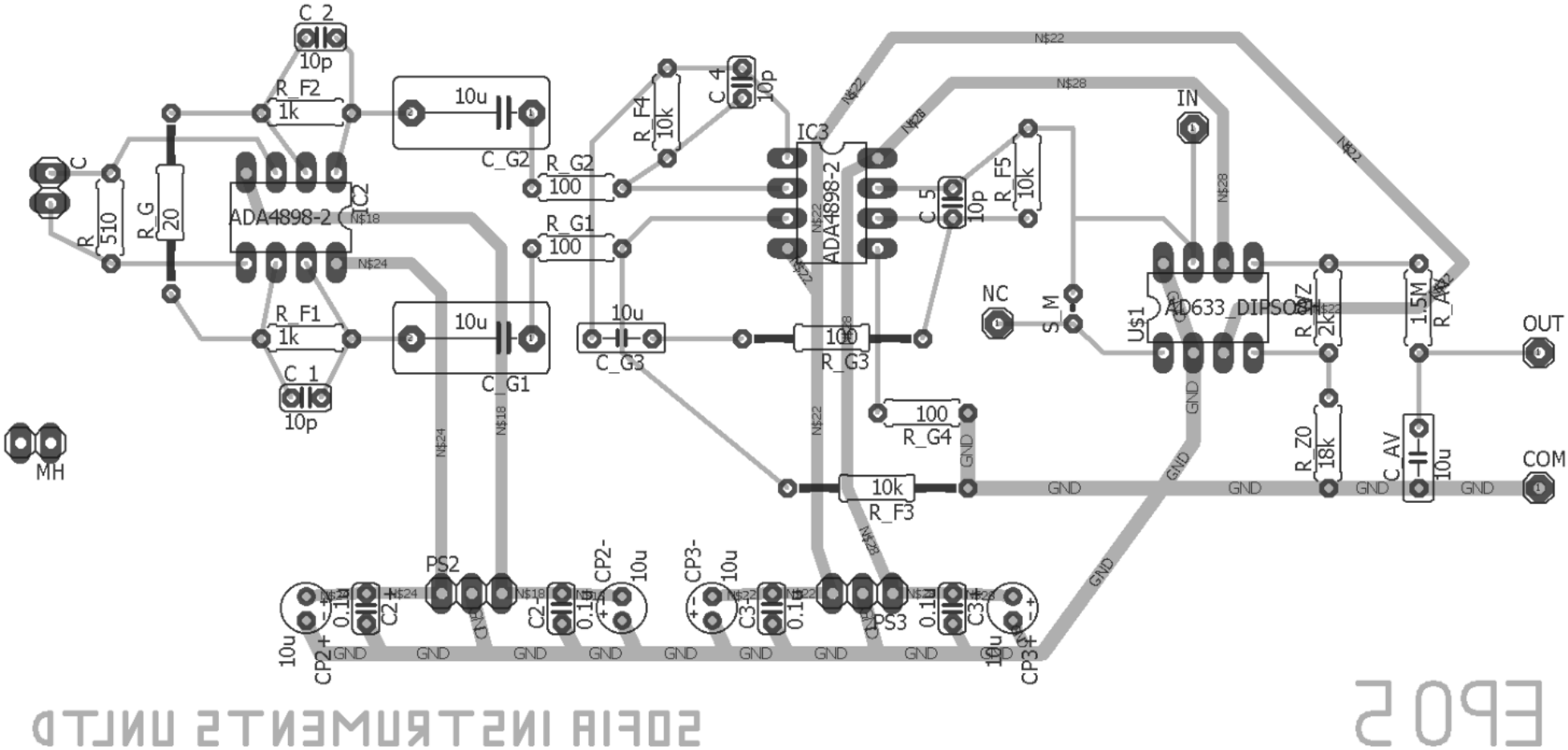


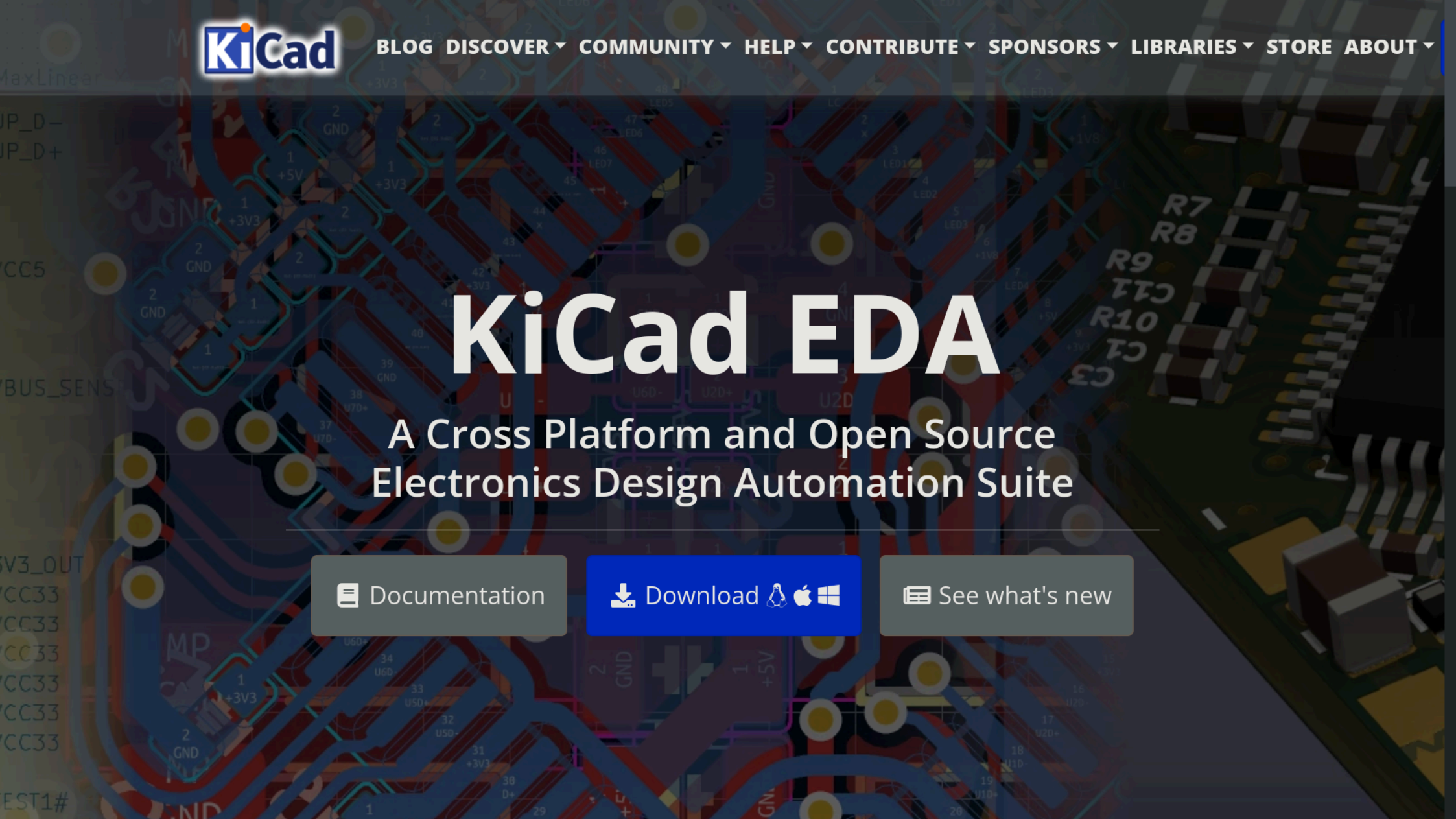
$$S_n(\omega) = |H(\omega)|^2\ 4k_BTR$$



$$\overline{V_o}^2 = \frac{k_BT}{C}$$

Original Layout

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Project Files

- main-board.kicad_pro
  - main-board-backups
  - footprints.pretty
  - gerber_files
  - module_3Dmodels
  - main-board.kicad_dru
  - main-board.kicad_pcb
  - main-board.kicad_sch
  - module_boards.kicad_sym

Schematic Editor
Edit the project schematic

Symbol Editor
Edit global and/or project schematic symbol libraries

PCB Editor
Edit the project PCB design

Footprint Editor
Edit global and/or project PCB footprint libraries

Gerber Viewer
Preview Gerber files

Image Converter
Convert bitmap images to schematic symbols or PCB footprints

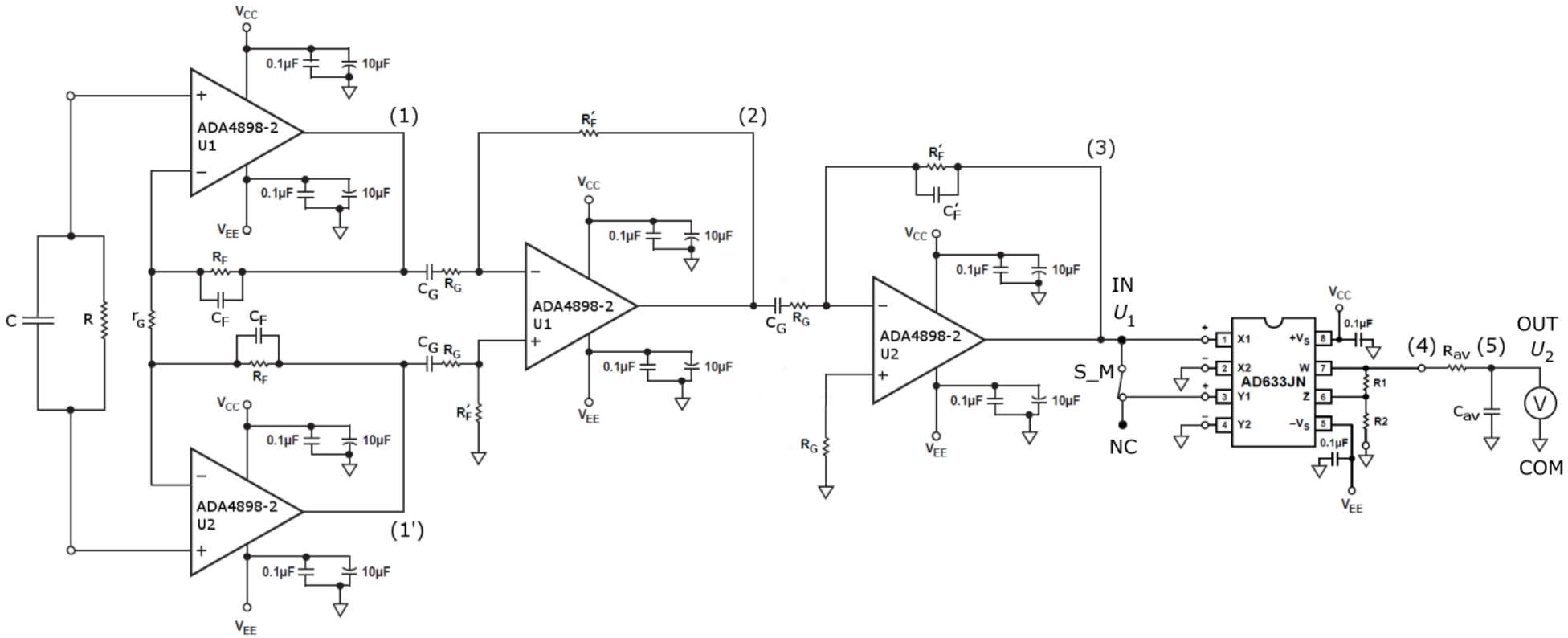
Calculator Tools
Show tools for calculating resistance, current capacity, etc.

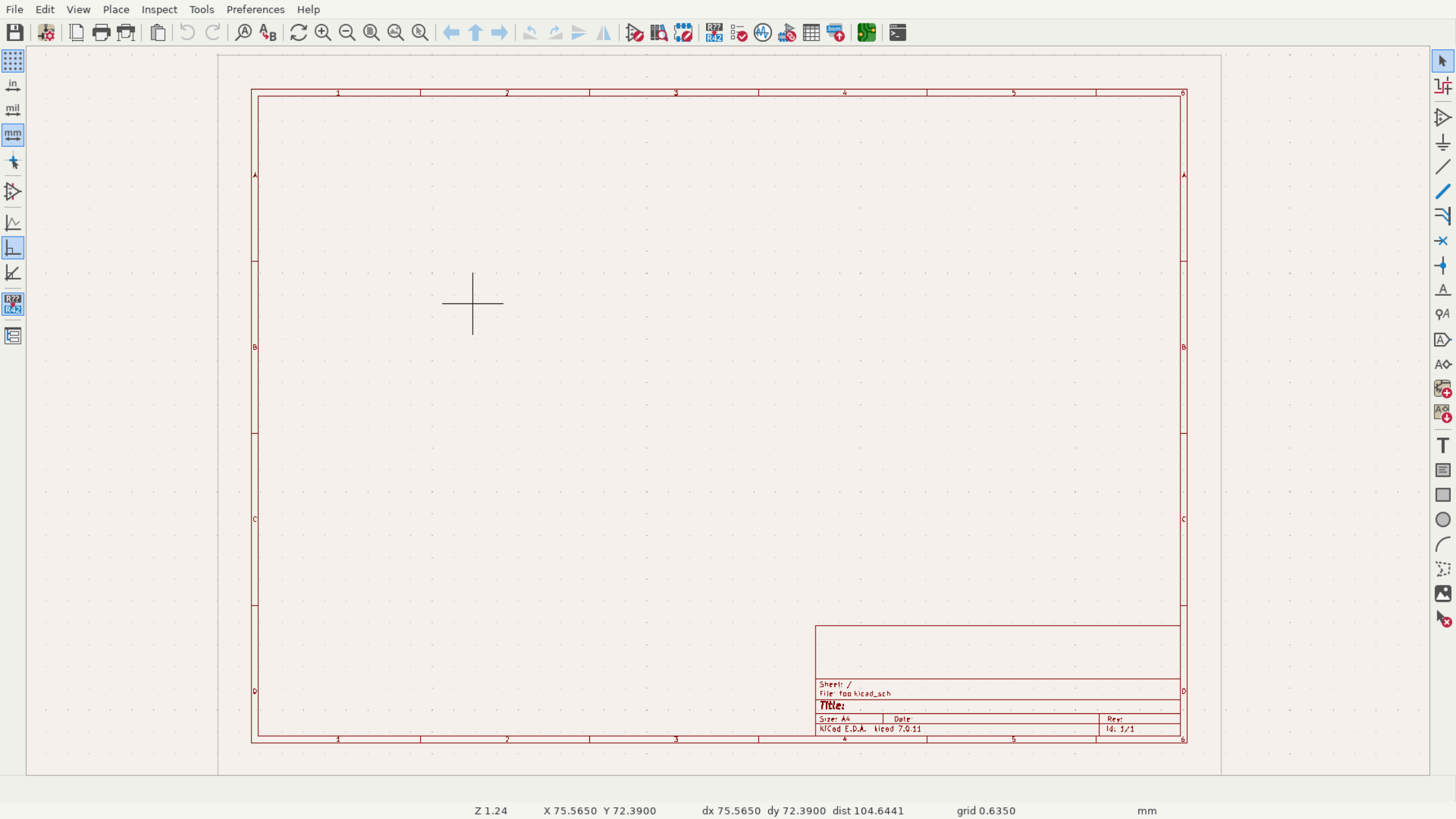
Drawing Sheet Editor
Edit drawing sheet borders and title blocks for use in schematics and PCB designs

Plugin and Content Manager
Manage downloadable packages from KiCad and 3rd party repositories

Project: /home/coveiro/Documents.../main-board/main-board.kicad_pro

Original Schematics



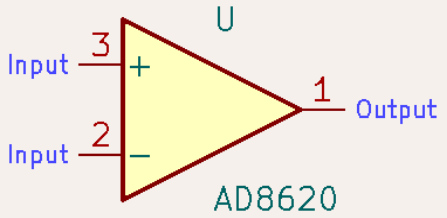

File Edit View Place Inspect Tools Preferences Help
Sheet: /
File: foo.kicad_sch
Title:
Size: A4
Date:
Rev:
KiCad E.D.A. kicad 7.0.11
Id: 1/1
Z 1.24
X 75.5650 Y 72.3900
dx 75.5650 dy 72.3900 dist 104.6441
grid 0.6350
mm

File Edit View Place Inspect Tools Preferences Help

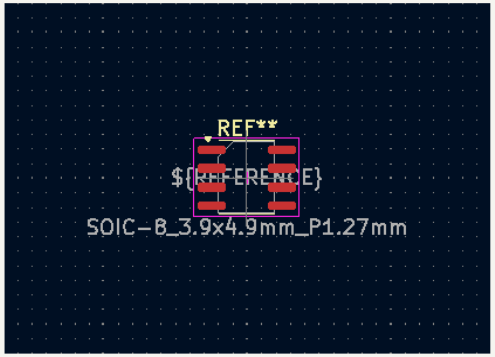
Choose Symbol (20659 items loaded)

opamp

Item	Description
AD8021ARM	Operational Amplifier, 4.5-24V single/dual supply, low noise, high speed, MSOP
AD8603	Precision Micropower, Low Noise CMOS, Rail-to-Rail Input/Output Operational A
AD8610xR	Single Precision, Very Low Noise, Low Input Bias Current, Wide Bandwidth JFET C
AD8610xRM	Single Precision, Very Low Noise, Low Input Bias Current, Wide Bandwidth JFET C
AD8620	Dual Precision, Very Low Noise, Low Input Bias Current, Wide Bandwidth JFET Op
Unit A	
Unit B	
Unit C	
AD8620xRM	Dual Precision, Very Low Noise, Low Input Bias Current, Wide Bandwidth JFET Op
AD8655	Single Low Noise, Precision CMOS Amplifier
AD8656	Dual Low Noise, Precision CMOS Amplifier
AD8676xR	Dual operational amplifier, Ultra-precision, 36V, Rail-to-rail output, SOIC-8
ADA4075-2	Ultralow Noise Amplifier at Lower Power, SOIC-8/LFCSP-8
ADA4077-1xR	4MHz, 7nV/sqrtHz, Low Offset and Drift, High Precision Amplifier, SOIC-8
ADA4077-1xRM	4MHz, 7nV/sqrtHz, Low Offset and Drift, High Precision Amplifier, MSOP-8
ADA4084-4xCP	30V Quad Low Noise, Rail-to-Rail Input/Output, Low Power Operational Amplifie
ADA4530-1	Femtoampere Input Bias Current Electrometer Amplifier, SOIC-8
ADA4610-1xR	Low Noise, Precision, Rail-to-Rail Output, JFET Single Op Amp, SOIC-8



[Default] Package_SO:SOIC-8_3.9x4.9mm_P1.27mm



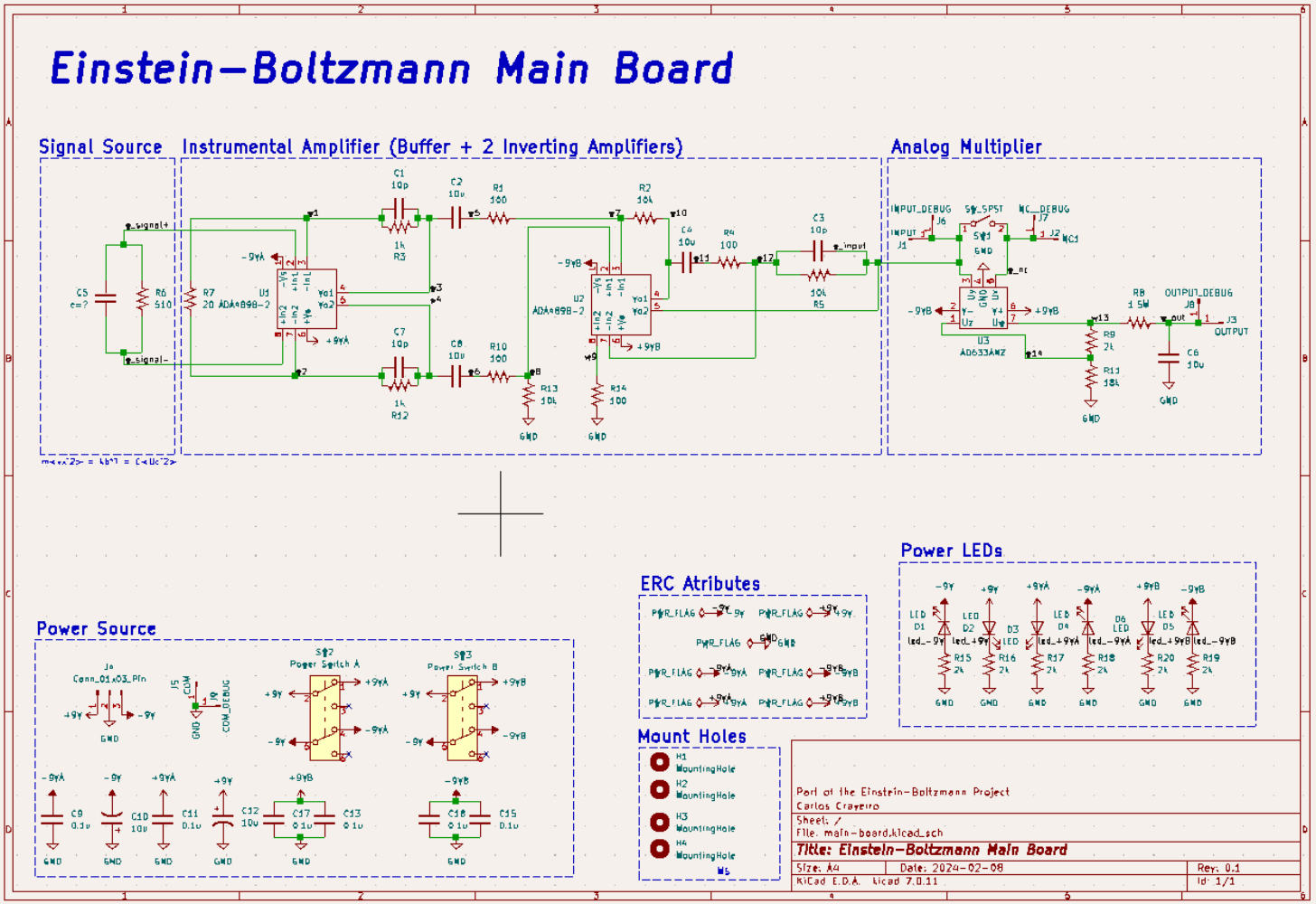
AD8620
Derived from LM2904 (Dual Operational Amplifiers, DIP-8/SOIC-8/TSSOP-8/VSSOP-8)
Dual Precision, Very Low Noise, Low Input Bias Current, Wide Bandwidth JFET Operational Amplifiers, SOIC-8
Keywords: dual opamp

Reference U?
Footprint Package_SO:SOIC-8_3.9x4.9mm_P1.27mm

Select with Browser | Place repeated copies | Place all units | Cancel | OK

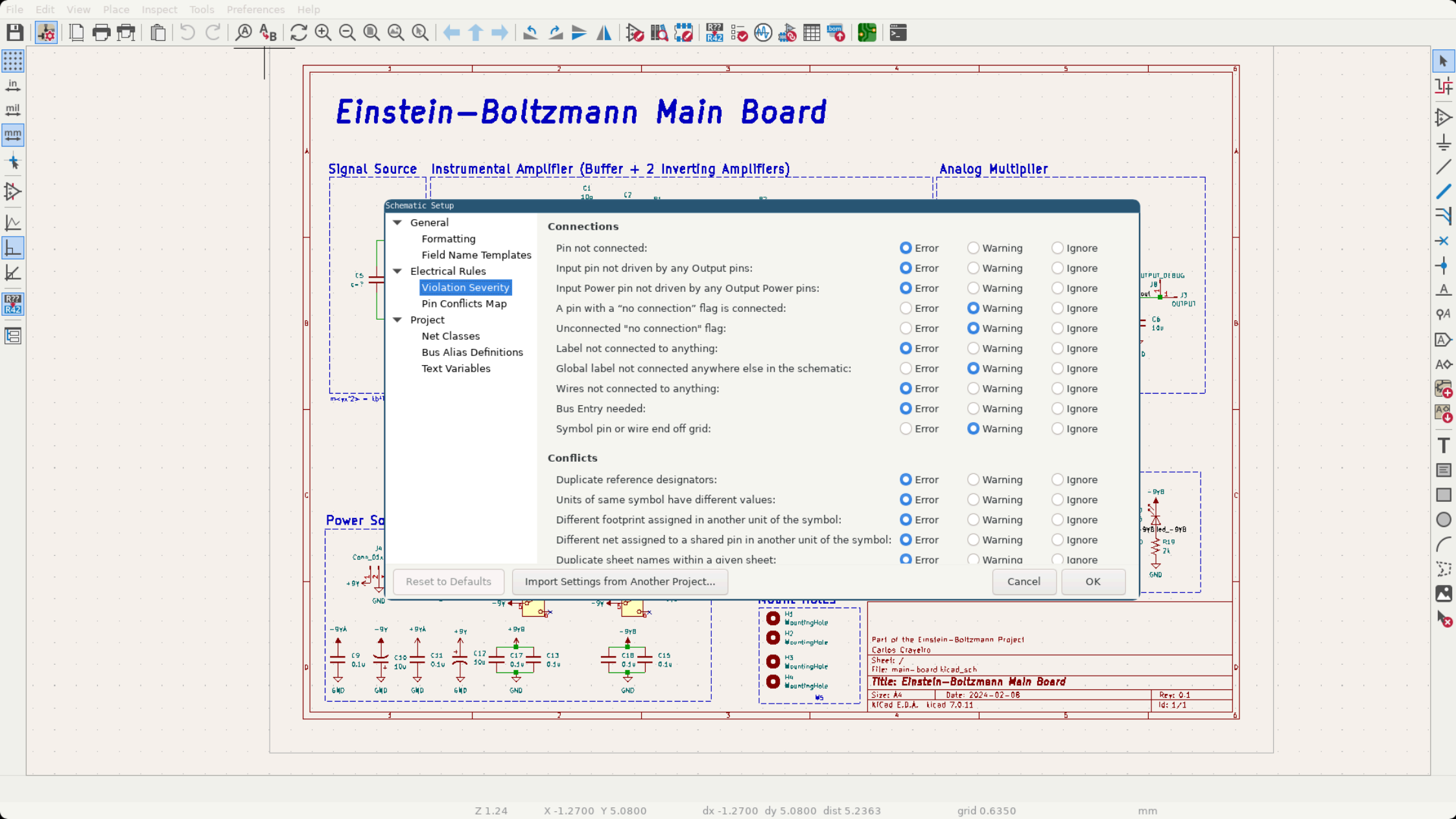
Title:
Size: A4 | Date: | Rev:
KiCad E.D.A. kicad 7.0.11 | Id: 1/1

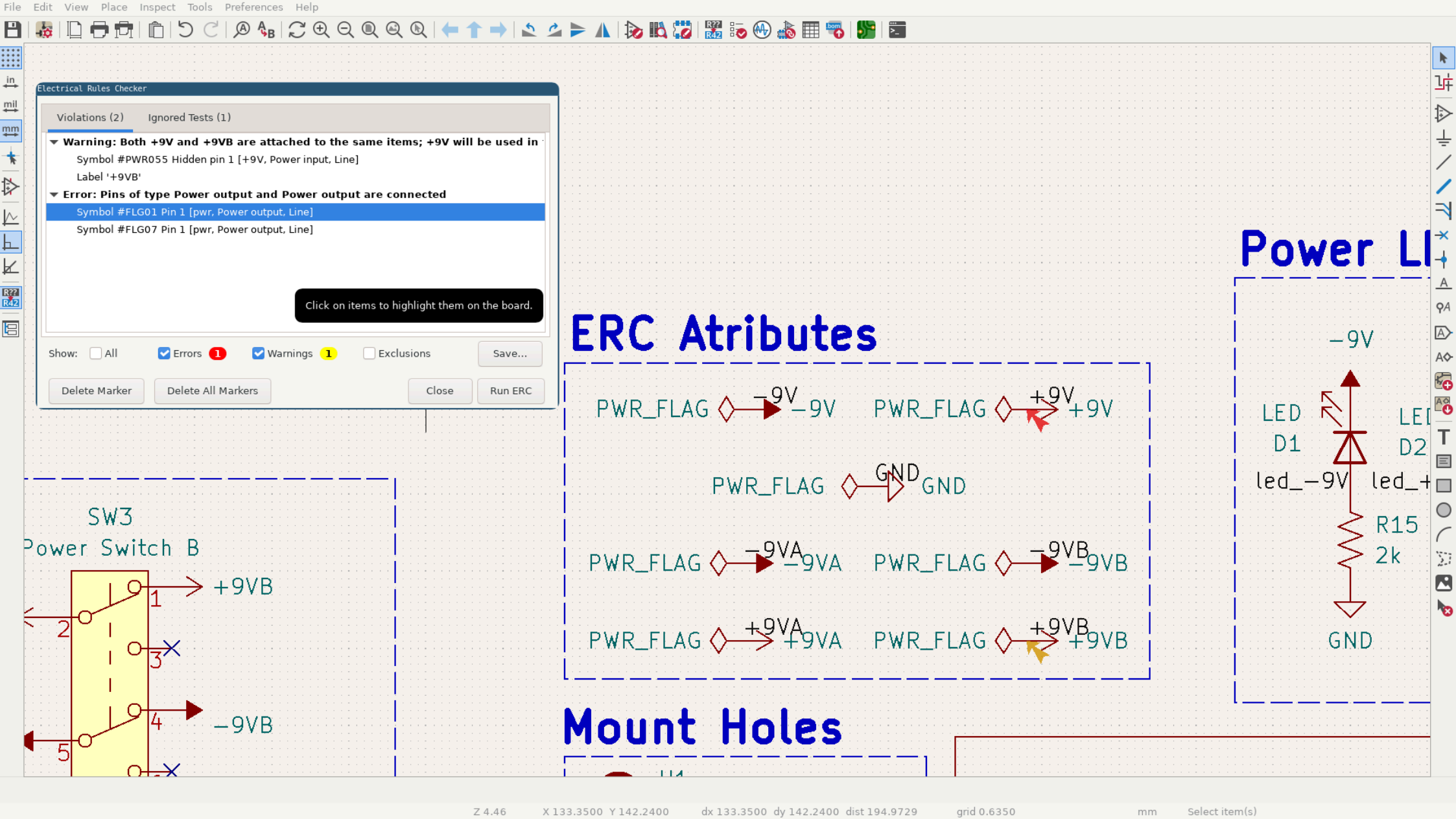
Z 1.24 X 133.9850 Y 123.1900 dx 133.9850 dy 123.1900 dist 182.0103 grid 0.6350 mm Add Symbol

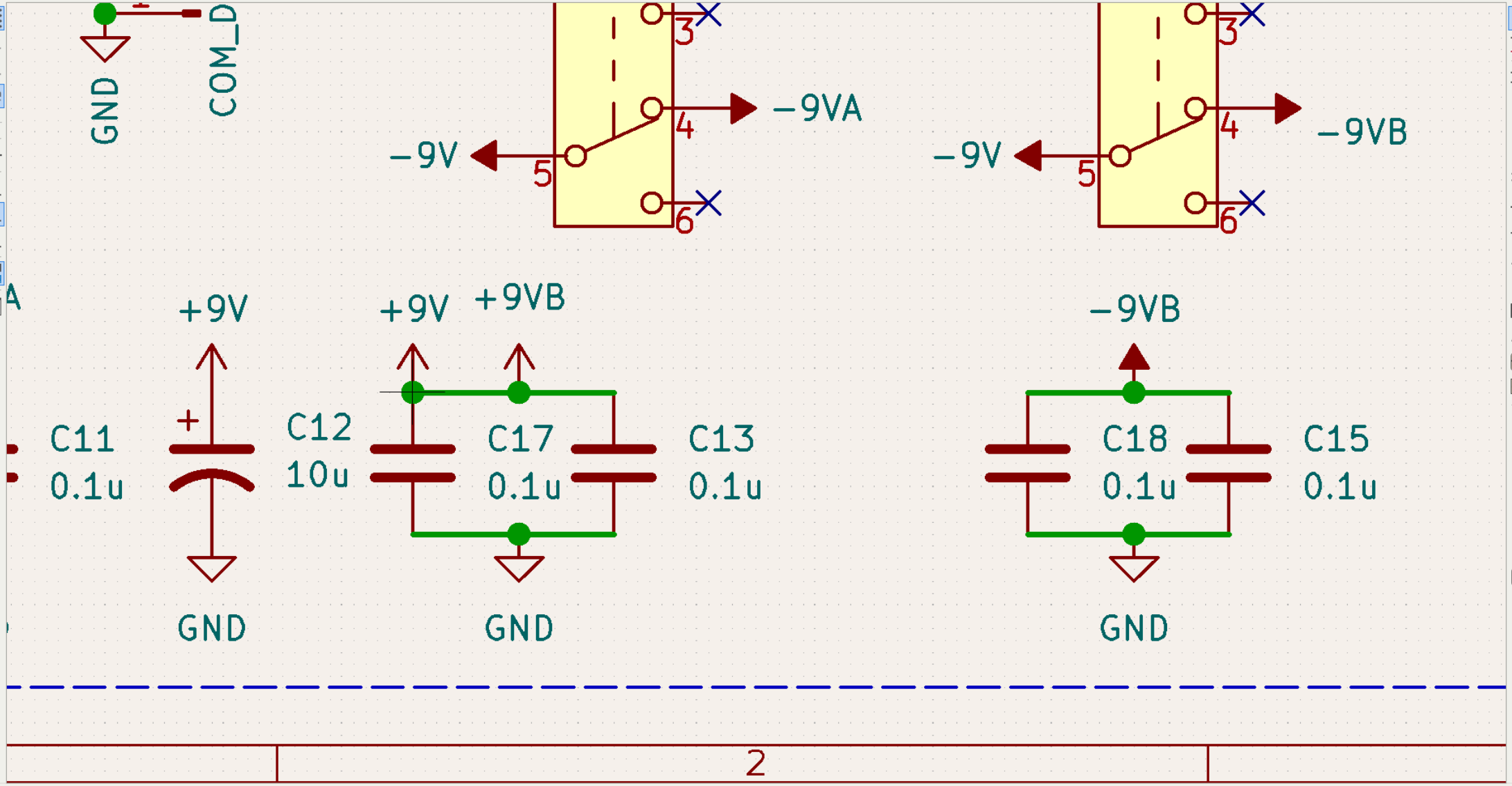

Einstein–Boltzmann Main Board
Signal Source
Instrumental Amplifier (Buffer + 2 Inverting Amplifiers)
Analog Multiplier
Power Source
ERC Atributes
Power LEDs
Mount Holes
Part of the Einstein–Boltzmann Project
Carlos Crayeiro
Sheet: /
File: main-board.kicad_sch
Title: Einstein–Boltzmann Main Board
Size: A4
Date: 2024-02-08
Rev: 0.1
KiCad E.D.A. kicad 7.0.11
Id: 1/1

Electric Rule Checker

- Correctness of power and ground connections
- Problems with the SPICE simulation models
- Unconnected inputs or shorted outputs
- Conflicting information on schematic


Einstein–Boltzmann Main Board
Signal Source
Instrumental Amplifier (Buffer + 2 Inverting Amplifiers)
Analog Multiplier
Power So
Schematic Setup
General
Formatting
Field Name Templates
Electrical Rules
Violation Severity
Pin Conflicts Map
Project
Net Classes
Bus Alias Definitions
Text Variables
Connections
Pin not connected: Error Warning Ignore
Input pin not driven by any Output pins: Error Warning Ignore
Input Power pin not driven by any Output Power pins: Error Warning Ignore
A pin with a "no connection" flag is connected: Error Warning Ignore
Unconnected "no connection" flag: Error Warning Ignore
Label not connected to anything: Error Warning Ignore
Global label not connected anywhere else in the schematic: Error Warning Ignore
Wires not connected to anything: Error Warning Ignore
Bus Entry needed: Error Warning Ignore
Symbol pin or wire end off grid: Error Warning Ignore
Conflicts
Duplicate reference designators: Error Warning Ignore
Units of same symbol have different values: Error Warning Ignore
Different footprint assigned in another unit of the symbol: Error Warning Ignore
Different net assigned to a shared pin in another unit of the symbol: Error Warning Ignore
Duplicate sheet names within a given sheet: Error Warning Ignore
Reset to Defaults
Import Settings from Another Project...
Cancel
OK
Part of the Einstein–Boltzmann Project
Carlos Cravelro
Sheet: /
File: main–board.kicad_sch
Title: Einstein–Boltzmann Main Board
Size: A4
Date: 2024–02–08
Rev: 0.1
KiCad E.D.A. kicad 7.0.11
Id: 1/1

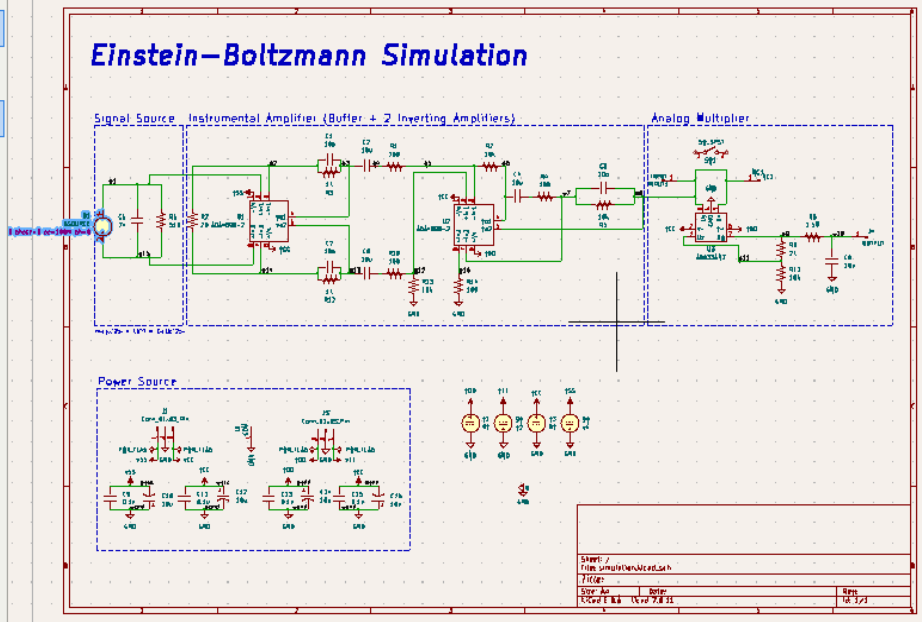

File Edit View Place Inspect Tools Preferences Help
Electrical Rules Checker
Violations (2)
Ignored Tests (1)
Warning: Both +9V and +9VB are attached to the same items; +9V will be used in
Symbol #PWR055 Hidden pin 1 [+9V, Power input, Line]
Label '+9VB'
Error: Pins of type Power output and Power output are connected
Symbol #FLG01 Pin 1 [pwr, Power output, Line]
Symbol #FLG07 Pin 1 [pwr, Power output, Line]
Click on items to highlight them on the board.
Show: All Errors 1 Warnings 1 Exclusions Save...
Delete Marker
Delete All Markers
Close
Run ERC
ERC Atributes
PWR_FLAG −9V −9V
PWR_FLAG +9V +9V
PWR_FLAG GND GND
PWR_FLAG −9VA −9VA
PWR_FLAG −9VB −9VB
PWR_FLAG +9VA +9VA
PWR_FLAG +9VB +9VB
SW3
Power Switch B
+9VB
−9VB
1
2
3
4
5
Mount Holes
Power Ll
−9V
LED
D1
led_−9V
R15
2k
GND
Z 4.46
X 133.3500 Y 142.2400
dx 133.3500 dy 142.2400 dist 194.9729
grid 0.6350
mm
Select item(s)


GND
COM_D
3
4
5
6
−9V
−9VA
−9V
−9VB
+9V
C11
0.1u
+9V
+9VB
C12
10u
C17
0.1u
C13
0.1u
−9VB
C18
0.1u
C15
0.1u
GND
GND
GND
2

Simulation

- Verify the theoretical behaviour of the board
- KiCAD natively integrates simulation capabilitys
- Uses NGSpice as the simulation engine
- Provides a variety of simulation types (DC Analysis, AC, Op, ...)

File Edit View Place Inspect Tools Preferences Help



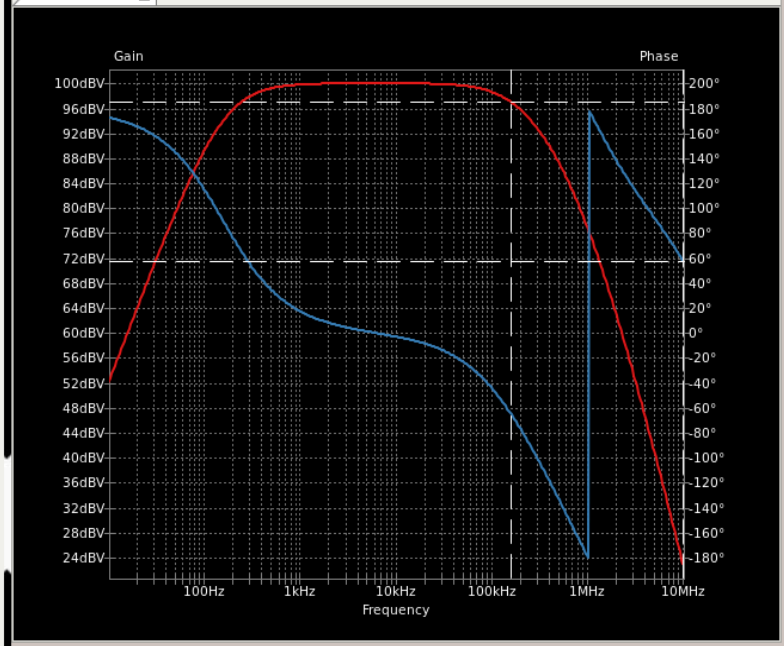
Reference	Value	Name	Library	Footprint	Description
B1	BSOURCE	BSOURCE	Simulation_SPICE	<Unknown>	Arbitrary behavioral voltage or current source

Z 0.72 X 189.8650 Y 108.5850 dx 189.8650 dy 108.5850 dist 218.7222 grid 0.6350 mm

File Simulation View

Run/Stop Simulation | Add Signals | Probe | Tune | Sim Command

Plot3 - AC




```
Note: Compatibility modes selected: ps a
Circuit: KiCad schematic
Reducing trtol to 1 for xspice 'A' devices
Doing analysis at TEMP = 27.000000 and TNOM = 27.000000
 Reference value :  1.00000e+01
No. of Data Rows : 601
```

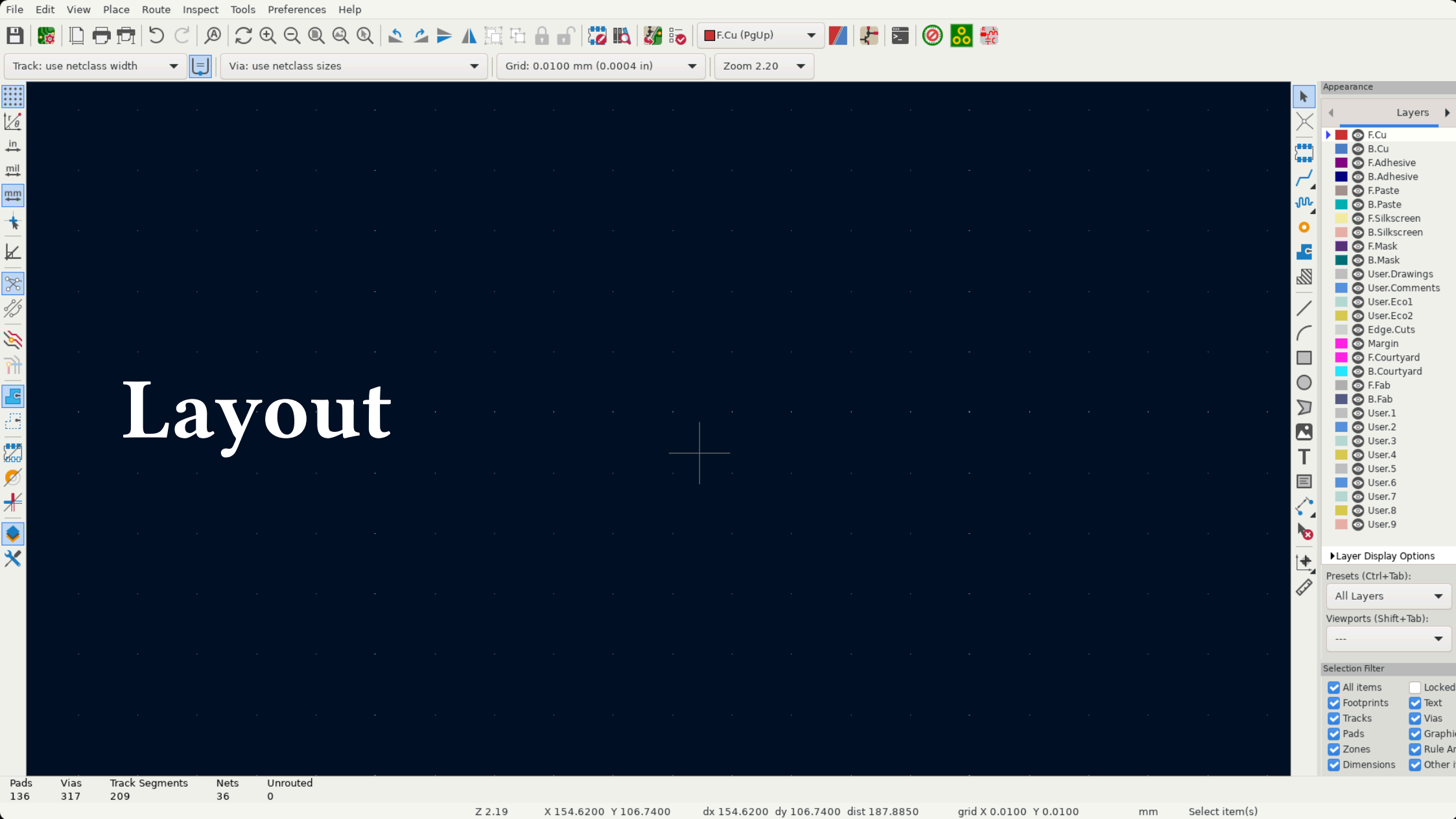
Signals

- V(/w8) (mag)
- V(/w8) (phase)

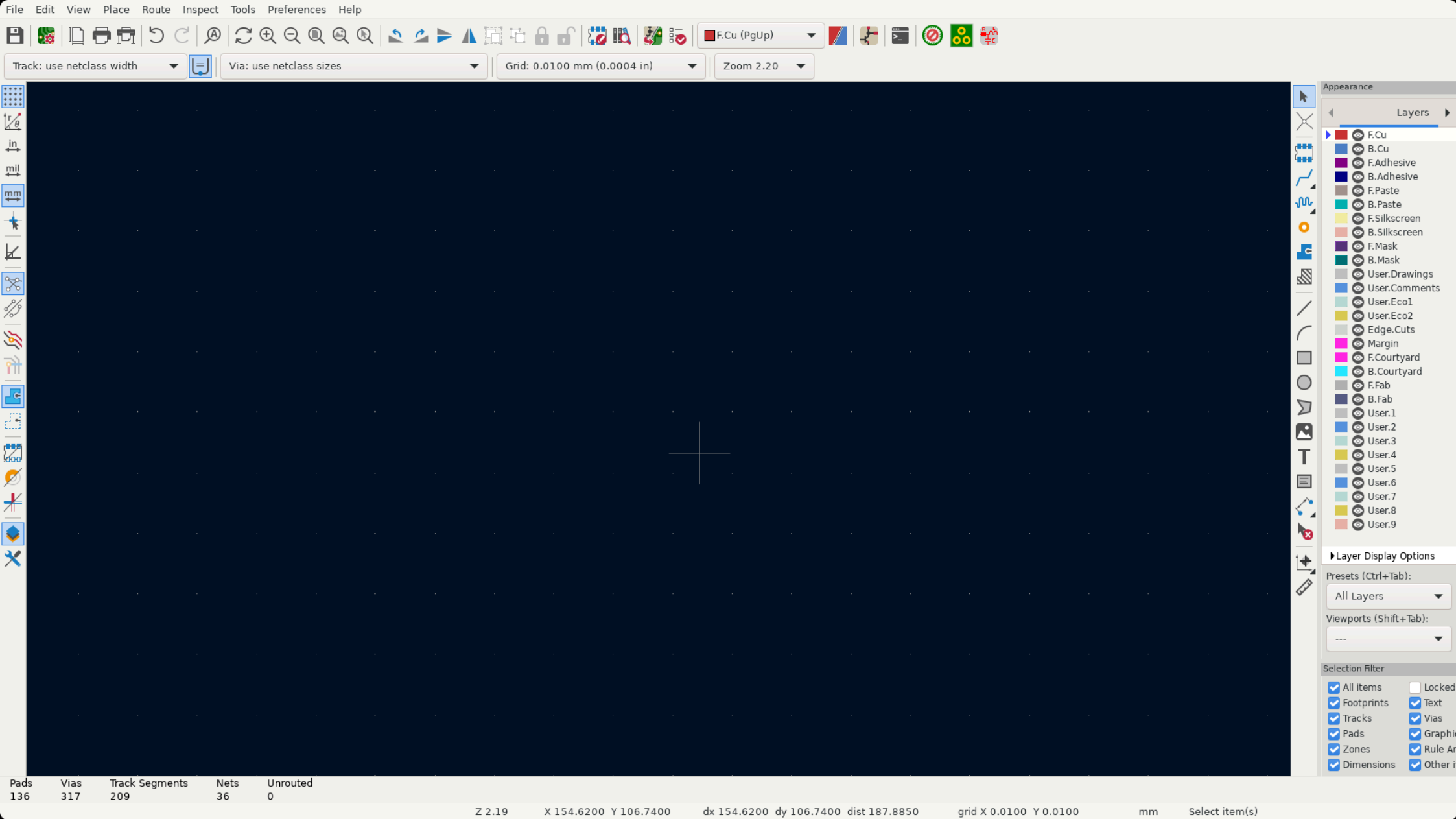
Cursors

Signal	Freq
V(/w8) (mag)	160.
V(/w8) (phase)	10M

Tune


File Edit View Place Route Inspect Tools Preferences Help
F.Cu (PgUp)
Track: use netclass width
Via: use netclass sizes
Grid: 0.0100 mm (0.0004 in)
Zoom 2.20
Layout
Appearance
Layers
F.Cu
B.Cu
F.Adhesive
B.Adhesive
F.Paste
B.Paste
F.Silkscreen
B.Silkscreen
F.Mask
B.Mask
User.Drawings
User.Comments
User.Eco1
User.Eco2
Edge.Cuts
Margin
F.Courtyard
B.Courtyard
F.Fab
B.Fab
User.1
User.2
User.3
User.4
User.5
User.6
User.7
User.8
User.9
Layer Display Options
Presets (Ctrl+Tab):
All Layers
Viewports (Shift+Tab):

Selection Filter
All items
Locked
Footprints
Text
Tracks
Vias
Pads
Graphi
Zones
Rule Ar
Dimensions
Other i
Pads
136
Vias
317
Track Segments
209
Nets
36
Unrouted
0
Z 2.19
X 154.6200 Y 106.7400
dx 154.6200 dy 106.7400 dist 187.8850
grid X 0.0100 Y 0.0100
mm
Select item(s)


File
Edit
View
Place
Route
Inspect
Tools
Preferences
Help
F.Cu (PgUp)
Track: use netclass width
Via: use netclass sizes
Grid: 0.0100 mm (0.0004 in)
Zoom 2.20
Appearance
Layers
F.Cu
B.Cu
F.Adhesive
B.Adhesive
F.Paste
B.Paste
F.Silkscreen
B.Silkscreen
F.Mask
B.Mask
User.Drawings
User.Comments
User.Eco1
User.Eco2
Edge.Cuts
Margin
F.Courtyard
B.Courtyard
F.Fab
B.Fab
User.1
User.2
User.3
User.4
User.5
User.6
User.7
User.8
User.9
Layer Display Options
Presets (Ctrl+Tab):
All Layers
Viewports (Shift+Tab):

Selection Filter
All items
Locked
Footprints
Text
Tracks
Vias
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Zones
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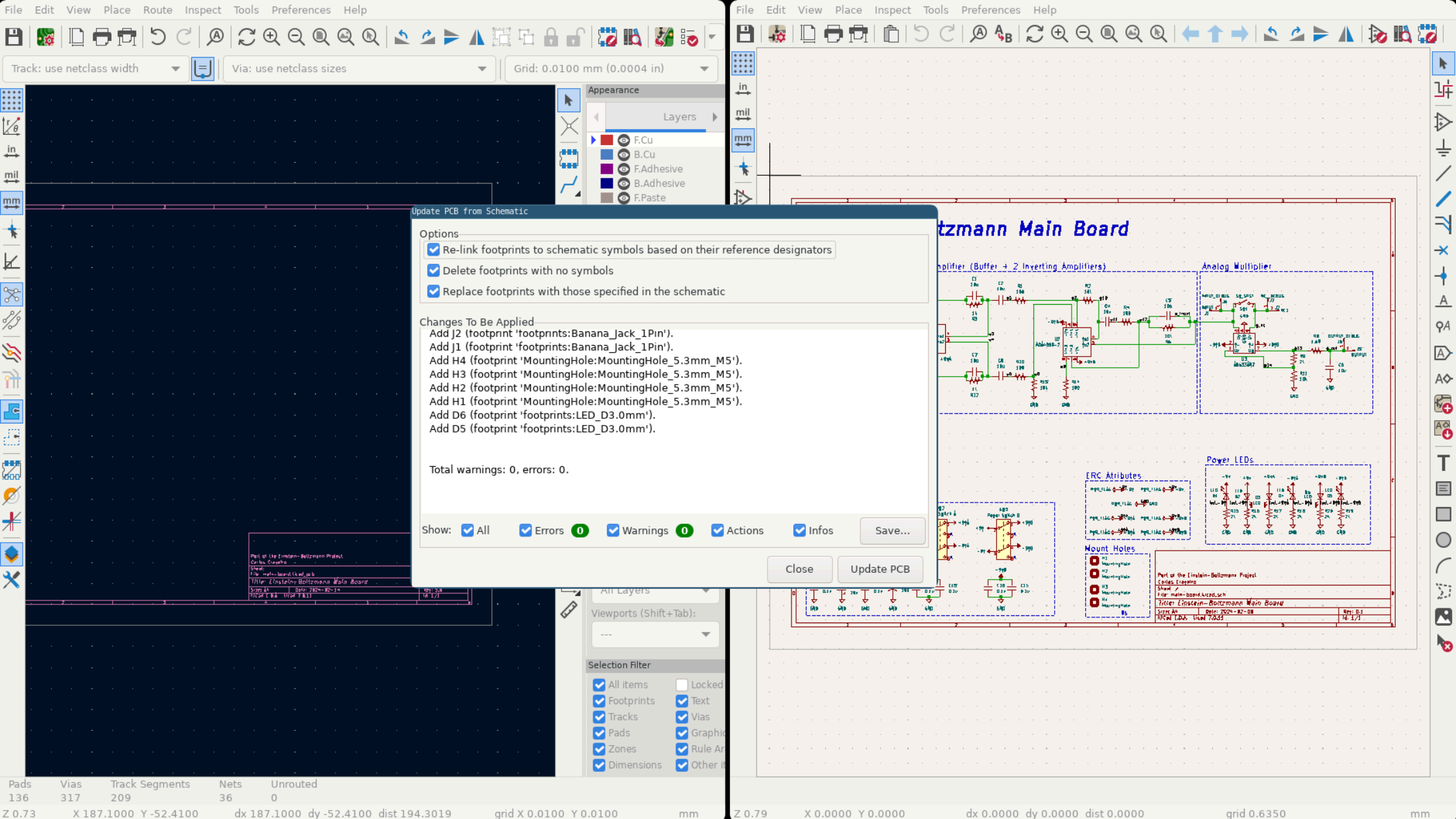
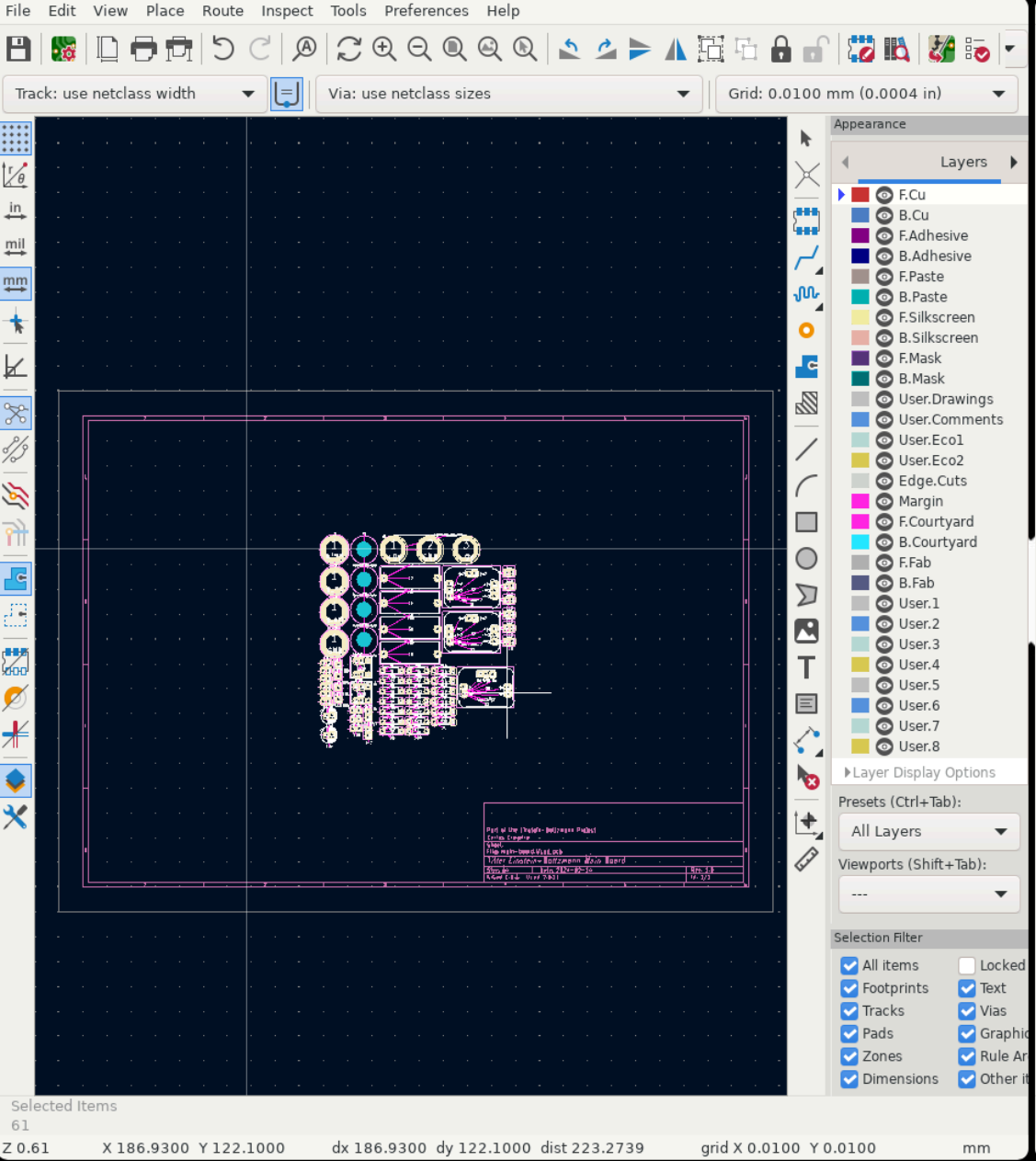
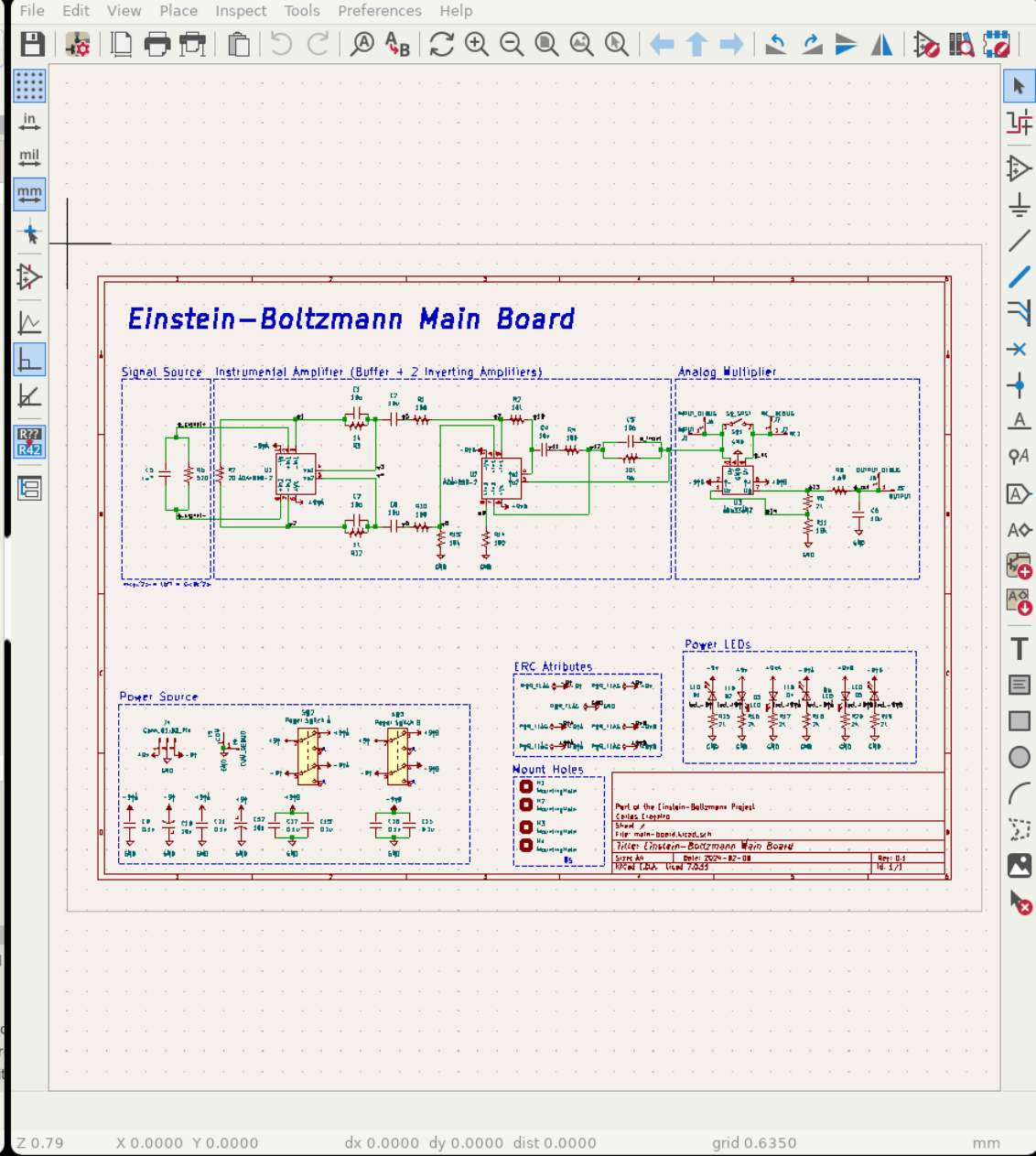
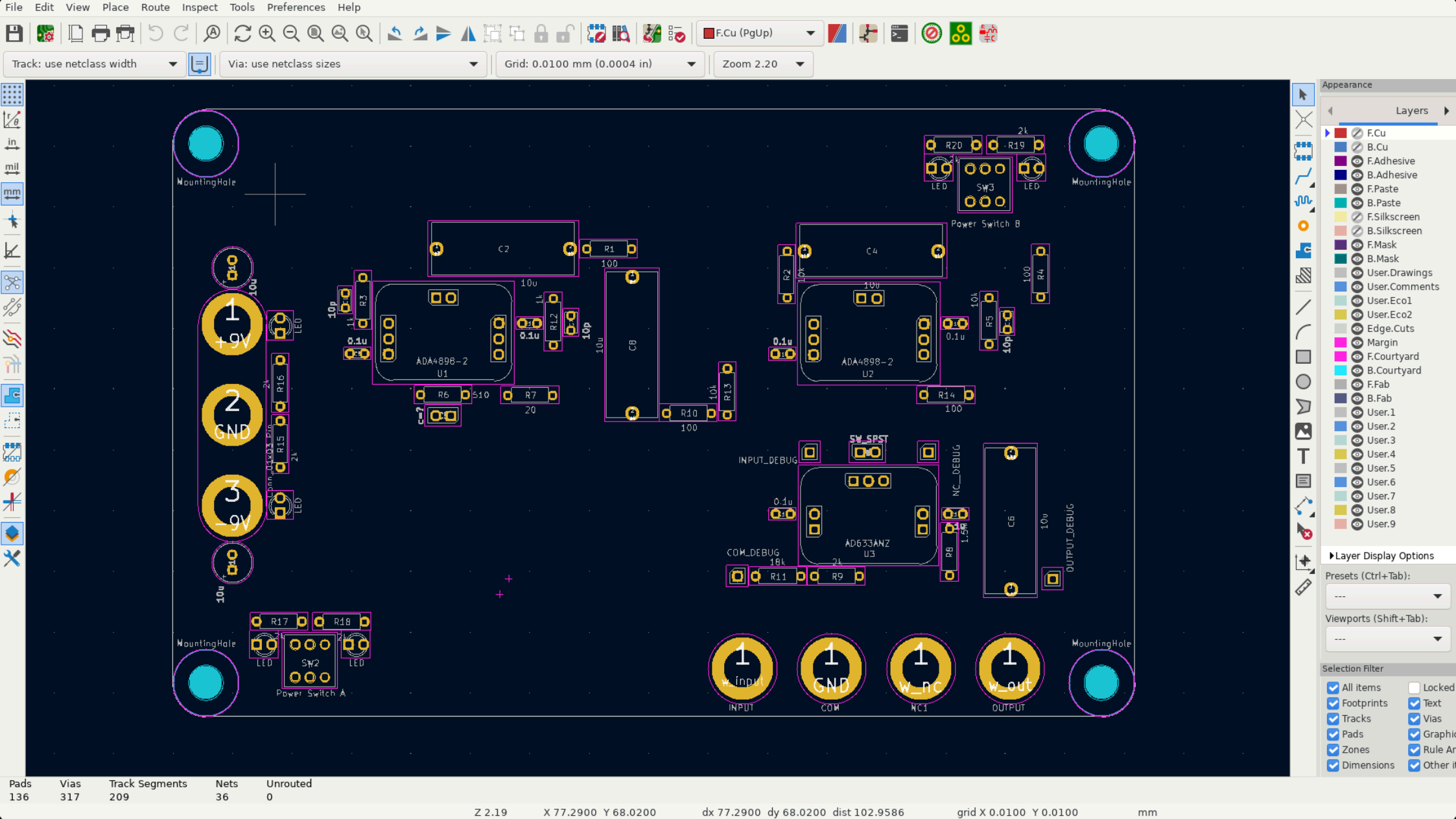
Dimensions
Other i
Pads
136
Vias
317
Track Segments
209
Nets
36
Unrouted
0
Z 2.19
X 154.6200 Y 106.7400
dx 154.6200 dy 106.7400 dist 187.8850
grid X 0.0100 Y 0.0100
mm
Select item(s)

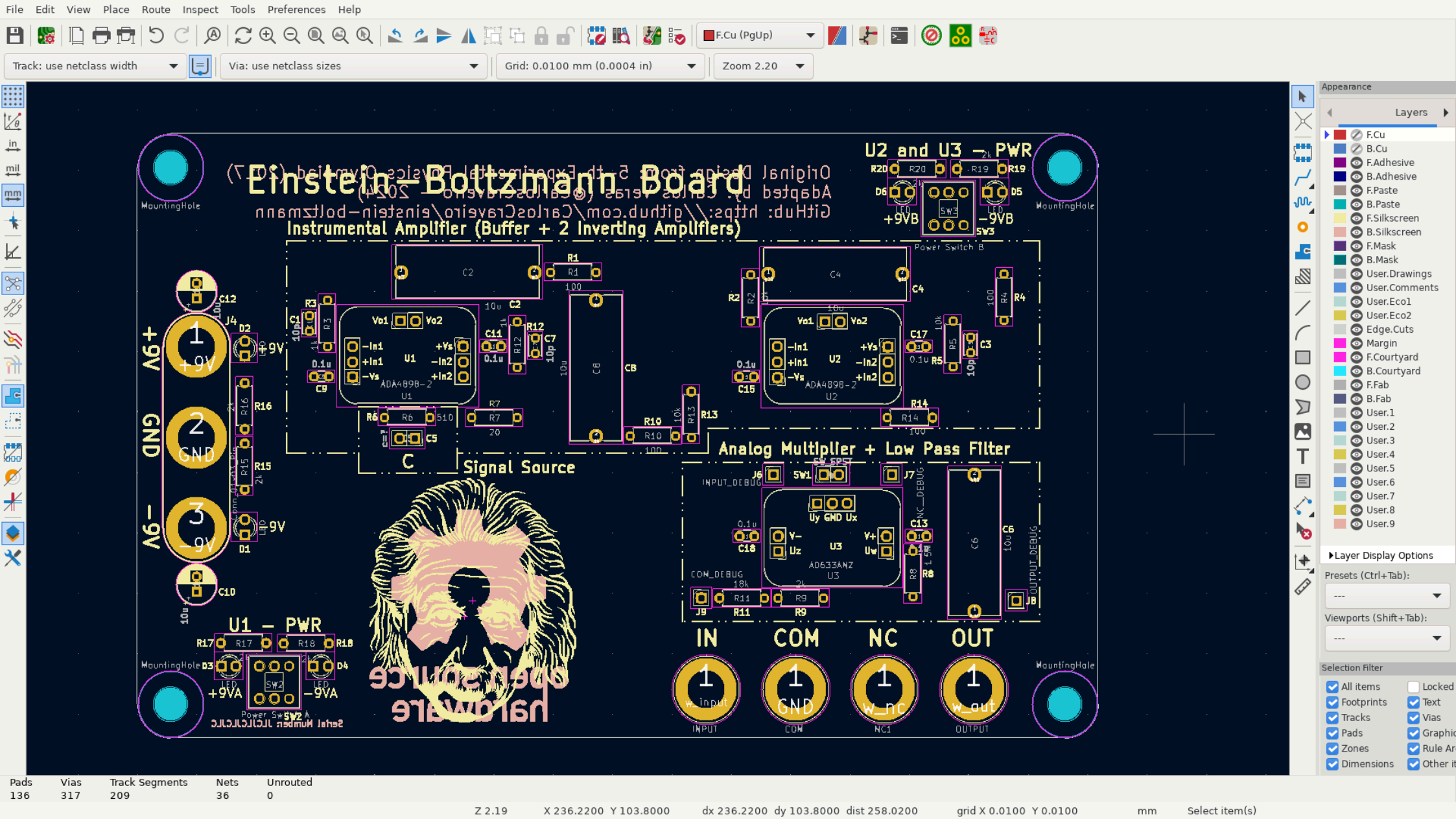

File Edit View Place Route Inspect Tools Preferences Help
Track: use netclass width
Via: use netclass sizes
Grid: 0.0100 mm (0.0004 in)
Appearance
Layers
F.Cu
B.Cu
F.Adhesive
B.Adhesive
F.Paste
Update PCB from Schematic
Options
Re-link footprints to schematic symbols based on their reference designators
Delete footprints with no symbols
Replace footprints with those specified in the schematic
Changes To Be Applied
Add J2 (footprint 'footprints:Banana_Jack_1Pin').
Add J1 (footprint 'footprints:Banana_Jack_1Pin').
Add H4 (footprint 'MountingHole:MountingHole_5.3mm_M5').
Add H3 (footprint 'MountingHole:MountingHole_5.3mm_M5').
Add H2 (footprint 'MountingHole:MountingHole_5.3mm_M5').
Add H1 (footprint 'MountingHole:MountingHole_5.3mm_M5').
Add D6 (footprint 'footprints:LED_D3.0mm').
Add D5 (footprint 'footprints:LED_D3.0mm').
Total warnings: 0, errors: 0.
Show: All Errors 0 Warnings 0 Actions Infos Save...
Close
Update PCB
All Layers
Viewports (Shift+Tab):
Selection Filter
All items
Locked
Footprints
Text
Tracks
Vias
Pads
Zones
Dimensions
Pads 136
Vias 317
Track Segments 209
Nets 36
Unrouted 0
Z 0.73 X 187.1000 Y -52.4100 dx 187.1000 dy -52.4100 dist 194.3019 grid X 0.0100 Y 0.0100 mm
File Edit View Place Inspect Tools Preferences Help
tzmann Main Board
Analog Multiplier
Power LEDs
ERC Attributes
Mount Holes
Z 0.79 X 0.0000 Y 0.0000 dx 0.0000 dy 0.0000 dist 0.0000 grid 0.6350 mm

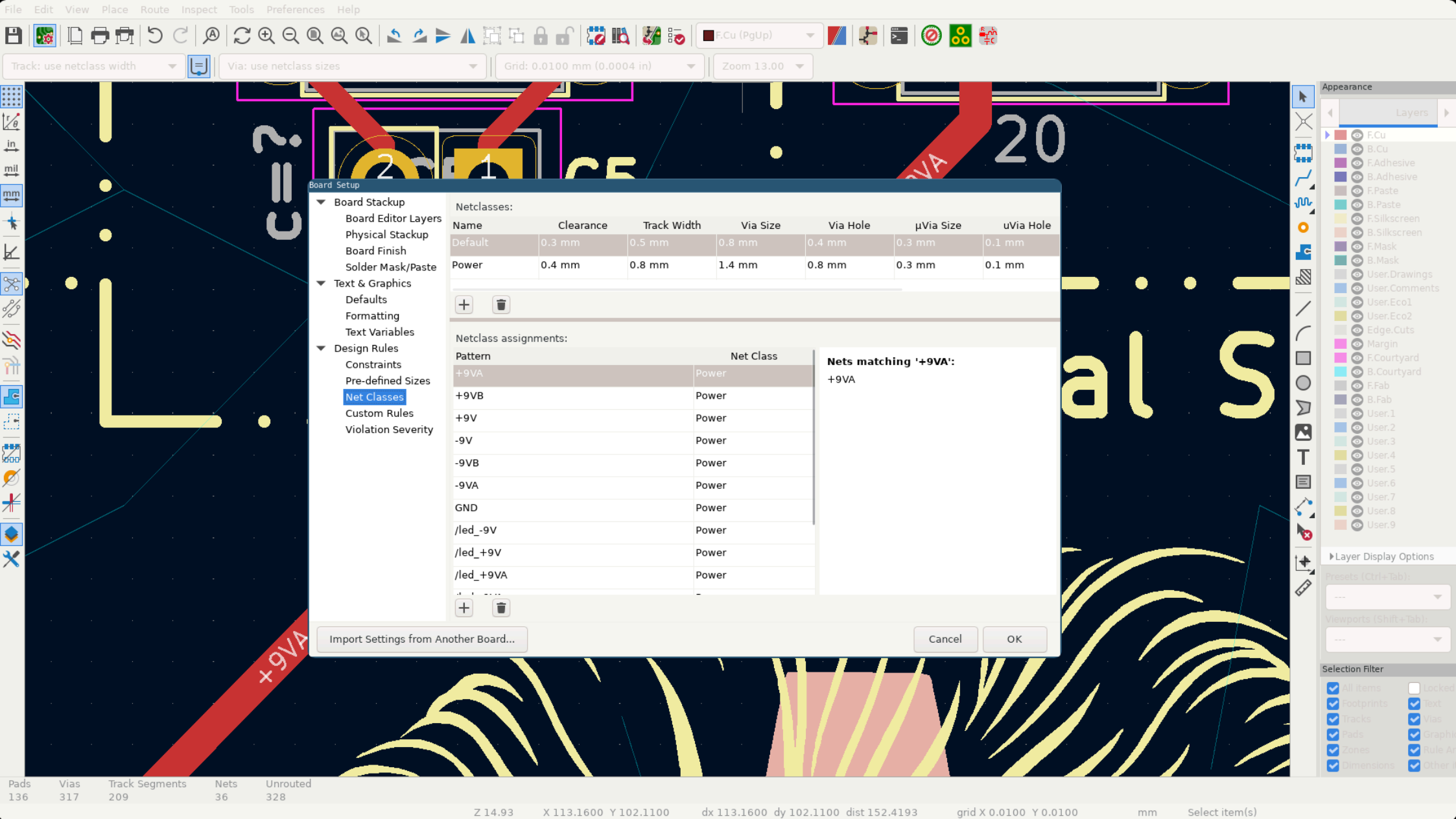

File Edit View Place Route Inspect Tools Preferences Help
Track: use netclass width
Via: use netclass sizes
Grid: 0.0100 mm (0.0004 in)
Appearance
Layers
F.Cu
B.Cu
F.Adhesive
B.Adhesive
F.Paste
B.Paste
F.Silkscreen
B.Silkscreen
F.Mask
B.Mask
User.Drawings
User.Comments
User.Eco1
User.Eco2
Edge.Cuts
Margin
F.Courtyard
B.Courtyard
F.Fab
B.Fab
User.1
User.2
User.3
User.4
User.5
User.6
User.7
User.8
Layer Display Options
Presets (Ctrl+Tab):
All Layers
Viewports (Shift+Tab):

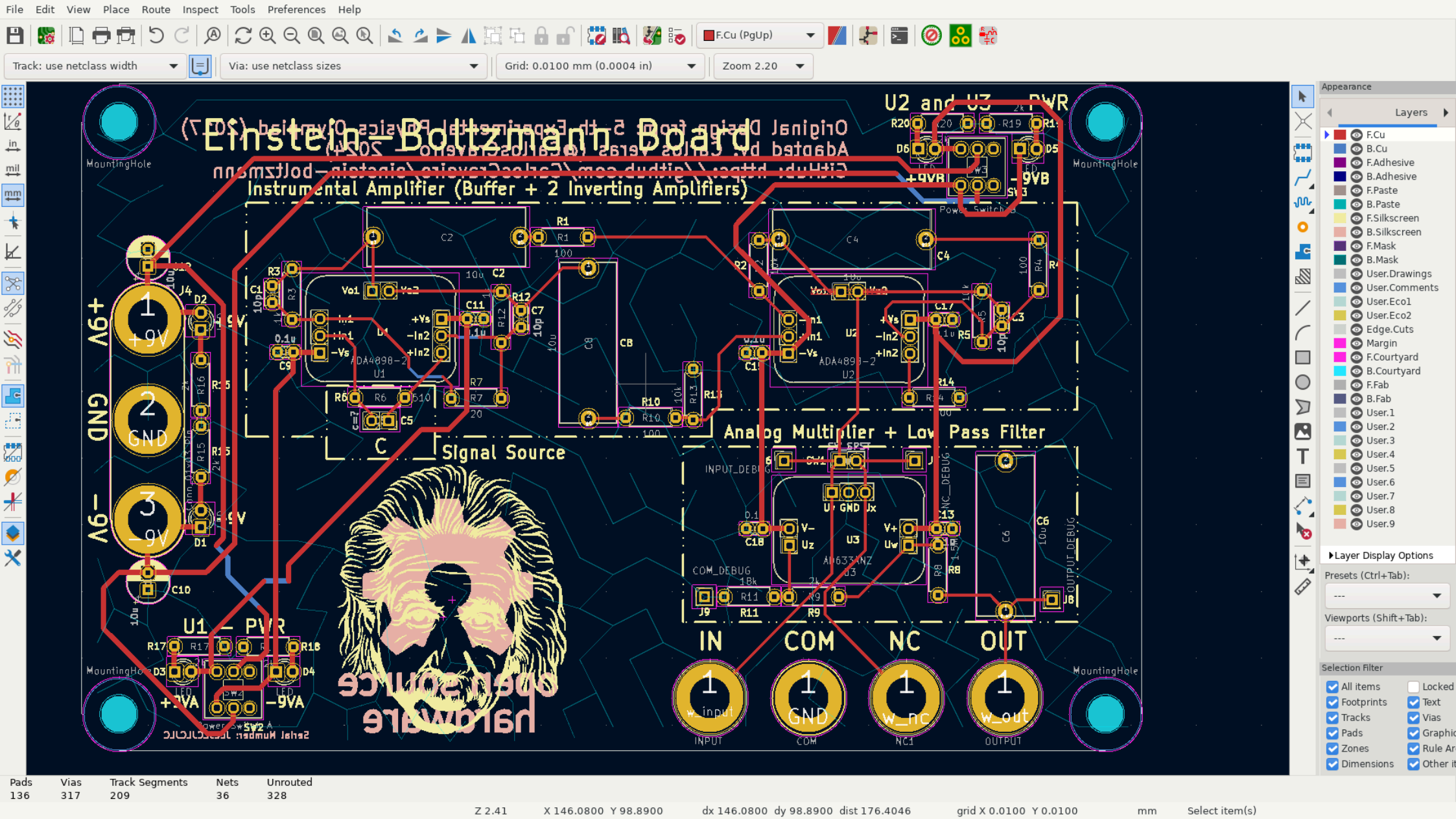
Selection Filter
All items
Locked
Footprints
Text
Tracks
Vias
Pads
Graphic
Zones
Rule Ar
Dimensions
Other it
Selected Items
61
Z 0.61
X 186.9300 Y 122.1000
dx 186.9300 dy 122.1000 dist 223.2739
grid X 0.0100 Y 0.0100
mm

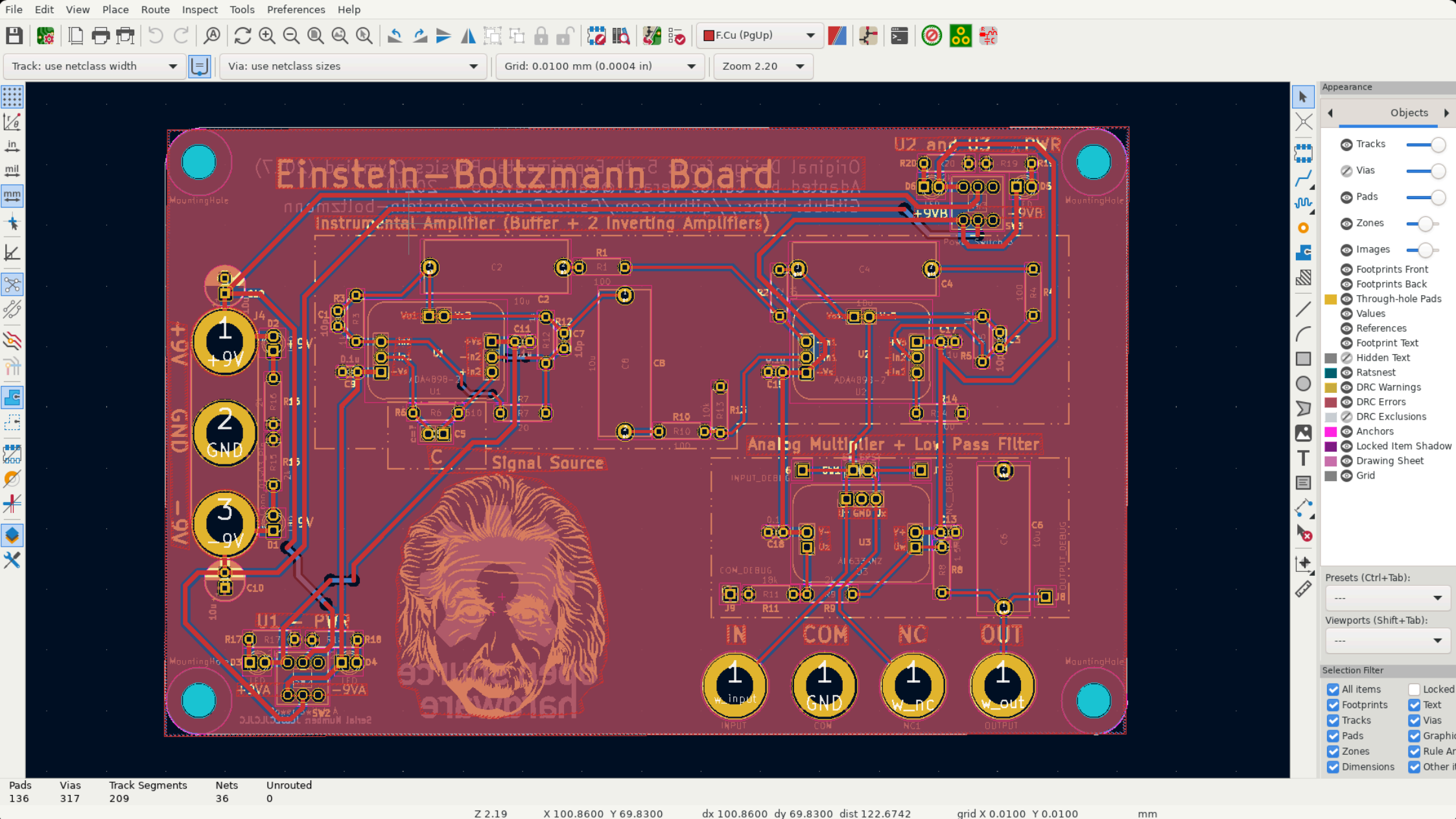

File Edit View Place Inspect Tools Preferences Help
Einstein–Boltzmann Main Board
Signal Source
Instrumental Amplifier (Buffer 4_2 Inverting Amplifiers)
Analog Multiplier
Power Source
ERC Attributes
Power LEDs
Mount Holes
Z 0.79
X 0.0000 Y 0.0000
dx 0.0000 dy 0.0000 dist 0.0000
grid 0.6350
mm

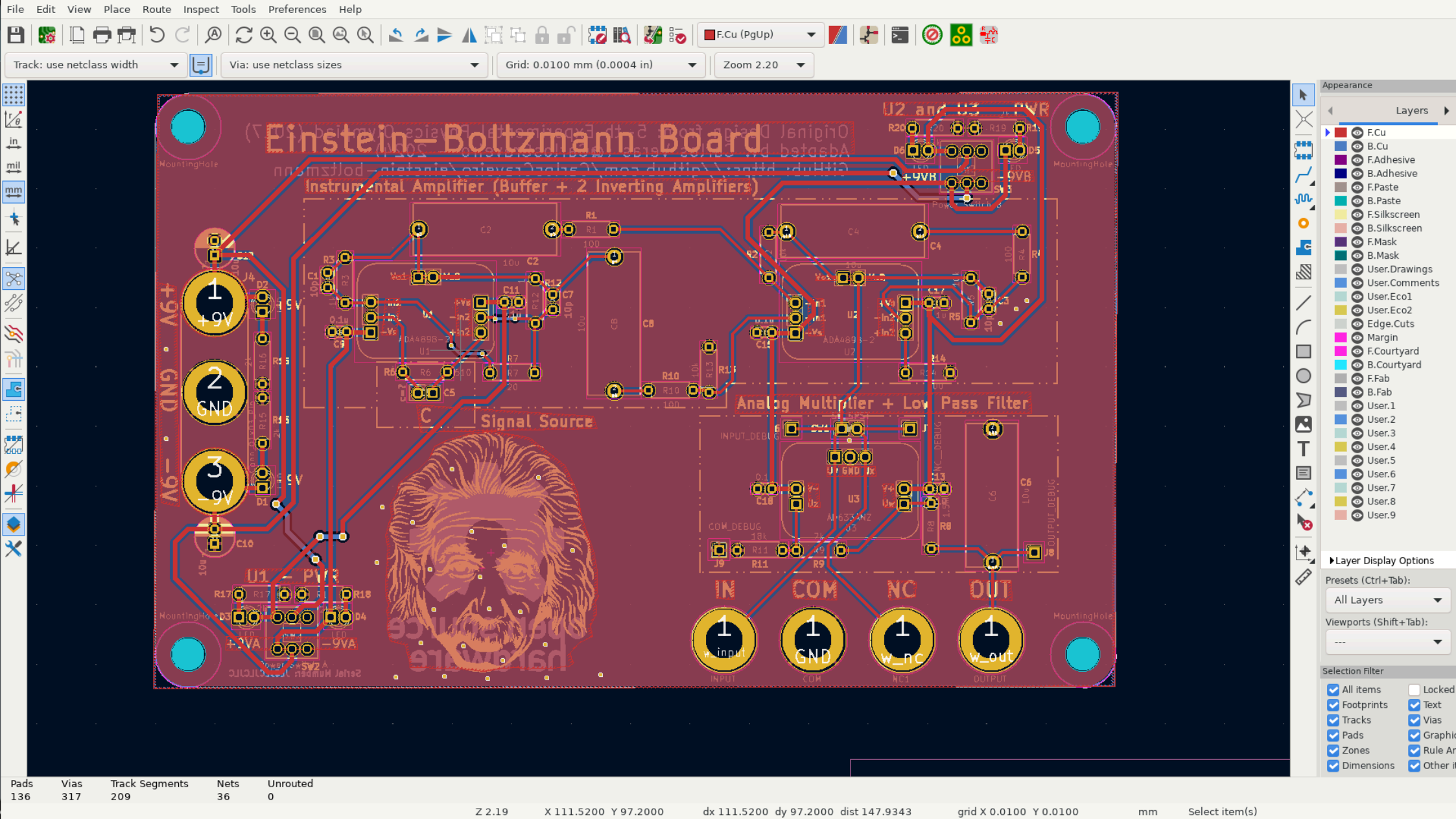

File Edit View Place Route Inspect Tools Preferences Help
F.Cu (PgUp)
Track: use netclass width
Via: use netclass sizes
Grid: 0.0100 mm (0.0004 in)
Zoom 2.20
MountingHole
MountingHole
MountingHole
MountingHole
+9V
GND
-9V
Conn_01x03_Pin
C2
R1
100
10u
ADA4898-2
U1
R3
1k
10p
0.1u
R12
R6
510
R7
20
C7
C8
R10
100
R13
10k
C4
R2
1.6k
100
ADA4898-2
U2
R5
10k
0.1u
10p
R4
100
R14
100
R20
R19
2k
LED
LED
SW3
Power Switch B
R16
2k
R15
2k
LED
10u
R17
R18
LED
LED
SW2
Power Switch A
SW_SPST
INPUT_DEBUG
0.1u
AD633ANZ
U3
NC_DEBUG
R8
1.5M
COM_DEBUG
18k
R11
2k
R9
C6
10u
OUTPUT_DEBUG
W_input
INPUT
GND
COM
W_nc
NC1
W_out
OUTPUT
Appearance
Layers
F.Cu
B.Cu
F.Adhesive
B.Adhesive
F.Paste
B.Paste
F.Silkscreen
B.Silkscreen
F.Mask
B.Mask
User.Drawings
User.Comments
User.Eco1
User.Eco2
Edge.Cuts
Margin
F.Courtyard
B.Courtyard
F.Fab
B.Fab
User.1
User.2
User.3
User.4
User.5
User.6
User.7
User.8
User.9
Layer Display Options
Presets (Ctrl+Tab):
Viewports (Shift+Tab):
Selection Filter
All items
Locked
Footprints
Text
Tracks
Vias
Pads
Graphic
Zones
Rule Ar
Dimensions
Other it
Pads 136
Vias 317
Track Segments 209
Nets 36
Unrouted 0
Z 2.19
X 77.2900 Y 68.0200
dx 77.2900 dy 68.0200 dist 102.9586
grid X 0.0100 Y 0.0100
mm


File Edit View Place Route Inspect Tools Preferences Help
F.Cu (PgUp)
Track: use netclass width
Via: use netclass sizes
Grid: 0.0100 mm (0.0004 in)
Zoom 2.20
Einstein-Boltzmann Board
Instrumental Amplifier (Buffer + 2 Inverting Amplifiers)
U2 and U3 – PWR
Power Switch B
Analog Multiplier + Low Pass Filter
Signal Source
U1 – PWR
MountingHole
+9V
GND
-9V
IN
COM
NC
OUT
w_input
w_nc
w_out
ADA4898-2
AD633ANZ
Appearance
Layers
F.Cu
B.Cu
F.Adhesive
B.Adhesive
F.Paste
B.Paste
F.Silkscreen
B.Silkscreen
F.Mask
B.Mask
User.Drawings
User.Comments
User.Eco1
User.Eco2
Edge.Cuts
Margin
F.Courtyard
B.Courtyard
F.Fab
B.Fab
User.1
User.2
User.3
User.4
User.5
User.6
User.7
User.8
User.9
Layer Display Options
Presets (Ctrl+Tab):
Viewports (Shift+Tab):
Selection Filter
All items
Footprints
Tracks
Pads
Zones
Dimensions
Locked
Text
Vias
Graphic
Rule Ar
Other it
Pads 136
Vias 317
Track Segments 209
Nets 36
Unrouted 0
Z 2.19
X 236.2200 Y 103.8000
dx 236.2200 dy 103.8000 dist 258.0200
grid X 0.0100 Y 0.0100
mm
Select item(s)


Board Setup
Board Stackup
Board Editor Layers
Physical Stackup
Board Finish
Solder Mask/Paste
Text & Graphics
Defaults
Formatting
Text Variables
Design Rules
Constraints
Pre-defined Sizes
Net Classes
Custom Rules
Violation Severity
Netclasses:
Name Clearance Track Width Via Size Via Hole µVia Size uVia Hole
Default 0.3 mm 0.5 mm 0.8 mm 0.4 mm 0.3 mm 0.1 mm
Power 0.4 mm 0.8 mm 1.4 mm 0.8 mm 0.3 mm 0.1 mm
Netclass assignments:
Pattern Net Class
+9VA Power
+9VB Power
+9V Power
-9V Power
-9VB Power
-9VA Power
GND Power
/led_-9V Power
/led_+9V Power
/led_+9VA Power
Nets matching '+9VA':
+9VA
Import Settings from Another Board...
Cancel
OK
+9VA
Appearance
Layers
F.Cu
B.Cu
F.Adhesive
B.Adhesive
F.Paste
B.Paste
F.Silkscreen
B.Silkscreen
F.Mask
B.Mask
User.Drawings
User.Comments
User.Eco1
User.Eco2
Edge.Cuts
Margin
F.Courtyard
B.Courtyard
F.Fab
B.Fab
User.1
User.2
User.3
User.4
User.5
User.6
User.7
User.8
User.9
Layer Display Options
Selection Filter
Pads 136
Vias 317
Track Segments 209
Nets 36
Unrouted 328
Z 14.93
X 113.1600 Y 102.1100
dx 113.1600 dy 102.1100 dist 152.4193
grid X 0.0100 Y 0.0100
mm
Select item(s)


File Edit View Place Route Inspect Tools Preferences Help
F.Cu (PgUp)
Track: use netclass width
Via: use netclass sizes
Grid: 0.0100 mm (0.0004 in)
Zoom 2.20
Einstein-Boltzmann Board
Instrumental Amplifier (Buffer + 2 Inverting Amplifiers)
U2 and U3 - PWR
Analog Multiplier + Low Pass Filter
Signal Source
U1 - PWR
+9V
GND
-9V
IN
COM
NC
OUT
MountingHole
Appearance
Layers
F.Cu
B.Cu
F.Adhesive
B.Adhesive
F.Paste
B.Paste
F.Silkscreen
B.Silkscreen
F.Mask
B.Mask
User.Drawings
User.Comments
User.Eco1
User.Eco2
Edge.Cuts
Margin
F.Courtyard
B.Courtyard
F.Fab
B.Fab
User.1
User.2
User.3
User.4
User.5
User.6
User.7
User.8
User.9
Layer Display Options
Presets (Ctrl+Tab):
Viewports (Shift+Tab):
Selection Filter
All items
Footprints
Tracks
Pads
Zones
Dimensions
Locked
Text
Vias
Graphic
Rule Ar
Other it
Pads 136
Vias 317
Track Segments 209
Nets 36
Unrouted 328
Z 2.41
X 146.0800 Y 98.8900
dx 146.0800 dy 98.8900 dist 176.4046
grid X 0.0100 Y 0.0100
mm
Select item(s)


File Edit View Place Route Inspect Tools Preferences Help
F.Cu (PgUp)
Track: use netclass width
Via: use netclass sizes
Grid: 0.0100 mm (0.0004 in)
Zoom 2.20
Einstein–Boltzmann Board
Instrumental Amplifier (Buffer + 2 Inverting Amplifiers)
U2 and U3 PWR
+9VBI
-9VB
Signal Source
Analog Multiplier + Low Pass Filter
+9V
GND
-9V
IN
COM
NC
OUT
w_input
GND
w_nc
w_out
Appearance
Objects
Tracks
Vias
Pads
Zones
Images
Footprints Front
Footprints Back
Through-hole Pads
Values
References
Footprint Text
Hidden Text
Ratsnest
DRC Warnings
DRC Errors
DRC Exclusions
Anchors
Locked Item Shadow
Drawing Sheet
Grid
Presets (Ctrl+Tab):
Viewports (Shift+Tab):
Selection Filter
All items
Footprints
Tracks
Pads
Zones
Dimensions
Locked
Text
Vias
Graphic
Rule Ar
Other it
Pads 136
Vias 317
Track Segments 209
Nets 36
Unrouted 0
Z 2.19
X 100.8600 Y 69.8300
dx 100.8600 dy 69.8300 dist 122.6742
grid X 0.0100 Y 0.0100
mm


File Edit View Place Route Inspect Tools Preferences Help
F.Cu (PgUp)
Track: use netclass width
Via: use netclass sizes
Grid: 0.0100 mm (0.0004 in)
Zoom 2.20
Einstein–Boltzmann Board
Instrumental Amplifier (Buffer + 2 Inverting Amplifiers)
U2 and U3 PWR
Signal Source
Analog Multiplier + Low Pass Filter
U1 - PWR
+9V
GND
-9V
IN
COM
NC
OUT
w_input
GND
w_nc
w_out
Appearance
Layers
F.Cu
B.Cu
F.Adhesive
B.Adhesive
F.Paste
B.Paste
F.Silkscreen
B.Silkscreen
F.Mask
B.Mask
User.Drawings
User.Comments
User.Eco1
User.Eco2
Edge.Cuts
Margin
F.Courtyard
B.Courtyard
F.Fab
B.Fab
User.1
User.2
User.3
User.4
User.5
User.6
User.7
User.8
User.9
Layer Display Options
Presets (Ctrl+Tab):
All Layers
Viewports (Shift+Tab):
Selection Filter
All items
Locked
Footprints
Text
Tracks
Vias
Pads
Graphic
Zones
Rule Ar
Dimensions
Other it
Pads 136
Vias 317
Track Segments 209
Nets 36
Unrouted 0
Z 2.19
X 111.5200 Y 97.2000
dx 111.5200 dy 97.2000 dist 147.9343
grid X 0.0100 Y 0.0100
mm
Select item(s)

KiCAD Addons

- Python plugins (Automate tasks and Add new capabilities)
- Content libraries (Shared 3rd party footprints, 3D models and symbols)
- Color themes (More customization options)

```
Aug 17, 19:25]
└─[$] <git:(main)> ssh-add ~/.ssh/github
Enter passphrase for /home/coveiro/.ssh/github:
Identity added: /home/coveiro/.ssh/github (carlos.craveiro@usp.br)
┌─[coveiro roxanne] - [~/Documents/Zedney/einstein-boltzmann] - [Sat Aug 17, 19:25]
└─[$] <git:(main)> git push --force
Enumerating objects: 9, done.
Counting objects: 100% (9/9), done.
Delta compression using up to 12 threads
Compressing objects: 100% (8/8), done.
Writing objects: 100% (8/8), 3.23 MiB | 1.58 MiB/s, done.
Total 8 (delta 1), reused 0 (delta 0), pack-reused 0 (from 0)
remote: Resolving deltas: 100% (1/1), completed with 1 local object.
To github.com:CarlosCraveiro/einstein-boltzmar
 + fc61df7...773ef03 main -> main (forced upda
┌─[coveiro roxanne] - [~/Documents/Zedney/eins
└─[$] <git:(main)> kicad amplifiers/amplifiers
Starting plugin CircularZone
Starting plugin ViaStitching
┌─[coveiro roxanne] - [~/Documents/Zedney/eins
└─[$] <git:(main*)> kicad tension-multiplier/t
Starting plugin CircularZone
Starting plugin ViaStitching
┌─[coveiro roxanne] - [~/Documents/Zedney/eins
└─[$] <git:(main*)> kicad main-board/main-boar
Starting plugin CircularZone
Starting plugin ViaStitching
┌─[coveiro roxanne] - [~/Documents/Zedney/eins
└─[$] <git:(main*)> kicad main-board/main-boar
Starting plugin CircularZone
Starting plugin ViaStitching
*** BUG ***
In pixman_region32_init_rect: Invalid rectangl
Set a breakpoint on '_pixman_log_error' to deb

*** BUG ***
In pixman_region32_init_rect: Invalid rectangl
Set a breakpoint on '_pixman_log_error' to deb

*** BUG ***
In pixman_region32_init_rect: Invalid rectangl
Set a breakpoint on '_pixman_log_error' to deb

Starting plugin CircularZone
Starting plugin ViaStitching
Starting plugin CircularZone
Starting plugin ViaStitching
```

File Edit View Tools Preferences Help

Project Files

- main-board.kicad_pro
  - main-board-backups
  - footprints.pretty
  - gerber_files
  - module_3Dmodels
  - main-board.kicad_dru
  - main-board.kicad_pcb
  - main-board.kicad_sch

Project: /home/coveiro.../main-board.kicad_pro

Schematic Editor — *Edit the project schematic*

Symbol Editor — *Edit global and/or project schematic symbol libraries*

PCB Editor — *Edit the project PCB design*

Footprint Editor — *Edit global and/or project PCB footprint libraries*

Gerber Viewer — *Preview Gerber files*

Image Converter — *Convert bitmap images to schematic symbols or PCB footpr*

Calculator Tools — *Show tools for calculating resistance, current capacity, etc.*

Drawing Sheet Editor — *Edit drawing sheet borders and title blocks for use in schem*

Plugin and Content Manager — *Manage downloadable packages from KiCad and 3rd party*

Plugin And Content Manager

Repository (81) | Installed (3) | Pending (0)

Filter | Update All

Parasitics
Plugin to analyze the wires in the PCB editor.
Uninstall

Arcana
A dark and vibrant color scheme by @lethalbit
Uninstall

kicad-action-scripts
ViaStitching and more tools
Uninstall

kicad-action-scripts

Via stitching action tool and circular zone builder action tool. Use the action menu/toolbar feature.

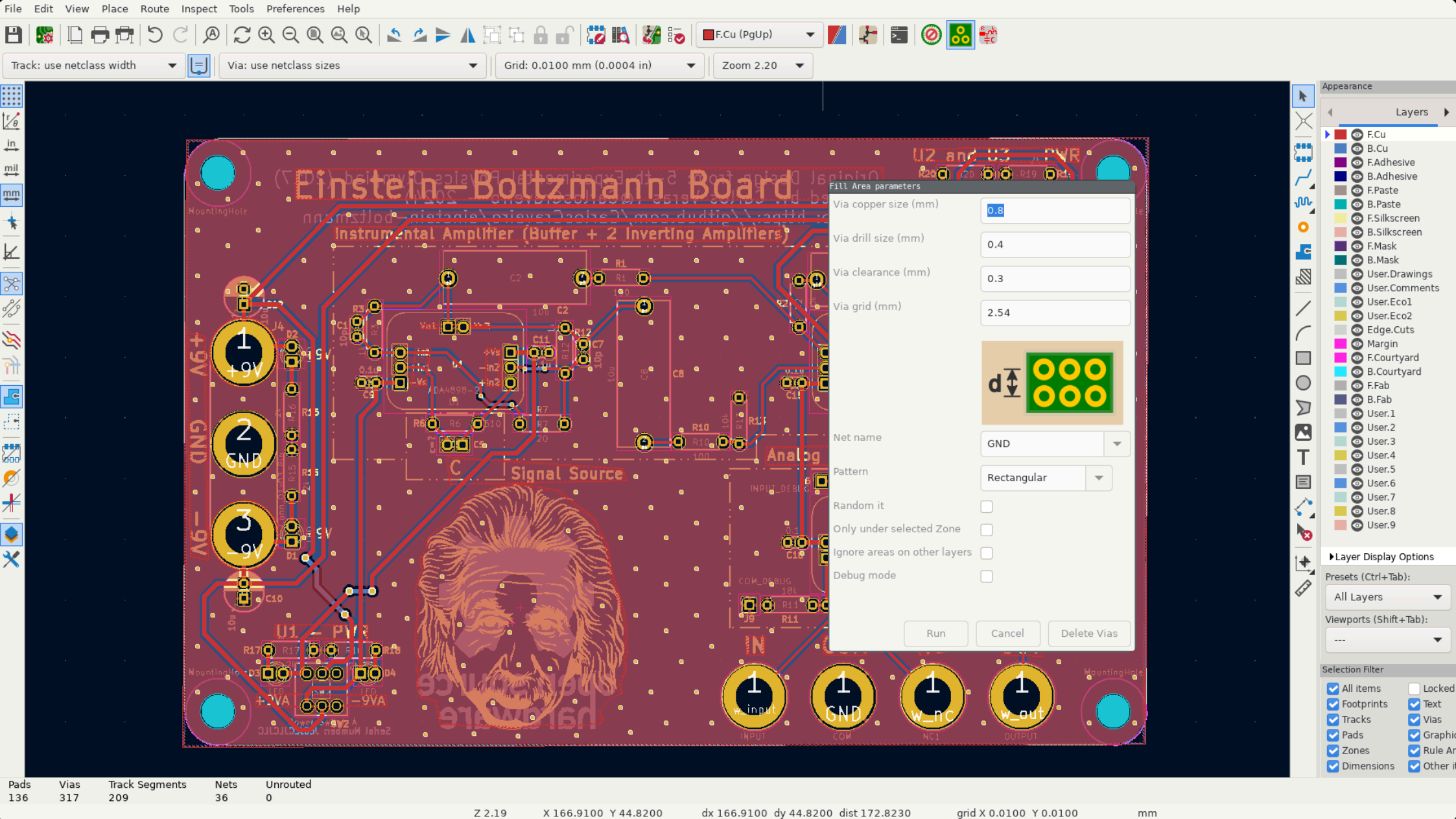
Metadata

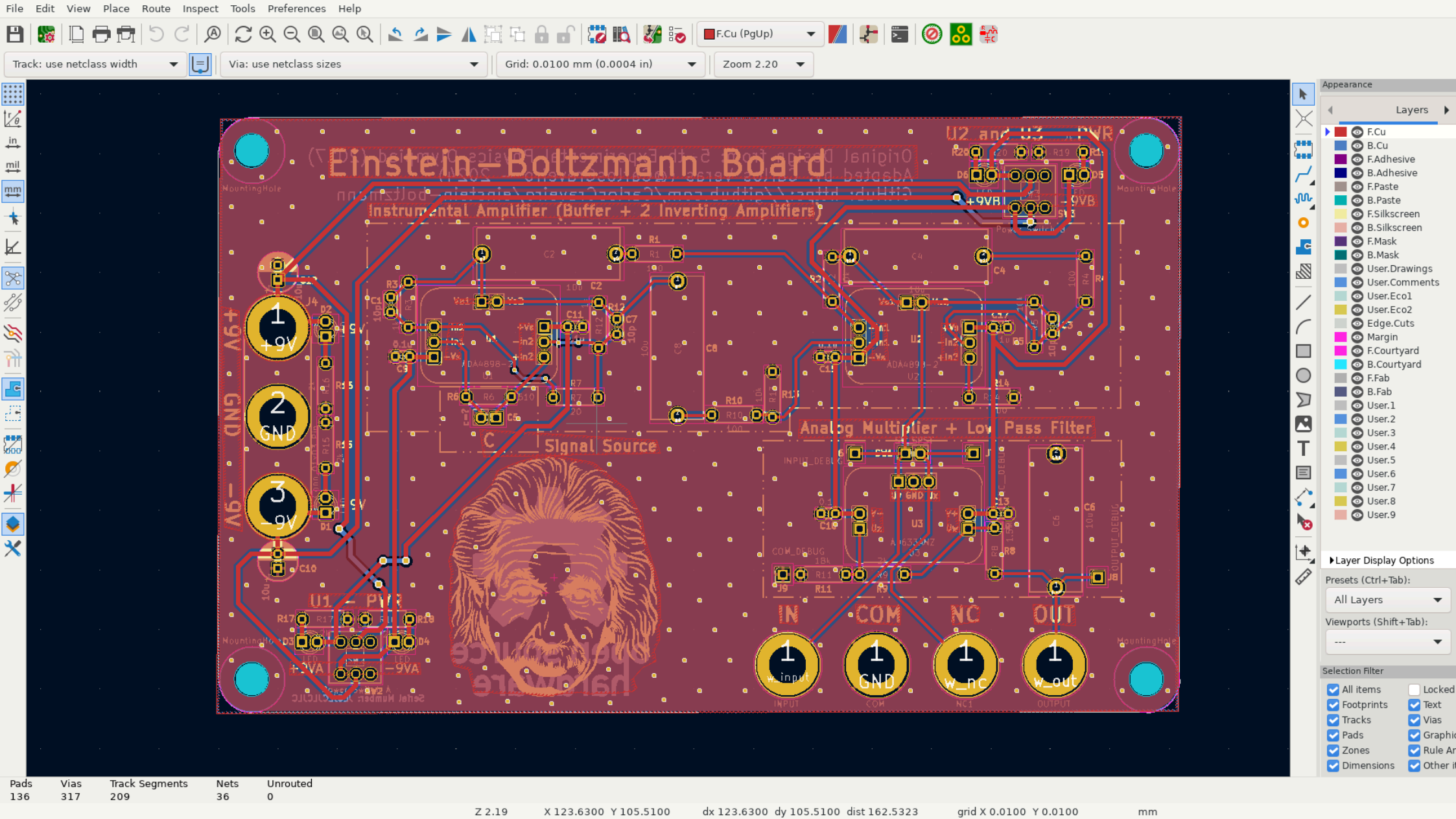
- Package identifier: com.github.jsreynaud.kicad-action-scripts
- License: GPL-2.0
- Tags: annular, pcbnew, dxf, grid, mcad
- Author: jsreynaud
  - email: js.reynaud@gmail.com
- Resources
  - Github: https://github.com/jsreynaud/kicad-action-scripts
  - Readme: https://github.com/jsreynaud/kicad-action-scripts/blob/master/READM

Version	Download Size	Install Size	Compatible	Status
7.0.4	51 kB	288 kB	✓	stable
7.0.3	51 kB	276 kB	✓	stable

Show all versions | Download | Uninstall

Refresh | Install from File... | Open Package Directory | Apply Pending Changes | Discard Pending Changes | Close

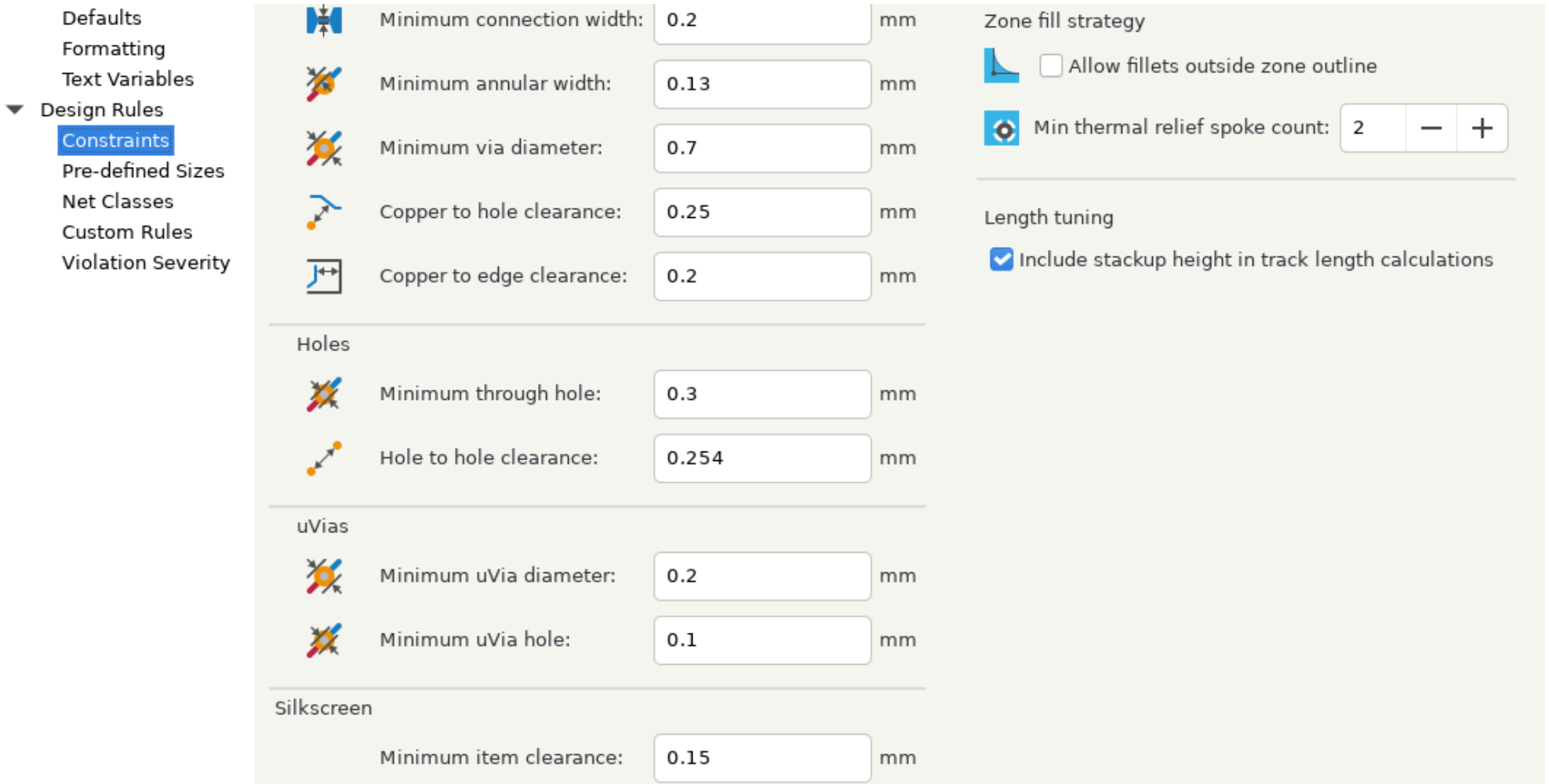

File Edit View Place Route Inspect Tools Preferences Help
F.Cu (PgUp)
Track: use netclass width
Via: use netclass sizes
Grid: 0.0100 mm (0.0004 in)
Zoom 2.20
Einstein–Boltzmann Board
Instrumental Amplifier (Buffer + 2 Inverting Amplifiers)
Signal Source
Analog
+9V
GND
-9V
+3VA
-9VA
w_input
w_nc
w_out
Fill Area parameters
Via copper size (mm)
0.8
Via drill size (mm)
0.4
Via clearance (mm)
0.3
Via grid (mm)
2.54
Net name
GND
Pattern
Rectangular
Random it
Only under selected Zone
Ignore areas on other layers
Debug mode
Run
Cancel
Delete Vias
Appearance
Layers
F.Cu
B.Cu
F.Adhesive
B.Adhesive
F.Paste
B.Paste
F.Silkscreen
B.Silkscreen
F.Mask
B.Mask
User.Drawings
User.Comments
User.Eco1
User.Eco2
Edge.Cuts
Margin
F.Courtyard
B.Courtyard
F.Fab
B.Fab
User.1
User.2
User.3
User.4
User.5
User.6
User.7
User.8
User.9
Layer Display Options
Presets (Ctrl+Tab):
All Layers
Viewports (Shift+Tab):
Selection Filter
All items
Locked
Footprints
Text
Tracks
Vias
Pads
Graphic
Zones
Rule Ar
Dimensions
Other it
Pads 136
Vias 317
Track Segments 209
Nets 36
Unrouted 0
Z 2.19
X 166.9100 Y 44.8200
dx 166.9100 dy 44.8200 dist 172.8230
grid X 0.0100 Y 0.0100
mm

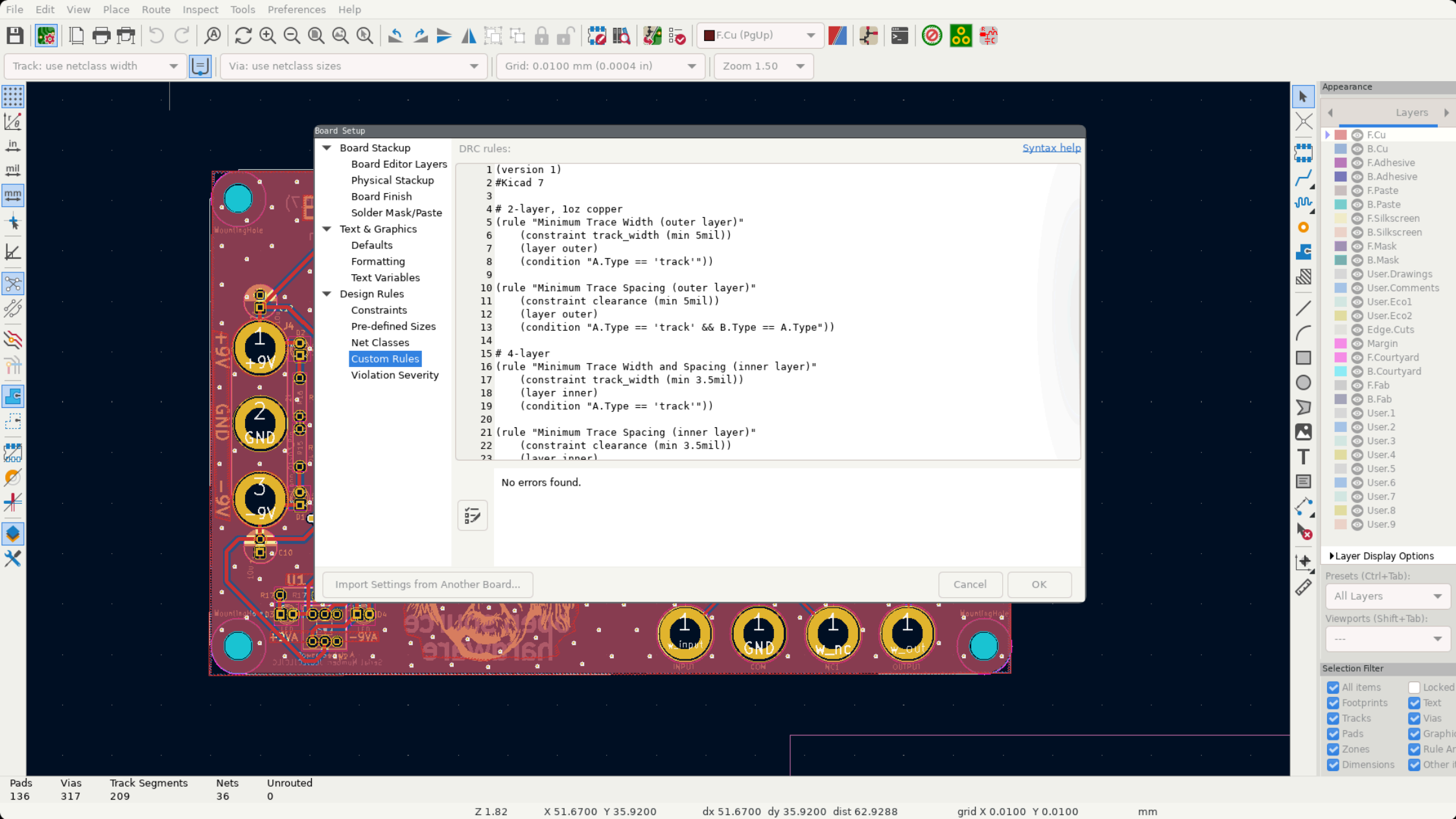

File Edit View Place Route Inspect Tools Preferences Help
F.Cu (PgUp)
Track: use netclass width
Via: use netclass sizes
Grid: 0.0100 mm (0.0004 in)
Zoom 2.20
Einstein–Boltzmann Board
Instrumental Amplifier (Buffer + 2 Inverting Amplifiers)
U2 and U3 PWR
Signal Source
Analog Multiplier + Low Pass Filter
U1 – PWR
+9V
GND
-9V
IN
COM
NC
OUT
w_input
w_nc
w_out
Appearance
Layers
F.Cu
B.Cu
F.Adhesive
B.Adhesive
F.Paste
B.Paste
F.Silkscreen
B.Silkscreen
F.Mask
B.Mask
User.Drawings
User.Comments
User.Eco1
User.Eco2
Edge.Cuts
Margin
F.Courtyard
B.Courtyard
F.Fab
B.Fab
User.1
User.2
User.3
User.4
User.5
User.6
User.7
User.8
User.9
Layer Display Options
Presets (Ctrl+Tab):
All Layers
Viewports (Shift+Tab):
Selection Filter
All items
Locked
Footprints
Text
Tracks
Vias
Pads
Graphic
Zones
Rule Ar
Dimensions
Other it
Pads 136
Vias 317
Track Segments 209
Nets 36
Unrouted 0
Z 2.19
X 123.6300 Y 105.5100
dx 123.6300 dy 105.5100 dist 162.5323
grid X 0.0100 Y 0.0100
mm

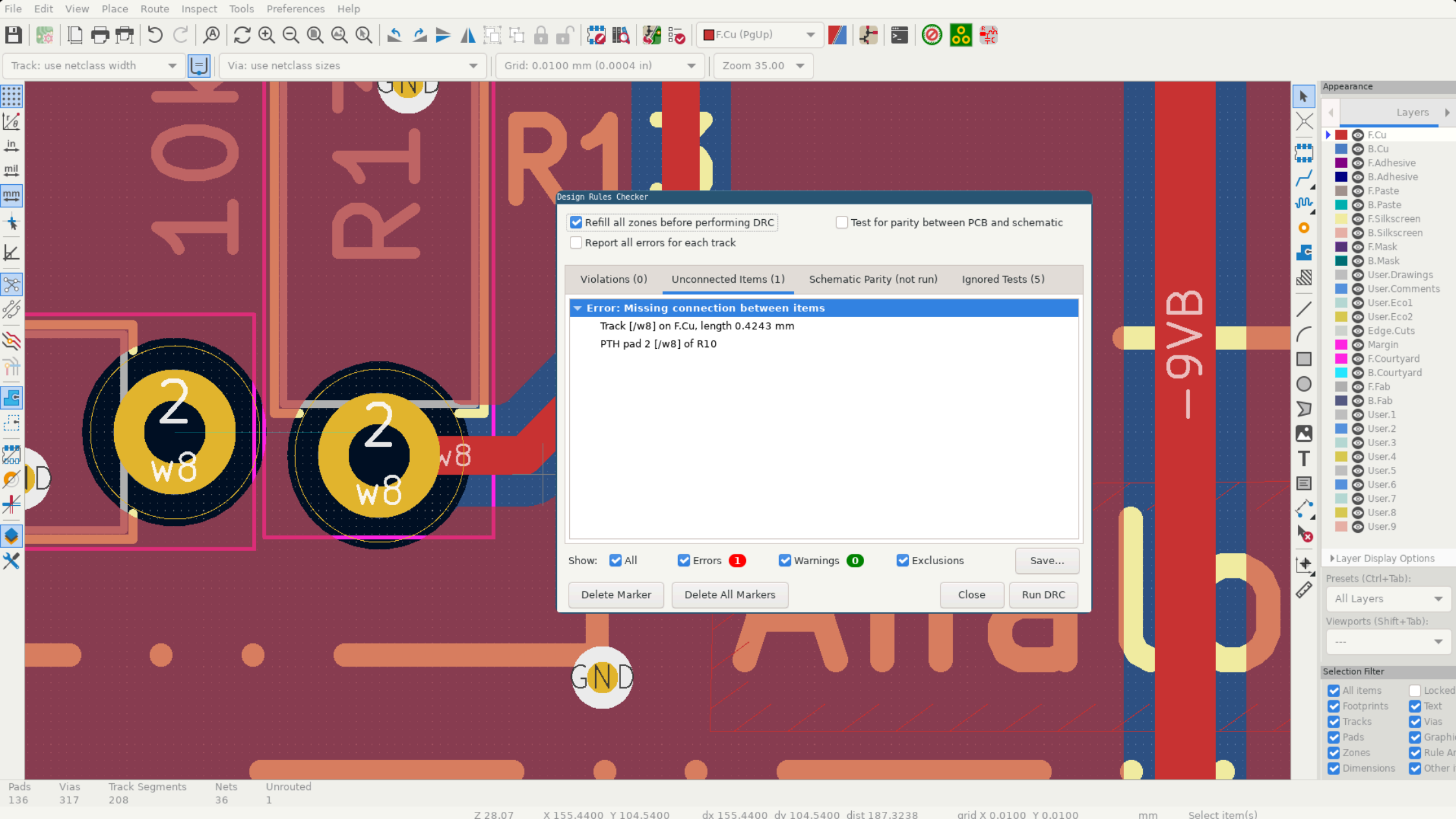
Design Rule Checking

- Geometric constraint imposed on circuit board
- Reflects the capability of the manufacture fabrication processes
- Major step during physical verification signoff on the design
- Also involves LVS (layout versus schematic) and ERC

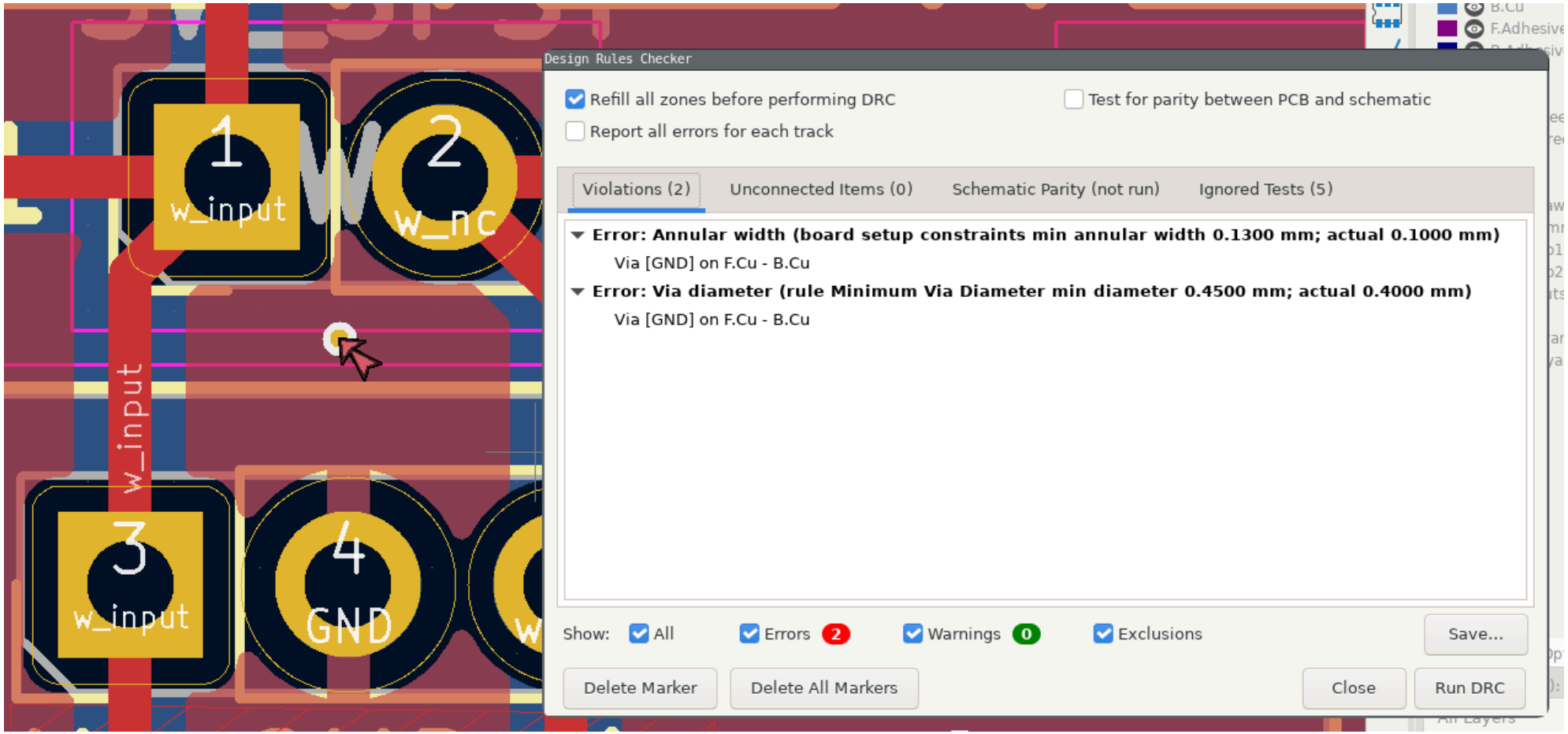
Design Rules Constraints UI




File Edit View Place Route Inspect Tools Preferences Help
Track: use netclass width
Via: use netclass sizes
Grid: 0.0100 mm (0.0004 in)
Zoom 1.50
F.Cu (PgUp)
Board Setup
Board Stackup
Board Editor Layers
Physical Stackup
Board Finish
Solder Mask/Paste
Text & Graphics
Defaults
Formatting
Text Variables
Design Rules
Constraints
Pre-defined Sizes
Net Classes
Custom Rules
Violation Severity
DRC rules:
Syntax help
1 (version 1)
2 #Kicad 7
3
4 # 2-layer, 1oz copper
5 (rule "Minimum Trace Width (outer layer)"
6 (constraint track_width (min 5mil))
7 (layer outer)
8 (condition "A.Type == 'track'"))
9
10 (rule "Minimum Trace Spacing (outer layer)"
11 (constraint clearance (min 5mil))
12 (layer outer)
13 (condition "A.Type == 'track' && B.Type == A.Type"))
14
15 # 4-layer
16 (rule "Minimum Trace Width and Spacing (inner layer)"
17 (constraint track_width (min 3.5mil))
18 (layer inner)
19 (condition "A.Type == 'track'"))
20
21 (rule "Minimum Trace Spacing (inner layer)"
22 (constraint clearance (min 3.5mil))
23 (layer inner)
No errors found.
Import Settings from Another Board...
Cancel
OK
Appearance
Layers
F.Cu
B.Cu
F.Adhesive
B.Adhesive
F.Paste
B.Paste
F.Silkscreen
B.Silkscreen
F.Mask
B.Mask
User.Drawings
User.Comments
User.Eco1
User.Eco2
Edge.Cuts
Margin
F.Courtyard
B.Courtyard
F.Fab
B.Fab
User.1
User.2
User.3
User.4
User.5
User.6
User.7
User.8
User.9
Layer Display Options
Presets (Ctrl+Tab):
All Layers
Viewports (Shift+Tab):
Selection Filter
All items
Locked
Footprints
Text
Tracks
Vias
Pads
Graphic
Zones
Rule Ar
Dimensions
Other it
+9V
GND
-9V
+9VA
-9VA
U1
INPUT
COM
NC1
OUTPUT
Pads 136
Vias 317
Track Segments 209
Nets 36
Unrouted 0
Z 1.82
X 51.6700 Y 35.9200
dx 51.6700 dy 35.9200 dist 62.9288
grid X 0.0100 Y 0.0100
mm

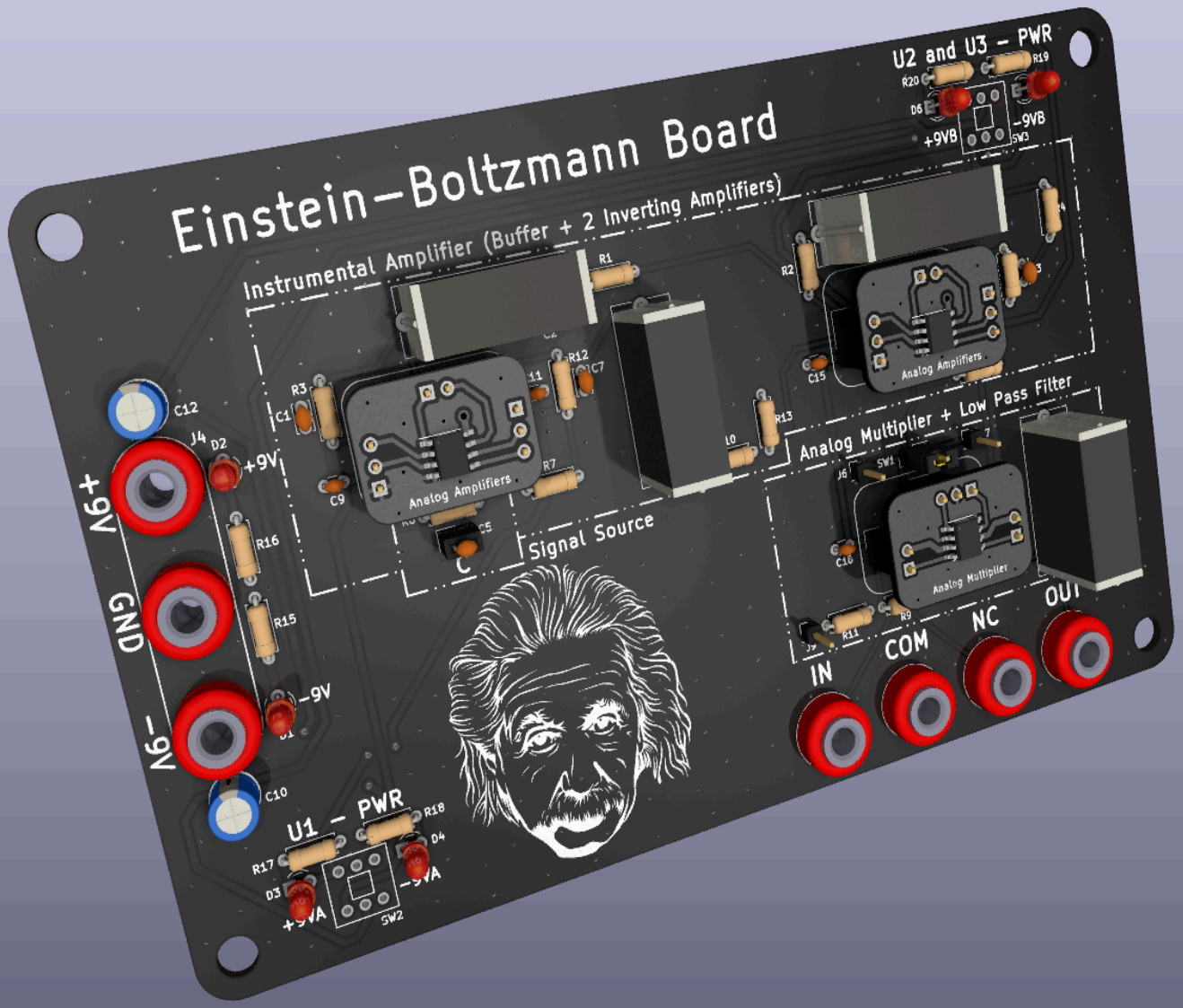

File Edit View Place Route Inspect Tools Preferences Help
F.Cu (PgUp)
Track: use netclass width
Via: use netclass sizes
Grid: 0.0100 mm (0.0004 in)
Zoom 35.00
Design Rules Checker
Refill all zones before performing DRC
Test for parity between PCB and schematic
Report all errors for each track
Violations (0)
Unconnected Items (1)
Schematic Parity (not run)
Ignored Tests (5)
Error: Missing connection between items
Track [/w8] on F.Cu, length 0.4243 mm
PTH pad 2 [/w8] of R10
Show: All Errors 1 Warnings 0 Exclusions
Save...
Delete Marker
Delete All Markers
Close
Run DRC
Appearance
Layers
F.Cu
B.Cu
F.Adhesive
B.Adhesive
F.Paste
B.Paste
F.Silkscreen
B.Silkscreen
F.Mask
B.Mask
User.Drawings
User.Comments
User.Eco1
User.Eco2
Edge.Cuts
Margin
F.Courtyard
B.Courtyard
F.Fab
B.Fab
User.1
User.2
User.3
User.4
User.5
User.6
User.7
User.8
User.9
Layer Display Options
Presets (Ctrl+Tab):
All Layers
Viewports (Shift+Tab):
Selection Filter
All items
Locked
Footprints
Text
Tracks
Vias
Pads
Zones
Dimensions
Pads 136
Vias 317
Track Segments 208
Nets 36
Unrouted 1
Z 28.07
X 155.4400 Y 104.5400
dx 155.4400 dy 104.5400 dist 187.3238
grid X 0.0100 Y 0.0100
mm
Select item(s)

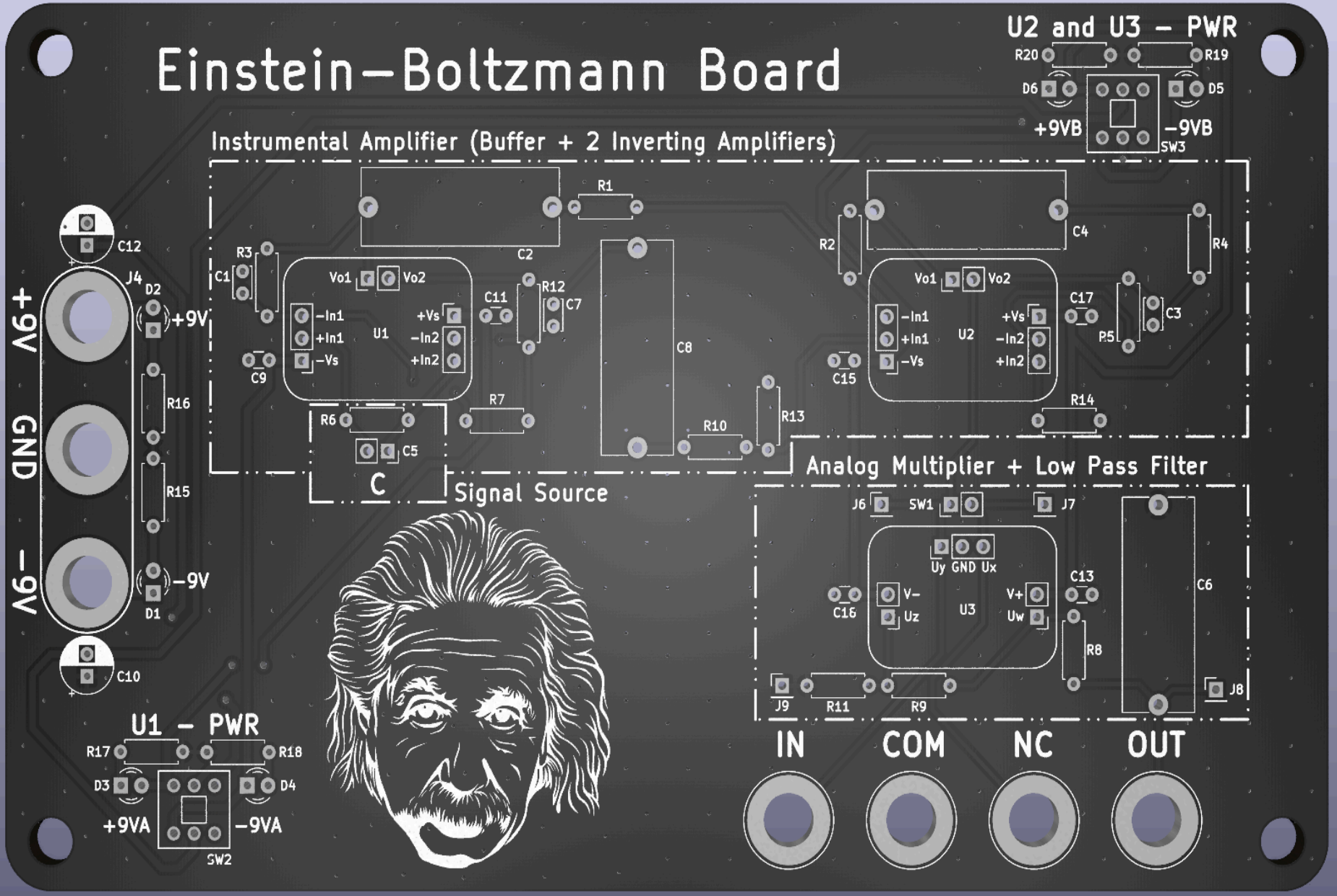
Constraint Violation

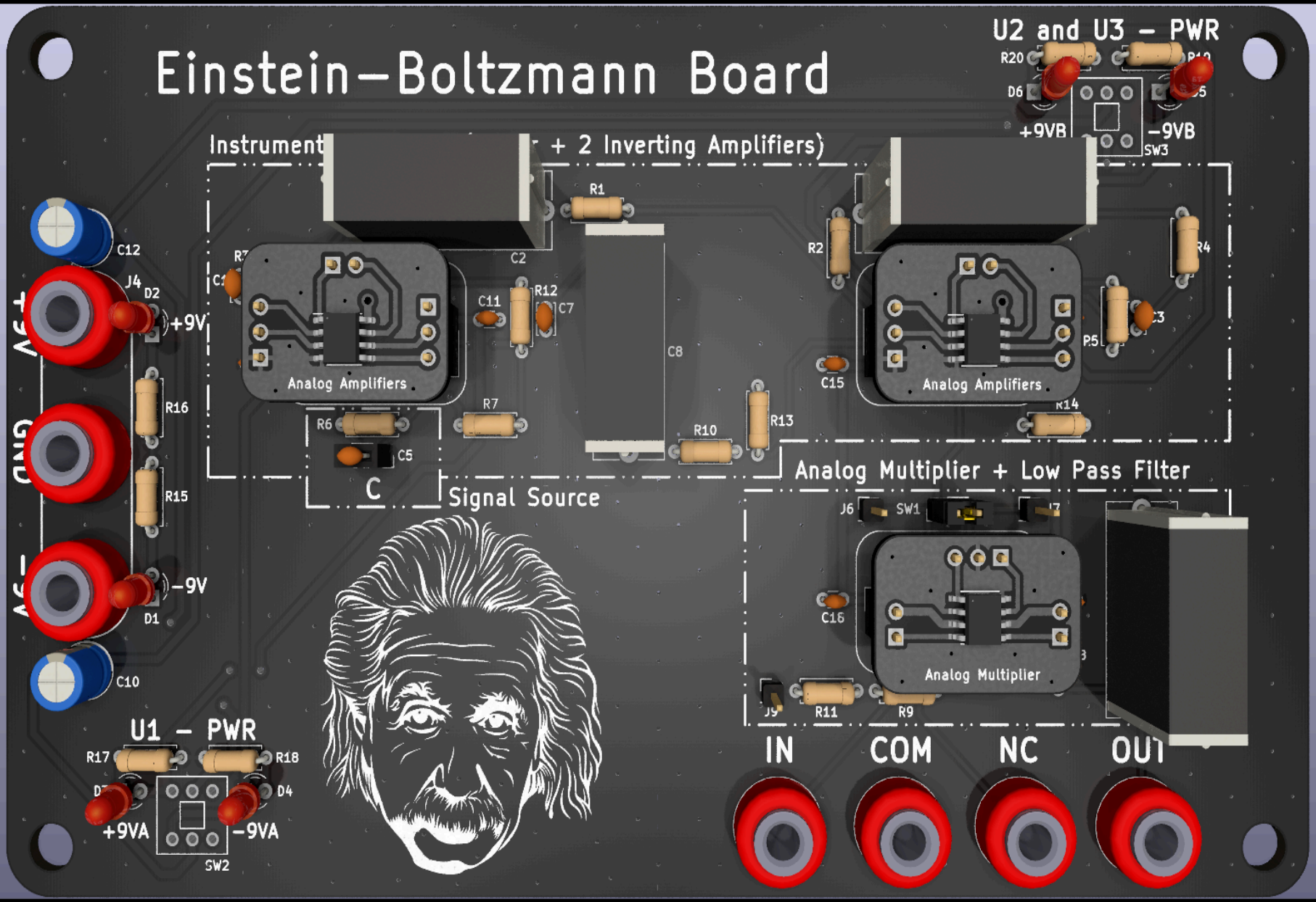


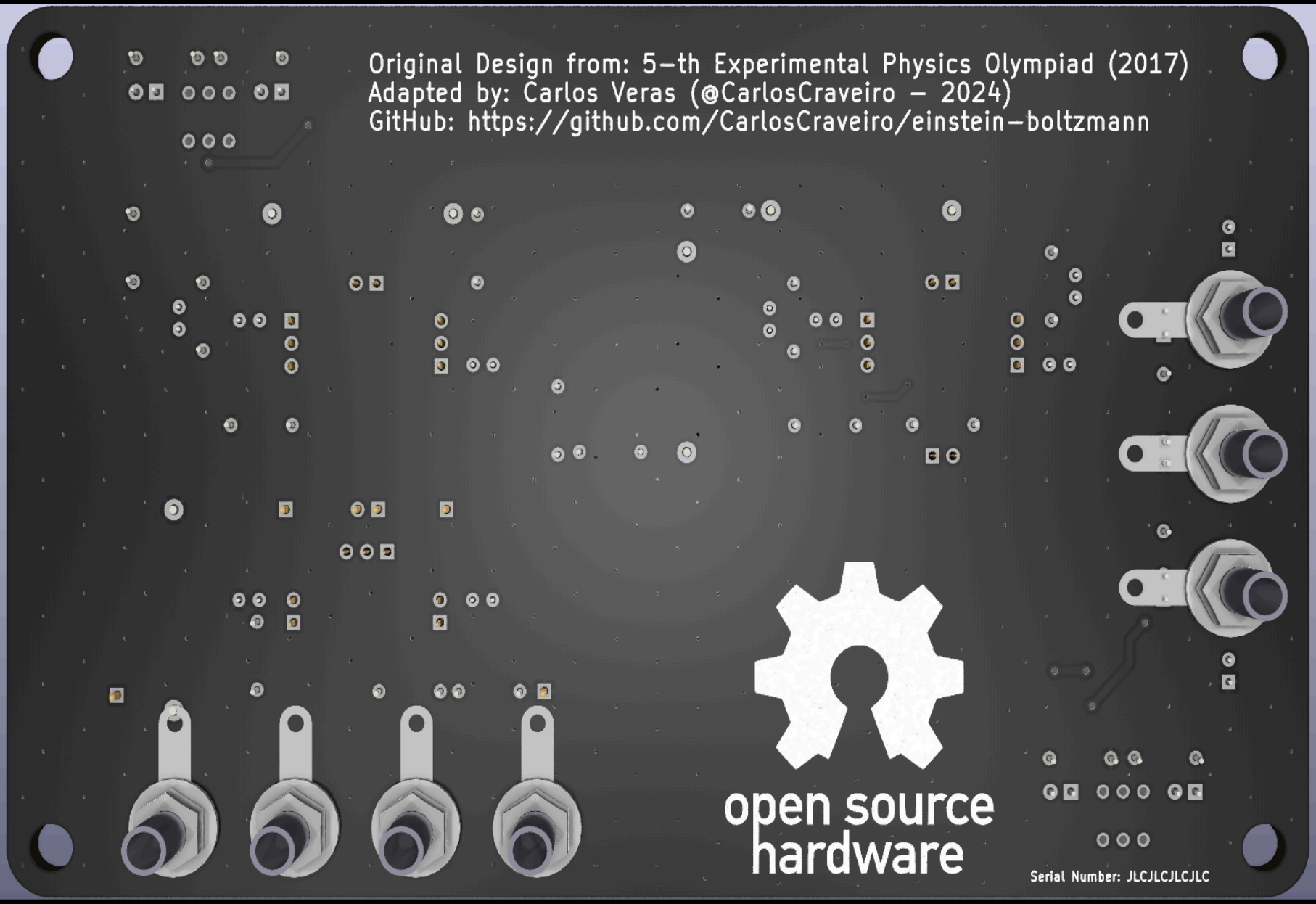
3D Visualization

- OpenGL (GPU accelerated), and ray tracing
- Helps to verify the Design by visual inspection
- Get an idea about how the project may look like when it is finished


Einstein–Boltzmann Board
Instrumental Amplifier (Buffer + 2 Inverting Amplifiers)
Analog Amplifiers
Signal Source
Analog Amplifiers
U2 and U3 – PWR
+9V8
–9V8
Analog Multiplier + Low Pass Filter
Analog Multiplier
+9V
GND
–9V
IN
COM
NC
OUT
U1 – PWR
+9VA
–9VA


Einstein–Boltzmann Board
U2 and U3 – PWR
R20
R19
D6
D5
+9VB
–9VB
SW3
Instrumental Amplifier (Buffer + 2 Inverting Amplifiers)
R1
C2
R3
C1
Vo1
Vo2
–In1
+In1
–Vs
U1
+Vs
–In2
+In2
C11
R12
C7
C8
C9
R6
C5
R7
R10
R13
C
Signal Source
R2
C4
R4
U2
C17
C3
P5
C15
R14
C12
J4
D2
+9V
R16
R15
GND
–9V
D1
C10
Analog Multiplier + Low Pass Filter
J6
SW1
J7
Uy
GND
Ux
V–
Uz
U3
V+
Uw
C16
C13
C6
R8
J9
R11
R9
J8
U1 – PWR
R17
R18
D3
D4
+9VA
–9VA
SW2
IN
COM
NC
OUT


Einstein–Boltzmann Board
U2 and U3 – PWR
+9VB
–9VB
Instrument
+ 2 Inverting Amplifiers)
Analog Amplifiers
Analog Amplifiers
Signal Source
Analog Multiplier + Low Pass Filter
Analog Multiplier
U1 – PWR
+9VA
–9VA
+9V
GND
–9V
+9V
–9V
IN
COM
NC
OUT


Original Design from: 5-th Experimental Physics Olympiad (2017)
Adapted by: Carlos Veras (@CarlosCraveiro - 2024)
GitHub: https://github.com/CarlosCraveiro/einstein-boltzmann
open source hardware
Serial Number: JLCJLCJLCJLC

Issues I faced

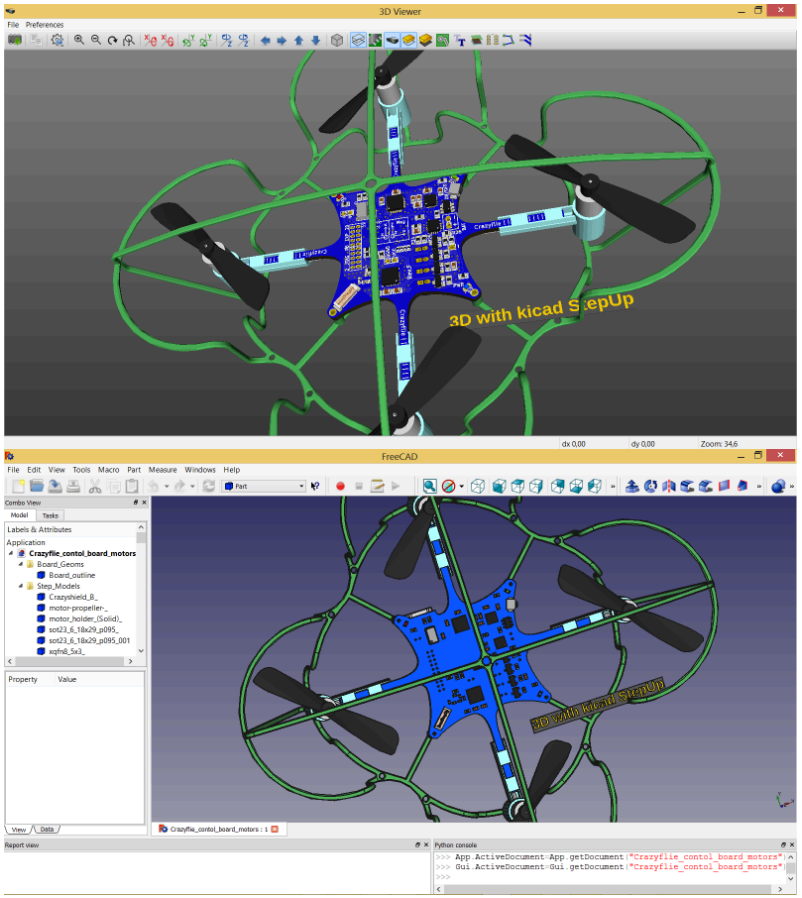
- Multi-project with KiCAD is terrible
- The simulation tool was poor documentaded (KiCAD 7)
- I couldn't simulate my circuit as I wanted
- Customization a bit too laborious (issues with shortcuts)

Future Work

- Check if the board actually works
- Determine the Boltzmann Constant (Have fun with the project!)
- Reduce costs: find cheaper OPAmps, decrease PCB size, ...
- Check for design flaws and possible improvements

Future Work

- Setup a KicadStepUp Workbench at FreeCAD
- Make the simulation work
- Improve project's documentation



References

- 1 - Mishonov, T. M., Petkov, E. G., Stefanov, A. A., & Petkov, A. P. (2018). **Measurement of the Boltzmann constant by Einstein: Problem of the 5th Experimental Physics Olympiad** (Sofia, 9 December 2017). Retrieved from https://arxiv.org/pdf/1801.00022v3

- 2 - Lathi, B. P., Ding, Z. (2009). Modern Digital and Analog Communication Systems. United Kingdom: Oxford University Press.

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