# Homework 02 Code Review

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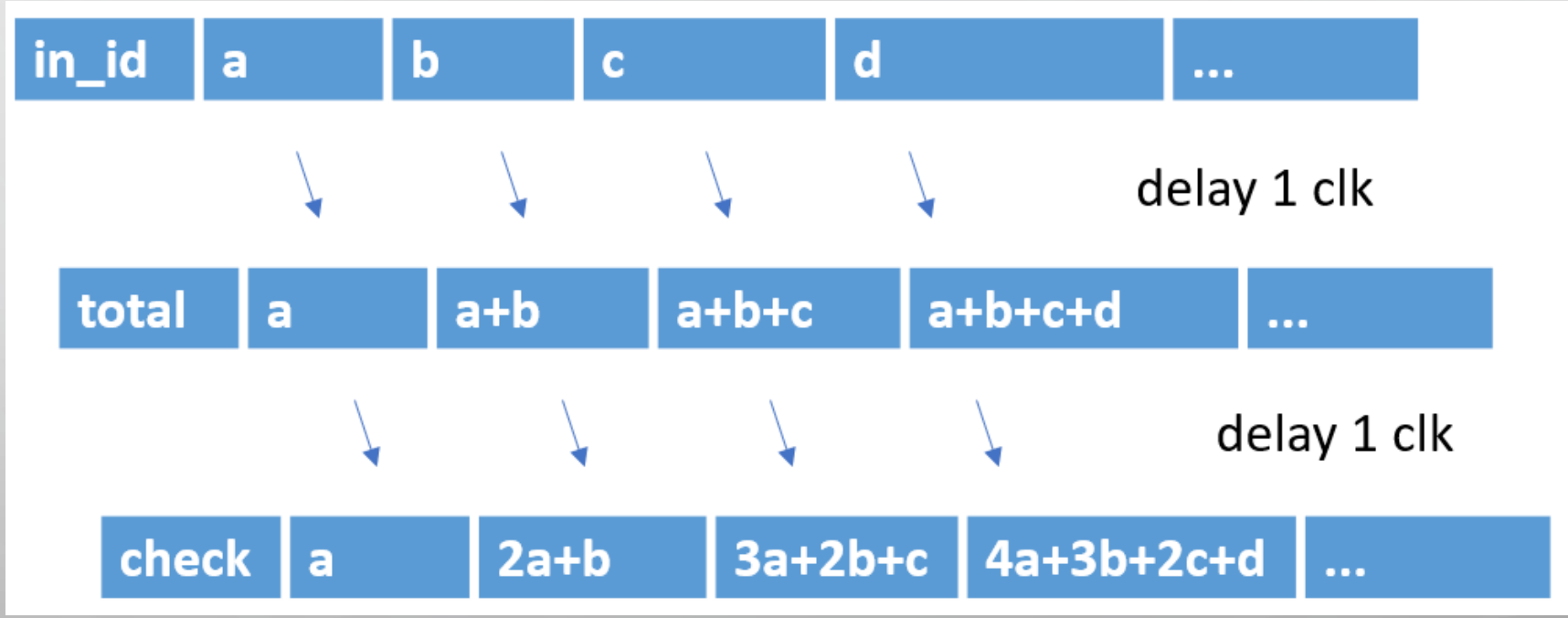
# Content

- Design Algorithm
- Optimization
  - Sequential Logic
  - Combinational Logic
  - Other
- Critical Path
- Structure Diagram
- Reports

# Design Algorithm

- algorithm 1: only check_reg
- algorithm 2: total_reg & check_reg



# Algorithm 1 Optimization

- using a downward counter as the multiplier

```
inx2 = in << 1;
inx3 = inx2 + in;
inx4 = in << 2;
inx5 = inx4 + in;
inx6 = inx3 << 1;
inx7 = inx6 + in;
inx8 = in << 3;
inx9 = inx8 + in;
```

**4 adders**

```
inxN = in * counter;
```

**~3 adders**

# Algorithm 1 Optimization

- take remain with mux (default value matter)

- in_id_reg
  - no input external delay
  - shorten critical path

# Design Algorithm

- **advantages:**
  - lower area (2 adders vs more than 3 adders)
  - less dependent on counter (later explain)
- **disadvantages:**
  - 2 clock delay
  - extra operation

# Design Algorithm

- **implementation details:**
  - special case: regional tenth unit
  - calculate before first count (earn back 1 clock)
  - get rid of in_id_reg
  - output from next state value (earn back 1 clock)
  - **take remain every clock**

**v1.area: 5000 to v2.area: 4000**

# Optimization

- **overall ideas:**
  - area vs critical path (later explain)
  - keep latency as low as possible (0 latency)
  - area lower method: share

# Optimization - Sequential

- idea: minimize the number of FFs / FFs' function
- out_legal_id by combinational (out_valid)
- check_reg not used in first count
  - store region tenth unit (originally added in last count)
- FF function: reset, enable
  - e.g. only out_valid needs reset using rst_n

**v2.area: 4000 to v3.area: 3700**

# Optimization - Combinational

- redundant if-else
  - especially on critical path
  - find multiple considered cases on the same path
- replace double-driven if-else with single-driven if-else
- replace operator to logic gates
  - don't care terms
  - truth table, K-map

**v3.area: 3700 to v4.area: 2400**

# Optimization - Other

- **counter**
  - idea: algorithm has small dependence on counter
  - dependence: first-count, last-count, total states
  - optimization: combinational
    - first-state logic
    - last-state logic
    - next-state logic

# Optimization - Other

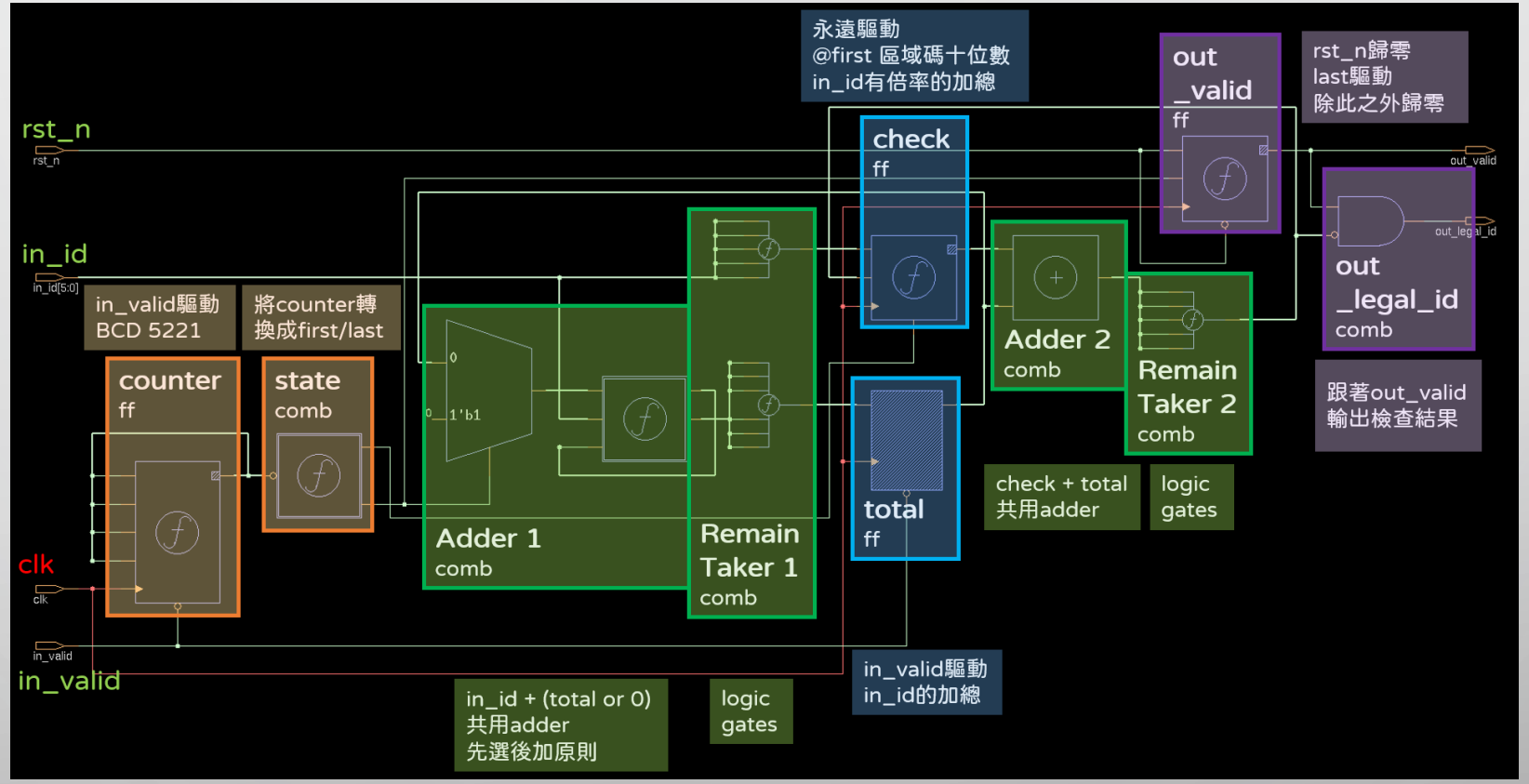
- **counter**
  - result: BCD 5221
- other minor combinational logic optimizations

**v4.area: 2400 to v5.area: 2200**

# Critical Path

- slack violation vs large area
- redundant logic on critical path matters more (3~4 times)
- guess: synthesizer optimization

# Structure Diagram



# Reports

```
****************************************
Report : area
Design : IDC
Version: T-2022.03
Date   : Mon Apr 15 19:04:22 2024
****************************************

Library(s) Used:

    slow (File: /usr/cad/umc018/Synthesis/slow.db)

Number of ports:                          11
Number of nets:                          126
Number of cells:                         117
Number of combinational cells:           104
Number of sequential cells:               13
Number of macros/black boxes:              0
Number of buf/inv:                        18
Number of references:                     34

Combinational area:               1520.164822
Buf/Inv area:                      179.625607
Noncombinational area:             705.196808
Macro/Black Box area:                0.000000
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:                  2225.361629
Total area:                 undefined
```

```
Startpoint: total_reg_reg_0_
            (rising edge-triggered flip-flop clocked by clk)
Endpoint: out_legal_id
          (output port clocked by clk)
Path Group: clk
Path Type: max

Point                                    Incr       Path
-----------------------------------------------------------
clock clk (rise edge)                    0.00       0.00
clock network delay (ideal)              0.00       0.00
total_reg_reg_0_/CK (DFFHQX1)            0.00       0.00 r
total_reg_reg_0_/Q (DFFHQX1)             0.37       0.37 r
U166/Y (NAND2X1)                         0.12       0.49 f
U79/Y (OAI21X1)                          0.25       0.74 r
U167/Y (AOI21X1)                         0.16       0.90 f
U91/Y (XOR2X1)                           0.37       1.27 r
U170/Y (XOR2X1)                          0.26       1.53 f
U90/Y (NOR4X1)                           0.14       1.66 r
U73/Y (INVXL)                            0.11       1.77 f
U69/Y (INVX2)                            0.22       1.99 r
out_legal_id (out)                       0.00       1.99 r
data arrival time                                   1.99

clock clk (rise edge)                    4.00       4.00
clock network delay (ideal)              0.00       4.00
output external delay                   -2.00       2.00
data required time                                  2.00
-----------------------------------------------------------
data required time                                  2.00
data arrival time                                  -1.99
-----------------------------------------------------------
slack (MET)                                         0.01
```

# The End