

DCS Lab 06 Pattern

Pattern

- 這次Lab寫pattern去測錯誤的design ,找到其 錯誤
- 這次Lab只需要寫00_TESTBED/pattern.sv
- lab06_1.sv代表第一個spec錯誤的design,依此類推。lab06.sv 是正確的design。
- lab06_x.sv & lab06.sv 都不要動到
- 可以參考之前幾次的pattern和講義

lab06.sv

Input Signal	Bit Width	Definition		
clk	1	10 ns Clock for 1 cycle		
rst_n	1	Asynchronous reset when reset negedge, all output should be zero		
in_number	4	範圍(-8,7),連續給4個數字。方便之後說 明,分別用in_1、in_2、in_3跟in_4代表		
mode	2	幾種運算模式,請看下一頁		
in_valid	1	in_valid high when giving number		

Output Signal	Bit Width	Definition		
out_valid	1	High for 4 cycles		
out_result	7	Output for 4 cycles,輸出計算後的結果,如下頁所示		

mode

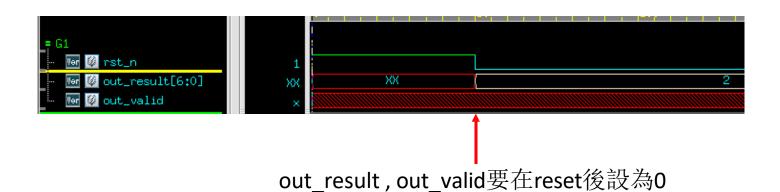
需先將input四個數值(in_1~in_4)進行排序由小至大, 假設以下經過排序後sort_1最小, sort_4最大 out_result輸出如下表所示

mode	Cycle 1	Cycle 2	Cycle 3	Cycle 4
0	Sort_1	Sort_2	Sort_3	Sort_4
1	Sort_4	Sort_3	Sort_2	Sort_1
2	Sort_1 + sort_2	Sort_2 + sort_3	Sort_3 + sort_4	Sort_4 + sort_1
3	Sort_1 - sort_2	Sort_2 - sort_3	Sort_4 - sort_3	Sort_4 - sort_1

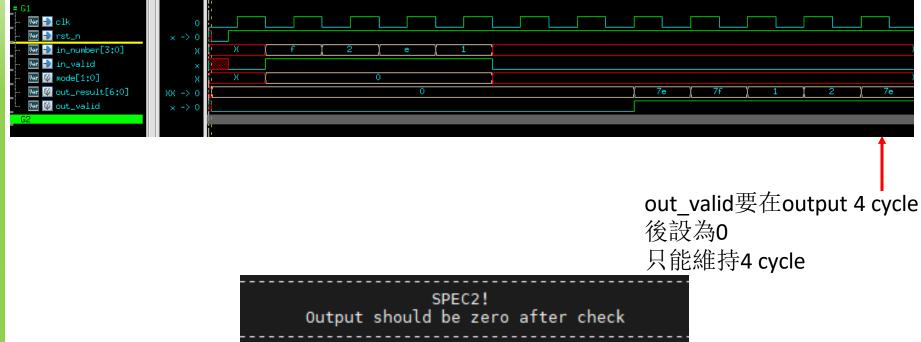
Specifications

- Top module name : lab06 (File name: lab06.sv)
- Spec1 : reset後所有的output signal要歸零
- Spec2:計算完吐完值後4 cycles, out_valid要歸零 (out_valid只維持4 cycles)
- Spec3: outvalid 不能跟 invalid重疊
- Spec4:100cycle內要計算完成(out_valid為high之前)
- Spec5: function要對(前一頁的公式會有錯要檢查出來)
- Spec6:當out_valid是0時,out_result要歸零
- 註:請用random多跑幾組去檢測(建議100以上)

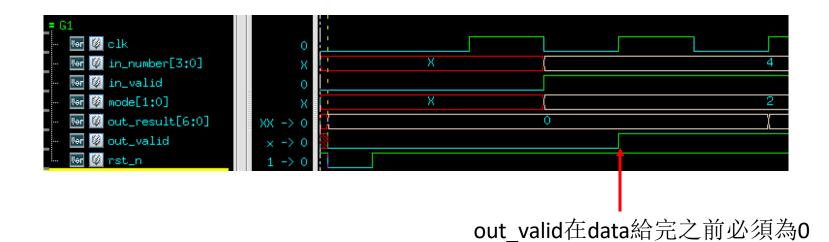
- Waveform SPEC1 error
 - reset後output signal要歸零



- Waveform SPEC2 error
 - 計算完吐完值後4 cycles, out_valid要歸零(out_valid 只維持4 cycles)

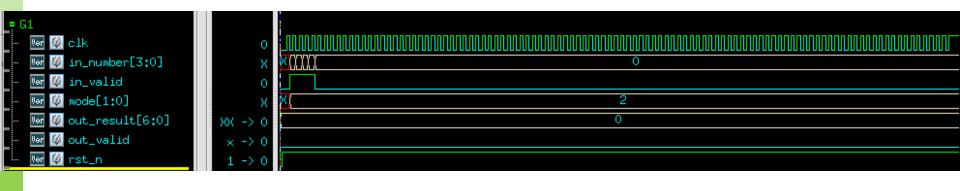


- Waveform SPEC3 error
 - input data 給完之前,out_valid不能為high



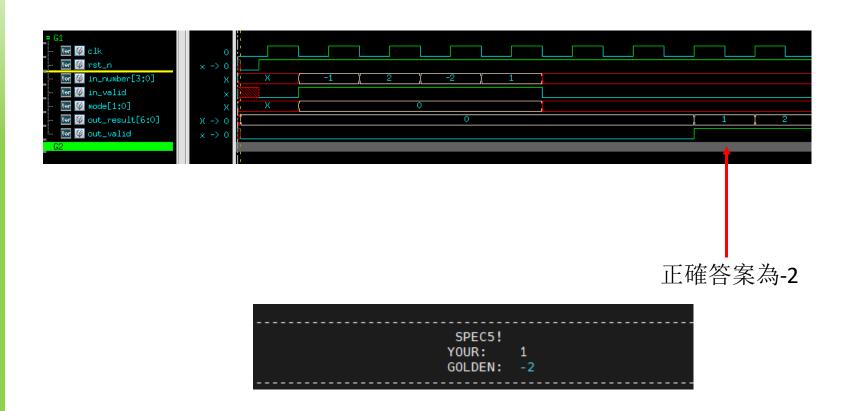
SPEC3!
Outvalid should be zero before give data finish

- Waveform SPEC4 error
 - 100cycle內要計算完成(out_valid為high)

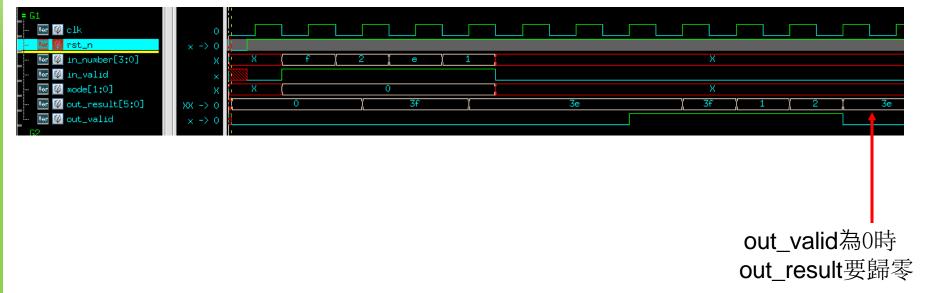


```
SPEC4!
The execution latency are over 100 cycles
```

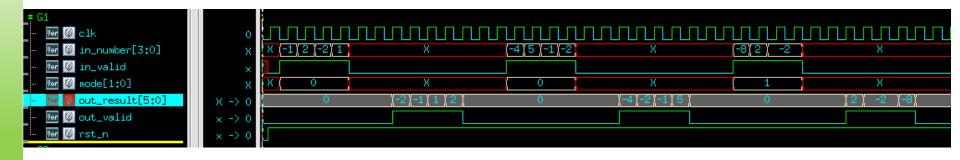
- Waveform SPEC5 error
 - function要對(前幾頁的公式會有錯要檢查出來)



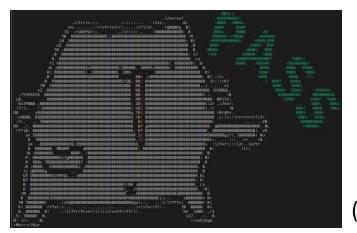
- Waveform SPEC6 error
 - -當out_valid為0時out_result要歸零



- Waveform PASS
 - function要對



Congratulations! You have passed all patterns! time: 2713000 ns



(非必要)

Command

- tar -xvf ~dcsTA01/Lab06.tar
- ./01_run_spec1 : run for check spec1(should display SPEC1 Fail)
- ./01_run_spec2 : run for check spec2(should display SPEC2 Fail)
- ./01_run_spec3 : run for check spec3(should display SPEC3 Fail)
- ./01_run_spec4 : run for check spec4(should display SPEC4 Fail)
- ./01_run_spec5 : run for check spec5(should display SPEC5 Fail)
- ./01_run_spec6 : run for check spec6(should display SPEC6 Fail)
- ./01_run : run for right design(should display Congratulation)
- You should Pass all spec!

Command

請參考pattern.sv裡這段,
 需要各自秀出SPEC1.2.3.4.5.6等資訊,
 以免助教demo時抓不到

```
Outvalid should be zero after check
Outvalid should not be overlapped with invalid
  The execution latency are over 100 cycles
     Output should be zero when outvalid is zero
```

Command

- tar -xvf ~dcsTA01/Lab06.tar
- Upload
 - cd 09_upload
 - ./01_upload
 - ./02_download demoX

Tips

- CYCLE 記得要給值喔~
- 不然模擬會卡住