HW02 code review

Design review

- 身份證字號驗證
  - Cycle 1: 地區碼

A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T	U	V	W	X	Y	Z
10	11	12	13	14	15	16	17	34	18	19	20	21	22	35	23	24	25	26	27	28	29	32	30	31	33

  - Cycle 2: 性別碼，包含 1, 2
  - Cycle 3~9: 流水編號，包含0~9
  - Cycle 10: 驗證碼，包含0~9

Design review

- 身份證字號驗證

Step 1: 依照權重相乘

	A									檢查號碼
	1	0	1	2	3	4	5	6	7	8	9
權重	x1	x9	x8	x7	x6	x5	x4	x3	x2	x1	

Step 2: 結果相加

$$
\begin{array}{rl}
 & 1 \times 1 = 1 \\
 & 0 \times 9 = 0 \\
 & 1 \times 8 = 8 \\
 & 2 \times 7 = 14 \\
 & 3 \times 6 = 18 \\
 & 4 \times 5 = 20 \\
 & 5 \times 4 = 20 \\
 & 6 \times 3 = 18 \\
 & 7 \times 2 = 14 \\
+) & 8 \times 1 = 8 \\
\hline
 & 121
\end{array}
$$

Step 3: 相加除以10取餘數

$$121 / 10 = 12 \ldots 1$$

Step 4: 10減去餘數

$$10 - 1 = 9$$

Some methods from report

- counter從9數下來，順便當權重
- 取個位數就好，每次算完都直接取mod，減少除法器和取mod硬體的bit數，也減少DFF儲存的bit數，降低area

1x1 = 1……取1
0x9+1 = 1 ……取1
1x8+1 = 9……取9
2x7+9 = 23……取3
3x6+3 = 21……取1
4x5+1 = 21……取1
5x4+1 = 21……取1
6x3+1 = 19……取9
7x2+9 = 23……取3
8x1+3 = 11……取1
檢查碼 = 10-1 = 9

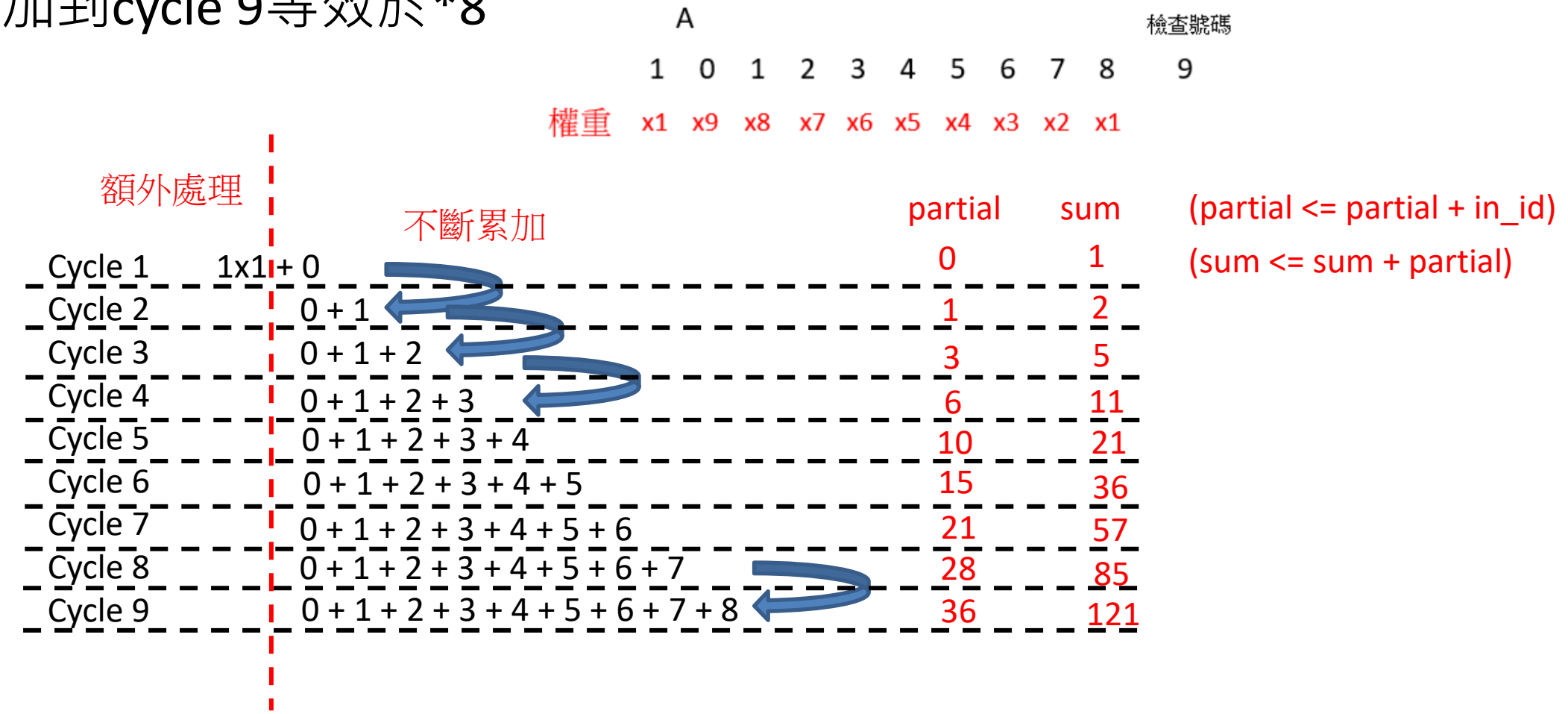
Some methods from report

- 對於有限的輸入，比如區域碼、性別碼等等，用LUT來取代
- 用99乘法表

```
case (in_id_reg)
    11: res = 0;
    22: res = 0;
    33: res = 0;
    10: res = 1;
    21: res = 1;
    32: res = 1;
    19: res = 2;
    20: res = 2;
    31: res = 2;
    18: res = 3;
    29: res = 3;
    30: res = 3;
    17: res = 4;
    28: res = 4;
    16: res = 5;
    27: res = 5;
    15: res = 6;
    26: res = 6;
    14: res = 7;
    25: res = 7;
    13: res = 8;
    24: res = 8;
    35: res = 8;
    12: res = 9;
    23: res = 9;
    34: res = 9;
    default: res = 0;
endcase
```

Some methods from report

- 使用連續加法來取代乘法，cycle 1累加到cycle 9等效於*9，cycle 2累加到cycle 9等效於*8

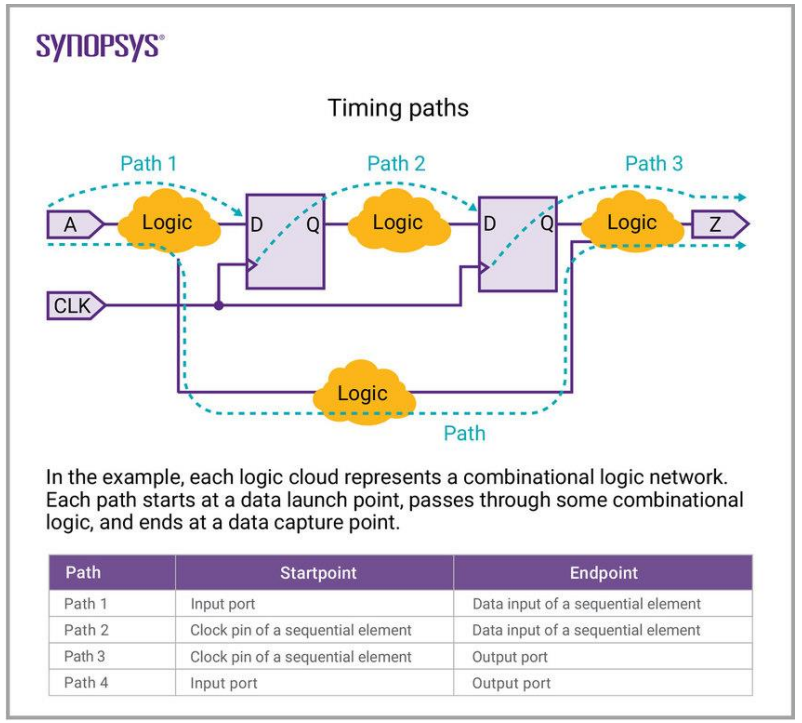


External delay

- 因為我們design的module通常要和別人的module相接，但不確定別人design的輸出狀況，所以input external delay就是模擬前一級的output接到我們的input delay，output external delay就是模擬我們的output接到後一級的input delay，在02合成的tcl檔中會設定，而半個cycle就是一人給一半很公平

Q&A from report

- 4種timing path
- Path1 & 3，和input/output port有關
  - 有external delay，檔DFF比較robust
- Path 2
  - 運算太長，平均分配運算量
- Path 4
  - 有input/output external delay
  - 原則上直接timing violation



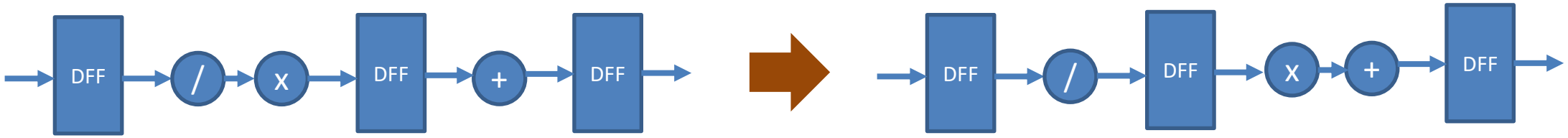
Lecture 5 page 10

Q&A from report

- Timing和area關係?
  - Trade off between area and speed
- 在02合成時，在timing充足時，Design Compiler會全力幫我們縮小面積，但當timing條件很難達到時，就會嘗試用面積比較大、速度更快的cell來合成，如果連最快的cell都滿足不了就會timing violation

Q&A from report

- 降低critical path的負擔或者盡可能平衡每個cycle的工作量也是降低area的策略之一
  - 盡量避免在一個cycle內完成太複雜的運算



- 我的優化方法別人不行，別人的優化方法我不行，面積還變大?
  - 優化要根據架構去做
    - Critical path越小，area就越有優化空間

Q&A from report

- 01 pass, but 03 fail…
- timing violation
  - 減少combinational電路的運算量、多切幾個cycle來做…

```
patcount:          0


Warning!  Timing violation
          $setuphold<setup>( posedge CK &&& (flag == 1):54 NS, negedge D:53763165 FS,  0.408991 : 408991 FS,  -0.11479
3 : -114793 FS );
           File: /RAID2/COURSE/iclab/iclabta01/umc018/Verilog/umc18_neg.v, line = 6480
          Scope: TESTBED.I_design.mult_reg1_reg_4__12_
           Time: 54 NS


Warning!  Timing violation
          $setuphold<setup>( posedge CK &&& (flag == 1):54 NS, negedge D:53607838 FS,  0.397058 : 397058 FS,  -0.10092
7 : -100927 FS );
           File: /RAID2/COURSE/iclab/iclabta01/umc018/Verilog/umc18_neg.v, line = 6480
          Scope: TESTBED.I_design.mult_reg1_reg_4__11_
           Time: 54 NS


Warning!  Timing violation
          $setuphold<setup>( posedge CK &&& (flag == 1):54 NS, negedge D:53730869 FS,  0.409031 : 409031 FS,  -0.11484
0 : -114840 FS );
           File: /RAID2/COURSE/iclab/iclabta01/umc018/Verilog/umc18_neg.v, line = 6480
          Scope: TESTBED.I_design.mult_reg2_reg_4__11_
           Time: 54 NS


Warning!  Timing violation
          $setuphold<setup>( posedge CK &&& (flag == 1):66 NS, negedge D:65794684 FS,  0.397058 : 397058 FS,  -0.10092
7 : -100927 FS );
           File: /RAID2/COURSE/iclab/iclabta01/umc018/Verilog/umc18_neg.v, line = 6480
          Scope: TESTBED.I_design.mult_reg1_reg_4__11_
           Time: 66 NS
```

Q&A from report

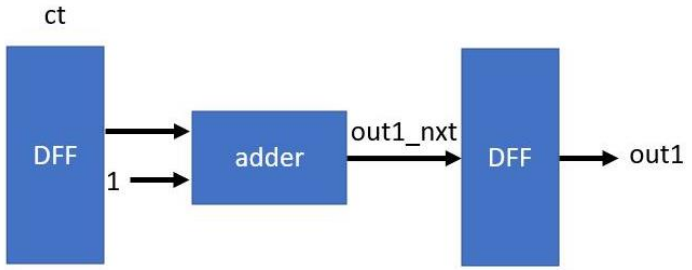
- 01 pass, but 03 fail…
- 03波型出現unknown
  - 常常是因為沒有根據in_valid來接收input，導致後面的register吃到unknown，最後的輸出也變成unknown
  - 回去01看DFF有沒有reset或吃到unknown，後面又拿這個來算

```
assign in_id_nxt = in_valid? in_id : 0;
always_ff @(posedge clk or negedge rst_n)begin
    if (!rst_n)begin
        in_id_reg <= 0;
    end
    else begin
        in_id_reg <= in_id_nxt;
    end
end
```

Q&A from report

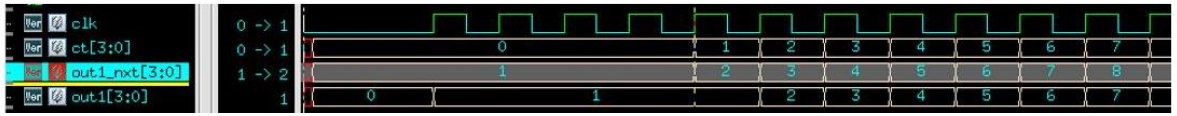
- 01 pass, but 03 fail…
- 一個always block不要放太多變數，debug比較容易
- 有一個好的coding style，比較不會讓01和03出現落差，新手推薦combinational和sequential分開寫，心中比較容易想像出電路

combinational和sequential電路分開寫的寫法




```
always_comb begin
    out1_nxt = ct + 1;
end

always_ff @(posedge clk or negedge rst_n)begin
    if(!rst_n)begin
        out1 <= 0;
    end
    else begin
        out1 <= out1_nxt;
    end
end
```



Q&A from report

- syn.log怎麼看
  - 可以注意的資訊
  - Register xxx is a constant and will be removed
    - may cause 03 fail sometimes with extremely low cell area
  - Break xxx loop
    - Usually there are combinational loop in RTL design
    - 也可能會在01_RTL進入無限迴圈，模擬無法終止，此時要用Ctrl+C結束，不要用Ctrl+Z，Ctrl+Z只是放到背景執行而已，否則可能產生.lock檔鎖住，不能進行下一次模擬

```
  Beginning Pass 1 Mapping
  ------------------------
  Processing 'Conv'
Information: Added key list 'DesignWare' to design 'Conv'. (DDB-72)
Information: The register 'image_88_ff_reg[0][3]' is a constant and will be removed. (OPT-1206)
Information: The register 'state_reg[1]' is a constant and will be removed. (OPT-1206)
Information: The register 'cnt_ff_reg[5]' is a constant and will be removed. (OPT-1206)
Information: The register 'cnt_ff_reg[4]' is a constant and will be removed. (OPT-1206)
Information: The register 'cnt_ff_reg[3]' is a constant and will be removed. (OPT-1206)
Information: The register 'cnt_ff_reg[2]' is a constant and will be removed. (OPT-1206)
Information: The register 'cnt_ff_reg[1]' is a constant and will be removed. (OPT-1206)
```

```
Information: Changed wire load model for '*ADD_UNS_OP_7_1_7' from '(none)' to 'G5K'. (OPT-170)
Information: Updating design information... (UID-85)
Warning: Design 'MRA' contains 82 high-fanout nets. A fanout number of 1000 will be used for delay calculations involving these nets. (TIM-134)
Information: Timing loop detected. (OPT-150)
        C496043/A C496043/Z C496044/B C496044/Z I_30499/A I_30499/Z C589238/B C589238/Z B_32/A B_32/Z C564394/CONTROL1_0 C564394/Z_1 C564395/DATA2_1 C564395/Z
_1 C588971/DATA3_8191 C588971/Z_8191 C588972/DATA1_8191 C588972/Z_8191 C589062/D0_0 C589062/Z_0 C589055/D0_0 C589055/Z_0 C588973/DATA1_0 C588973/Z_0 C564364/D
ATA5_1 C564364/Z_1
Information: Timing loop detected. (OPT-150)
        C496060/A C496060/Z C496061/B C496061/Z I_30502/A I_30502/Z C589242/B C589242/Z B_33/A B_33/Z C564395/CONTROL1_0 C564395/Z_1 C588971/DATA3_8191 C58897
1/Z_8191 C588972/DATA1_8191 C588972/Z_8191 C589062/D0_0 C589062/Z_0 C589055/D0_0 C589055/Z_0 C588973/DATA1_0 C588973/Z_0 C564364/DATA5_1 C564364/Z_1
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'C496043'
         to break a timing loop. (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'C496060'
         to break a timing loop. (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'C498846'
         to break a timing loop. (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'C498864'
         to break a timing loop. (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'C501776'
         to break a timing loop. (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'C501794'
         to break a timing loop. (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'C504707'
         to break a timing loop. (OPT-314)
Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'C504726'
         to break a timing loop. (OPT-314)
```

Note

- Verilog是硬體描述語言!!!! 不是軟體語言

數電HW

大部分人:

作業好難，還要拚Performance，花了好多時間。

有人:

我改了Pattern貓貓的顏色。

After finishing the homework, I started to study the cute cat in pattern. I realized that the color of cat can be change. So I create my own 'rainbow' cat as follow figure.