Lab02 Merge Sort

Sorting

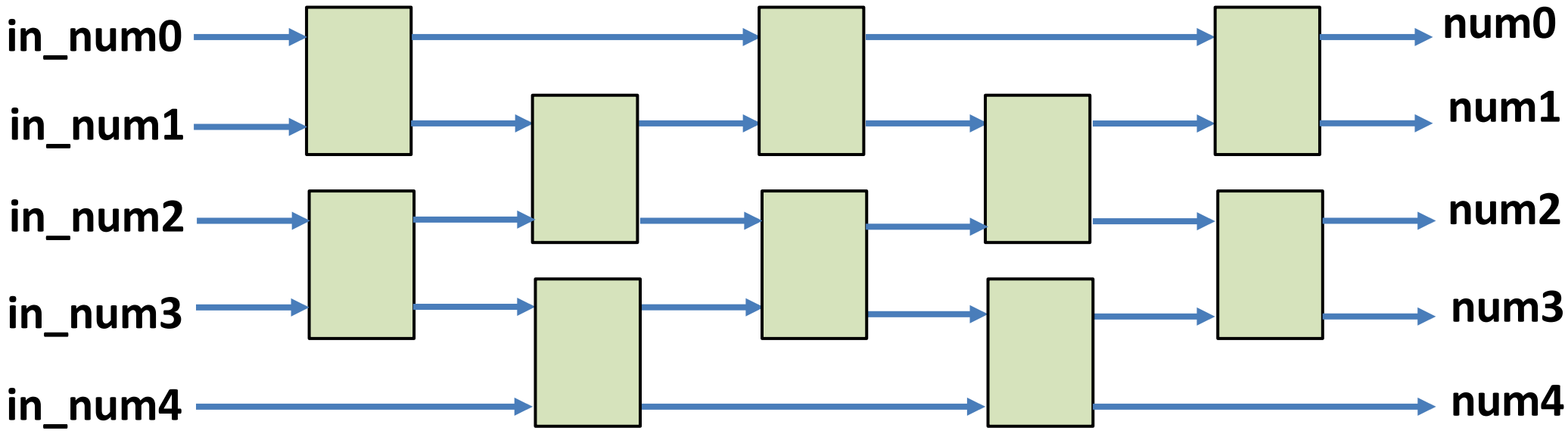
- 輸入五個數字{in_num0, in_num1, in_num2, in_num3, in_num4}
- 將五個數字由小至大進行排序之後，輸出中位數 out_num

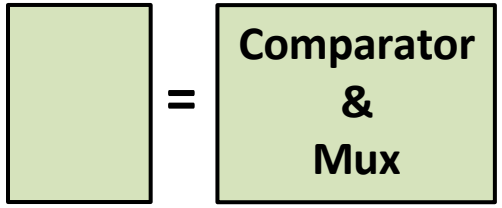
- Ex: 輸入數字: 5, 4, 1, 3, 2 → 輸出: 3
  - Bubble sort, Merge sort

Sorting

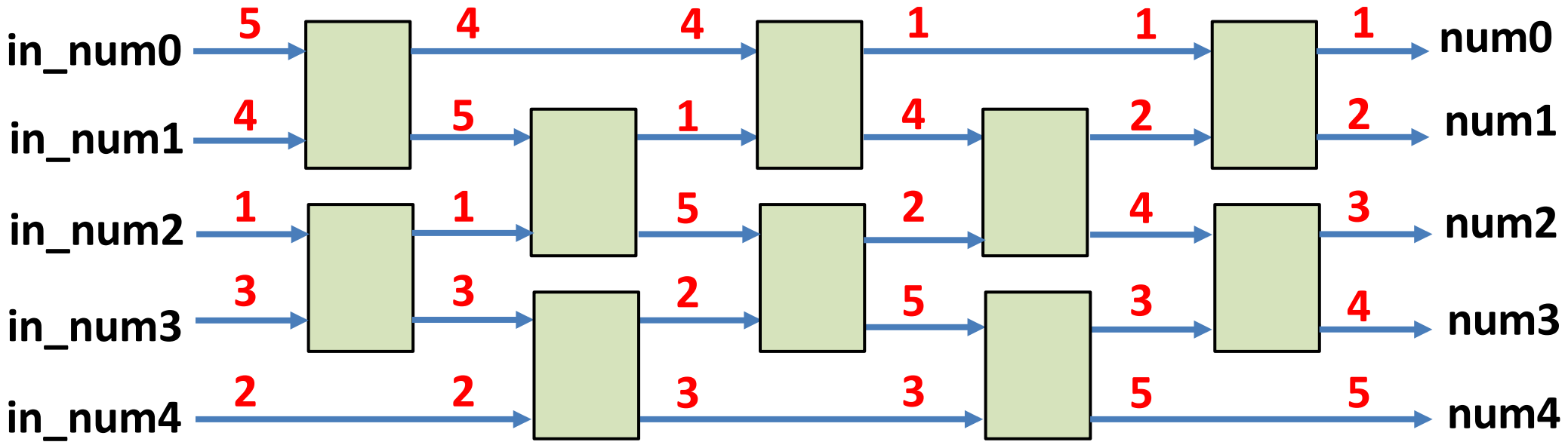
- 氣泡排序法 (Bubble sort)
  - Easy for software
  - Use recursive function, for loop
- 合併排序法 (Merge sort)
  - Easy for hardware
  - Use comparator

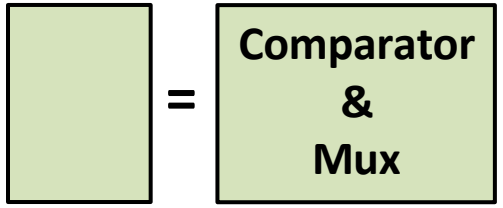
參考架構 (Merge Sort)





參考架構 (Merge Sort)





Sort.sv

Input Signal	Bit width	Definition
in_num0	6	Random 6-bit numbers
in_num1	6	
in_num2	6	
in_num3	6	
in_num4	6	

Output Signal	Bit width	Definition
out_num	6	Median of the input numbers

Directory

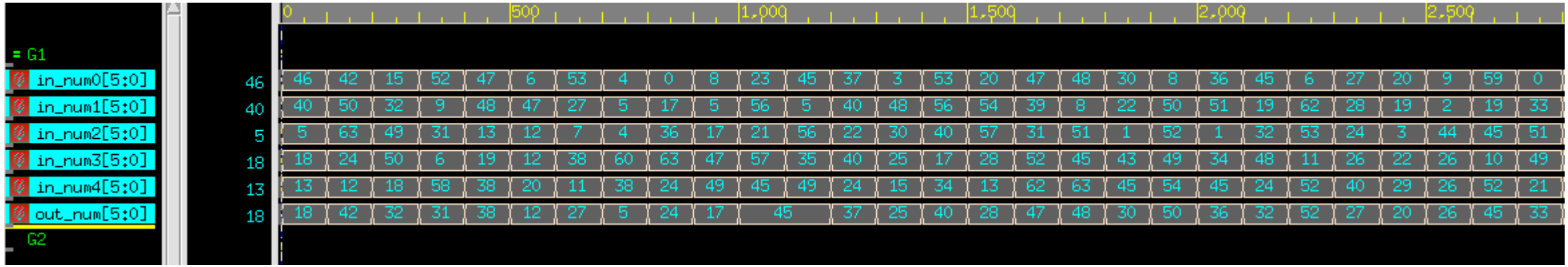
- 00_TESTBED
  - TESTBED.sv
  - PATTERN.sv
- 01_RTL
  - 01_run
  - 09_clean_up
  - Sort.sv
- 02_SYN
  - 01_run_dc
  - 09_clean_up
- 03_GATE
  - 01_run
  - 09_clean_up
- 09_UPLOAD
  - 01_upload
  - 02_download

Command

- tar -xvf ~dcsTA01/Lab02.tar
- cd Lab02/01_RTL/

RTL simulation

- cd Lab02/01_RTL/
- ./01_run (電路模擬)
- ./09_clean_up (清除波型檔)
- verdi & (看波型)
  - 範例波型

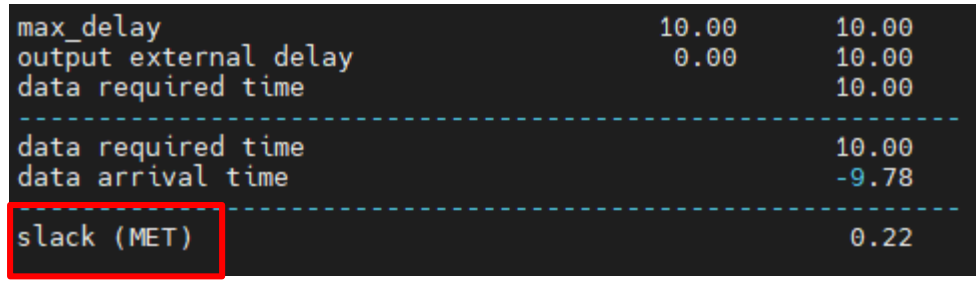


Synthesis

- cd ../02_SYN/
- ./01_run_dc (合成電路)
- ./09_clean_up (清除合成結果)
  - 合成結果: (不能有Error、 要有Area report、Timing report slack met、不能有latch)

Synthesis

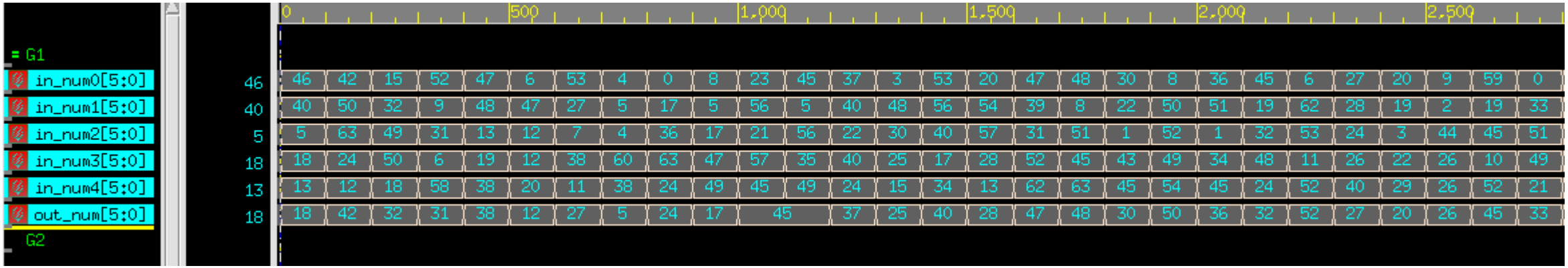
- 合成的timing report中的 slack必須≧0 (MET)
- 如果出現timing violation → Demo Fail ! (slack < 0)



- 記得檢查是否合成出Latch和error
  - 可以在syn.log用ctrl+F尋找關鍵字latch、error
- 如果出現latch 、error → Demo Fail

Gate-level simulation

- cd Lab02/03_GATE/
- ./01_run (電路模擬)
- ./09_clean_up (清除波型檔)
- verdi & (看波型)
  - 範例波型



Grading policy

- Pass the RTL & Synthesis & Gate-level simulation: 100%
  - 合成結果: (沒有Error、有Area report、Timing report slack met、沒有latch)

- Demo2 打7折

Upload

- cd ../09_UPLOAD/
- ./01_upload (上傳code)
- ./02_download [argument] (下載上傳結果)
  - [argument] = demo1 or demo2
  - 檢查是否上傳成功&正確
- Demo1: 3/7, 17:30:00, Demo2: 3/8, 23:59:59