

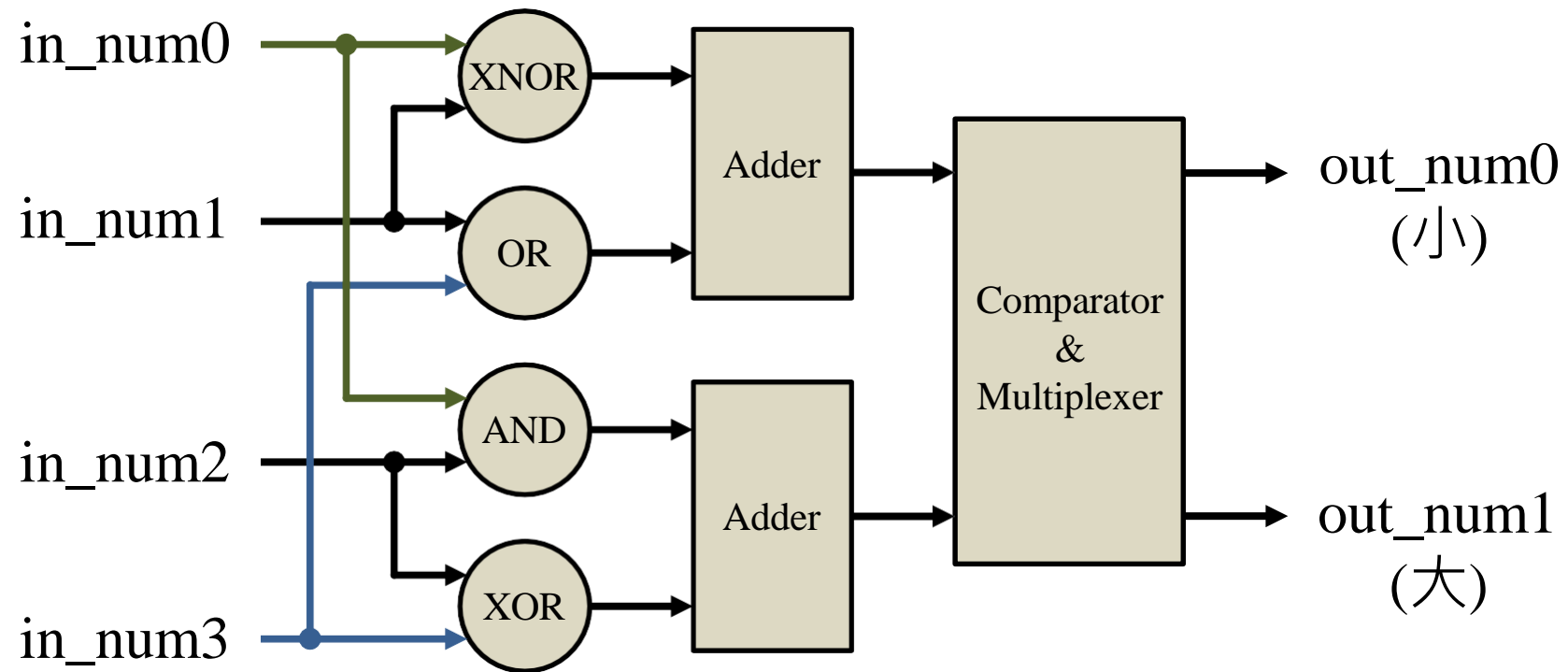
# Lab01 Combinational

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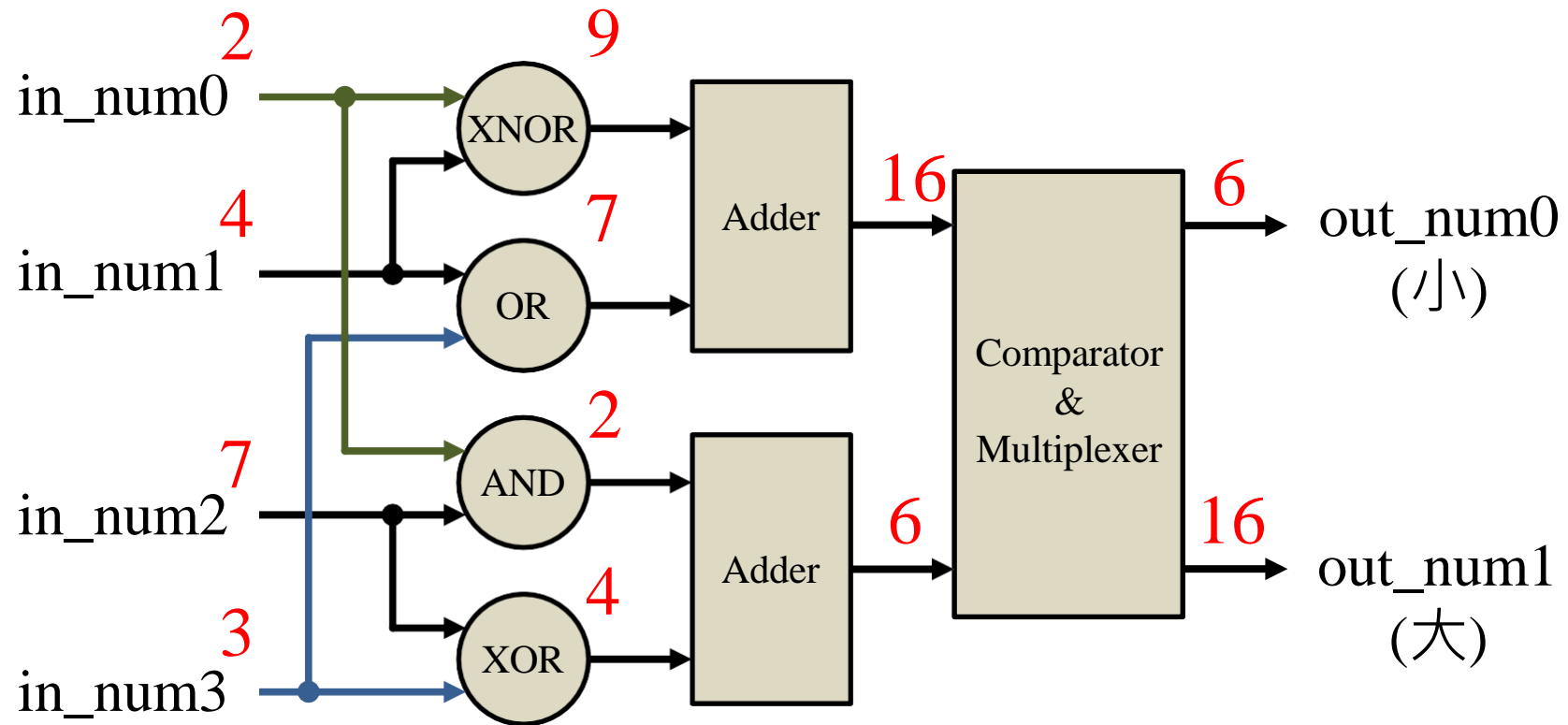
# Combinational

- 會有四個數字輸入  $\text{in\_num0} \sim \text{in\_num3}$ 
  - Ex:  $\text{in\_num0} \sim \text{in\_num3} = [2, 4, 7, 3]$
- 將數字依照範例，分別做 **Bitwise** XNOR, OR, AND, XOR 後，
  - Ex:  $A = \text{in\_num0} \text{ XNOR } \text{in\_num1} = 0010 \text{ XNOR } 0100 = 1001 = 9$   
 $B = \text{in\_num1} \text{ OR } \text{in\_num3} = 0100 \text{ OR } 0011 = 0111 = 7$   
 $C = \text{in\_num0} \text{ AND } \text{in\_num2} = 0010 \text{ AND } 0111 = 0010 = 2$   
 $D = \text{in\_num2} \text{ XOR } \text{in\_num3} = 0111 \text{ XOR } 0011 = 0100 = 4$
- 再將運算後的數字依照範例，分 AB、CD 兩組相加，
  - Ex:  $A + B = 9 + 7 = 16$ ,  $C + D = 2 + 4 = 6$
- 最後排序由小至大輸出。
  - Ex:  $\text{out\_num0} = 6$ ,  $\text{out\_num1} = 16$

# Block diagram for your reference



# Block diagram for your reference



# Comb.sv

Input Signal	Bit width	Definition
in_num0	4	Random 4-bit numbers
in_num1	4	
in_num2	4	
in_num3	4	

Output Signal	Bit width	Definition
out_num0	5	$out\_num0 \leq out\_num1$
out_num1	5	

# Directory

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- 00\_TESTBED
  - TESTBED.sv
  - PATTERN.sv
- 01\_RTL
  - 01\_run
  - 09\_clean\_up
  - Comb.sv

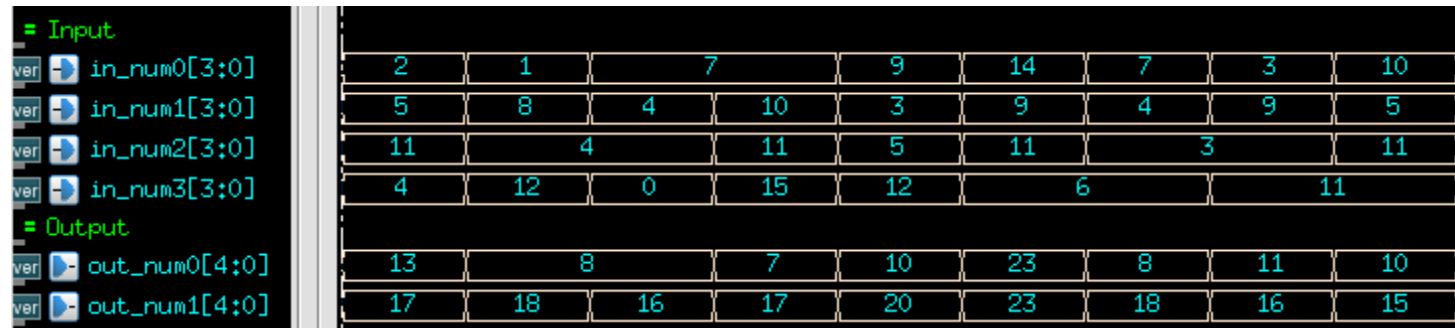
# Command

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- `tar -xvf ~dcsTA01/Lab01.tar`
- `cd Lab01/01_RTL/`

# RTL simulation

- cd Lab01/01\_RTL/
- ./01\_run (電路模擬)
- ./09\_clean\_up (清除波型檔)
- verdi &
  - 範例波型



The screenshot shows a Verilog simulation waveform viewer. On the left, a list of signals is displayed: four input signals (in\_num0[3:0], in\_num1[3:0], in\_num2[3:0], in\_num3[3:0]) and two output signals (out\_num0[4:0], out\_num1[4:0]). The signals are grouped under 'Input' and 'Output' headers. The main area shows the waveform for these signals over time, with values changing at discrete intervals. The input signals are 4-bit, and the output signals are 5-bit.

Time	in_num0[3:0]	in_num1[3:0]	in_num2[3:0]	in_num3[3:0]	out_num0[4:0]	out_num1[4:0]
0	2	1	7	9	13	17
1	1	8	4	10	8	18
2	7	4	11	5	7	16
3	9	3	9	4	10	17
4	14	9	4	9	23	20
5	7	4	3	11	8	23
6	3	9	11	6	11	18
7	10	5	11	11	10	16



# Questions

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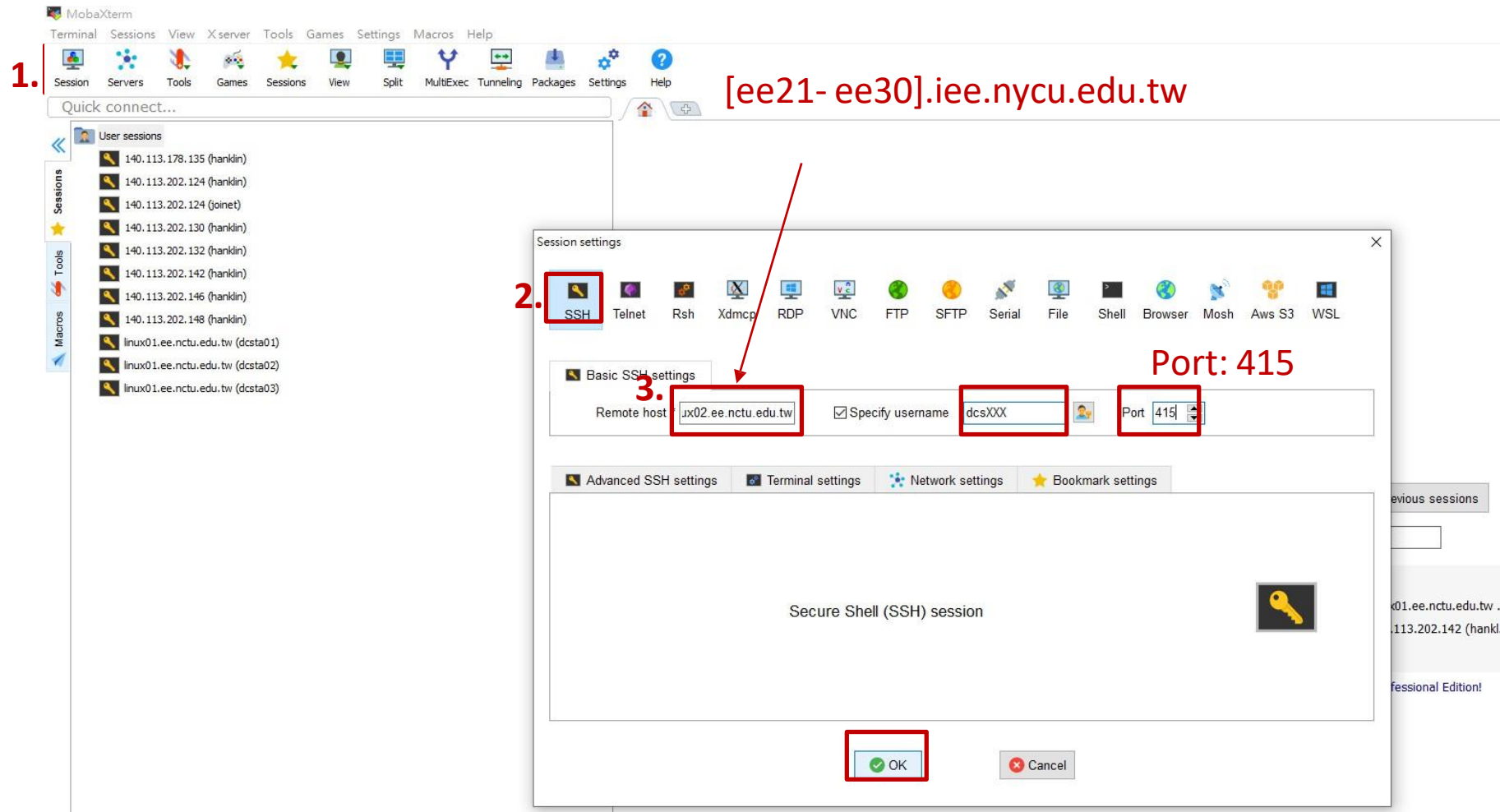
- At 60ns, what's the value of num\_xor and num\_add2 in decimal?
- At 100ns, what's the value of num\_xnor and out\_num0 in binary?
- Trace which signals drives out\_num0 (use nTrace)
- Trace which signal is loading from num\_xor (use nTrace)
- Please paste screenshot to answer the questions

# Grading policy

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- Write a report including:
  - nTrace screenshot
  - nWave screenshot
  - nSchema screenshot
  - Answer the Question
- Deadline: 3/6, 23:59:59
- Please upload student\_ID.docx to E3 platform

# MobaXterm Available Server



# MobaXterm Available Server

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- 使用linux server如果遇到以下訊息可以忽略

```
*Verdi* Loading libsscore_ius152.so
ncsim: *W,LIBLDL: Failed to load dynamic library debpli:
      debpli.so: cannot open shared object file: No such file or directory or file is not valid ELFCLASS32 library..
ncsim> source /RAID2/EDA/cadence/INCISIV/INCISIVE_15.20.084/tools/inca/files/ncsimrc
ncsim> run
```