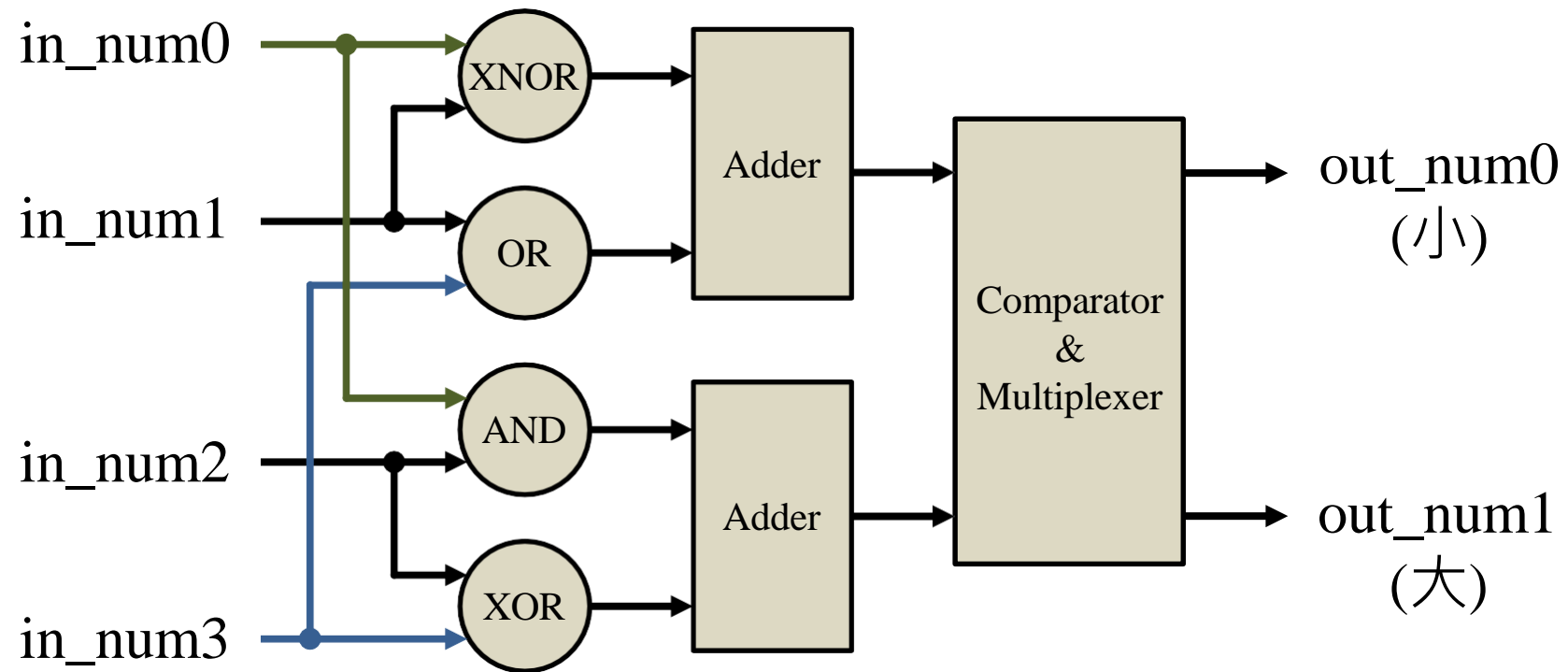


Lab01 Combinational

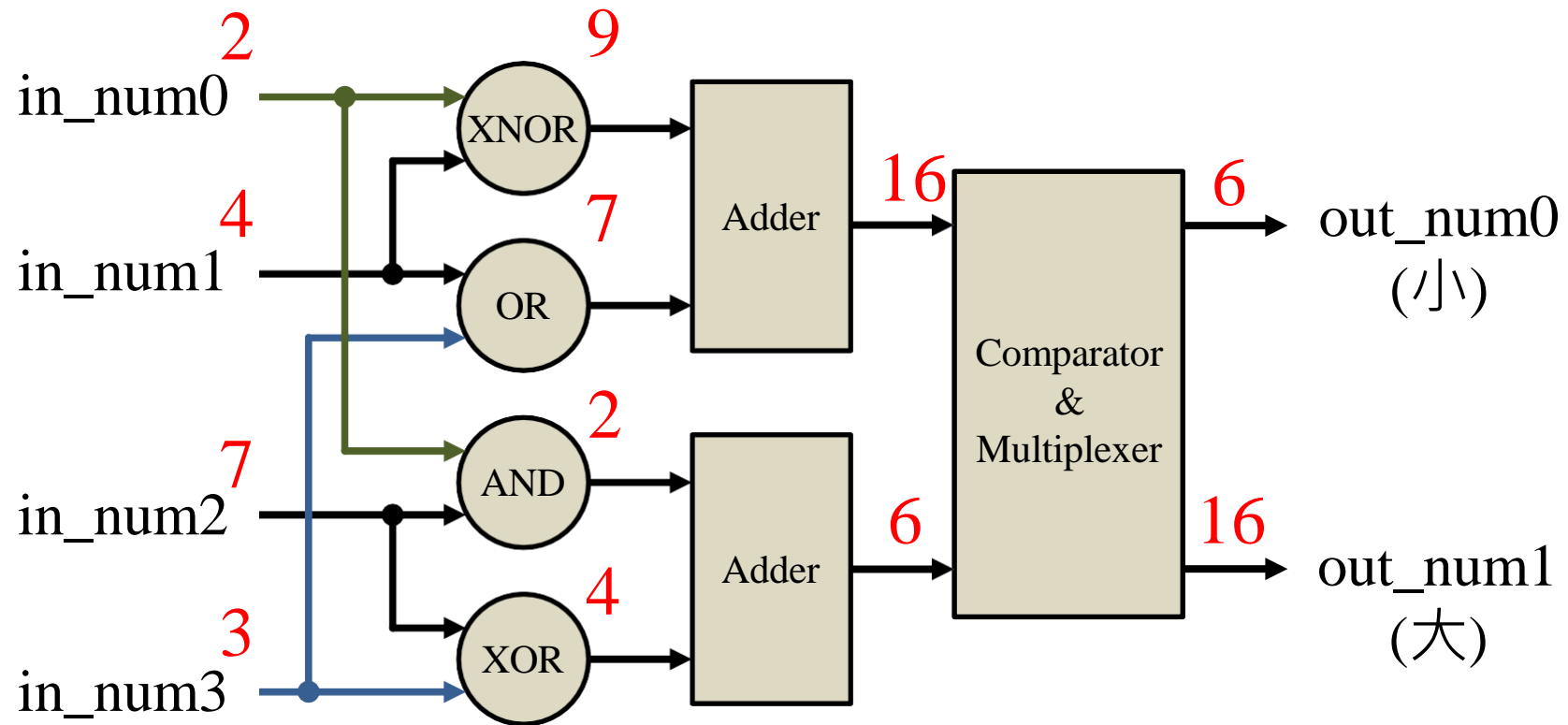
Combinational

- 會有四個數字輸入 $\text{in_num0} \sim \text{in_num3}$
 - Ex: $\text{in_num0} \sim \text{in_num3} = [2, 4, 7, 3]$
- 將數字依照範例，分別做 **Bitwise** XNOR, OR, AND, XOR 後，
 - Ex: $A = \text{in_num0} \text{ XNOR } \text{in_num1} = 0010 \text{ XNOR } 0100 = 1001 = 9$
 $B = \text{in_num1} \text{ OR } \text{in_num3} = 0100 \text{ OR } 0011 = 0111 = 7$
 $C = \text{in_num0} \text{ AND } \text{in_num2} = 0010 \text{ AND } 0111 = 0010 = 2$
 $D = \text{in_num2} \text{ XOR } \text{in_num3} = 0111 \text{ XOR } 0011 = 0100 = 4$
- 再將運算後的數字依照範例，分 AB、CD 兩組相加，
 - Ex: $A + B = 9 + 7 = 16$, $C + D = 2 + 4 = 6$
- 最後排序由小至大輸出。
 - Ex: $\text{out_num0} = 6$, $\text{out_num1} = 16$

Block diagram for your reference



Block diagram for your reference



Comb.sv

Input Signal	Bit width	Definition
in_num0	4	Random 4-bit numbers
in_num1	4	
in_num2	4	
in_num3	4	

Output Signal	Bit width	Definition
out_num0	5	$out_num0 \leq out_num1$
out_num1	5	

Directory

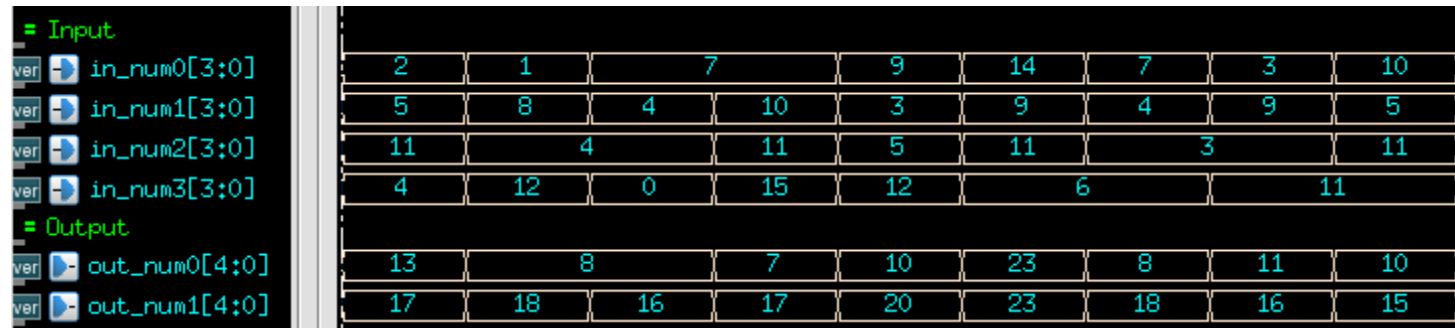
- 00_TESTBED
 - TESTBED.sv
 - PATTERN.sv
- 01_RTL
 - 01_run
 - 09_clean_up
 - Comb.sv

Command

- `tar -xvf ~dcsTA01/Lab01.tar`
- `cd Lab01/01_RTL/`

RTL simulation

- cd Lab01/01_RTL/
- ./01_run (電路模擬)
- ./09_clean_up (清除波型檔)
- verdi &
 - 範例波型



The screenshot shows a Verilog simulation waveform viewer with two sections: 'Input' and 'Output'. The 'Input' section lists four signals: in_num0[3:0], in_num1[3:0], in_num2[3:0], and in_num3[3:0]. The 'Output' section lists two signals: out_num0[4:0] and out_num1[4:0]. The waveform displays a sequence of values for each signal over time, with each value occupying a specific time slot.

Signal	Value 1	Value 2	Value 3	Value 4	Value 5	Value 6	Value 7	Value 8
in_num0[3:0]	2	1	7	9	14	7	3	10
in_num1[3:0]	5	8	4	10	3	9	4	9
in_num2[3:0]	11	4	11	5	11	3	11	11
in_num3[3:0]	4	12	0	15	12	6	11	
out_num0[4:0]	13	8	7	10	23	8	11	10
out_num1[4:0]	17	18	16	17	20	23	18	15

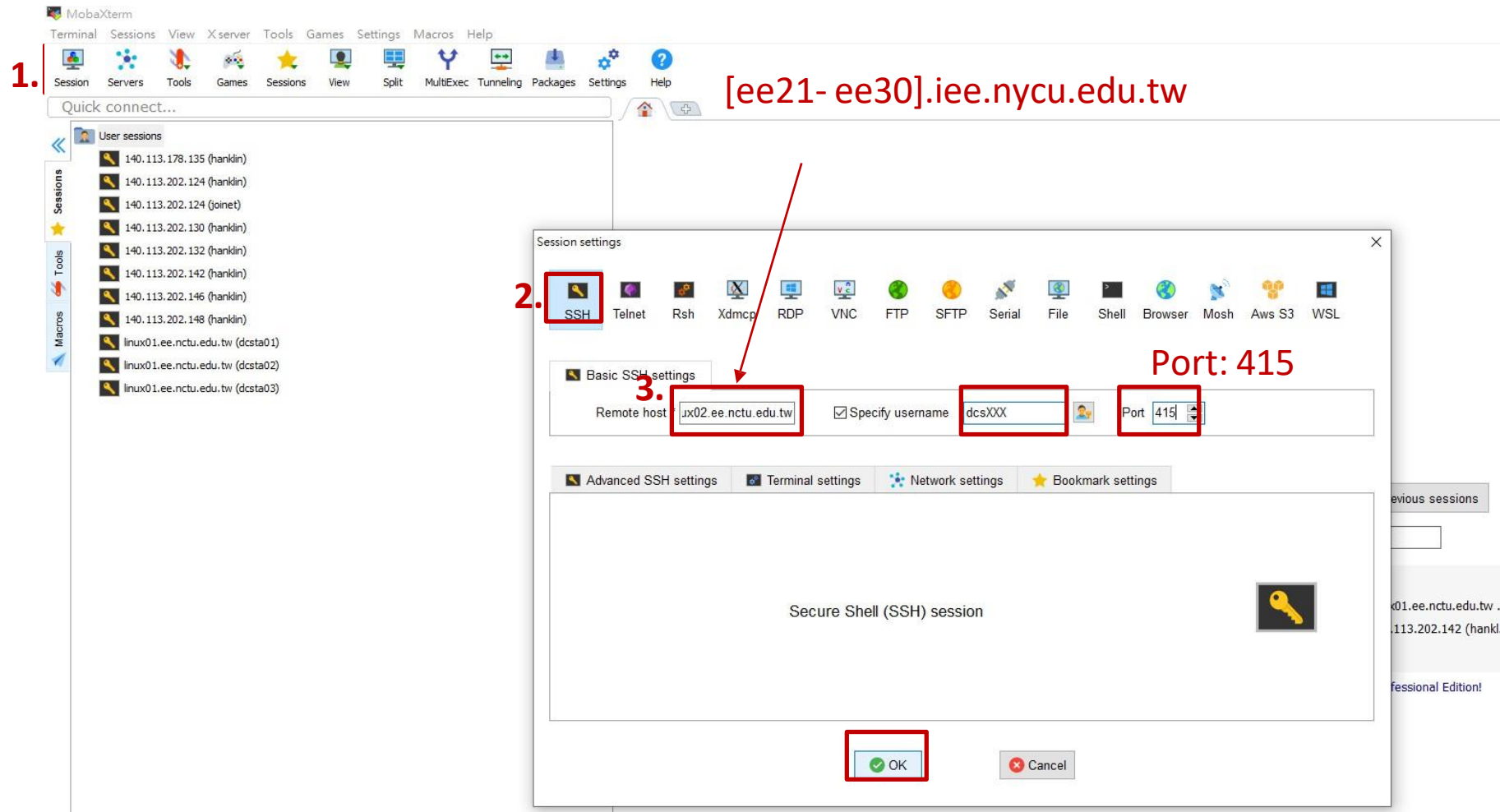
Questions

- At 60ns, what's the value of num_xor and num_add2 in decimal?
- At 100ns, what's the value of num_xnor and out_num0 in binary?
- Trace which signals drives out_num0 (use nTrace)
- Trace which signal is loading from which signal (use nTrace)
- Please paste screenshot to answer the questions

Grading policy

- Write a report including:
 - nTrace screenshot
 - nWave screenshot
 - nSchema screenshot
 - Answer the Question
- Deadline: 3/6, 23:59:59
- Please upload student_ID.docx to E3 platform

MobaXterm Available Server



MobaXterm Available Server

- 使用linux server如果遇到以下訊息可以忽略

```
*Verdi* Loading libsscore_ius152.so
ncsim: *W,LIBLDFL: Failed to load dynamic library debpli:
    debpli.so: cannot open shared object file: No such file or directory or file is not valid ELFCLASS32 library..
ncsim> source /RAID2/EDA/cadence/INCISIV/INCISIVE_15.20.084/tools/inca/files/ncsimrc
ncsim> run
```