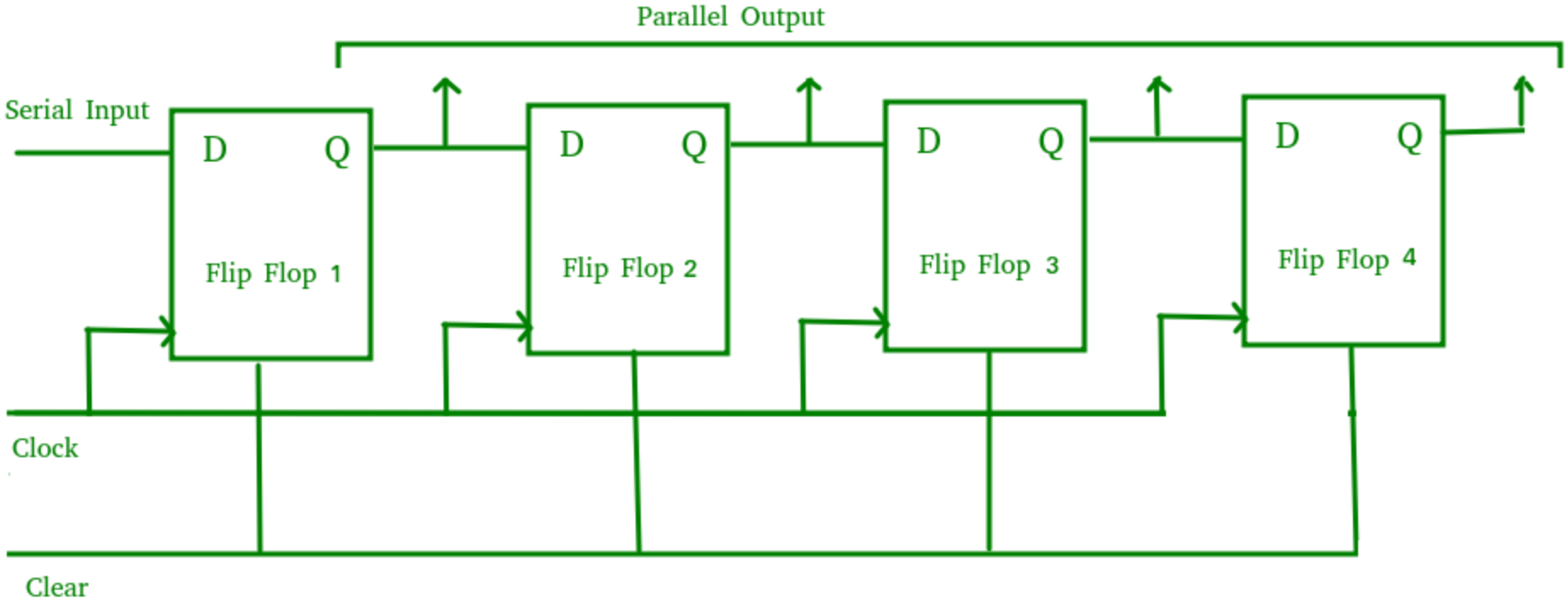
Lab03 SIPO Shift Register

SIPO

- SIPO stands for Serial-In Parallel-Out
- A SIPO shift register is a sequential logic
  - Can store and shift data bits
  - Data buffering, communication…

- Ex: Serial in 1, 0, 1, 1 with consecutive cycles
  → raise out_valid at 4^{th} cycle: 1011

Reference block diagram



※Just a rough block diagram, you should follow the spec in this lab

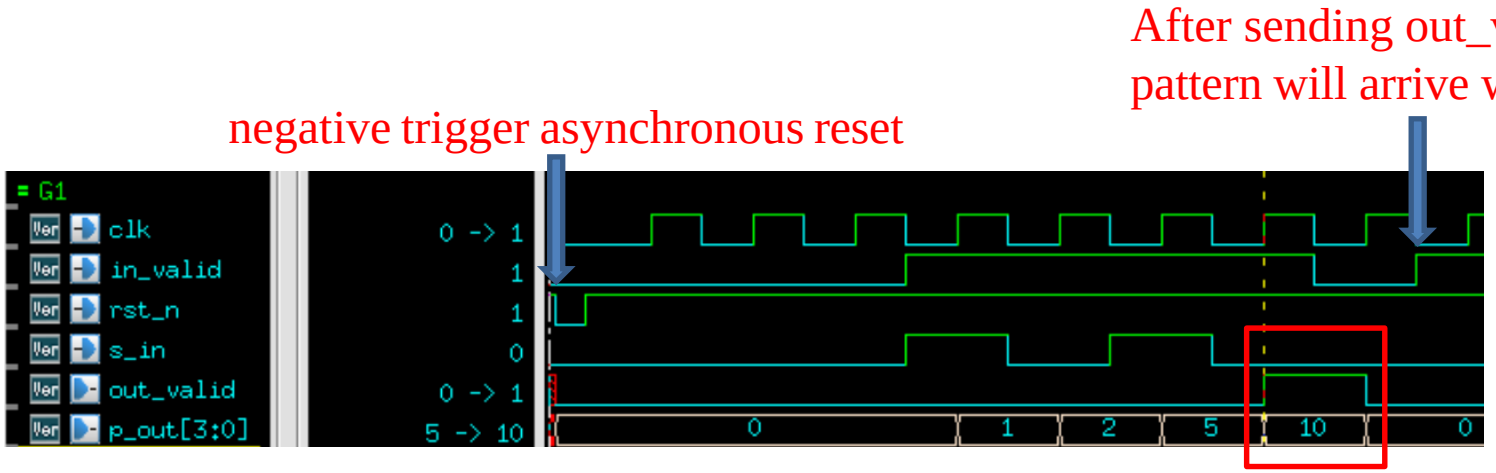
SIPO.sv

Input Signal	Bit width	Definition
clk	1	10ns clock signal
rst_n	1	Asynchronous negedge reset signal
s_in	1	Random 1-bit serial input data
in_valid	1	Pulled high during transmit input

Output Signal	Bit width	Definition
p_out	4	Parallel 4-bit output
out_valid	1	Pulled high during transmit output

※All output signals should be reset to make sure it’s not unknown

Waveform



※All output signals should be reset to make sure it's not unknown

Command & spec

- tar -xvf ~dcsTA01/Lab03.tar
- 02_SYN
  - No Latch
  - No error
  - No timing violation (MET)
- 03_GATE
  - Simulation need pass and no timing violation

DEMO1: 3/14 17:30:00

DEMO2: 3/15 23:59:59