# Digital Integrated Circuits

## #Homework 1 2024.09.20 (Due: 09.27 15:30 ED520)

**Given VDD=0.9V, $W_{min}$=64nm, $L_{min}$=32nm with resolution of 1nm; there are three kinds of $V_t$: High $V_t$, Medium $V_t$ and Low $V_t$ CMOS**

(1) MOS and Inverter with medium threshold voltages (30%)

A. Run SPICE to draw the I-V DC curves for PMOS and NMOS with minimum feature size using High $V_t$, Medium $V_t$, and Low $V_t$ respectively. (24%)

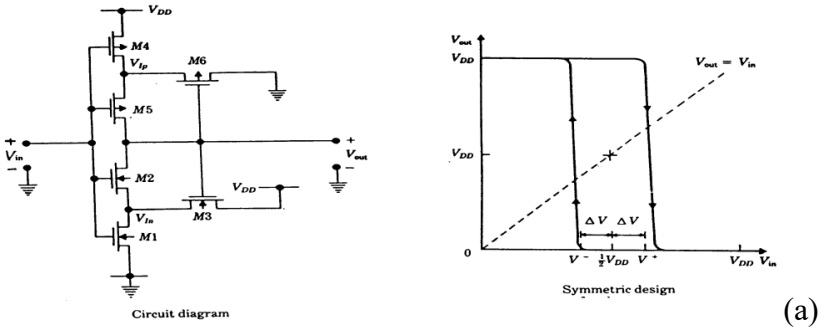
B. Keep L equals to $L_{min}$, design the W of each transistor using medium $V_t$ such that the logic threshold of inverter is at 0.5VDD. **Discuss your design procedures** and the way you choose your MOS dimensions. Run SPICE to verify your results. (6%)

(2) Design a CMOS schmitt trigger shown at Fig. 1(b) such that $V^+$ = 0.54-0.57V and $V^-$ = 0.36-0.33V with CT=VDD (70%)

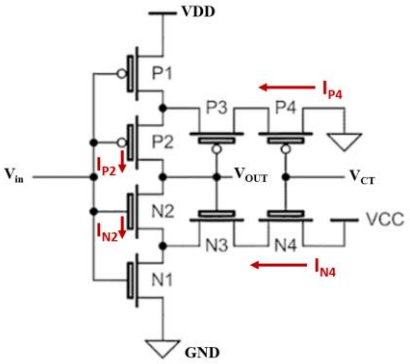
A. **Discuss the difference between Fig. 1(a) and (b).** Give the W/L of each device (in table form) of Fig. 1(b) with CT=VDD and **discuss your design procedures** to determine the size of each transistor using medium $V_t$. (30%)

B. Run SPICE to verify your results. Your report must have the figures of VTC, $I_{N2}$ vs $V_{in}$, and $I_{N4}$ vs $V_{in}$ (20%)

C. Use the same size as in part A, and modify CT to 0.8VDD. Repeat part B to have figures to indicate the new $V^-$ and $V^+$ (20%)




(a)




(b) Schmitt trigger with controllable hysteresis

**Fig. 1 Schmitt Trigger Circuit**