Digital Integrated Circuits

Hspice Example

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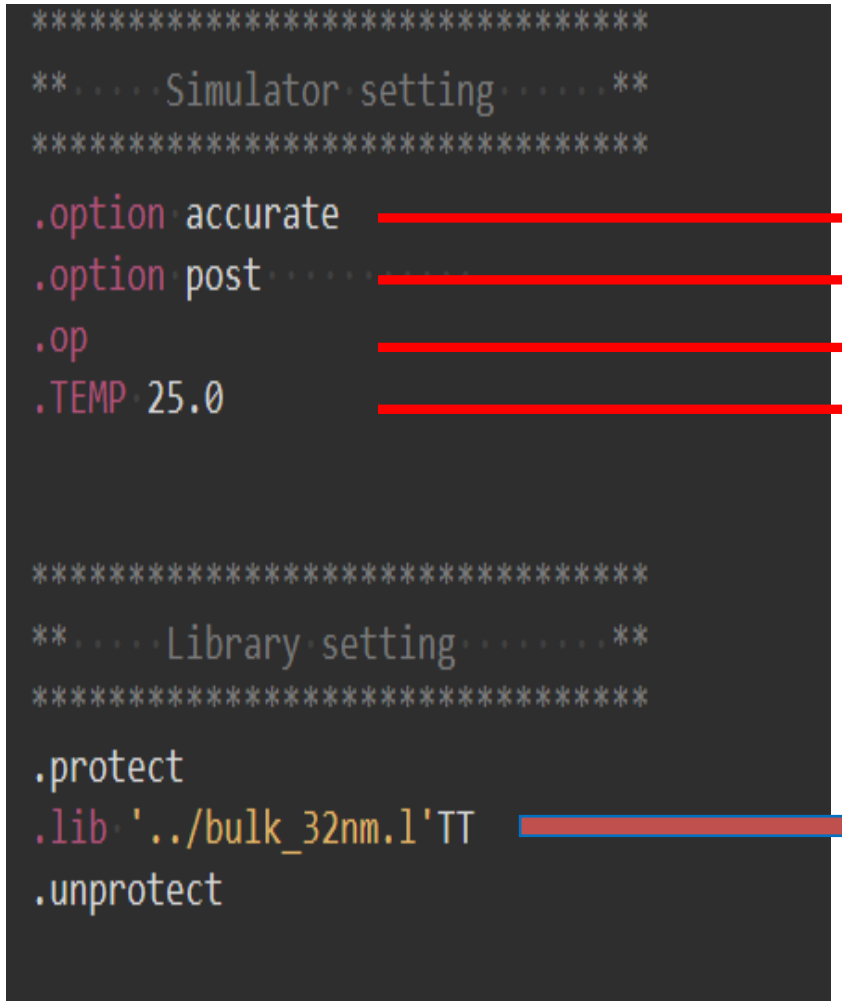
Basic(1/2)

- Hspice範例code請至以下路徑複製：
  /RAID2/COURSE/dic/dicTA01/dic_2024_spring/Tutorial_Example



較精準的模擬

輸出波型檔

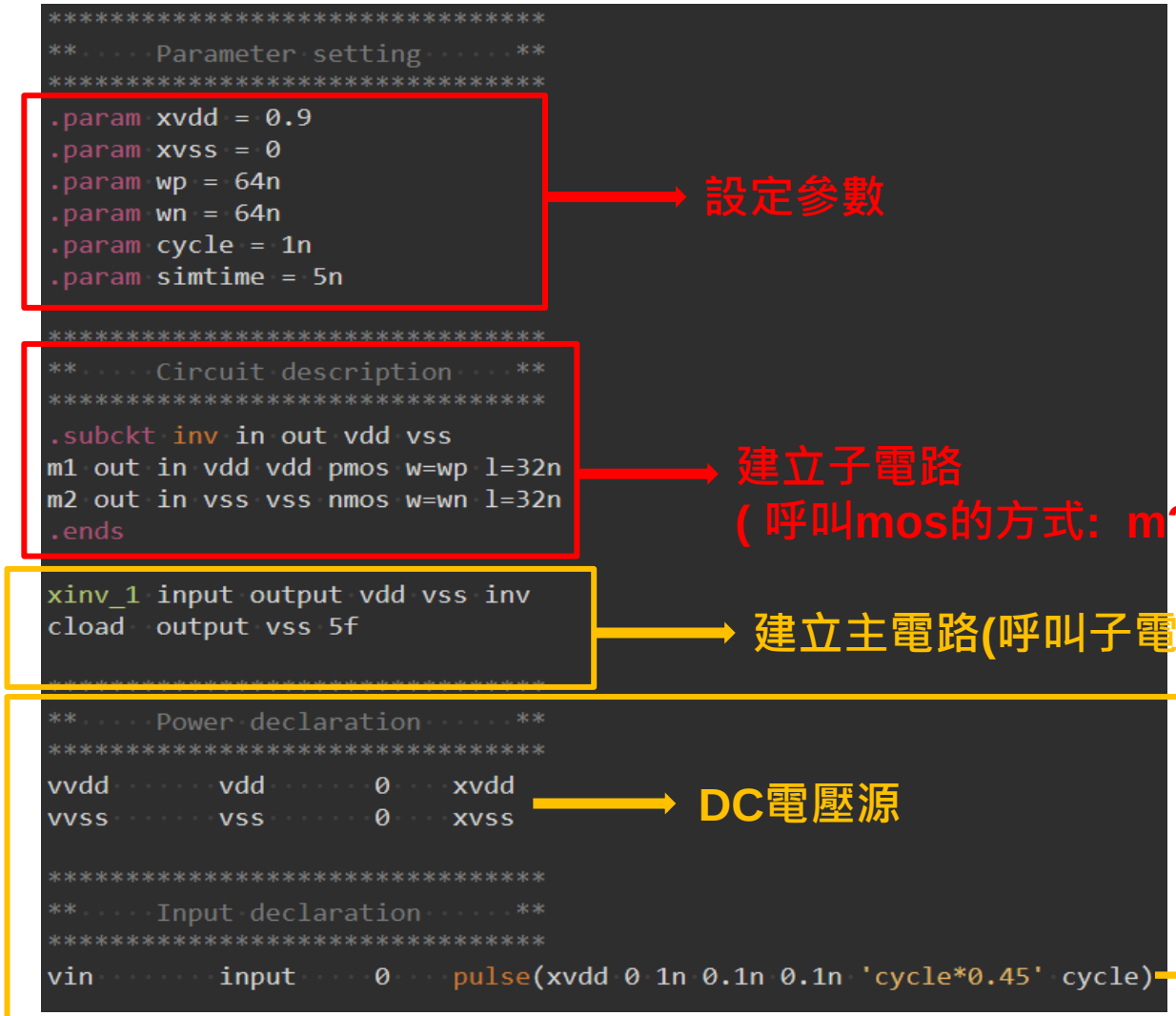
輸出元件工作點於.lis檔

設定環境溫度

包含在裡頭的檔案資訊
不會秀在.lis檔

引入模擬所需的library檔
(路徑與製程檔放置位置要一致)

Basic(2/2)



設定參數

建立子電路

(呼叫mos的方式: m?? D G S B pmos/nmos w=? l=?)

建立主電路(呼叫子電路用x開頭；呼叫電容用c開頭)

DC電壓源

呼叫電壓源用v開頭

pulse電壓源

DC Analysis

```
1  ********************************
2  **      Simulator setting      **
3  ********************************
4  .option accurate
5  .option post
6  .op
7  .TEMP 25.0
8
9
10 ********************************
11 **      Library setting       **
12 ********************************
13 .protect
14 .lib '../bulk_32nm.l'TT
15 .unprotect
16
17
18 ********************************
19 **      Parameter setting     **
20 ********************************
21 .param xvdd = 0.9
22 .param xvss = 0
23 .param wp = 64n
24 .param wn = 64n
25 .param cycle = 1n
26 .param simtime = 5n
27
28
29 ********************************
30 **      Circuit description   **
31 ********************************
32 .subckt inv in out vdd vss
33 m1 out in vdd vdd pmos w=wp l=32n
34 m2 out in vss vss nmos w=wn l=32n
35 .ends
36
37 xinv_1 input output vdd vss inv
38 cload  output vss 5f
39
```

```
********************************
**      Power declaration     **
********************************
vvdd      vdd      0    xvdd
vvss      vss      0    xvss


********************************
**      Input declaration     **
********************************
vin       input    0    pulse(xvdd 0 1n 0.1n 0.1n 'cycle*0.45' cycle)
```

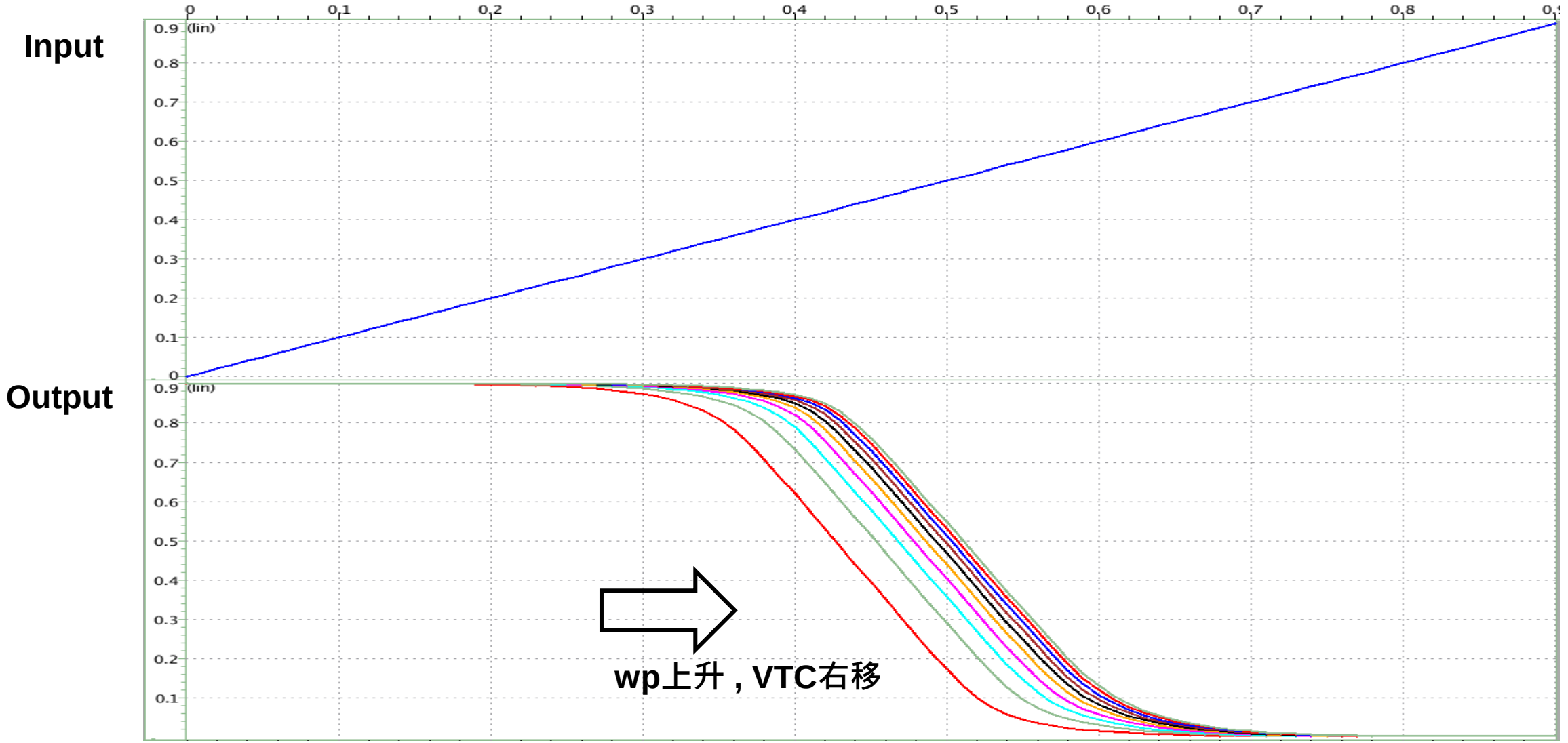
```
************************************
**      Analysis setting          **
************************************

.dc vin 0 0.9 0.01 sweep wp 100n 1000n 100n

.end
```

對vin電壓源從0v到0.9v以step=0.01v做DC分析 (sweep wp變數，從wp=100n開始，每step=100n 重複模擬一次到wp=1000n)

尋找輸出： .sw0檔案 (for DC analysis)



Transient Analysis

```
1  ********************************
2  **      Simulator setting      **
3  ********************************
4  .option accurate
5  .option post
6  .op
7  .TEMP 25.0
8
9
10 ********************************
11 **      Library setting       **
12 ********************************
13 .protect
14 .lib '../bulk_32nm.l'TT
15 .unprotect
16
17
18 ********************************
19 **      Parameter setting     **
20 ********************************
21 .param xvdd = 0.9
22 .param xvss = 0
23 .param wp = 64n
24 .param wn = 64n
25 .param cycle = 1n
26 .param simtime = 5n
27
28
29 ********************************
30 **      Circuit description   **
31 ********************************
32 .subckt inv in out vdd vss
33 m1 out in vdd vdd pmos w=wp l=32n
34 m2 out in vss vss nmos w=wn l=32n
35 .ends
36
37 xinv_1 input output vdd vss inv
38 cload  output vss 5f
39
```

```
*****************************
**     Power declaration     **
*****************************
vvdd      vdd      0     xvdd
vvss      vss      0     xvss


*****************************
**     Input declaration     **
*****************************
vin       input    0     pulse(xvdd 0 1n 0.1n 0.1n 'cycle*0.45' cycle)
```

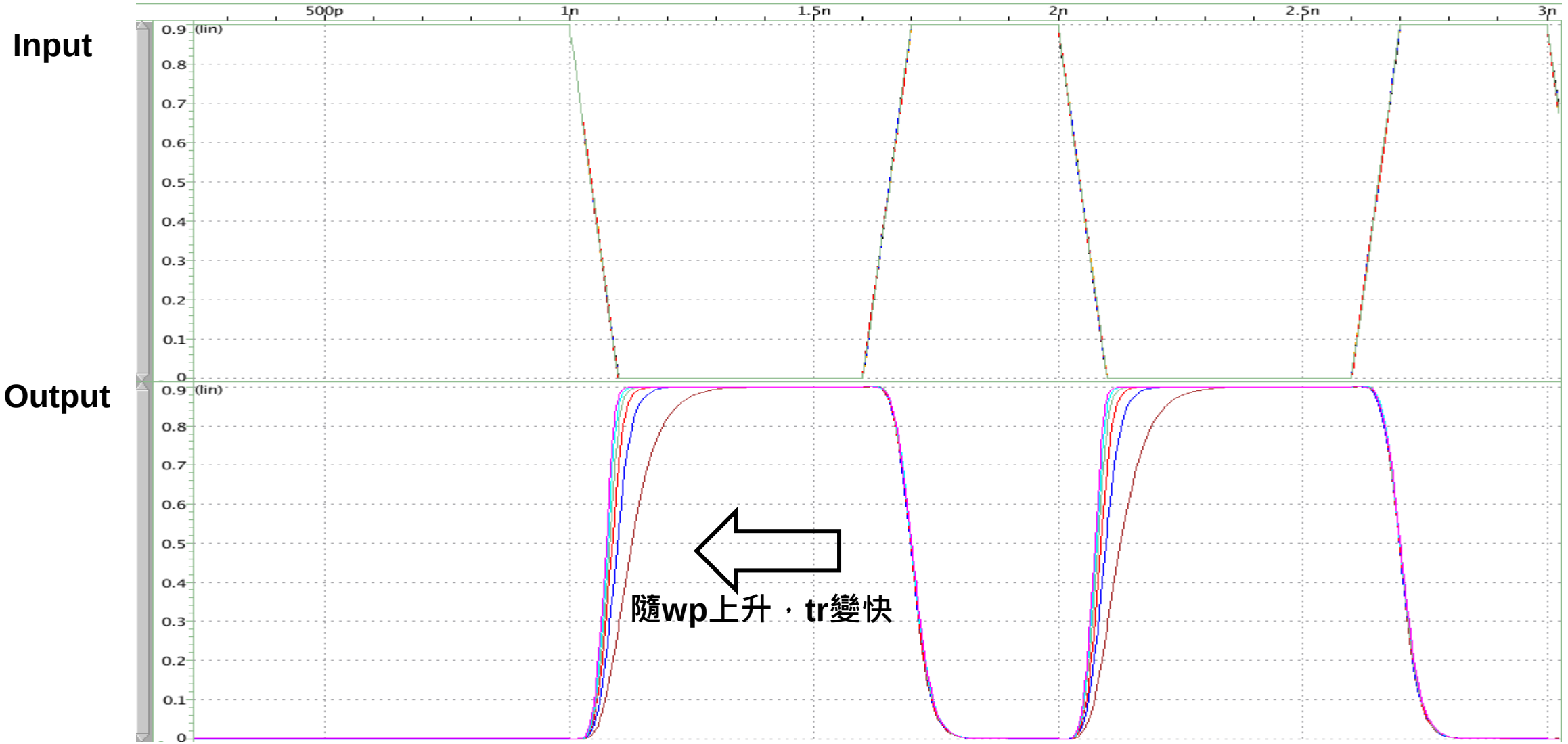
```
*********************************
**      Analysis setting       **
*********************************

.tran 1p simtime sweep wp 64n 384n 64n


.end
```

以1ps的間隔模擬總共simtime的時間做暫態分析(sweep wp變數，從wp=64n開始每step=64n重複做一次模擬到wp=384n)

尋找輸出： .tr0檔案 (for Transient analysis)



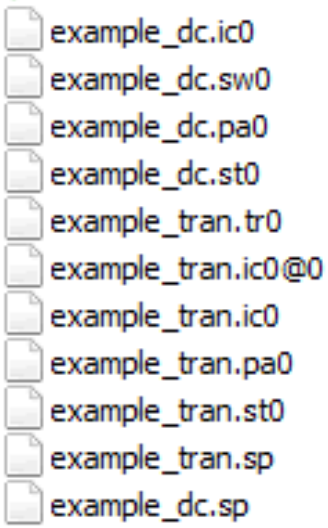
執行模擬指令以及開啟波形軟體

```
ee05 [dicta01/example_1]%
ee05 [dicta01/example_1]%
ee05 [dicta01/example_1]%
ee05 [dicta01/example_1]%
ee05 [dicta01/example_1]%
ee05 [dicta01/example_1]%
ee05 [dicta01/example_1]%
ee05 [dicta01/example_1]% hspice -i example_dc.sp
```

or

```
ee05 [dicta01/example_1]%
ee05 [dicta01/example_1]%
ee05 [dicta01/example_1]%
ee05 [dicta01/example_1]%
ee05 [dicta01/example_1]%
ee05 [dicta01/example_1]%
ee05 [dicta01/example_1]%
ee05 [dicta01/example_1]% hspice -i example_dc.sp -o
```

不會輸出.lis檔案(但會顯示在螢幕上)




```
linux15 [dicta02/example]%
linux15 [dicta02/example]%
linux15 [dicta02/example]%
linux15 [dicta02/example]% wv &
```

開啟波形軟體