IPC based closed loop control of decentralized Servo Drives with eXtreme Fast Control (EtherCAT XFC)

Conference Paper · November 2007

CITATION
1

READS
166

2 authors:

Jens Onno Krah
Technische Hochschule Köln
135 PUBLICATIONS **704** CITATIONS
SEE PROFILE

Christoph Klarenbach
Beckhoff Automation Gmbh & Co.KG
18 PUBLICATIONS **62** CITATIONS
SEE PROFILE

IPC based closed loop control of decentralized Servo Drives with eXtreme Fast Control (EtherCAT XFC)

Prof. Dr.-Ing. Jens Onno Krah,
M. Sc. Christoph Klarenbach,

Cologne University of Applied Science

Faculty of Information, Media and Electrical Engineering

Introduction

By using an FPGA and ΣΔ analog to digital conversion (ADC) technology, a Servo Drive can combine the advantages of analog and digital control at no trade-off. Utilizing EtherCAT as an extremely fast Fieldbus and an Embedded PC with Floating-Point-Unit (FPU), a Motion Control system with centralized feedback control can be built as open system. Motion Control is going to be freely programmable with the option of using Intellectual Property (IP). To customize Servo Loops there will be no need for interaction with a Servo Drive manufacturer any more.

1. Motion Control with Servo Drives

For a long time, high performance motion control was associated with the direct current (DC) motor. The power stage consisted of four power electronic switches and analog current control was implemented using operational amplifiers. Even in the velocity loop analog circuits were often used and a separate tacho sensor generated the velocity feedback signal. Usually a dedicated motion controller was employed for the position control loop. The Motion Controller was feeding the velocity loop command of the of the Servo Drive. The actual value of the position was made available by an Encoder.

Over the years the typical Servo Drive was modified step by step:

- To increase the reliability and to reduce the motor size electronic commutation (6-Step) is introduced. (Brushless direct current – BLDC)
- To reduce the torque ripple, brushless motors are commutated sinusoidally. (Brushless alternating current – BLAC)
- Further motor size reduction is achieved by introducing single tooth windings.
- Instead of using a separate analog tacho sensor the velocity feedback signal is generated by numerical differentiation of the digital feedback position signal.
- Current and velocity control loops are realized by sampling control and using µController technology. Due to the digitalization parameters are exactly reproducible instead “adjusting a potentiometer to 1:00 pm”.
- Command values from analog inputs are replaced by digital fieldbus process data objects.

Digitalization also allows implementation of more complex control algorithms:

- Field oriented control (FOC) of BLAC and induction machines (IM).
- Predictive algorithms to reduce the switching frequency without reducing the control loop bandwidth (Smith Predictor).

- Model based algorithms to increase the control loop gain.
  (Luenberger Observer)
- Consideration of non-linear behavior due to iron saturation in case of high current operation.
- Motion control functionality is implemented more and more as a software module inside the Servo Drive or the machine controller (PLC) / Industrial PC (IPC).

With Sercos – the “Servo Fieldbus” – closing all control loops inside the drive is more or less the open standard in the machine tool industry. By focusing on the control theory this decentralized approach is a great advantage because the dead time of the fieldbus is not reducing the bandwidth (phase margin) of the control loops. In many industrial applications this approach is successful used.

A disadvantage of the µController based digital control is the associated dead time of sampling control $T_D = T_S/2$. The sampling time is usually in a range between 50 and 250 µs. By using switching frequencies up to 10 kHz this is a good fit. With higher switching frequencies the sampling control can significantly limit the achievable current loop bandwidth.

2. Is the intelligent Servo Drive a “dead end”?

Today, a competitive situation by offering the motion control functionalities has evolved between the producers of Servo Drives and the machine controller manufacturers in. The product management of the Servo Drive vendors did push more and more computing power into the Servo Drives. Thus, today most Servo Drives offer a more or less powerful PLC-functionality (IEC 61131) inside the drive.

Due to different requirements there are only a few common application specific strategies visible:

- In CNC and robotic applications the motion control functionality is realized in nearly all solutions centralized inside the machine controller (IPC):
  - \+ The algorithms of coupled Servo Drives are calculated with at least one fast CPU – often with floating-point-unit (FPU).
  - \- High fieldbus bandwidth is required – at least like Sercos.
- In special technology applications, like for example a flying saw the motion control functionality is often realized inside the Servo Drive:
  - \- The Servo Drive needs a powerful µController with large memory
  - \+ High fieldbus bandwidth is not required.
- In camming applications a clear trend is not visible. Closing the loops inside the drive is traditionally the preferred solution in Europe – even with analog Servo Drives. In the US it is more preferred to close only the current loop inside the drive. Position and velocity loop are often closed by the machine controller.

Especially in applications with several axes the distributed computing power of the Servo Drives is utilized extremely inefficient:

- There are no intentions to partition the algorithms (computing load) over the distributed CPUs.
- The execution of the Servo Drive PLC programs is more similar to high level language interpretation (BASIC) than to executing a compiled program (C). (Only the Danaher Motion ServoStar© is utilizing a drive internal compiler) [1].

- A significant part of the µController computing power is also used by some fieldbus interfaces. (For example by Powerlink).

Another disadvantage of closing all loops inside the Servo Drive is that the user can only parameterize the control loops, but he can't modify the control structure itself. The user can **configure** and **parameterize Motion Control**, but motion control is ***not* freely programmable**! This has lead to the situation that some Servo Drives offer up to 1000 parameters to configure these drives. This is unacceptable in terms of usability.

Due to cost reasons Servo Drive vendors can only install fast µControllers in larger drives (> 1 kW) because of the additional effort of the computing power. But in nearly all applications the Servo Drive PLC functionality is not able to replace the machine controller PLC. Therefore, installing more and more computing power into Servo Drives is a dead end.

3. A new Approach: the FPGA based Servo Drive

In this article a new approach is presented where the Servo Drive control functionality is not using a dedicated µController any more. A Field Programmable Gate Array (FPGA) – programmed in VHDL – is used instead. This innovative approach is based on several new technologies:

- EtherCAT Fieldbus with Distributed Clocks (DC) and eXtreme Fast Control (XFC)
- ΣΔ-Modulator for Analog to Digital Conversion (ADC)
- Digital Encoder Interfaces (EnDAT 2.2, BiSS or just A quad B)
- FPGA based digital signal processing (DSP)
- Flexible 6-phase PWM in VHDL
- Soft Core µController in FPGAs (System on a programmable chip: NIOS II)
- Embedded PC/PLC with Floating-Point-Unit

4. EtherCAT Fieldbus with Distributed Clocks (DC) and eXtreme Fast Control

EtherCAT™ is an Ethernet based real time fieldbus. The following list shows the special features oft the EtherCAT fieldbus [2]:

- Standard Ethernet hardware: RJ45 connector, transformer, cable and PHY
  (Also standard MAC in the IPC / EtherCAT Master)
- The slave interface connection needs only an ASIC or FPGA (I/O, drive, …)
- The protocol is open and standardized:
  EtherCAT is IEC standard (IEC/PAS 62407, IEC 61158)
  EtherCAT is part of ISO 15745-4
- Distributed Clocks (DC) - high precision synchronization (<< 1 µs) due to the continuous adjustment of distributed clocks within the slave interface
- eXtreme Fast Control: Within one sampling period
  - the actual values are first read via EtherCAT from a bus terminal (Encoder)
  - then the IPC calculates with the control algorithm a new command value
  - and these values are immediately send via EtherCAT to the bus terminal (Drive)

An EtherCAT-slave-interface is available as FPGA IP-Core (Intellectual Property). To save FPGA resources the design engineer can disable not requested functionality of

the IP-Core. Only two PHYs and two RJ45 connectors with some passive components are necessary in addition to the used FPGA logic elements.

The process data, commands and actual values, are processed inside the FPGA according to a VHDL program (utilizing “hardware”) with no delay. Parameters like gains and monitor functions (EtherCAT: Mailbox) are processed from an FPGA internal soft-core-processor (NIOS II).

5. ΣΔ-Modulator for Analog to Digital Conversion (ADC)

The quality of analog-to-digital conversion is a key factor of high performance Servo Drives. Especially the motor phase-current measurements are not trivial. Traditionally these currents are measured with compensated hall sensors. These sensors are converting the phase currents into proportional electrically isolated voltages/signals witch are feeding successive approximation (SAR) ADCs. Suppressing the current ripple with a low pass filter and its phase lag to avoid aliasing is not common. Instead, most drive suppliers sample the currents at a special point in time within the PWM cycle where the current value shows no distortion due to the ripple. Very often additional analog comparators are used to detect over current with no sampling delay to be able to disable the power stage as fast as possible.

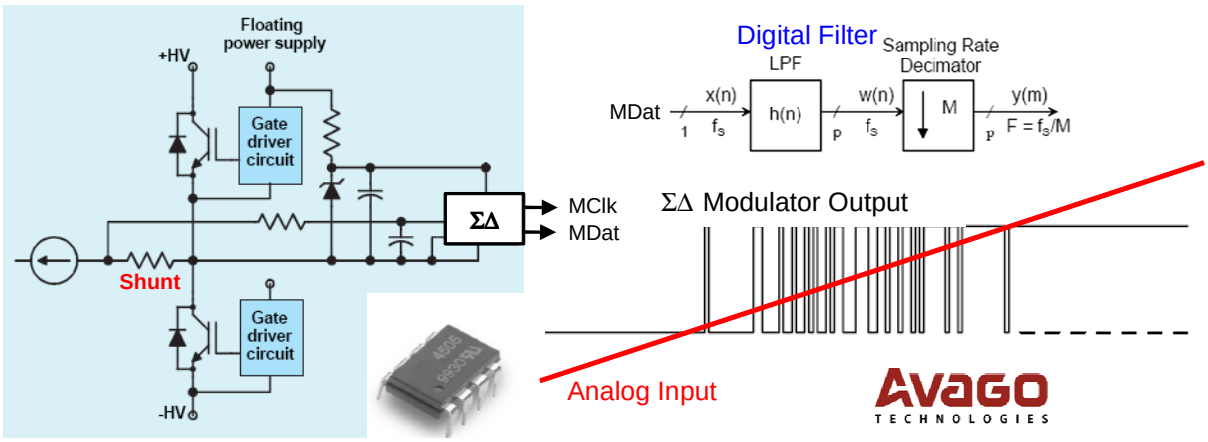

Fig. 1: An integrated ΣΔ-modulator generates an isolated bit-stream (digital) from the analog input signal.

Thanks to the new integrated ΣΔ-ADCs the current control quality can be significantly increased with less effort in cost and printed circuit board space. Several semiconductor suppliers are offering integrated circuits with internal galvanic isolation (Avago, Ti, Analog Devices), fig. 1. The differential analog input of these ICs can be directly connected to a shunt for current measurement. The (isolated) bit-stream is designed to be directly connected to digital circuits like an FPGA. Signal transmission, filtering and also sampling is carried out in the digital domain. If the ΣΔ-modulator is placed very near to the shunt, signal distortion during transmission, filtering or sampling from the fast switching power stage (EMI) is by principle not possible.

The bit-stream is processed within the FPGA with three parallel decimation filters in three channels:

- Very fast for over current detection (2% precision)
- Standard with about 12-Bit precision for the proportional-component of the PI-controller

- High precision (integration over one PWM period) for the integral-component of the PI-controller

The patent of this new current control scheme is pending.

6. Digital Encoder Interfaces (EnDAT 2.2, BiSS, A quad B)

Digital encoder interfaces allow a fast transmission of the high resolution position (motor shaft angle) data of modern sine-cosine-encoders. Even long cables are not reducing the position signal quality. In addition to the process data (position) these digital interfaces also allow to store and read encoder or motor parameters (electronic type plate). The optional transmission of the motor temperature sensor information can also save separate wires in the cables between motor and drive, fig. 2.

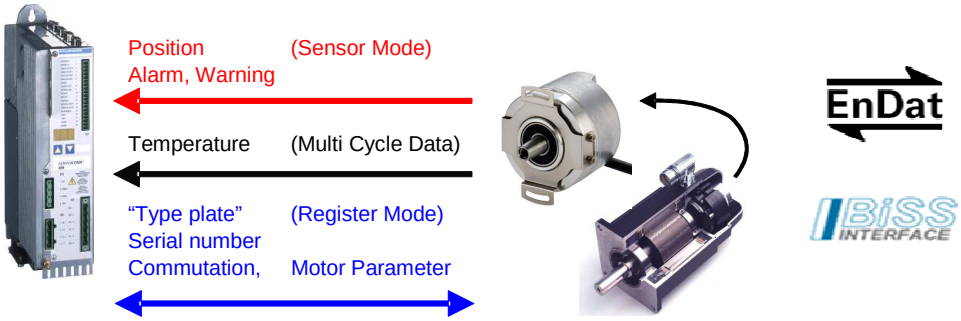

Fig. 2: Using a digital encoder interface the drive can also access additional parameters. Transmission of EMI sensible analog signals is not necessary.

Classical µControllers offer special hardware support for standard A quad B (TTL) encoders. Most controllers have to use an interrupt to use the zero marker channel. Fine interpolation, EnDAT 2.2 (Heidenhain) or BiSS (IC Haus) are never supported by µController hardware.

An interface with fine interpolation (+6 Bit) for standard TTL-encoders and/or the EnDAT 2.2 / BiSS interface or a resolver digital conversion are perfect for FPGA implementations. These VHDL-modules are very cost efficient and need only a few external driver circuits [3, 4].

The EtherCAT distributed clocks functionality (sync-signal) is used to start / synchronize the encoder position latch process. This is also an FPGA internal VHDL program module. The position data is routed internally inside the FPGA with no additional delay to the EtherCAT IP-Core. The next EtherCAT-frame can transmit the process data to the PLC/IPC.

It is not longer necessary to connect the feedback (encoder / resolver) directly to the Servo Drive. It is now also possible to close the servo loop by connecting the feedback to a separate EtherCAT bus coupler without bandwidth limitations.

7. FPGA based digital signal processing

Signal processing like control algorithms are traditionally implemented with analog operational amplifiers or with digital signal processors (DSP). This functionality can also be done with digital FPGA signal processing blocks. Thanks to the massive parallel execution even complex algorithms can be executed in less than 100 ns. A CPU with its sequential processing is much slower in executing complex control algorithms. **FPGA based control technology can combine the advantages of analog and digital control without any drawback:**

- Analog control → no dead time, no aliasing
- DSP based control → reproducible parameters, complex algorithms

Using the FPGA DSP-functionality even a complex current controller with more than 20 kHz power stage PWM frequency can be realized completely digitally. A µController based architecture would reduce the achievable bandwidth due to the slower sampling frequency.

8. Flexible 6-phase PWM in VHDL

Several µControllers optimized for motion control offer a special 6-phase PWM for the 6 inverter switches (IGBT or MOSFET). A value in a register is compared with a triangular carrier signal for each motor phase. The blocking times for the three half bridges are also freely adjustable. Space vector modulation (inverse Clarke transformation) has to be carried out in software. Over modulation or block commutation is not possible [5].

These limitations disappear by implementing the 6-phase-PWM in VHDL. In addition to a standard PWM the following features are supportable:

- Space Vector Modulation (SVM)
- Modified Space Vector Modulation (MSVM - one phase is not switching)
- Over modulation / Block commutation
- Boot strap gate driver model for each motor phase
- Optional PLL to synchronize the PWM with the motion controller
- On line configuration of the switching frequency in 1 Hz steps
- On line configuration of the blocking time in 20 ns steps

9. Soft Core µController in FPGAs

For initialization and to process the service data objects (SDOs) a µController is still a successful approach. The “system on a programmable chip” soft-core microcontroller NIOS II from Altera is ideally suited for this purpose. The program for the µController and the FPGA configuration can be permanently stored in a parallel flash memory. According to the selected FPGA type and the application requirements an additional external RAM can be necessary. The clock frequency of the soft-core µControllers NIOS II is usually in the range of 50 MHz. This is more than enough for initialization and service data processing [6, 7].

Fig. 3 shows the block diagram of a field oriented drive for FPGA implementation. To reduce the complexity not all signals for initialization and configuration are shown.

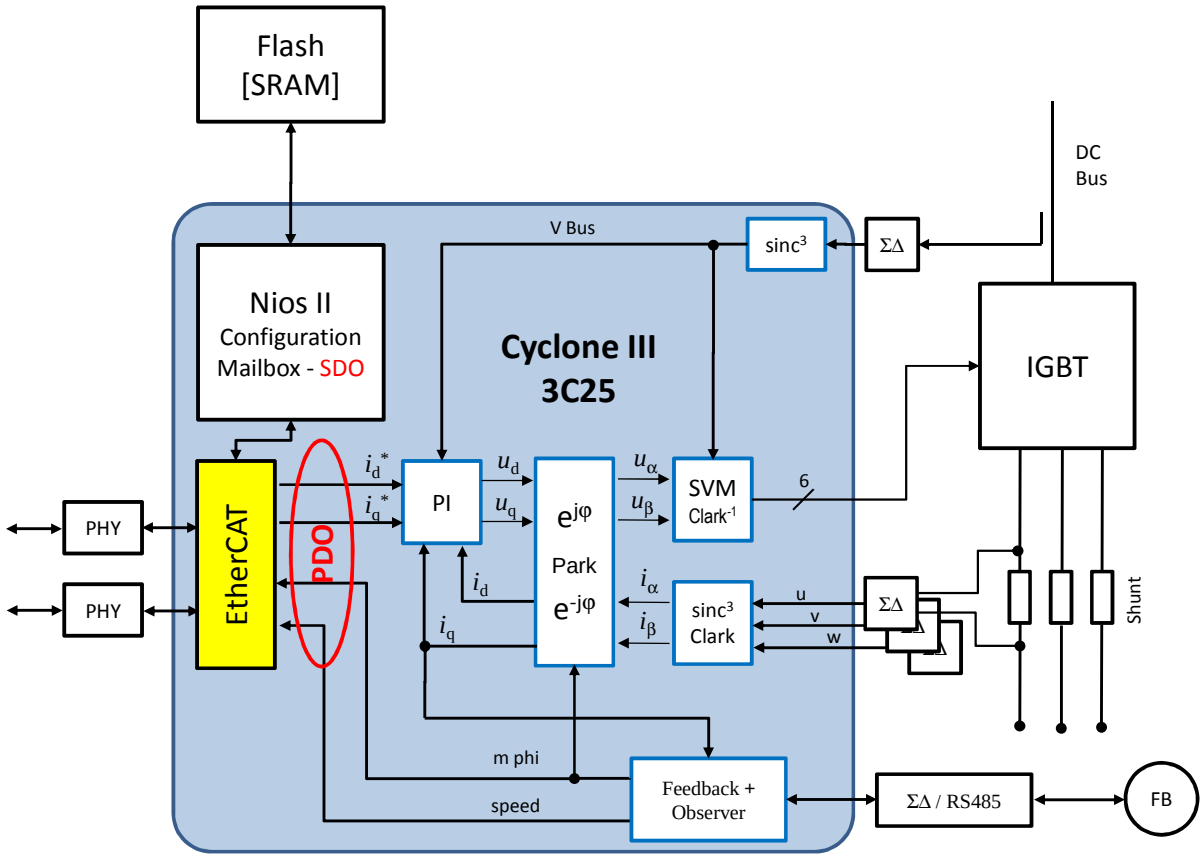

Fig. 3: Due to the new FPGA-based concept are in addition to the FPGA only a few integrated circuits necessary to build a Servo Drive

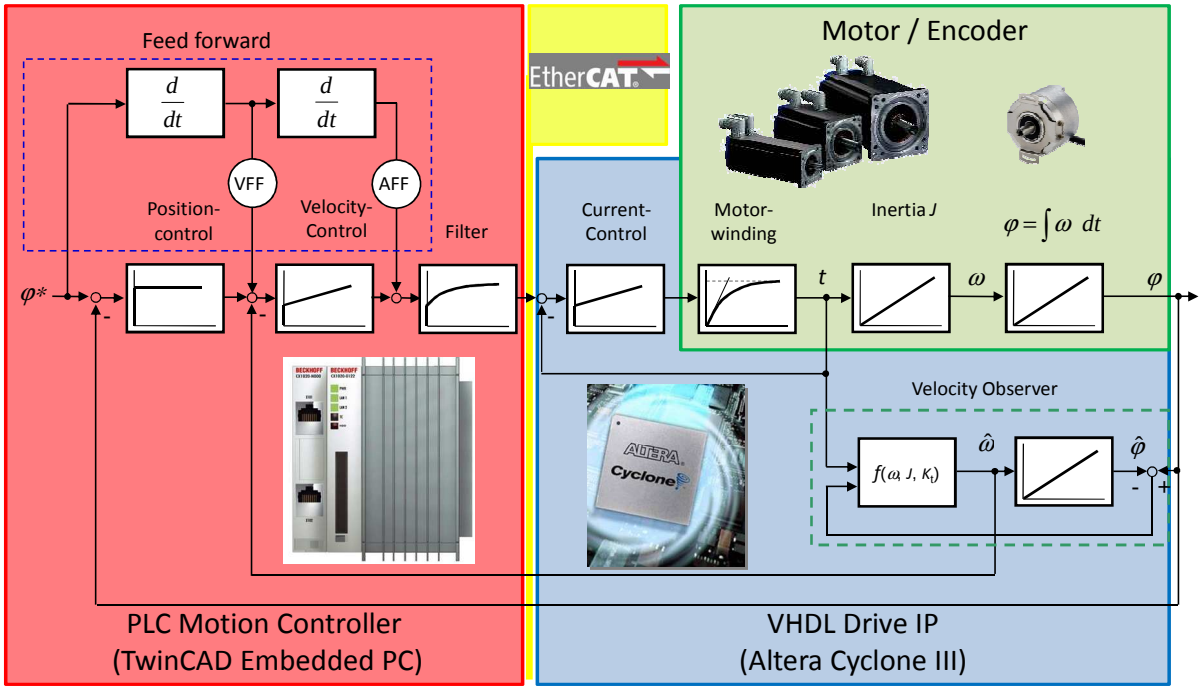

Fig. 4: Using the standard cascade control only the current loop is closed inside the FPGA. Velocity and position loop of one or more servo axes are closed without additional dead time in the IPC via EtherCAT XFC.

The soft-core controller NIOS II can process EtherCAT Mailbox data to configure the drive functionality via the dual port RAM of the EtherCAT IP-Core. In case of a fieldbus error the CPU can shut down the servo motor according to a preconfigured stop modus. This can be done using a second velocity loop executed from the NIOS II controller, or with a “controlled” active current short cutting of the servo motor.

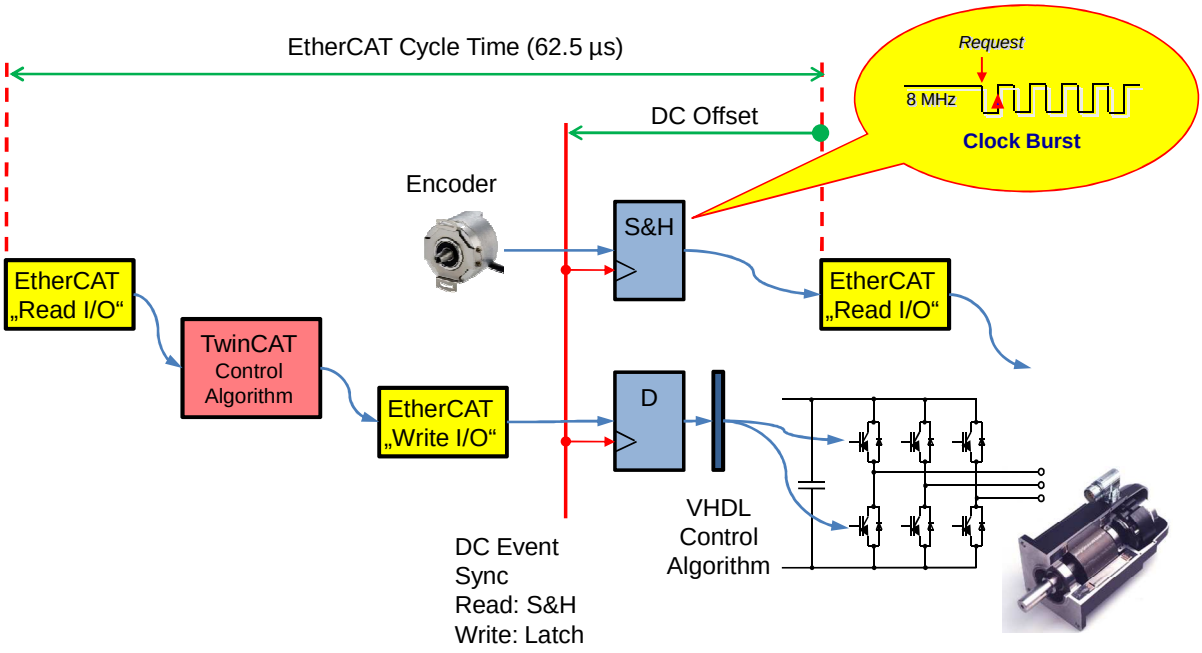

Fig. 5: Time schedule of velocity and position loop:
1. EtherCAT “Read I/O” to read the actual values
2. TwinCAT calculates the control algorithms
3. EtherCAT “Write I/O” to write the current command
   The FPGA internal synchronization uses the DC-sync signal:
   - Latch of the position
   - Latch of the new current command

10. Embedded PC/PLC with Floating-Point-Unit

Today, most compact Programmable Logic Controllers (PLCs) use Intel compatible processors with Floating-Point-Unit (FPU). The Embedded PC CX1020 from Beckhoff Automation is such a compact PLC, fig. 4:

- Intel Celeron M ULV, 1 GHz Clock frequency
- 64MB DDR RAM (extendable up to 1 Gbyte)
- Microsoft Windows XP Embedded
- TwinCAT PLC IEC1131-3 Multi-PLC
- EK1110 EtherCAT Extension

The software TwinCAT PLC converts a standard PC with Windows operating system in a real time Programmable Logic Controller (PLC) with cycle times of 50 µs and up. The task scheduler is configured in a way, that Windows gets only the remaining CPU time, that is not requested from the real time PLC tasks. Due to the really fast floating-point-unit even complex control algorithms for one or more servo axes are easily programmable in a high level language with excellent development support. The TwinCAT integrated development environment allows Monitoring, Powerflow, Breakpoint, Single-Step and ScopeView [8].

Conclusion

In this paper a new FPGA based Servo Drive concept is presented, where the position loop and the velocity loop are closed in an IPC based PLC via EtherCAT with eXreme Fast Control (XFC) and Distributed Clocks (DC). The advantages of this EtherCAT / FPGA Servo Drives are:

- The Servo Drive can combine the advantages of analog and digital control at no trade-off due to digital signal processing inside the FPGA.
- The position feedback from motor and/or load can be connected via EtherCAT bus couplers to close the loops.
- A standard frequency inverter with an FPGA based EtherCAT interface can be part of a high performance Servo Drive.
- Customizing the control structure can be done easily in a IEC 61131 high level language by coding floating point algorithms.
- There is no bandwidth limitation by closing the loops via EtherCAT XFC up to 8 kHz switching frequency (T_a = 62.5 µs)
- The open architecture is forcing innovations: Motion Control IP is possible.

Literature

1. www.danahermotion.net
2. www.ethercat.org
3. Jens Onno Krah, R. Vonderbank, J. Bücher, R. Berger: Resource Optimized BiSS Master Interface for High Resolution Encoders, *PCIM Power Conversion Intelligent Motion*, Nürnberg, June 2006 pp 479-484.
4. Jens Onno Krah, H. Schmirgel, M. Albers: FPGA Based Resolver to Digital Converter Using ΣΔ Analog to Digital Technology, *PCIM Power Conversion Intelligent Motion*, Nürnberg, June 2006 pp 931-936.
5. J. O. Krah, J. Holtz: High-Performance Current Regulation and Efficient PWM Implementation for Low Inductance Servo Motors. *IEEE Transactions on Industry Applications*, Vol. 35, No. 5, Sept/Oct 1999, pp. 1039-1049.
6. www.altera.com
7. J. O. Krah, K. Neumayer: System-on-a-Programmable-Chip – Enhanced Solutions for High Performance Servo Drives, PCIM Power Conversion Intelligent Motion, Nürnberg, May 2003, pp. 105-110.
8. www.beckhoff.de