Project1

ID	Task Mode	Task Name	Duration	Start	Finish
1		Scope and preliminars	21 days	Wed 01.04.20	Wed 29.04.20
2		Kick-Off Meeting	1 day	Wed 29.04.20	Wed 29.04.20
3		SW and HW Development for 1st PCB	23 days	Thu 30.04.20	Mon 01.06.20
4		Report of tests with 1st PCB	1 day	Tue 02.06.20	Tue 02.06.20
5		SW for EtherCAT comm/control features	16 days	Wed 03.06.20	Wed 24.06.20
6		Report of tests with EtherCAT comm/control features	1 day	Thu 25.06.20	Thu 25.06.20
7		SW for EtherCAT Data features	23 days	Fri 26.06.20	Tue 28.07.20
8		Report of tests with EtherCAT data features	1 day	Wed 29.07.20	Wed 29.07.20
9		HW Development for 2nd PCB	15 days	Thu 30.07.20	Wed 19.08.20
10		Final test with 2nd PCB	3 days	Thu 20.08.20	Mon 24.08.20
11		Final presentation	1 day	Wed 26.08.20	Wed 26.08.20
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13		SoSe Examination Period	32 days	Wed 29.07.20	Thu 10.09.20

Predecessors	Resource Names
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