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Component Placement Checklist for the LAN9252, 64-pin SQFN Package

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Component Placement Checklist for LAN9252

Information Particular for the 64-pin SQFN Package

LAN9252 SQFN Port A Copper Twisted Pair Phy Interface:

1. If the Auto MDIX functionality is enabled, place the 49.9 Ω TX termination pull-up (TXPA, pin 53) as close to the LAN9252 as possible. If the Auto MDIX feature is disabled in the application, place this pull-up termination as close as possible to the magnetics.

2. If the Auto MDIX functionality is enabled, place the 49.9 Ω TX termination pull-up (TXNA, pin 52) as close to the LAN9252 as possible. If the Auto MDIX feature is disabled in the application, place this pull-up termination as close as possible to the magnetics.

3. Place the 49.9 Ω RX termination pull-up (RXPA, pin 55) as close to the LAN9252 as possible.

4. Place the 49.9 Ω RX termination pull-up (RXNA, pin 54) as close to the LAN9252 as possible.

5. Place the four optional, low-valued, common mode capacitors for each differential signal as close as possible to the magnetics. They should be placed as to create the smallest possible stub.

LAN9252 SQFN Port B Copper Twisted Pair Phy Interface:

1. If the Auto MDIX functionality is enabled, place the 49.9 Ω TX termination pull-up (TXPB, pin 62) as close to the LAN9252 as possible. If the Auto MDIX feature is disabled in the application, place this pull-up termination as close as possible to the magnetics.

2. If the Auto MDIX functionality is enabled, place the 49.9 Ω TX termination pull-up (TXNB, pin 63) as close to the LAN9252 as possible. If the Auto MDIX feature is disabled in the application, place this pull-up termination as close as possible to the magnetics.

3. Place the 49.9 Ω RX termination pull-up (RXPB, pin 60) as close to the LAN9252 as possible.

4. Place the 49.9 Ω RX termination pull-up (RXNB, pin 61) as close to the LAN9252 as possible.

5. Place the four optional, low-valued, common mode capacitors for each differential signal as close as possible to the magnetics. They should be placed as to create the smallest possible stub.

LAN9252 SQFN Port A Copper Twisted Pair Phy Magnetic:

1. Place the 0.022 μF TX/RX Channel Center Tap termination capacitor as close to the magnetics as possible.

2. Place the 75 Ω cable side center tap termination resistors and the 1000 ρF, 2KV capacitor ($C_{magterm}$) cap as close to the magnetics as possible.

LAN9252 SQFN Port B Copper Twisted Pair Phy Magnetic:

1. Place the 0.022 μF TX/RX Channel Center Tap termination capacitor as close to the magnetics as possible.

2. Place the 75 Ω cable side center tap termination resistors and the 1000 ρF, 2KV capacitor ($C_{magterm}$) cap as close to the magnetics as possible.

Copper Twisted Pair RJ45 Connectors Ports A & B:

1. Place the RJ45 connector, the magnetics and the LAN9252 SQFN as close together as possible.

2. If No. 1 is not possible, keep the RJ45 connector and the magnetics as close as possible. This will allow remote placement of the LAN9252 SQFN.

3. Select and place the magnetics as to set up the best routing scheme from the LAN9252 SQFN to the magnetics to the RJ45 connector. There are many styles and sizes of magnetics with different pin outs to facilitate this operation. Investigate Tab-Up & Tab-Down RJ45 connectors in order to facilitate layout.

4. Place the Unused Wire Pair termination resistors and the 1000 ρF, 2KV capacitor (C_{rjterm}) as close to the RJ45 connector as possible.

5. Make sure to not place any other components in or near the TX Channel & RX Channel lanes of the PCB. These lanes should be clear of any other signals and components.

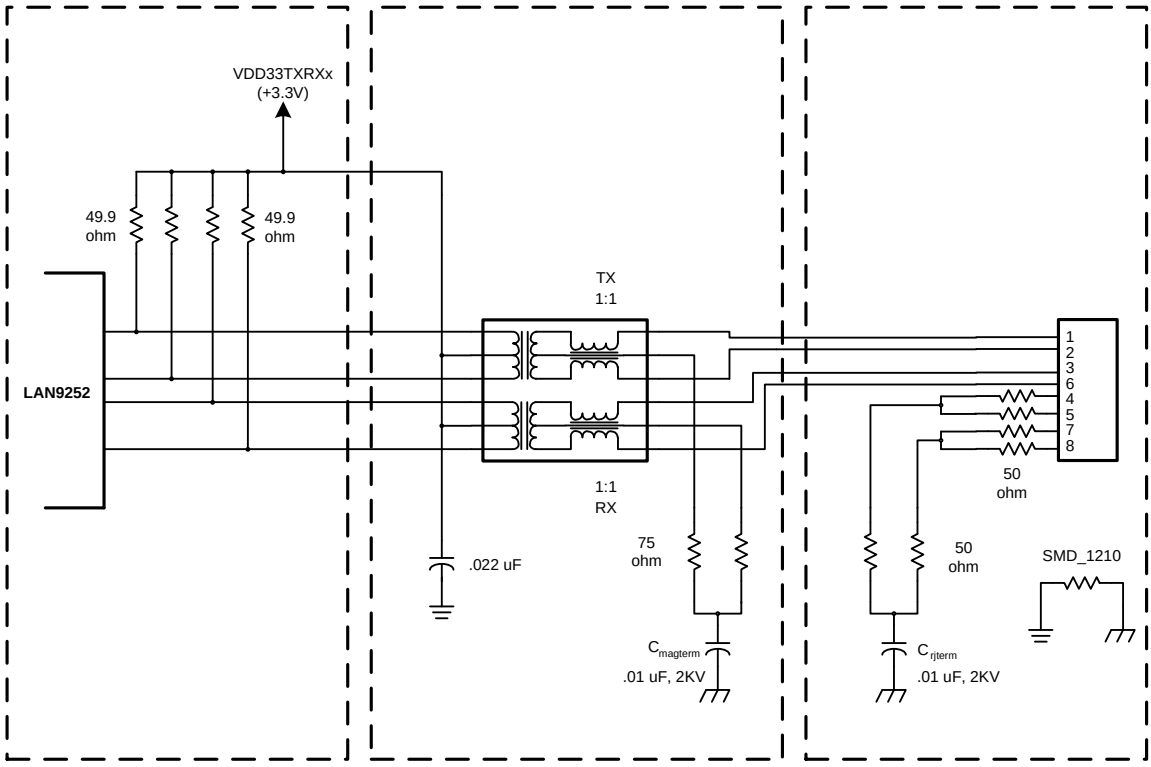

Figure No.1 Indicating Component Placement

The figure above shows the pull-up terminations for the TXPx & TXNx signals placed close to the LAN9252 for an Auto MDIX enabled application. For an Auto MDIX disabled application, these same two resistors should be located as close as possible to the magnetics.

LAN9252 SQFN Port A Fiber Phy (100BASE-FX) Interface:

1. Place the split-load terminations for the PECL signals of the TX channel (TXPA, pin 53) as close as possible to the Fiber module on the PCB.

2. Place the split-load terminations for the PECL signals of the TX channel (TXNA, pin 52) as close as possible to the Fiber module on the PCB.

3. Place the split-load terminations for the PECL signals of the RX channel (RXPA, pin 55) as close as possible to the LAN9252 IC on the PCB.

4. Place the split-load terminations for the PECL signals of the RX channel (RXNA, pin 54) as close as possible to the LAN9252 IC on the PCB.

LAN9252 SQFN Port B Fiber Phy (100BASE-FX) Interface:

1. Place the split-load terminations for the PECL signals of the TX channel (TXPB, pin 62) as close as possible to the Fiber module on the PCB.

2. Place the split-load terminations for the PECL signals of the TX channel (TXNB, pin 63) as close as possible to the Fiber module on the PCB.

3. Place the split-load terminations for the PECL signals of the RX channel (RXPB, pin 60) as close as possible to the LAN9252 IC on the PCB.

4. Place the split-load terminations for the PECL signals of the RX channel (RXNB, pin 61) as close as possible to the LAN9252 IC on the PCB.

CTP / FX-SD / FX-LOS Configuration Pins:

1. There are no component placement issues associated with the CTP / FX-SD / FX-LOS configuration terminations of the LAN9252 SQFN.

+3.3V Power Supply Connections:

1. Place the (1) VDD33 decoupling capacitor for the LAN9252 SQFN as close to the power pin as possible. Using an SMD_0603 package will make this task easier.

2. Place the (1) VDD33TXRX1 decoupling capacitor for the LAN9252 SQFN as close to the power pin as possible. Using an SMD_0603 package will make this task easier.

3. Place the (1) VDD33TXRX2 decoupling capacitor for the LAN9252 SQFN as close to the power pin as possible. Using an SMD_0603 package will make this task easier.

4. Place the (1) VDD33BIAS decoupling capacitor for the LAN9252 SQFN as close to the power pin as possible. Using an SMD_0603 package will make this task easier.

+1.8V to +3.3V Variable I/O Power Supply Connections:

1. Place the (5) VDDIO decoupling capacitors for the LAN9252 SQFN as close to each power pin as possible. Using an SMD_0603 package will make this task easier.

VDDCR:

1. VDDCR (pins 6, 24 & 38) each pin requires a 0.01 μF bypass capacitor and pin 6 requires a low ESR, 1.0 μF bulk capacitor placed as close as possible to pin 6.

2. VDD12TX1 (pin 56) and VDD12TX2 (pin 59) each require a 0.01 μF bypass capacitor placed as close as possible to pins 56 & 59.

Ground Connections:

1. There are no component placement issues associated with the LAN9252 SQFN ground connections. Since the PCB design has an all encompassing digital ground plane, the ground plane connections will automatically be as short as possible.

Crystal Connections:

1. Place the 25.000 MHz crystal and the associated 15 – 33 ρF capacitors as close together as possible and as close to the LAN9252 SQFN (OSCI, pin 1 & OSCO, pin 2) as possible. They should form a tight loop. Keep the crystal circuitry away from any other sensitive circuitry (address lines, data lines, Ethernet traces, etc.)

2. Place all the crystal components on the component side of the PCB with a digital ground plane layer on the next layer. This will minimize vias in the circuit connections and assure that all the crystal components are referenced to the same reference plane.

RBIAS Resistor:

1. Place the RBIAS resistor as close to pin 57 of the LAN9252 SQFN as possible.

Required External Pull-ups/Pull-downs:

2. There are no component placement issues associated with the External Pull-ups/Pull-downs required by the LAN9252 SQFN.

MII Interface:

1. If the designer has determined that series terminations are required, they should be placed appropriately. Any series termination should be placed as close as possible to the associated driver of the MII signal.

Host Bus Interface (HBI) Indexed Mode Pins:

1. There are no component placement issues associated with the Host Bus Interface on the LAN9252 SQFN.

Host Bus Interface (HBI) Multiplexed Mode Pins:

1. There are no component placement issues associated with the Host Bus Interface on the LAN9252 SQFN.

EtherCAT® Digital I/O Mode Pins:

1. There are no component placement issues associated with the EtherCAT Digital I/O interface on the LAN9252 SQFN.

Serial Peripheral Interface (SPI) Bus Pins:

1. There are no component placement issues associated with the Serial Peripheral Bus Interface on the LAN9252 SQFN.

GPI Pins:

1. There are no component placement issues associated with the GPI on the LAN9252 SQFN.

GPO Pins:

1. There are no component placement issues associated with the GPO on the LAN9252 SQFN.

LED Pins:

1. There are no component placement issues associated with the LED pins on the LAN9252 SQFN.

SYNC / LATCH Pins:

1. There are no component placement issues associated with the SYNC / LATCH pins on the LAN9252 SQFN.

I^2C EEPROM Pins:

1. There are no component placement issues associated with the I^2C EEPROM Interface supported by the LAN9252 SQFN device.

Dedicated Configuration Strap Pins:

1. There are no component placement issues associated with the Dedicated Configuration Strap Pins on the LAN9252 SQFN.

Miscellaneous:

1. Bulk capacitors for each power plane can reside anywhere on the plane they serve.

2. Place the SMD_1210 Digital Ground / Chassis Ground shorting resistor near the RJ45 in a logical place to short the two planes.