HAN'S ROBOT GERMANY

Development of an Embedded Communication Hub for the Acquisition of Sensor Data in a Robotic System

Project Thesis

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Draft (2020.04.22)

Contents

Background

- Robotic applications increasing their multi-connectivity
- Several industrial protocols
  - Fieldbuses standardized in IEC 61158 (CPFs)
  - DeviceNet and CANopen developed separately
- Industrial shift into the Real Time Connectivity
- Open-source developed tools that offer compatibility with specific vendors.

Real-Time Ethernet Networks

- Started during 2000s (evolution of the field buses)
- Referenced to IEC61784 part II
- Two strategies to ensure RT communication:
  - TDMA and CIP (Common Industrial Protocol)
- IEC based solutions might not be compatible with the IEEE 802.3 Ethernet
- TSN Group improves the Data Link and MAC Layer (IEEE802.1Qbv)

Licensed RTE Solutions:

PROFINET®

hilscher COMPETENCE IN COMMUNICATION

ETHERNET POWERLINK

EtherCAT®

Open source tools:

freeRTOS

CMSIS COMPLIANT ARM® Cortex™ Microcontroller Software Interface Standard

Open EtherCAT Society

Simple Open Source EtherCAT Master & Slave Society

Main goal

“Develop a device using open-source tools to read out sensor data from a robot axis and it will be able to be interfaced in a RTE Network.

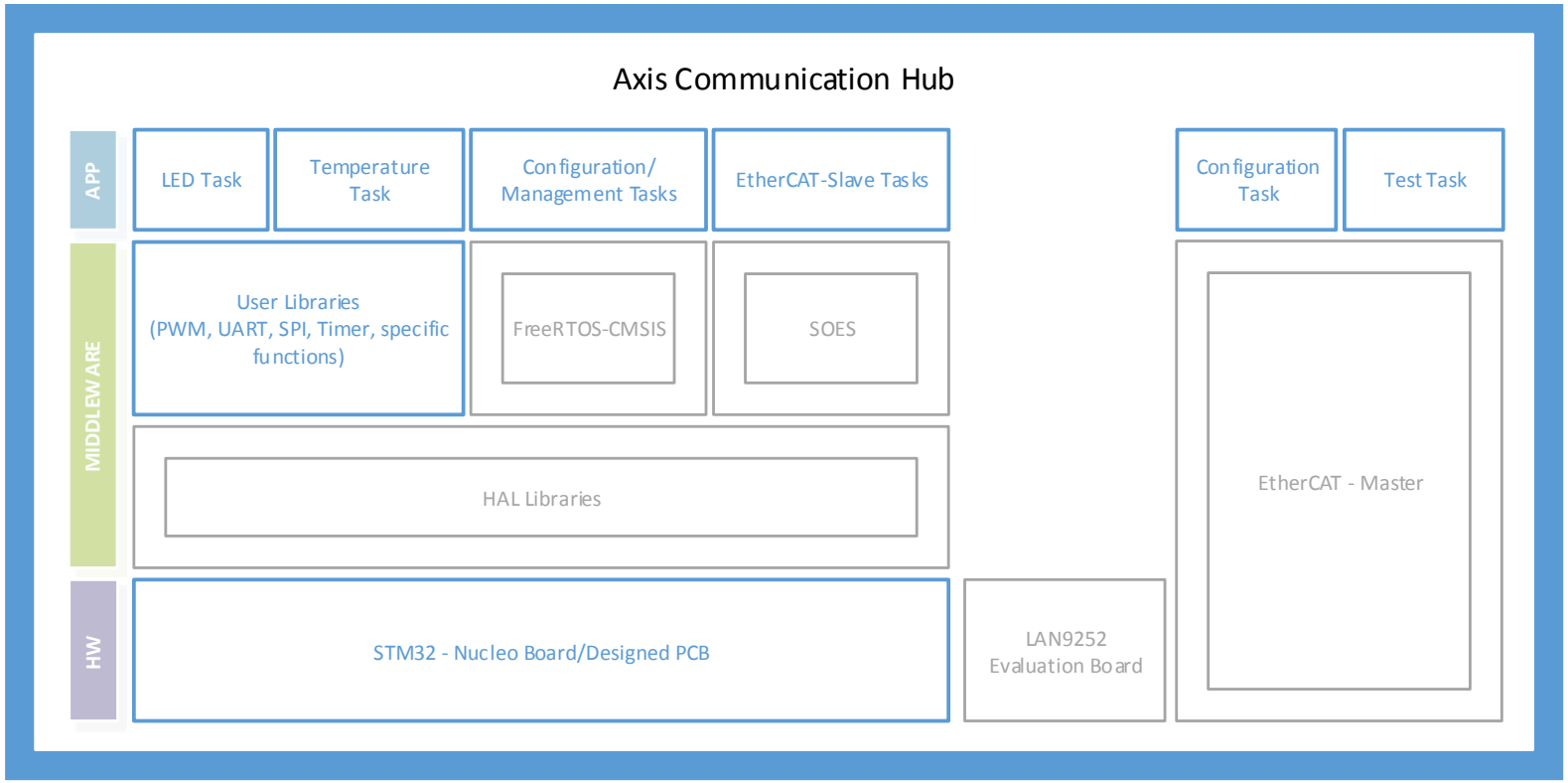
The device could be used afterwards as a test platform within an industrial environment to characterize its compatibility with the ongoing IEC/IEEE 60802 TSN Profile for Industrial Automation.”

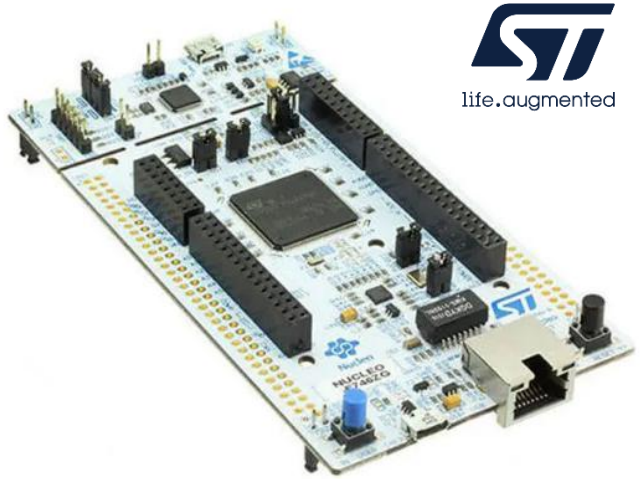
Specific goals

- To specify the requirements of the system
  - Taking into account the state of the art for RTE Industrial Networks
- To develop the embedded system as a functional EtherCAT Slave Device
  - Integrating FreeRTOS-CMSIS with SOES (Open-source tools)
  - Integrating the LAN9252 (SoC over SPI)
  - Reading out of axis temperature sensors
  - Controlling the axis LED Ring (WS2812b)
  - Designing the required user application libraries
- To design and manufacture a PCB prototype using Altium Designer
- To test and report the system functionality

Solution proposal

- Layered structure of functional blocks
  - Main HW: STM32Nucleo Board, Microchip LAN9252 SPI Eval Board



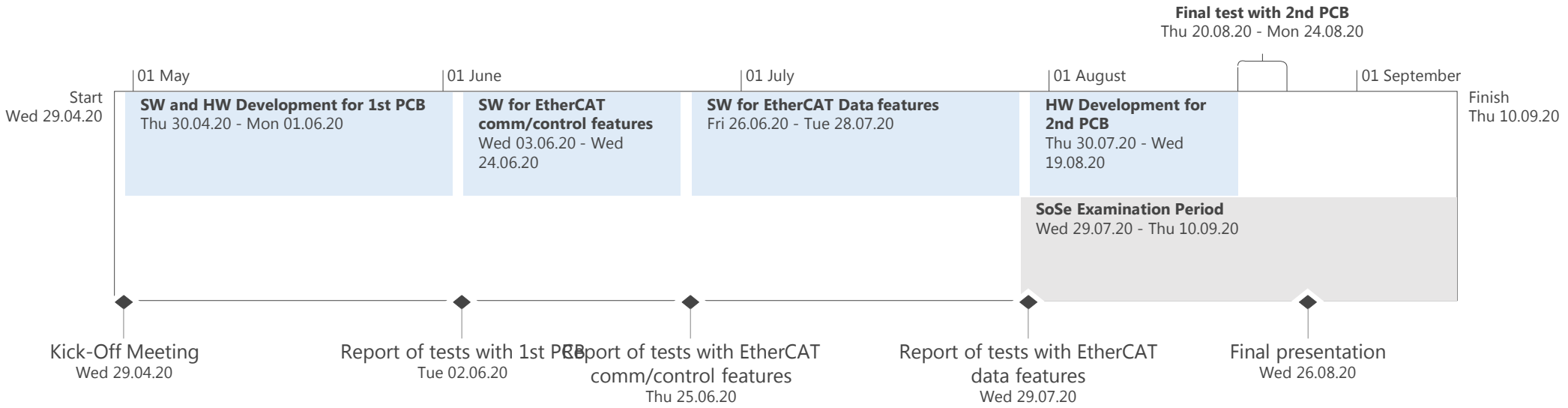


Timetable

Task Name	Duration	Start	Finish
1. Kick-Off Meeting	1 day	Wed 29.04.20	Wed 29.04.20
2. SW and HW Development for 1st PCB	23 days	Thu 30.04.20	Mon 01.06.20
3. Report of tests with 1st PCB	1 day	Tue 02.06.20	Tue 02.06.20
4. SW for EtherCAT comm/control features	16 days	Wed 03.06.20	Wed 24.06.20
5. Report of tests with EtherCAT comm/control features	1 day	Thu 25.06.20	Thu 25.06.20
6. SW for EtherCAT Data features	23 days	Fri 26.06.20	Tue 28.07.20
7. Report of tests with EtherCAT data features	1 day	Wed 29.07.20	Wed 29.07.20
8. HW Development for 2nd PCB	15 days	Thu 30.07.20	Wed 19.08.20
9. Final test with 2nd PCB	3 days	Thu 20.08.20	Mon 24.08.20
10 .Final presentation	1 day	Wed 26.08.20	Wed 26.08.20
SoSe Examination Period	32 days	Wed 29.07.20	Thu 10.09.20

Timeline

» Duration: 4 Months
» Official start: 29.04 Final Presentation: 26.08 (Proposal)



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Dankeschön für Ihre Aufmerksamkeit!