AN4616
Application note

Migrating from STM32F401/411 lines to STM32L4 series microcontrollers

Introduction

For designers of STM32 microcontroller applications, it is important to be able to easily replace one microcontroller type by another one in the same product family. Migrating an application to a different microcontroller is often needed, when product requirements grow, putting extra demands on memory size, or increasing the number of I/Os. On the other hand, cost reduction objectives may also be an argument to switch to smaller components and shrink the PCB area.

This application note is written to help analyzing the steps required to migrate an existing design from STM32F401/411 lines to STM32L4 series. It groups together the most important information and lists the vital aspects that need to be addressed.

This document lists the “full set” of features available for the STM32F401/411 lines and STM32L4 series (some products may have less features depending on their part number).

In order to migrate an application to STM32L4 series, these three aspects need to be considered: the hardware migration, the peripheral migration and the firmware migration.

To fully benefit from the information in this application note, the user should be familiar with the STM32 microcontrollers documentation available on *www.st.com*, with a particular focus on:

- The STM32F401/411 lines reference manuals:
  - RM0368 (STM32F401xB/C and STM32F401xD/E)
  - RM0383 (STM32F411xC/E)
- The STM32F401/411 lines datasheets.
- The STM32L4 series family reference manual:
  - RM0351 (STM32L4x6)
- The STM32L4 series datasheets.

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1 STM32L4 series overview

The STM32L4 series forms a perfect fit in terms of ultra-low-power, performances, memory size, and peripherals at a cost effective price.

In particular, the STM32L4 series allows high frequency/performance operation, including a ARM® Cortex®-M4 @80 MHz and optimized Flash memory access through the adaptive real-time memory accelerator (ART Accelerator™).

The STM32L4 series increases low-power efficiency in dynamic mode (µA/MHz) still reaching very low level of static power consumption on various available low-power modes.

The detailed list of available features and packages for each product can be found in the respective datasheet.

The STM32L4 series includes a larger set of peripherals with advanced features compared to the STM32F401/F411 lines.

- Advanced encryption hardware accelerator (AES)
- Touch sensing controller (TSC)
- Controller area network (bxCAN)
- Single wire protocol interface (SWPMI)
- Serial audio interface (SAI)
- Low-power UART (LPUART)
- Infrared interface (IRTIM)
- Low-power timer (LPTIM)
- Liquid crystal display controller (LCD)
- Digital filter for sigma delta modulators (DFSDM)
- Operational amplifiers (OPAMP)
- Voltage reference buffer (VREFBUF)
- Digital to analog converter with low power Sample and Hold feature (DAC)
- Quad-SPI interface (QUADSPI)
- Flexible memory controller (FMC)
- Firewall (FW)
- Additional SRAM2 (32 Kbyte) with data preservation in Standby mode
- Dual bank boot and 8-bit ECC on Flash memory

It also provides optimized power consumption and enriched set of low-power mode.

2 Hardware migration

WLCSP packages in STM32F401/411 lines are not equivalent to WLCSP packages in STM32L4 series (different die sizes for both products).

Only LQFP64, LQFP100 packages are available in both families, other packages in STM32F401/411 lines are not available in STM32L4 series.

The ultra-low-power STM32L4 series and the STM32F401/411 lines share high level of pin compatibility. Most peripherals share the same pins in the two families.

The transition from the STM32F401/411 lines to the STM32L4 series is simple since only a few pins are impacted, see *Table 1* below:

Table 1. STM32F401/411 lines and STM32L4 series pinout differences (QFP)

STM32F401/411 lines			STM32L4 series			
QFP64	**QFP100**	**Pinout**	**QFP64**	**QFP100**	**QFP144**	**Pinout**
-	19	**VDD**	-	19	30	**VSSA**
30	48	**VCAP1**	30	48	-	**PB11**
-	73	**VCAP2**	-	73	106	**VDDUSB**
48	-	**VDD**	48	-		**VDDUSB**(1)

1. VDDUSB pin can be connected externally to VDD.

Recommendations to migrate from STM32F401/411 lines board to STM32L4 series board

The pin VDD (pin 19 on QFP100) is now used as VSSA in STM32L4 series.

A dedicated V_{DDUSB} supply is used in STM32L4 series. It should be connected to pin VDDUSB (pin 48 on QFP64, pin 73 on QFP100). In STM32F401/411 lines the pin was used for VCAP2 (QFP64) (not needed for STM32L4 series) or VDD (QFP100).

The pins VCAP1, VCAP2 used in STM32F401/411 lines for regulator stabilization through external capacitor, are not needed in STM32L4 series. Those pins are now mapped onto PB11 and VDDUSB (see *Table 1*).

The figures below show examples of board designs migrating from STM32F4 lines to STM32L4 series.

Figure 1. LQFP100 compatible board design

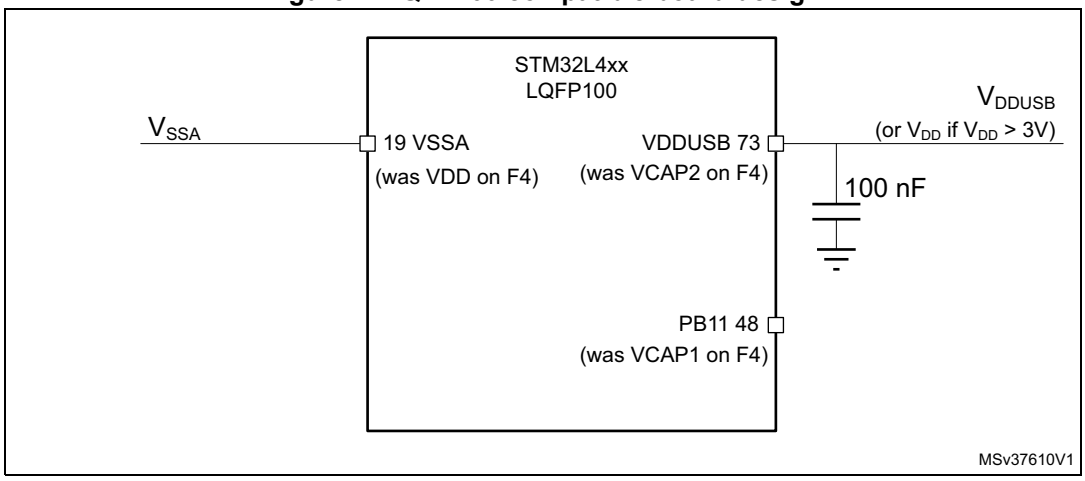
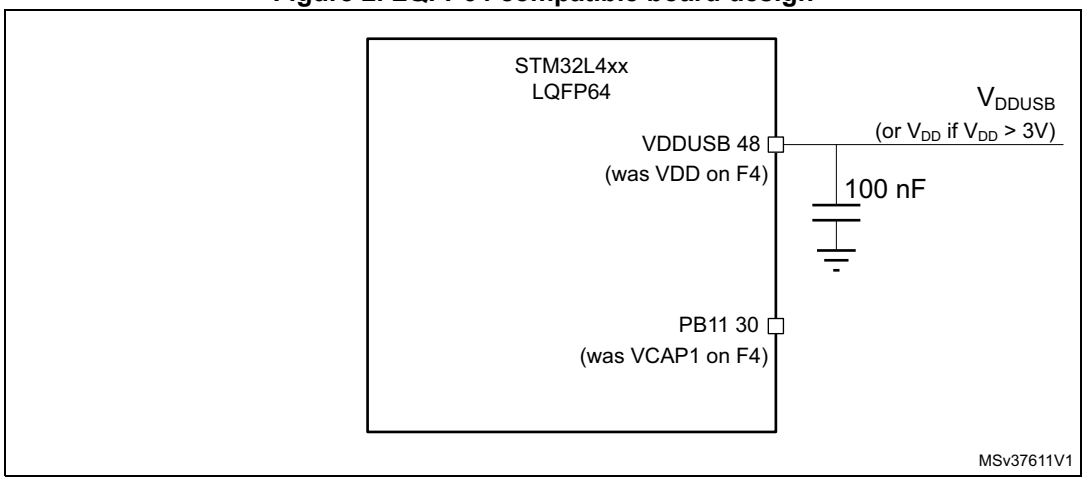


Figure 2. LQFP64 compatible board design



3 Boot mode selection

The way to select the boot mode differs between the STM32F401/411 lines and the STM32L4 series. In the STM32F401/411 lines the boot mode is selected with two pins. In the STM32L4 series the boot mode is selected with one pin and the nBOOT1 option bit located in the user option bytes at memory address 0x1FFF7800. For both STM32F401/411 lines and STM32L4 series, the boot mode can be selected among these three options: boot from main Flash memory, boot from SRAM or boot from system memory.

Table 2 summarizes the different configurations available for selecting the boot mode.

Table 2. Boot modes

STM32L4 series / STM32F401/411 lines boot mode selection		Boot mode	Aliasing
BOOT1(1)	BOOT0		
x	0	Main Flash memory	Main Flash memory is selected as boot space
0	1	System memory	System memory is selected as boot space
1	1	Embedded SRAM	Embedded SRAM is selected as boot space

1. The BOOT1 value is the opposite of the nBOOT1 option bit.

Embedded boot loader

The embedded boot loader is located in the system memory, programmed by ST during production. It is used to reprogram the Flash memory using one of the following serial interfaces (for more details please refer to AN2606):

Table 3. Bootloader interfaces

Peripheral	Pin	STM32F401/411 lines	STM32L4 series
DFU	USB_DM (PA11) USB_DP (PA12)	X	X
USART1	USART1_TX (PA9) USART1_RX (PA10)	X	X
USART2	USART2_TX (PD5) USART2_RX (PD6)	X	-
	USART2_TX (PA2) USART2_RX (PA3)	-	X
USART3	USART3_TX (PB10) USART3_RX (PB11)	X	-
USART3	USART3_TX (PC10) USART3_RX (PC11)	X	X

Table 3. Bootloader interfaces (continued)

Peripheral	Pin	STM32F401/411 lines	STM32L4 series
I2C1	I2C1_SCL (PB6) I2C1_SDA (PB7)	X	X
I2C2	I2C2_SCL (PB10) I2C2_SDA (PB11)	X	X
I2C3	I2C3_SCL (PA8) I2C3_SDA (PB4)	X	-
	I2C3_SCL (PC0) I2C3_SDA (PC1)	-	X
SPI1	SPI1_NSS (PA4) SPI1_SCK (PA5) SPI1_MISO (PA6) SPI1_MOSI (PA7)	X	X
SPI2	SPI2_NSS (PB12) SPI2_SCK (PB13) SPI2_MISO (PB14) SPI2_MOSI (PB15)	X	X
SPI3	SPI3_NSS (PA15) SPI3_SCK (PC10) SPI3_MISO (PC11) SPI3_MOSI (PC12)	X	X

Please refer to AN2606 for more details on the bootloader.

4 Peripheral migration

4.1 STM32 product cross-compatibility

The STM32 series embeds a set of peripherals which can be classified in three categories:

- The first category is for the peripherals that are common to all products. Those peripherals are identical on all products, so they have the same structure, registers and control bits. There is no need to perform any firmware change to keep the same functionality at the application level after migration. All the features and behavior remain the same.
- The second category is for the peripherals that present minor differences from one product to another (usually differences due to the support of new features). Migrating from one product to another is very easy and does not require any significant new development effort.
- The third category is for peripherals which have been considerably modified from one product to another (new architecture, new features...). For this category of peripherals, migration will require new development at application level.

Table 4 gives a general overview of this classification.

The “software compatibility” mentioned in the table below only refers to the register description for “low level” drivers.

The STMCube™ hardware abstraction layer (HAL) between STM32F401/411 lines and STM32L4 series is compatible.

Table 4. STM32 peripheral compatibility analysis STM32F401/411 lines versus STM32L4 series

Peripheral	Nb inst. in F401/ F411	Nb inst. in L4	Compatibility (migrating from STM32F401/411 lines to STM32L4 series)		
			Software	Pinout	Comments
SPI **I2S (full duplex)**	4/5 2	3 0	Partial compatibility	Partial compatibility	I2S is no more supported by SPI but replaced by dedicated Serial Audio Interface (SAI) in STM32L4 series. Some alternate function not mapped on same GPIO for SPI2/SPI3.
WWDG	1	1	Full Compatibility	NA	-
IWDG	1	1	Full Compatibility	NA	-
DBGMCU	1	1	Full Compatibility	NA	-
CRC	1	1	Partial compatibility	NA	Additional features in STM32L4 series.
EXTI	1	1	Partial compatibility	Full compatibility	Only PH2 GPIO not available as EXTI input in STM32L4 series.

Table 4. STM32 peripheral compatibility analysis STM32F401/411 lines versus STM32L4 series

Peripheral	Nb inst. in F401/ F411	Nb inst. in L4	Compatibility (migrating from STM32F401/411 lines to STM32L4 series)		
			Software	Pinout	Comments
USB OTG FS	1	1	Partial compatibility	Partial compatibility	More endpoints in L4. A few register control are different. V_{DDUSB} merged with V_{DD} in STM32F401/411 lines.
DMA	2	2	No compatibility	NA	Different features and DMA mapping requests differ (see *Section 4.3: DMA*).
TIM Basic General P. Advanced Low-power	8 0 7 1 0	13 2 7 2 2	Full Compatibility	Partial compatibility	Some pins not mapped on same GPIO. Timer instance name may differ. Internal connections may differ.
SDIO/ SDMMC	1	1	Full Compatibility	Full Compatibility	Some pins not mapped on same GPIO.
PWR	1	1	Partial compatibility	NA	-
RCC	1	1	Partial compatibility	NA	-
USART **UART** **LPUART**	3 0	3 2 1	Partial compatibility	Full Compatibility	Additional features in L4. Pinout fully compatible for USART1/2/3.
I2C	3	3	No compatibility	Partial compatibility	Pinout fully compatible for I2C1/2. I2C3 mapped on different GPIOs. Additional features in L4.
ADC	1	3	No compatibility	Partial compatibility	Additional features in L4. Some pins mapped on different GPIOs.
RTC	1	1	Partial compatibility	Full Compatibility	Additional features in L4.
FLASH	1	1	No compatibility	NA	New peripheral.
GPIO	Up to 82 IOs	Up to 114 IOs	Full compatibility	Full compatibility	At reset, STM32F401/411 lines configured in input floating mode, L4 in analog mode.
SYSCFG	1	1	Partial compatibility	NA	-

Color key:

= No compatibility (new feature or new architecture)

= Partial compatibility (minor changes)

= Full Compatibility (from STM32F401/411 lines to L4)

= not applicable

4.2 Memory mapping

The peripheral address mapping has been changed in the STM32L4 series versus the STM32F401/411 lines.

The table below provides the peripheral address mapping correspondence between STM32F401/411 lines and STM32L4 series.

Table 5. Peripheral address mapping differences between STM32F401/411 lines and STM32L4 series

Peripheral	STM32F4 lines		STM32L4 series	
	Bus	Base address	Bus	Base address
USB OTG FS	AHB2	0x50000000	AHB2	0x50000000
DMA2	AHB1	0x40026400	AHB1	0x40020400
DMA1		0x40026000		0x40020000
Flash Interface Reg.		0x40023C00		0x40022000
RCC		0x40023800		0x40021000
CRC		0x40023000		0x40023000
GPIOH		0x40021C00	AHB2	0x48001C00
GPIOE		0x40021000		0x48001000
GPIOD		0x40020C00		0x48000C00
GPIOC		0x40020800		0x48000800
GPIOB		0x40020400		0x48000400
GPIOA		0x40020000		0x48000000
SPI5	APB2	0x4001 5000	NA	
TIM11		0x40014800		
TIM10		0x40014400		
TIM9		0x40014000		
EXTI		0x40013C00	APB2	0x40010400
SYSCFG		0x40013800		0x40010000
SPI4		0x40013400	NA	
SPI1		0x40013000	APB2	0x40013000
SDIO/SDMMC		0x40012C00		0x40012800
ADC1 - ADC2 - ADC3		0x40012000	AHB2	0x50040000
USART6		0x40011400	NA	
USART1		0x40011000	APB2	0x40013800
TIM1		0x40010000		0x40012C00
PWR	APB1	0x40007000	APB1	0x40007000
I2C3		0x40005C00		0x40005C00
I2C2		0x40005800		0x40005800

Table 5. Peripheral address mapping differences between STM32F401/411 lines and STM32L4 series (continued)

Peripheral	STM32F4 lines		STM32L4 series	
	Bus	Base address	Bus	Base address
I2C1	APB1	0x40005400	APB1	0x40005400
USART2		0x40004400		0x40004400
I2S3ext		0x40004000	NA	
SPI3 / I2S3		0x40003C00	APB1	0x40003C00
SPI2 / I2S2		0x40003800		0x40003800
I2S2ext		0x40003400	NA	
IWDG		0x40003000	APB1	0x40003000
WWDG		0x40002C00		0x40002C00
RTC (inc. BKP registers)		0x40002800		0x40002800
TIM5		0x40000C00		0x40000C00
TIM4		0x40000800		0x40000800
TIM3		0x40000400		0x40000400
TIM2		0x40000000		0x40000000
Peripherals in STM32L4 series not available in STM32F401/411 lines				
QUADSPI	NA		AHB3	0xA0001000
FMC				0xA0000000
RNG			AHB2	0x50060800
AES				0x50060000
GPIOG			AHB1	0x48001800
GPIOF				0x48001400
TSC				0x40024000
DFSDM			APB2	0x40016000
SAI2				0x40015800
SAI1				0x40015400
TIM17				0x40014800
TIM16				0x40014400
TIM15				0x40014000
TIM8				0x40013400
FIREWALL				0x40011C00
COMP				0x40010200

Table 5. Peripheral address mapping differences between STM32F401/411 lines and STM32L4 series (continued)

Peripheral	STM32F4 lines		STM32L4 series	
	Bus	Base address	Bus	Base address
VREF	NA		APB2	0x40010030
LPTIM2			APB1	0x40009400
SWPMI1				0x40008800
LPUART1				0x40008000
LPTIM1				0x40007C00
OPAMP				0x40007800
DAC				0x40007400
CAN1				0x40006400
UART5				0x40005000
UART4				0x40004C00
USART3				0x40004800
LCD				0x40002400
TIM7				0x40001400
TIM6				0x40001000

Color key:

= base address or bus change

= not applicable

The system memory mapping has been updated between STM32F401/411 lines and STM32L4 series, please refer to reference manuals or datasheets for more details.

While in STM32F401/411 lines only one SRAM1 is available, in STM32L4 series two SRAMs are implemented (SRAM1, SRAM2) and the SRAM2 (32 Kbyte) includes additional features listed below:

- Maximum performance through ICode bus access without physical remap
- Parity check option (32-bit + 4-bit parity check)
- Write protection with 1 Kbyte granularity
- Read protection (RDP)
- Erase by system reset (option byte) or by software
- Content is preserved in Low-power run, Low-power sleep, Stop 1, Stop 2 mode
- Content can be preserved (RRS bit set in PWR_CR3 register) in Standby mode (not the case for SRAM1).

4.3 DMA

The STM32F401/411 lines implements an “enhanced” DMA compared to STM32L4 series.

The table below shows main differences.

Table 6. DMA differences between STM32F401/411 lines and STM32L4 series

DMA	STM32F401/411 lines	STM32L4 series
Architecture	Dual AHB master. – 1 DMA controller for memory accesses – 1 DMA controller for peripheral accesses	Both DMA controllers can access memory and peripherals.
Streams	8 streams per controller 8 channels per stream	7 channels per controller (“streams” in STM32F401/411 lines). 8 requests per channel (“channels” in STM32F401/411 lines).
Data Management	Four-word depth 32 first-in, first-out memory buffers (FIFOs) per stream, that can be used in FIFO mode or direct mode.	NA
Color key: = Feature not available (NA) = Difference between STM32F401/411 lines and STM32L4 series highlight		

The table below presents the correspondence between the peripheral DMA requests in the STM32F401/411 lines and in the STM32L4 series.

Table 7. DMA request differences migrating STM32F401/411 lines to STM32L4 series

Peripheral	DMA request	STM32F401/411 lines	STM32L4 series
ADC1	**ADC1**	DMA2_Stream0 DMA2_Stream4	DMA1_Channel1 DMA2_Channel3
DAC	**DAC1** **DAC2**	NA	DMA1_Channel3 DMA2_Channel4 DMA1_Channel4 DMA2_Channel5
SPI1	**SPI1_Rx** **SPI1_Tx**	DMA2_Stream0 DMA2_Stream2 DMA2_Stream3 DMA2_Stream5	DMA1_Channel2 DMA2_Channel3 DMA1_Channel3 DMA2_Channel4
SPI2	**SPI2_Rx** **SPI2_Tx**	DMA1_Stream3 DMA1_Stream4	DMA1_Channel4 DMA1_Channel5
SPI3	**SPI3_Rx** **SPI3_Tx**	DMA1_Stream0 DMA1_Stream2 DMA1_Stream5 DMA1_Stream7	DMA2_Channel1 DMA2_Channel2

Table 7. DMA request differences migrating STM32F401/411 lines to STM32L4 series

Peripheral	DMA request	STM32F401/411 lines	STM32L4 series
SPI4	**SPI4_Rx** **SPI4_Tx**	DMA2_Stream0 DMA2_Stream3 DMA2_Stream1 DMA2_Stream4	NA
SPI5	**SPI5_Rx** **SPI5_Tx**	DMA2_Stream5(1) DMA2_Stream6(1)	NA
USART1	**USART1_Rx** **USART1_Tx**	DMA2_Stream2 DMA2_Steam5 DMA2_ Stream7	DMA1_Channel5 DMA2_Channel7 DMA1_Channel4 DMA2_Channel6
USART2	**USART2_Rx** **USART2_Tx**	DMA1_Stream5 DMA1_Stream6	DMA1_Channel6 DMA1_Channel7
USART3	**USART3_Rx** **USART3_Tx**	NA	DMA1_Channel3 DMA1_Channel2 NA
UART4	**UART4_Rx** **UART4_Tx**	NA	DMA2_Channel5 DMA2_Channel3
UART5	**UART5_Rx** **UART5_Tx**	NA	DMA2_Channel2 DMA2_Channel1
USART6	**USART6_Rx** **USART6_Tx**	DMA2_Stream1 DMA2_Stream2 DMA2_Stream6 DMA2_Stream7	NA
I2C1	**I2C1_Rx** **I2C1_Tx**	DMA1_Stream0 DMA1_Stream5 DMA1_Stream6 DMA1_Stream7	DMA1_Channel7 DMA2_Channel6 DMA1_Channel6 DMA2_Channel7
I2C2	**I2C2_Rx** **I2C2_Tx**	DMA1_Stream2 DMA1_Stream3 DMA1_Stream7	DMA1_Channel5 DMA1_Channel4
I2C3	**I2C3_Rx** **I2C3_Tx**	DMA1_Stream1 DMA1_Stream2 DMA1_Stream4 DMA1_Stream5	DMA1_Channel3 DMA1_Channel2
SDIO **SDMMC**	**SDIO** **SDMMC**	DMA2_Stream3 DMA2_Stream6 NA NA	NA NA DMA2_Channel4 DMA2_Channel5

Table 7. DMA request differences migrating STM32F401/411 lines to STM32L4 series

Peripheral	DMA request	STM32F401/411 lines	STM32L4 series
TIM1		DMA2_Stream5	NA
	TIM1_UP	DMA2_Stream0	
	TIM1_TRIG	DMA2_Stream4	
		DMA2_Stream4	
	TIM1_COM		
		DMA2_Stream1	
	TIM1_CH1	DMA2_Stream3	
		DMA2_Stream6	
	TIM1_CH2	DMA2_Stream2	
		DMA2_Stream6	
	TIM1_CH3		
		DMA2_Stream6	
	TIM1_CH4		
		DMA2_Stream4	
TIM2	TIM2_UP	DMA1_Stream1 DMA1_Stream7	DMA1_Channel2
	TIM2_CH1	DMA1_Stream5	DMA1_Channel5
	TIM2_CH2	DMA1_Stream6	DMA1_Channel7
	TIM2_CH3	DMA1_Stream1	DMA1_Channel1
	TIM2_CH4	DMA1_Stream6 DMA1_Stream7	DMA1_Channel7
TIM3	TIM3_UP	DMA1_Stream2	DMA1_Channel3
	TIM3_TRIG	DMA1_Stream4	DMA1_Channel6
	TIM3_CH1	DMA1_Stream4	DMA1_Channel6
	TIM3_CH2	DMA1_Stream5	NA
	TIM3_CH3	DMA1_Stream7	DMA1_Channel2
	TIM3_CH4	DMA1_Stream2	DMA1_Channel3
TIM4	TIM4_UP	DMA1_Stream6	DMA1_Channel7
	TIM4_CH1	DMA1_Stream0	DMA1_Channel1
	TIM4_CH2	DMA1_Stream3	DMA1_Channel4
	TIM4_CH3	DMA1_Stream7	DMA1_Channel5
TIM5	TIM5_UP	DMA1_Stream0 DMA1_Stream6	DMA2_Channel2
	TIM5_CH1	DMA1_Stream2	DMA2_Channel5
	TIM5_CH2	DMA1_Stream4	DMA2_Channel4
	TIM5_CH3	DMA1_Stream0	DMA2_Channel2
	TIM5_CH4	DMA1_Stream1 DMA1_Stream3	DMA2_Channel1
	TIM5_TRIG	DMA1_Stream1	DMA2_Channel1
	TIM5_COM	DMA1_Stream3 NA	DMA2_Channel1

Table 7. DMA request differences migrating STM32F401/411 lines to STM32L4 series

Peripheral	DMA request	STM32F401/411 lines	STM32L4 series
TIM6	**TIM6_UP**	NA	DMA1_Channel3 DMA2_Channel4
TIM7	**TIM7_UP**	NA	DMA1_Channel4 DMA2_Channel5
AES	**CRYP_OUT** **CRYP_IN** **AES_OUT** **AES_IN**	NA	NA NA DMA2_Channel3 DMA2_Channel2 DMA2_Channel5 DMA2_Channel1
I2S	**I2S2_EXT_Rx** **I2S2_EXT_Tx** **I2S3_EXT_Rx** **I2S3_EXT_Tx**	DMA1_Stream3 DMA1_Stream4 DMA1_Stream0 DMA1_Stream2 DMA1_Stream5	NA
Color key: = Feature not available (NA) = Difference between STM32F401/411 lines and STM32L4 series highlight			

1. Except STM32F401 lines.

4.4 Interrupts

The table below presents the interrupt vectors in the STM32F401/411 lines versus the STM32L4 series.

Table 8. Interrupt vector differences between STM32F401/411 lines and STM32L4 series

Position	STM32F401/411 lines	STM32L4 series
0	WWDG	WWDG
1	PVD	PVD / PVM
2	TAMP_ STAMP	TAMPER / CSS
3	RTC_WKUP	RTC_WKUP
4	FLASH	FLASH
5	RCC	RCC
6	EXTI0	EXTI0
7	EXTI1	EXTI1
8	EXTI2	EXTI2
9	EXTI3	EXTI3
10	EXTI4	EXTI4
11	DMA1_Stream0	DMA1_Channel1
12	DMA1_Stream1	DMA1_Channel2
13	DMA1_Stream2	DMA1_Channel3
14	DMA1_Stream3	DMA1_Channel4
15	DMA1_Stream4	DMA1_Channel5
16	DMA1_Stream5	DMA1_Channel6
17	DMA1_Stream6	DMA1_Channel7
18	ADC	ADC1_2
19	NA	CAN1_TX
20	NA	CAN1_RX0
21	NA	CAN1_RX1
22	NA	CAN1_SCE
23	EXTI9_5	EXTI9_5
24	TIM1_BRK / TIM9	TIM1_BRK / TIM15
25	TIM1_UP / TIM10	TIM1_UP / TIM16
26	TIM1_TRG_COM / TIM11	TIM1_TRG_COM / TIM17
27	TIM1_CC	TIM1_CC
28	TIM2	TIM2
29	TIM3	TIM3

Table 8. Interrupt vector differences between STM32F401/411 lines and STM32L4 series (continued)

Position	STM32F401/411 lines	STM32L4 series
30	TIM4	TIM4
31	I2C1_EV	I2C1_EV
32	I2C1_ER	I2C1_ER
33	I2C2_EV	I2C2_EV
34	I2C2_ER	I2C2_ER
35	SPI1	SPI1
36	SPI2	SPI2
37	USART1	USART1
38	USART2	USART2
39	NA	USART3
40	EXTI15_10	EXTI15_10
41	RTC_Alarm	RTC_Alarm
42	USB_FS_WKUP	DFSDM
43	NA	TIM8_BRK
44	NA	TIM8_UP
45	NA	TIM8_TRG_COM
46	NA	TIM8_CC
47	DMA1_Stream7	ADC3
48	NA	FMC
49	SDIO	SDMMC
50	TIM5	TIM5
51	SPI3	SPI3
52	NA	UART4
53	NA	UART5
54	NA	TIM6_DACUNDER
55	NA	TIM7
56	DMA2_Stream0	DMA2_Channel1
57	DMA2_Stream1	DMA2_Channel2
58	DMA2_Stream2	DMA2_Channel3
59	DMA2_Stream3	DMA2_Channel4
60	DMA2_Stream4	DMA2_Channel5
61	NA	DFSDM1
62	NA	DFSDM2
63	NA	DFSDM3
64	NA	COMP

Table 8. Interrupt vector differences between STM32F401/411 lines and STM32L4 series (continued)

Position	STM32F401/411 lines	STM32L4 series
65	NA	LPTIM1
66	NA	LPTIM2
67	OTG_FS	OTG_FS
68	DMA2_Stream5	DMA2_CH6
69	DMA2_Stream6	DMA2_CH7
70	DMA2_Stream7	LPUART1
71	USART6	QUADSPI
72	I2C3_EV	I2C3_EV
73	I2C3_ER	I2C3_ER
74	NA	SAI1
75	NA	SAI2
76	NA	SWPMI1
77	NA	TSC
78	NA	LCD
79	NA	AES
80	NA	RNG
81	FPU	FPU

Color key:

= Same feature, but specification change or enhancement

= Feature not available (NA)

= Difference between STM32F401/411 lines and STM32L4 series highlight

4.5 RCC

The main differences related to the RCC (reset and clock controller), between the STM32L4 series and the STM32F401/411 lines, are presented in the table below.

Table 9. RCC differences between STM32F401/411 lines and STM32L4 series

RCC	STM32F401/411 lines	STM32L4 series
MSI	NA	MSI is a low power oscillator with programmable frequency up to 48 MHz. It can replace PPLs as system clock (faster wakeup, lower consumption). It can be used as USB device clock (no need for external high speed crystal oscillator). Multi Speed RC factory and user trimmed (100 kHz, 200 kHz, 400 kHz, 800 kHz, 1 MHz, 2 MHz, 4 MHz (default value), 8 MHz, 16 MHz, 24 MHz, 32 MHz and 48 MHz) Auto calibration from LSE
HSI	16 MHz RC factory and user trimmed	
LSI	32 kHz	32 kHz RC Lower consumption, higher accuracy (refer to product datasheet)
HSE	4 - 26 MHz	4 - 48 MHz
LSE	32.768 kHz. Configurable drive/consumption (not in STM32F401 lines). Available in backup domain (VBAT).	
PLL	– Main PLL for system – 1 PLL (PLLI2S) for I2S The PLL sources are HSI, HSE.	– Main PLL for system – 2 PLLs for SAI1/2, ADC, RNG, SDMMC and OTG FS clock. Each PLL can provide up to 3 independent outputs. The PLL multiplication/division factors are different from STM32F401/411 lines. PLL clock sources: MSI, HSI16, HSE.
System clock source	HSI, HSE or PLL	MSI, HSI16, HSE or PLL
System clock frequency	Up to 84 MHz (STM32F401 lines), 100 MHz (STM32F411 lines) 16 MHz after reset using HSI	Up to 80 MHz 4 MHz after reset using MSI
AHB frequency	Up to 84 MHz (STM32F401 lines), 100 MHz (STM32F411 lines)	Up to 80 MHz

Table 9. RCC differences between STM32F401/411 lines and STM32L4 series (continued)

RCC	STM32F401/411 lines	STM32L4 series
APB1 frequency	Up to 42 MHz (STM32F401 lines), 50 MHz (STM32F411 lines)	Up to 80 MHz
APB2 frequency	Up to 84 MHz (STM32F401 lines), 100 MHz (STM32F411 lines)	Up to 80 MHz
RTC clock source	LSI, LSE or HSE (1 MHz) using 1/2, 1/3, ¼ clock pre-divider	LSI, LSE or HSE/32
MCO clock source	– MCO1 pin (PA8): HSI, LSE, HSE, PLLCLK – MCO2 pin (PC9): HSE, PLLCLK, SYSCLK, PLLI2S With configurable prescaler, 1, 2, 3, 4, 5 for each output.	– MCO pin (PA8): SYSCLK, HSI16, HSE, PLLCLK, MSI, LSE or LSI With configurable prescaler, 1, 2, 4, 8 or 16 for each output.
CSS	CSS (Clock Security System) CSS on LSE	
Internal oscillator measurement / calibration	– LSE connected to TIM5 CH4 IC: can measure HSI with respect to LSE clock high precision – LSI connected to TIM5 CH4 IC: can measure LSI with respect to HSI or HSE clock precision – HSE connected to TIM11 CH1 IC: can measure HSE with respect to LSE/HSI clock	(mainly replacing TIM5/TIM11 in STM32F401/411 lines by TIM15/16/17 in STM32L4 series) – LSE connected to TIM15 or TIM16 CH1 IC: can measure HSI16 or MSI with respect to LSE clock high precision – LSI connected to TIM16 CH1 IC: can measure LSI with respect to HSI16 or HSE clock precision – HSE/32 connected to TIM17 CH1 IC: can measure HSE with respect to LSE/HSI16 clock – MSI connected to TIM17 CH1 IC: can measure MSI with respect to HSI16/HSE clock
Interrupt	– CSS (linked to NMI IRQ) – LSIRDY, LSERDY, HSIRDY, HSERDY, PLLRDY, PLLI2SRDY (linked to RCC global IRQ)	– CSS (linked to NMI IRQ) – LSECSS, LSIRDY, LSERDY, HSIRDY, MSIRDY, HSERDY, PLLRDY, *PLLSAI1RDY, PLLSAI2RDY* (linked to RCC global IRQ)

Color key:

= New feature or new architecture (difference between STM32F401/411 lines and STM32L4 series)

= Same feature, but specification change or enhancement

= Feature not available (NA)

= Difference between STM32F401/411 lines and STM32L4 series highlight

In addition to the differences described in the table above, the following additional adaptation steps may be needed for the migration.

4.5.1 Performance versus V_{CORE} ranges

In STM32L4 series the maximum system clock frequency and number of Flash memory wait state depend on the selected voltage range V_{CORE}.

Table 10. STM32L4 series Performance versus V_{CORE} ranges

CPU performance	Power performance	VCORE Range	Typical Value (V)	Max frequency (MHz)				
				4 WS	3 WS	2 WS	1 WS	0 WS
High	Medium	1	1.2	80	64	48	32	16
Medium	High	2	1.0	26	26	18	12	6

In STM32F401/411 lines the maximum system clock frequency and number of Flash memory wait state depend on the selected voltage range V_{DD}.

Table 11. Number of wait states according to CPU clock (HCLK) frequency (STM32F401xB/C and STM32F401xD/E)

Wait states (WS) (LATENCY)	HCLK (MHz)			
	Voltage range 2.7 V - 3.6 V	Voltage range 2.4 V - 2.7 V	Voltage range 2.1 V - 2.4 V	Voltage range 1.71 V - 2.1 V
0 WS (1 CPU cycle)	0 < HCLK ≤ 30	0 < HCLK ≤ 24	0 < HCLK ≤ 18	0 < HCLK ≤ 16
1 WS (2 CPU cycles)	30 < HCLK ≤ 60	24 < HCLK ≤ 48	18 < HCLK ≤ 36	16 < HCLK ≤ 32
2 WS (3 CPU cycles)	60 < HCLK ≤ 84	48 < HCLK ≤ 72	36 < HCLK ≤ 54	32 < HCLK ≤ 48
3 WS (4 CPU cycles)	-	72 < HCLK ≤ 84	54 < HCLK ≤ 72	48 < HCLK ≤ 64
4 WS (5 CPU cycles)	-	-	72 < HCLK ≤ 84	64 < HCLK ≤ 80
5 WS (6 CPU cycles)	-	-	-	80 < HCLK ≤ 84

Table 12. Number of wait states according to CPU clock (HCLK) frequency (STM32F411xC/E)

Wait states (WS) (LATENCY)	HCLK (MHz)			
	Voltage range 2.7 V - 3.6 V	Voltage range 2.4 V - 2.7 V	Voltage range 2.1 V - 2.4 V	Voltage range 1.71 V - 2.1 V
0 WS (1 CPU cycle)	0 < HCLK ≤ 30	0 < HCLK ≤ 24	0 < HCLK ≤ 18	0 < HCLK ≤ 16
1 WS (2 CPU cycles)	30 < HCLK ≤ 64	24 < HCLK ≤ 48	18 < HCLK ≤ 36	16 <HCLK ≤ 32
2 WS (3 CPU cycles)	64 < HCLK ≤ 90	48 < HCLK ≤ 72	36 < HCLK ≤ 54	32 < HCLK ≤ 48
3 WS (4 CPU cycles)	90 < HCLK ≤ 100	72 < HCLK ≤ 96	54 < HCLK ≤ 72	48 < HCLK ≤ 64
4 WS (5 CPU cycles)	-	96 < HCLK ≤ 100	72 < HCLK ≤ 90	64 < HCLK ≤ 80
5 WS (6 CPU cycles)	-	-	90 < HCLK ≤ 100	80 < HCLK ≤ 96
6 WS (7 CPU cycles)	-	-	-	96 < HCLK ≤ 100

On top of V_{DD} voltage range specified in above tables, the maximum frequency is limited by the power scale value indicated by software in VOS[1:0] bits of PWR_CR register.

Those bits are modifying the internal digital logic voltage from the power regulator.

This voltage scaling allows optimizing the power consumption when the device is clocked below the maximum system frequency.

4.5.2 Peripheral access configuration

Since the address mapping of some peripherals has been changed in STM32L4 series versus STM32F401/411 lines, different registers need to be used to [enable/disable] or [enter/exit] the peripheral [clock] or [from reset mode].

Table 13. RCC registers used for peripheral access configuration

Bus	Register STM32F401/411 lines	Register STM32L4 series	Comments
AHB	RCC_AHB1RSTR (AHB1) RCC_AHB2RSTR (AHB2)		Used to [enter/exit] the AHB peripheral from reset
	RCC_AHB1ENR (AHB1) RCC_AHB2ENR (AHB2)		Used to [enable/disable] the AHB peripheral clock
	RCC_AHB1LPENR RCC_AHB2LPENR	RCC_AHB1SMENR (AHB1) RCC_AHB2SMENR (AHB2) RCC_AHB3SMENR (AHB3)	Used to [enable/disable] the AHB peripheral clock in Sleep mode
APB1	RCC_APB1RSTR	RCC_APB1RSTR1 RCC_APB1RSTR2(1)	Used to [enter/exit] the APB1 peripheral from reset
	RCC_APB1ENR	RCC_APB1ENR1 RCC_APB1ENR2(1)	Used to [enable/disable] the APB1 peripheral clock
	RCC_APB1LPENR	RCC_APB1SMENR1 RCC_APB1SMENR2(1)	Used to [enable/disable] the APB1 peripheral clock in Sleep mode
APB2	RCC_APB2RSTR	RCC_APB2RSTR	Used to [enter/exit] the APB2 peripheral from reset
	RCC_APB2ENR	RCC_APB2ENR	Used to [enable/disable] the APB2 peripheral clock
	RCC_APB2LPENR	RCC_APB2SMENR	Used to [enable/disable] the APB2 peripheral clock in Sleep mode

1. Register configuring peripherals not present in STM32F401/411 lines, so it should not be needed from a migration-only stand point.

The configuration to access a given peripheral involves:

- identifying the bus to which the peripheral is connected, refer to *Table 5 on page 12*
- selecting the right register according the needed action, refer to *Table 13* above.

For example, USART1 is connected to APB2 bus. In order to enable the USART1 clock, the RCC_APB2ENR register needs to be configured as follows:

```
__HAL_RCC_USART1_CLK_ENABLE();
```

with STM32Cube HAL driver RCC API.

In order to disable USART1 clock during Sleep mode (to reduce power consumption) the RCC_APB2SMENR register needs to be configured as follows:

```
__HAL_RCC_USART1_CLK_SLEEP_ENABLE();
```

with STM32Cube HAL driver RCC API.

4.5.3 Peripheral clock configuration

Some peripherals have a dedicated clock source independent from the system clock that is used to generate the clock required for their operation.

- USB:

  In STM32F401/411 lines: the USB 48 MHz clock is derived from the PLL48CLK main PLL “Q” output.

  In STM32L4 series: the USB 48 MHz clock is derived from one of the three following sources: main PLL VCO (PLLUSB1CLK), PLLSAI1 VCO (PLLUSB2CLK) or MSI clock (when the MSI clock is auto-trimmed with the LSE, it can be used by the USB OTG FS device).

- SDIO/SDMMC:

  In STM32F401/411 lines: the SDIO clock (SDIOCLK) is derived from the PLL48CLK main PLL “Q” output and should be less than 48 MHz.

  In STM32L4 series: the SDMMC clock is derived from one of the three following sources: main PLL VCO (PLLUSB1CLK), PLLSAI1 VCO (PLLUSB2CLK) or MSI clock.

- RTC:

  In STM32F401/411 lines: the RTC clock is derived from one of the three following sources: LSE, LSI or HSE divided by prescaler (1 to 31) and should be equal to 1 MHz

  In STM32L4 series: the RTC (and LCD Glass clock) is derived from one of the three following sources: LSE clock, LSI clock or HSE clock divided by 32 (PCLK frequency should always be greater than or equal to RTC Clock frequency).

- ADC:

  In STM32F401/411 lines, the ADC clock is the PCLK2 clock divided by a programmable factor (2, 4, 6, 8).

  In STM32L4 series, the input clock of the two ADCs (master and slave) can be selected between two different clock sources:

  – The ADCs clock can be derived (selected by software) from one of the three following sources: system clock (SYSCLK), PLLSAI1 VCO (PLLADC1CLK) or PLLSAI2 VCO (PLLADC2CLK). In this mode, a programmable divider factor can be selected (1, 2, …, 256 according to bits PREC[3:0]).

  – The ADC clock can be derived from the AHB clock of the ADC bus interface, divided by a programmable factor (1, 2 or 4). In this mode, a programmable divider factor can be selected (1, 2 or 4 according to bits CKMODE[1:0])(please refer to the STM32L4 series reference manual for more details).

- DAC:

  In STM32L4 series, in addition to the PCLK1 clock, LSI clock is used for the sample and hold operation.

- U(S)ARTs:

  In STM32F401/411 lines, the U(S)ART clock is APB1 or APB2 clock (depending on which APB bus is mapped the U(S)ART).

  In STM32L4 series, the U(S)ART clock is derived from one of the four following sources: system clock (SYSCLK), HSI16, LSE, APB1 or APB2 clock (depending on which APB bus the U(S)ART is mapped).

  Using a source clock independent from the system clock (example: HSI16) allows to change the system clock on the fly without need to reconfigure U(S)ART peripheral baud rate prescalers.

- I2Cs:

  In STM32F401/411 lines, the I2C clock is APB1 clock (PCLK1).

  In STM32L4 series, the I2C clock is derived from one of the three following sources: system clock (SYSCLK), HSI16 or APB1 (PCLK1).

  Using a source clock independent from the system clock (example: HSI16) allows to change the system clock on the fly without need to reconfigure I2C peripheral timing register.

  I2S clock is not available in STM32L4 series compared to STM32F401/411 lines.

4.6 PWR

In STM32L4 series the PWR controller presents some differences versus STM32F401/411 lines, these differences are summarized in *Table 14*.

Table 14. PWR differences between STM32F401/411 lines and STM32L4 series

PWR	STM32F401/411 lines	STM32L4 series
Power supplies	V_{DD} = 1.7 to 3.6 V (when internal voltage regulator is disabled) V_{DD} = 1.8 to 3.6 V (when internal voltage regulator is enabled) External power supply for I/Os, Flash memory and internal regulator. It is provided externally through VDD pins.	V_{DD} = 1.71 to 3.6 V: external power supply for I/Os, Flash memory and internal regulator. It is provided externally through VDD pins.
	V_{CORE} = 1.2 V (scalable). V_{CORE} is the power supply for digital peripherals, SRAM and Flash memory. It is generated by an internal voltage regulator. The voltage regulator requires one or two external capacitors connected to dedicated pins VCAP_1, VCAP_2. In application Run mode, the voltage regulator output voltage can be scaled by software (lowered) to save power consumption when the device is clocked below the maximum frequency.	V_{CORE} = 1.0 to 1.2 V. V_{CORE} is the power supply for digital peripherals, SRAM and Flash memory. It is generated by an internal voltage regulator. Two V_{CORE} ranges can be selected by software depending on target frequency.
	V_{BAT} = 1.65 to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.	V_{BAT} = 1.55 to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.
	V_{DD} and V_{DDA} must be at the same voltage value.	Independent power supplies (V_{DDA}, V_{DDUSB}, V_{DDIO2}) allow to improve power consumption by running MCU at lower supply voltage than analog and USB.
	V_{SSA}, V_{DDA}: 1.8 V to 3.6 V (1.7V with external power-supply supervisor). V_{DDA} is the external analog power supply for A/D and D/A converters. V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS} respectively.	V_{SSA}, V_{DDA} = 1.62 V (ADCs/COMPs) to 3.6 V 1.8 V (DACs/OPAMPs) to 3.6 V 2.4 V (VREFBUF) to 3.6 V. V_{DDA} is the external analog power supply for A/D and D/A converters, voltage reference buffer, operational amplifiers and comparators. The V_{DDA} voltage level is independent from the V_{DD} voltage.
	NA	V_{LCD} = 2.5 to 3.6 V. The LCD controller can be powered either externally through the VLCD pin, or internally from an internal voltage generated by the embedded step-up converter.
	N/A USB OTG FS powered by V_{DD}. V_{DD} should be > 3.0 V (or degraded electrical characteristic between 2.7 V to 3V).	V_{DDUSB} = 3.0 to 3.6 V. V_{DDUSB} is the external independent power supply for USB transceivers. The V_{DDUSB} voltage level is independent from the V_{DD} voltage.
	N/A No VDDIO2 supply in STM32F401/411 lines.	V_{DDIO2} = 1.08 V to 3.6 V V_{DDIO2} is the external power supply for 14 I/Os (Port G[15:2]). The V_{DDIO2} voltage level is independent from the V_{DD} voltage.

Table 14. PWR differences between STM32F401/411 lines and STM32L4 series (continued)

PWR	STM32F401/411 lines	STM32L4 series
Battery backup domain	– RTC with backup registers (80 bytes) – LSE – PC13 to PC15 I/Os	– RTC with backup registers (128 bytes) – LSE – PC13 to PC15 I/Os
Power supply supervisor	Integrated POR / PDR circuitry Programmable voltage detector (PVD)	Integrated POR / PDR circuitry Programmable Voltage Detector (PVD)
	Brownout reset (BOR) BOR can be disabled after power-on	Brownout reset (BOR) BOR is always enabled, except in Shutdown mode
	NA	4 Peripheral Voltage Monitoring (PVM) – PVM1 for V_{DDUSB} – PVM2 for V_{DDIO2} – PVM3/PVM4 for V_{DDA} (~1.65 V/ ~2.2 V)
Low-power modes	Sleep mode	Sleep mode
	NA	Low Power Run mode System clock is limited to 2 MHz. I2C and U(S)ART/LPUART can be clocked with HSI16 at 16 MHz. Consumption is reduced at lower frequency thanks to LP regulator usage.
	NA	Low power Sleep mode System clock is limited to 2 MHz. I2C and U(S)ART/LPUART can be clocked with HSI16 at 16 MHz. Consumption is reduced at lower frequency thanks to LP regulator usage.
	Stop mode (all clocks are stopped)	Stop1 and Stop2 mode Some additional functional peripherals (cf wakeup source)
	Standby mode (V_{CORE} domain powered off)	Standby mode (V_{CORE} domain powered off) – Optional SRAM2 retention – Optional I/O pull-up or pull-down configuration
	NA	Shutdown mode (V_{CORE} domain powered off and power monitoring off)

Table 14. PWR differences between STM32F401/411 lines and STM32L4 series (continued)

PWR	STM32F401/411 lines	STM32L4 series
Wake-up sources	Sleep mode – Any peripheral interrupt/wakeup event	Sleep mode – Any peripheral interrupt/wakeup event
	Stop mode – Any EXTI line event/interrupt – PVD, RTC	Stop mode – Any EXTI line event/interrupt – BOR, PVD, PVM, COMP, RTC, USB, IWDG, – U(S)ART, LPUART, I2C, SWP, LPTIM, LCD
	Standby mode – WKUP pin (PA0) rising edge – RTC event – External reset in NRST pin – IWDG reset	Standby mode – 5 WKUP pins rising or falling edge – RTC event – External reset in NRST pin – IWDG reset
	NA	Shutdown mode – 5 WKUP pins rising or falling edge – RTC event – External reset in NRST pin
Wake-up clocks	Wake-up from Stop – HSI 16 MHz	Wake-up from Stop – HSI16 16 MHz or MSI (all ranges up to 48 MHz) allowing 5 µs wakeup at high speed without waiting for PLL startup time.
	Wake-up from Standby – HSI 16 MHz	Wake-up from Standby – MSI (ranges from 1 to 8 MHz)
	NA	Wake-up from Shutdown – MSI 4 MHz
Configuration	-	In STM32L4 series the registers are different: From 2 registers in STM32F401/411 lines to 23 registers in STM32L4 series – 4 control registers – 2 status registers – 1 status clear register – 2 registers per GPIO port (A,B,..H) for controlling pull-up and pull-down (16registers). Most configuration bits from STM32F401/411 lines can be found in STM32L4 series (but sometime may have different programming mode).

Color key:

= New feature or new architecture (difference between STM32F401/411 lines and STM32L4 series)

= Same feature, but specification change or enhancement

= Feature not available (NA)

= Difference between STM32F401/411 lines and STM32L4 series highlight

4.7 RTC

The STM32L4 series and STM32F401/411 lines implement almost the same features on the RTC.

The table below shows the differences.

Table 15. RTC differences between STM32F401/411 lines and STM32L4 series

RTC	STM32F401/411 lines	STM32L4 series
Features	Coarse digital calibration. (kept for compatibility only, new developments should only use smooth calibration).	Only smooth calibration available
	1 tamper pin (available in VBAT)	3 tamper pin (available in VBAT
	80 bytes backup registers	128 bytes backup registers
Configuration	-	Coarse digital calibration not available in STM32L4 series: – RTC_CR/DCE not available – RTC_CALIBR register not available – RTC_TAFCR (F4) → RTC_TAMPCR (L4) Except a few bits
Color key: = Same feature, but specification change or enhancement = Feature not available (NA)		

For more information about STM32L4 series RTC features, please refer to RTC chapter of STM32L4 series reference manuals.

4.8 SYSCFG

The STM32L4 series SYSCFG implements additional features compared to STM32F401/411 lines.

The table below shows the differences.

Table 16. SYSCFG differences between STM32F401/411 lines and STM32L4 series

SYSCFG	STM32F401/411 lines	STM32L4 series
Features	– Remapping memory areas. – Managing the external interrupt line connection to the GPIOs.	– Remapping memory areas. – Managing the external interrupt line connection to the GPIOs. – Managing robustness feature. – Setting SRAM2 write protection and software erase. – Configuring FPU interrupts. – Enabling the firewall. – Enabling /disabling I2C Fast-mode Plus driving capability on some I/Os and voltage booster for I/Os analog switches.
Configuration	-	Most registers from STM32F401/411 lines are identical in STM32L4 series. A few bits are different and EXTI configuration may differ (no GPIO PH[2:15] in STM32L4 series).
Color key: = Same feature, but specification change or enhancement		

4.9 GPIO

The STM32L4 series GPIO peripheral embeds identical features compared to STM32F401/411 lines.

The GPIO code written for the STM32F401/411 lines may require minor adaptations for STM32L4 series. This is due to the mapping of particular functions on different GPIOs (refer to pinout differences in *Section 2*, and to product datasheet for detailed alternate function mapping differences).

Below are the main GPIO features:

- GPIO mapped on AHB bus for better performance
- I/O pin multiplexer and mapping: pins are connected to on-chip peripherals/modules through a multiplexer that allows only one peripheral alternate function (AF) connected to an I/O pin at a time. In this way, there cannot be any conflict between peripherals sharing the same I/O pin.

At reset, STM32F401/411 lines GPIOs are configured in input floating mode while STM32L4 series GPIOs are configured in analog mode (to avoid consumption through the IO Schmitt trigger).

For more information about STM32L4 series GPIO programming and usage, please refer to the "I/O pin multiplexer and mapping” section in the GPIO chapter of the STM32L4 series

reference manuals and to the product datasheet for detailed description of the pinout and alternate function mapping.

4.10 EXTI source selection

The external interrupt/event controller (EXTI) is very similar on the STM32F401/411 lines and the STM32L4 series. The table below shows the main differences.

Table 17. EXTI differences between STM32F401/411 lines and STM32L4 series

EXTI	STM32F401/411 lines	STM32L4 series
Nb of event/interrupt lines	Up to 23 configurable lines	Up to 40 lines (14 direct, 26 configurable)
Configuration	-	Registers are slightly different to cope with different number of interrupts.
Color key: = Same feature, but specification change or enhancement		

4.11 FLASH

The table below presents the difference between the FLASH interface of STM32F401/411 lines and STM32L4 series.

The STM32L4 series instantiates a different FLASH module both in terms of architecture/technology and interface, consequently the STM32L4 series FLASH programming procedures and registers are different from the STM32F401/411 lines, and any code written for the FLASH interface in the STM32F401/411 lines needs to be rewritten to run in STM32L4 series.

For more information on programming, erasing and protection of the STM32L4 series Flash memory, please refer to the STM32L4 series reference manuals

Table 18. FLASH differences between STM32F401/411 lines and STM32L4 series

FLASH	STM32F401/411 lines	STM32L4 series
Main/Program memory	0x0800 0000 – (up to) 0x081F FFFF	0x0800 0000 - up to 0x080F FFFF
	Up to 512 Kbyte 4 sectors of 16 Kbyte 1 sector of 64 Kbyte 1 or 3 sectors of 128 Kbyte Programming granularity: 8, 16, 32, 64-bit Read granularity: 128-bit	Up to 1 Mbyte Split in 2 banks Each bank: 256 pages of 2 Kbyte Each page: 8 rows of 256 Byte Programming and read granularity: 72-bit (incl 8 ECC bits)
Features	NA	Read while write (RWW) Dual bank boot
	NA	ECC
Wait state	up to 6 (depending on the supply voltage and frequency)	up to 4 (depending on the core voltage and frequency)

Table 18. FLASH differences between STM32F401/411 lines and STM32L4 series (continued)

FLASH	STM32F401/411 lines	STM32L4 series
ART Accelerator™	Allowing 0 wait state when executing from the cache.	Allowing 0 wait state when executing from the cache.
One time programmable (OTP)	512 OTP bytes	1 KB OTP bytes (bank1)
Flash interface	NA	Different from STM32F401/411 lines
Erase granularity	Sector and mass erase	Page erase (2 Kbyte), bank erase and mass erase (both banks)
Read protection (RDP)	Level 0 no protection RDP = 0xAA	Level 0 no protection RDP = 0xAA
	Level 1 memory protection RDP ≠ {0xAA, 0xCC}	Level 1 memory protection RDP ≠ {0xAA, 0xCC}
	Level 2 RDP = 0xCC(1)	Level 2 RDP = 0xCC(1)
Proprietary code readout Protection (PCROP)	Granularity: 1 sector	2 PCROP areas (1 per bank) Granularity: 64-bit PCROP_RDP option: PCROP area preserved when RDP level decreased.
Write protection (WRP)	Granularity: 1 sector	4 write protection areas (2 per bank) Granularity: 2 Kbyte
User Option bytes	nRST_STOP	nRST_STOP
	nRST_STDBY	nRST_STDBY
	NA	nRST_SHDW
	WDG_SW	IWDG_SW
	NA	IWDG_STOP, IWDG_STDBY
	NA	WWDG_SW
	BOR_LEV[1:0]	BOR_LEV[2:0]
	NA	BFB2
	NA	nBOOT1
	NA	SRAM2_RST, SRAM2_PE
	NA	DUAL BANK
	SPRMOD	NA

Color key:

= New feature or new architecture (difference between STM32F401/411 lines and STM32L4 series)

= Same feature, but specification change or enhancement

= Feature not available (NA)

= Difference between STM32F401/411 lines and STM32L4 series highlight

1. Memory read protection level 2 is an irreversible operation. When level 2 is activated, the level of protection cannot be decreased to level 0 or level 1.

4.12 U(S)ART

The STM32L4 series implement several new features on the U(S)ART compared to STM32F401/411 lines.

The table below shows the differences.

Table 19. U(S)ART differences between STM32F401/411 lines and STM32L4 series

U(S)ART	STM32F401/411 lines	STM32L4 series
Instances	3 x USART	3 x USART 2 x UART 1 x LPUART
Baud rate	up to 2 x 10.5 Mbit/s + 1 x 5.25 Mb/s (F401) up to 2 x 12.5 Mbit/s + 1 x 6.25 Mb/s (F411)	up to 10 Mbit/s (when the clock frequency is 80 MHz and oversampling is by 8)
Clock	Single clock domain	Dual clock domain allowing: – UART functionality and wakeup from Stop mode – Convenient baud rate programming independent from the PCLK reprogramming
Data	Word length: programmable (8 or 9 bits)	Word length: programmable (7, 8 or 9 bits) Programmable data order with MSB-first or LSB-first shifting
interrupt	10 interrupt sources with flags	14 interrupt sources with flags
Features	Hardware flow control (CTS/RTS) Continuous communication using DMA Multiprocessor communication Single-wire half-duplex communication IrDA SIR ENDEC block LIN mode SPI master	
	Smartcard mode T = 0 and T = 1 is to be implemented by software	Smartcard mode T = 0 and T = 1 supported (features are added to support T = 1 such as receiver timeout, block length, end of block detection, binary data inversion, etc…)
	Number of stop bits: 0.5, 1, 1.5, 2	Number of stop bits: 1, 1.5, 2

Table 19. U(S)ART differences between STM32F401/411 lines and STM32L4 series (continued)

U(S)ART	STM32F401/411 lines	STM32L4 series
Features (continued)	NA	– Wakeup from Stop mode (Start bit, received byte, address match) – Support for ModBus communication Timeout feature CR/LF character recognition – Receiver timeout interrupt – Auto baud rate detection – Driver Enable – Swappable Tx/Rx pin configuration LPUART does not support synchronous mode (SPI Master), smartcard mode, IrDA, LIN, ModBus, receiver timeout interrupt, auto baud rate detection.
	NA	STM32F401/411 lines registers and associated bits are not identical in STM32L4 series. Please refer to STM32L4 series reference manuals for details
Color key: = New feature or new architecture (difference between STM32F401/411 lines and STM32L4 series) = Same feature, but specification change or enhancement = Feature not available (NA) = Difference between STM32F401/411 lines and STM32L4 series highlight		

4.13 I2C

The STM32L4 series implements a different I2C peripheral allowing easy software management.

The table below shows the differences.

Table 20. I2C differences between STM32F401/411 lines and STM32L4 series

I2C	STM32F401/411 lines	STM32L4 series
Instances	x3 (I2C1, I2C2, I2C3)	
Features	7-bit and 10-bit addressing mode SMBus Standard mode (Sm, up to 100 kHz) Fast mode (Fm, up to 400 kHz)	
	NA	Fast mode Plus (Fm+, up to 1 MHz) Independent clock Wakeup from STOP on address match

Table 20. I2C differences between STM32F401/411 lines and STM32L4 series (continued)

I2C	STM32F401/411 lines	STM32L4 series
Configuration	-	Register configuration is very different in STM32F401/411 lines and STM32L4 series. Please refer to STM32L4 series reference manuals for details.

Color key:

= New feature or new architecture (difference between STM32F401/411 lines and STM32L4 series)

= Feature not available (NA)

= Difference between STM32F401/411 lines and STM32L4 series highlight

4.14 SPI/I2S/SAI

The STM32L4 series and STM32F401/411 lines implement almost the same feature on the SPI (apart from I2S).

The table below shows the differences.

Table 21. SPI differences between STM32F401/411 lines and STM32L4 series

SPI	STM32F401/411 lines	STM32L4 series
Instances	x4 (F401) x5 (F411)	x3
Features	SPI + I2S	I2S feature is not supported by SPI in STM32L4 series 2 SAI interfaces are available instead
Data size	Fixed, configurable to 8 or 16 bits	Programmable from 4 to 16-bit
Data buffer	Tx & Rx 16-bit buffers (single data frame)	32-bit Tx & Rx FIFOs (up to 4 data frames)
Data packing	No (16-bit access only)	Yes (8-bit, 16-bit or 32-bit data access, programmable FIFOs data thresholds)
Mode	SPI TI mode SPI Motorola mode	SPI TI SPI Motorola mode NSSP mode
Speed	up to 42 Mbit/s (core at 84 MHz) (F401) up to 50 Mbit/s (core at 100 MHz) (F411)	up to 40Mbits/s (APB at 80MHz)
Configuration	-	The data size and Tx/Rx flow handling are different in STM32F401/411 lines and STM32L4 series hence requiring different software sequence.

Color key:

= New feature or new architecture (difference between STM32F401/411 lines and STM32L4 series)

= Same feature, but specification change or enhancement

= Difference between STM32F401/411 lines and STM32L4 series highlight

Migrating from I2S to SAI:

The STM32L4 series does not include I2S interface part of the SPI peripheral, instead it includes two serial audio interfaces.

The table below shows main differences between I2S and SAI. We only consider here the full duplex I2S instances.

Table 22. Migrating from I2S to SAI

I2S/SAI	STM32F401/411 lines (I2S)	STM32L4 series (SAI)
Instances Full duplex I2S	x2	x2 (SAI1, SAI2)
Features	Full-duplex communication	Two independent audio sub-blocks (per SAI) which can be transmitters or receivers with their respective FIFO.
	Master or slave operations	Synchronous or asynchronous mode between the audio sub-blocks. Possible synchronization between multiple SAIs. Master or slave configuration independent for both audio sub-blocks.
	8-bit programmable linear prescaler to reach accurate audio sample frequencies (from8 kHz to 192 kHz)	Clock generator for each audio block to target independent audio frequency sampling when both audio sub-blocks are configured in master mode.
	Data format may be 16-bit, 24-bit or 32-bit. Data direction is always MSB first.	Data size configurable: 8-, 10-, 16-, 20-, 24-, 32-bit. First active bit position in the slot is configurable. LSB first or MSB first for data transfer.
	Channel length is fixed to 16-bit (16-bit data size) or 32-bit (16-bit, 24-bit, 32-bit data size) by audio channel.	Up to 16 slots available with configurable size. Number of bits by frame can be configurable. Frame synchronization active level configurable (offset, bit length, level). Stereo/Mono audio frame capability.
	Programmable clock polarity (steady state).	Communication clock strobing edge configurable (SCK).
	16-bit register for transmission and reception with one data register for both channel sides.	8-word integrated FIFOs for each audio sub-block (facilitating interrupt mode).
	Supported I^2S protocols: – I^2S Philips standard – MSB-justified standard (left-justified) – LSB-justified standard (right-justified) – PCM standard (with short and long frame synchronization on 16-bit channel frame or 16-bit data frame extended to 32-bit channel frame).	Audio protocols: – I^2S, LSB or MSB-justified, PCM/DSP, TDM (up to 16 channels), AC'97 – SPDIF output
	DMA capability for transmission and reception (16-bit wide).	2-channel DMA per SAI.
	Master clock may be output to drive an external audio component. Ratio is fixed at 256 × F_S (where F_S is the audio sampling frequency).	
	Interruption sources when enabled: – Errors, – Tx Buffer Empty, Rx Buffer not Empty.	Interruption sources when enabled: – Errors, – FIFO requests.

Table 22. Migrating from I2S to SAI (continued)

I2S/SAI	STM32F401/411 lines (I2S)	STM32L4 series (SAI)
Features (continued)	Error flags with associated interrupts if enabled respectively. – Overrun and underrun detection, – Anticipated frame synchronization signal detection in slave mode, – Late frame synchronization signal detection in slave mode.	Idem STM32F401/411 lines + protection against misalignment in case of underrun and overrun.
Configuration	-	There is no compatibility between STM32F401/411 lines I2S and STM32L4 series SAI. User will have to configure the SAI interface for the target protocol. Please refer to the STM32L4 series reference manuals for details.

Color key:

= New feature or new architecture (difference between STM32F401/411 lines and STM32L4 series)

= Same feature, but specification change or enhancement

= Difference between STM32F401/411 lines and STM32L4 series highlight

The SAI peripheral improves robustness of communication in slave mode compared to I2S peripheral (in case of data clock glitch for example)

In master mode, while migrating an application from STM32F401/411 lines to STM32L4 series, the user should review the possible master clock (MCLK), data bit clock (SCK) and frame synchronization (FS) frequency reachable using STM32L4 series PLL multiplication factors and SAI internal clock divider for a given external oscillator which can be different than with STM32F401/411 lines I2S.

In STM32L4 series, the SAI1 and SAI2 input clocks are derived (selected by software) from one of the four following sources:

- an external clock mapped on SAI1_EXTCLK for SAI1 and SAI2_EXTCLK for SAI2.
- PLLSAI1 (P) divider output (PLLSAI1CLK)
- PLLSAI2 (P) divider output (PLLSAI2CLK)
- main PLL (P) divider output (PLLSAI3CLK)

When the clock is derived from one of the three internal PLLs, the three PLL inputs are either HSI16, HSE or MSI (between 4 and 8 MHz) divided by a programmable factor PLLM (from 1 to 8). This input is then multiplied by PLLN (from 8 to 86) to reach PLL VCO frequency (should be between 64 and 344 MHz). It is finally divided by PLLP (7 or 17) to provide the input clock of the SAI (max 80 MHz)

When the master clock MCLK is used by the external slave audio peripheral, the PLL output is divided by the SAI internal master clock divider factor (1, 2, 4, 6, 8, ..., 30) to provide the master clock (MCLK). The data bit clock is then derived from MCLK with the following formula:

$$SCK = MCLK \times (FRL + 1) / 256 = (MCLK) / (256 / (FRL + 1))$$

With:

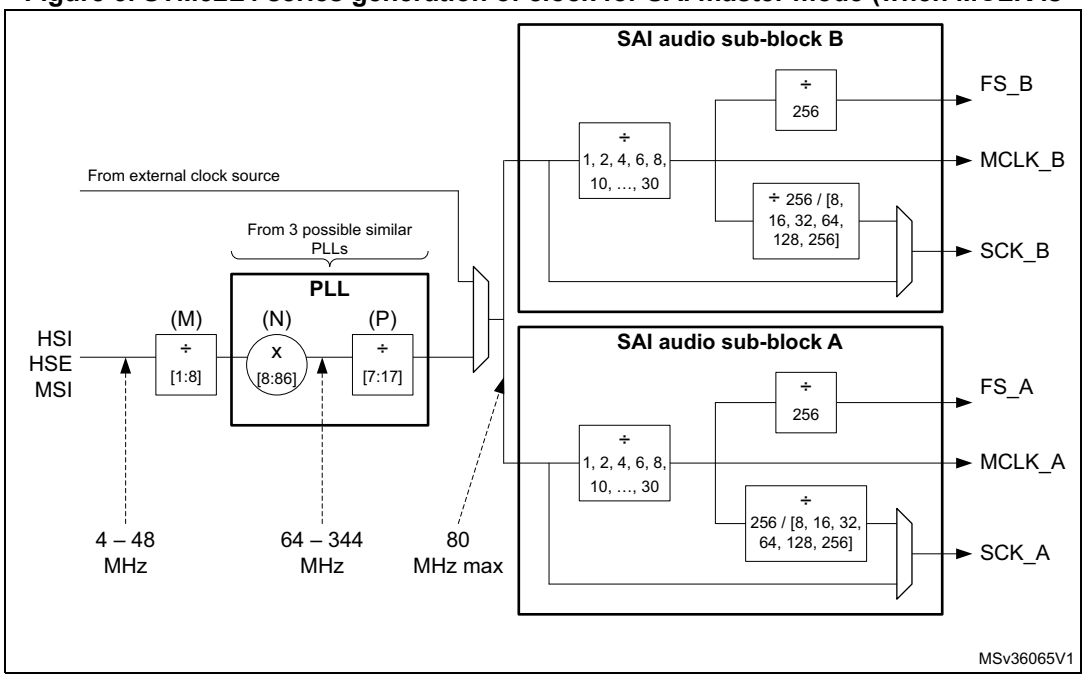
- FRL is the number of bit clock cycles - 1 in the audio frame (0 to 255).
- (FRL+ 1) should be a power of 2 higher or equal to 8
  – (FRL + 1) = 8, 16, 32, 64, 128, 256

SCK can also be directly connected to the input clock of the SAI when MCLK output is not needed.

The frame synchronization (FS) frequency is always MCLK/256.

Below is shown the clock generation scheme in STM32L4 series. Please refer to the STM32L4 series reference manuals for more details.

Figure 3. STM32L4 series generation of clock for SAI master mode (when MCLK is required)



4.15 CRC

The cyclic redundancy check (CRC) calculation unit is very similar in STM32F401/411 lines and STM32L4 series.

The table below shows the differences.

Table 23. CRC differences between STM32F401/411 lines and STM32L4 series

CRC	STM32F401/411 lines	STM32L4 series
Features	Single input/output 32-bit data register. CRC computation done in 4 AHB clock cycles (HCLK) for the 32-bit data size. General-purpose 8-bit register (can be used for temporary storage).	
	Use CRC-32 (Ethernet) polynomial: 0x4C11DB7. Handles 32-bit data size.	Fully programmable polynomial with programmable size (7, 8, 16, 32-bit). Handles 8-,16-, 32-bit data size. Programmable CRC initial value. Input buffer to avoid bus stall during calculation. Reversibility option on input and output.
Configuration	-	Configuration registers in STM32F401/411 lines are identical in STM32L4 series. The STM32L4 series includes additional registers for new features. Please refer to the STM32L4 series reference manuals for details.
Color key: = New feature or new architecture (difference between STM32F401/411 lines and STM32L4 series)		

4.16 USB OTG FS

The STM32L4 series and STM32F401/411 lines implement very similar USB OTG FS peripherals.

The key differences are listed below.

Table 24. USB OTG FS differences between STM32F401/411 lines and STM32L4 series

USB	STM32F401/411 lines	STM32L4 series
Features	Universal serial bus revision 2.0 Full support for the USB on-the-go (USB OTG).	
	FS mode: 1 bidirectional control endpoint 3 IN endpoints (bulk, interrupt, isochronous) 3 OUT endpoints (bulk, interrupt, isochronous)	FS mode: 1 bidirectional control endpoint 5 IN endpoints (bulk, interrupt, isochronous) 5 OUT endpoints (bulk, interrupt, isochronous)
	USB internal connect/disconnect feature with an internal pull-up resistor on the USB D + (USB_DP) line.	
	NA	Attach detection protocol (ADP) Battery charging detection (BCD)
	NA	Independent V_{DDUSB} power supply allowing lower V_{DDCORE} while using USB.
Mapping	AHB2	
Buffer memory	1.25 Kbyte data FIFOs. Management of up to 4 Tx FIFOs (1 for each IN end point) + 1 Rx FIFO.	1.25 Kbyte data FIFOs. Management of up to 6 Tx FIFOs (1 for each IN end point) + 1 Rx FIFO.
Low-power modes	USB suspend and resume.	USB suspend and resume Link power management (LPM) support
Configuration	-	In STM32L4 series the registers are different. Please refer to the STM32L4 series reference manuals for details.

Color key:

= New feature or new architecture (difference between STM32F401/411 lines and STM32L4 series)

= Same feature, but specification change or enhancement

= Feature not available (NA)

= Difference between STM32F401/411 lines and STM32L4 series highlight

4.17 ADC

The table below presents the differences between the STM32F401/411 lines and STM32L4 series ADC peripherals. These differences are the following:

- New digital interface
- New architecture and new features

Table 25. ADC differences between STM32F401/411 lines and STM32L4 series

ADC	STM32F401/411 lines		STM32L4 series	
ADC Type	SAR structure		SAR structure	
Instances	1 instance		3 instances	
Max Sampling freq	2.4 Msps		5.1 Msps (Fast channels) 4.8 Msps (Slow channels)	
Number of channels	Up to 16 channels		Up to 19 channels per ADC	
Resolution	12-bit		12-bit + digital oversampling up to 16-bit	
Conversion Modes	Single / continuous / scan / discontinuous		Single / continuous / scan / discontinuous Dual Mode	
DMA	Yes		Yes	
External Trigger	Yes		Yes	
	External event for regular group: TIM1 CC1 TIM1 CC2 TIM1 CC3 TIM2 CC2 TIM2 CC3 TIM2 CC4 TIM2_TRGO TIM3_CH1 TIM3 TRGO TIM4 CC4 TIM5_CC1 TIM5_CC2 TIM5_CC3 EXTI line 11	External event for injected group: TIM1_CH4 TIM1_TRGO TIM2_CH1 TIM2_TRGO TIM3_CH2 TIM3_CH4 TIM4_CH1 TIM4_CH2 TIM4_CH3 TIM4_TRGO TIM5_CH4 TIM5_TRGO EXTI line 15	External event for regular group: TIM1 CC1 TIM1 CC2 TIM1 CC3 TIM2 CC2 TIM3 TRGO TIM4 CC4 EXTI line 11 TIM8_TRGO TIM8_TRGO2 TIM1_TRGO TIM1_TRGO2 TIM2_TRGO TIM4_TRGO TIM6_TRGO TIM15_TRGO TIM3_CC4	External event for injected group: TIM1 TRGO TIM1 CC4 TIM2 TRGO TIM2 CC1 TIM3 CC4 TIM4 TRGO EXTI line15 TIM8_CC4 TIM1_TRGO2 TIM8_TRGO TIM8_TRGO2 TIM3_CC3 TIM3_TRGO TIM3_CC1 TIM6_TRGO TIM15_TRGO
Supply requirement	1.8 V to 3.6 V (1.7 V with external power-supply supervisor)		1.62 V to 3.6 V Independent power supply (V_{DDA})	
Reference Voltage	External V_{DDA} - V_{REF+} < 1.2 V		Reference voltage for STM32L4 series external (1.8 V to V_{DDA}) or internal (2.048 V or 2.5 V)	
Electrical Parameters	300 µA (Typ.) on V_{REF} DC current 1.8 mA (Typ.) on V_{DDA} DC current		Consumption proportional to conversion speed: 200 µA/Msps	

Table 25. ADC differences between STM32F401/411 lines and STM32L4 series (continued)

ADC	STM32F401/411 lines	STM32L4 series
Input range	$V_{REF-} \leq V_{IN} \leq V_{REF+}$	$V_{REF-} \leq V_{IN} \leq V_{REF+}$
Color key: = New feature or new architecture (difference between STM32F401/411 lines and STM32L4 series) = Same feature, but specification change or enhancement		

5 Revision history

Table 26. Document revision history

Date	Revision	Changes
21-Jul-2015	1	Initial release.