C35 Analog Trigger Backplane Test at Ciemat

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List of Abbreviations			

History		
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Distribution	

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1. Introduction

This document contains a description of the specific tests performed with Analog Trigger Backplanes (ATBP) during C35 test at Ciemat. The goal of the test is the verification of the functionality and performance of 35 modules one installed in the cluster holder structure and powered with final power supply

2. SET-UP description

The set-up used for this test is intended to be as close as possible to final operation conditions, with camera elements available at this moment. Figure 1 shows a block diagram of the test setup. Cluster elements are the same that will be used in the camera: Dragon board, L0 + L1 mezzanines and backplanes. Cluster holder structure and power supply are also final. Power distribution cables and busbars, Ethernet cables, Ethernet switches and computer are not final. TIB and UCTs are faked with a backplane module with a simple firmware to provide Clock and PPS and implement a loopback for distributed L1 trigger and Camera Trigger. Figure shows a picture of the set-up.

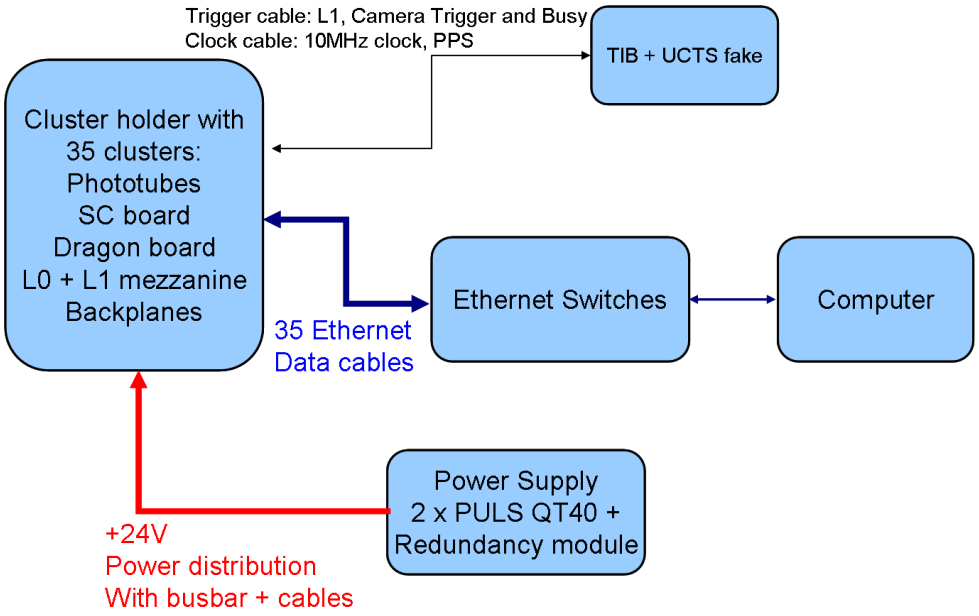

Figure 1 Simple block diagram of setup used in the test

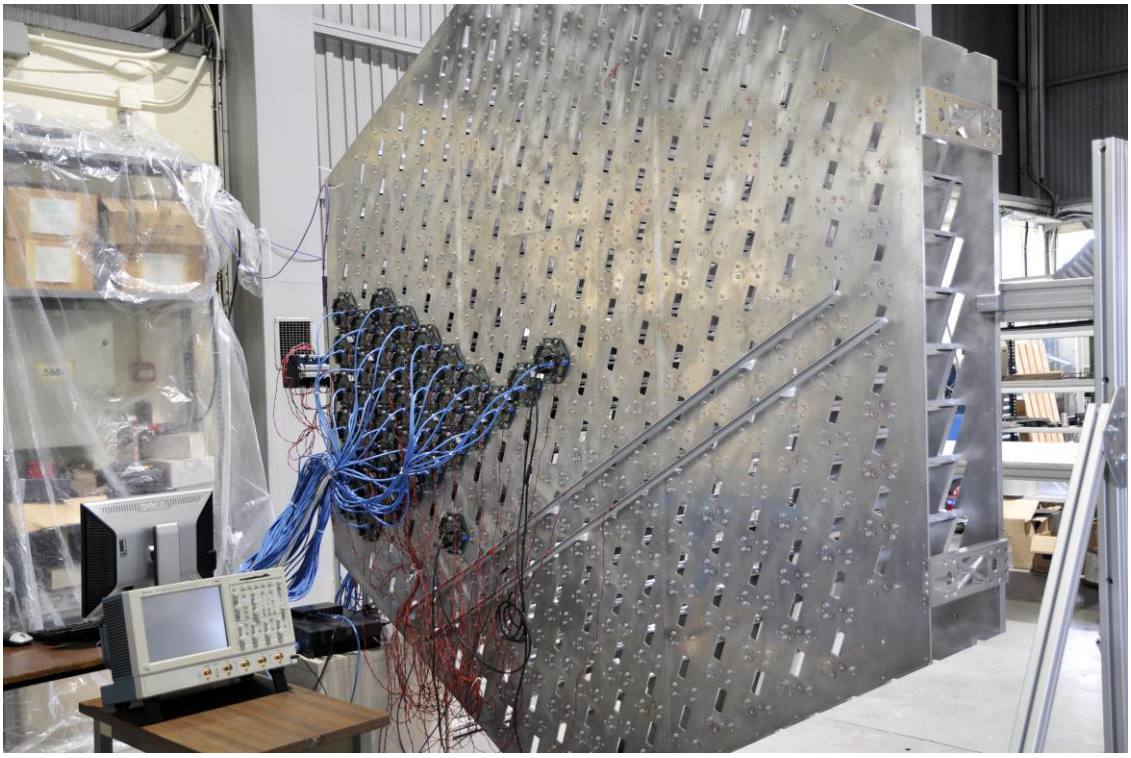

Figure 2 Picture of Setup installed at Ciemat

3. Test description and results

3.1. Power rails test

Backplane power rails noises were tested in several modules in order to confirm they are compatible with the values measured in the laboratory. No significant difference of noise was measured. Noise levels are not depending on the distance of the backplane to the power supply. Table 1 shows a comparison between noise levels measured in the setup and in the laboratory.

Power Rail	Rms noise @50Ks/s C35 test	Rms noise @50Ks/s Lab	Rms noise @1,25Gs/s C35 test	Rms noise @1,25Gs/s Lab
24V	14mV	10mV	18mV	12mV
+3.3V Analog	5mV	8mV	17mV	11mV
-3.3V Analog	5mV	8mV	17mV	11mV
+3.3V Digital	5mV	8mV	17mV	10mV
+2.5V Digital	5mV	8mV	17mV	10mV

+1.2V Digital	5mV	8mV	17mV	10mV

Table 1 Power rails noise in backplane

Figures 3, 4 and 5 show some examples of noise measurements performed with the scope.

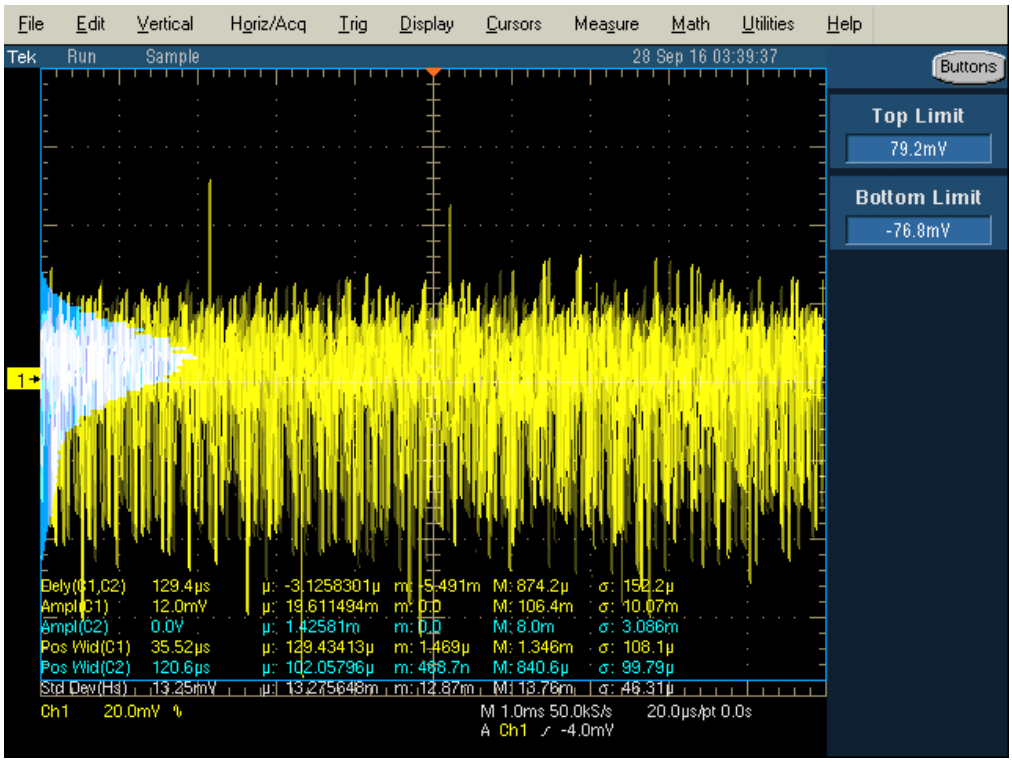

Figure 3 24V rms noise

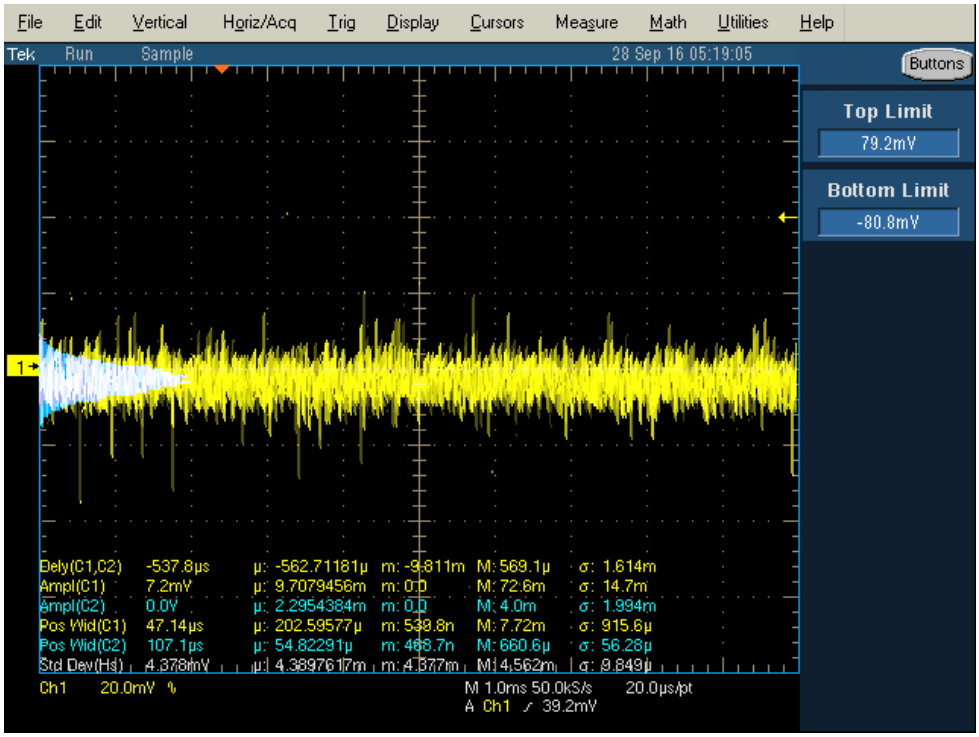

Figure 4 -3.3V Analog rms noise

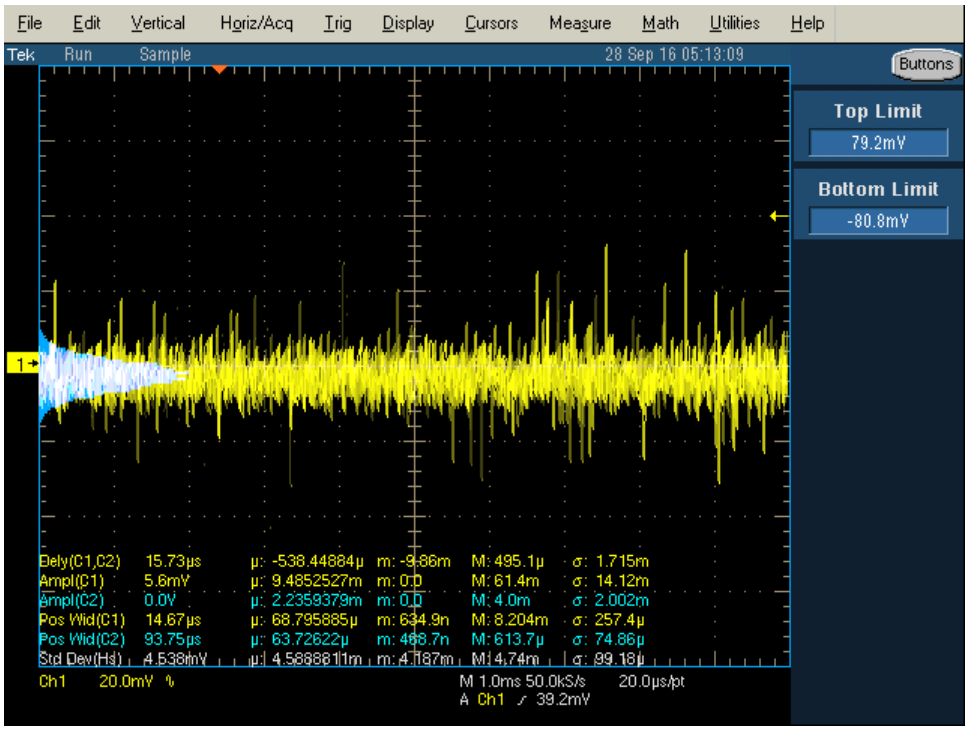

Figure 5 2.5V Digital rms noise

3.2. L1 and Camera Trigger distribution test

3.2.1. Trigger distribution Latency

Delay of trigger distribution was measured with a scope for every backplane in the set-up connected to a cluster with L0 + L1 mezzanine. It was measured in the so-called UP direction, that is, from L1 trigger input at backplane to L1 trigger input at TIB fake module, and in the so-called DOWN direction, that is, from TIB fake L1 trigger input to backplane Camera Trigger output. In both cases the measurement was done with and without coarse delay set in the backplane.

IP	Ring	UP Latency (no coarse) ns	UP Latency (coarse) ns	DOWN Latency (no coarse) ns	DOWN Latency (coarse) ns
82	0	29,3	148,5	27,85	138,88
10	1	49,22	150,08	36,9	140,21
20	2	58,78	149,31	45,95	139,11
108	3	68,62	151,35	55,2	140,25
78	4	77,73	149,06	63,88	137,65
12	4	77,33	149,94	64,15	139
75	5	87,15	151,8	73,51	139,4
150	5	87,18	149,9	72,82	136,6
83	5	87,21	153,82	73,58	141,75
144	6	96,6	151,75	82,35	139,85
57	6	96,5	152,17	82,28	140,12
80	6	97,08	151,77	82,07	138,73
130	6	96,75	152,68	82,62	141,09
30	7	106,3	152,4	91,65	139,4
77	7	106	152,4	91,35	139,27
105	7	106,07	152,55	91,17	139,42
19	7	107	154,22	91,5	140,69
119	7	106,29	154,42	91,72	141,5
89	8	115,87	154,95	100,7	140,15
145	8	115,78	155,92	100,6	140,92
61	8	115,45	153,7	100,22	138,56
66	8	115,85	154,84	100,64	139,83
47	8	116,3	154,45	100,26	138,05
149	8	115,78	155,05	100,62	139,8
15	9	124,96	154,2	109,3	139,19
14	9	124,95	154,35	109,18	138,67
135	9	125,3	155,17	109,47	139,8
74	9	125,34	154,54	109,42	139,19
24	9	125,69	156,4	109,8	140,88
73	9	125,3	155,45	109,62	140,35

Table 2 Trigger distribution latency

Without coarse delay correction, latency difference between two consecutive rings is around 10ns for all the backplanes in the setup, very similar to one coarse delay step. Latency in the outer ring is around 125ns for UP direction and 110ns for DOWN direction. Latency obtained with coarse delay correction can go up to 155ns for UP direction and 140ns for DOWN direction. Dispersion of latency after coarse correction is less than 10ns, so final latency in the full camera can be equalized with fine delay correction. There is some margin in the latency for bypassing one non-working backplane. If more contingency is needed, firmware can be adapted to have a wider margin.

3.2.2. Trigger distribution Jitter

Jitter of trigger distribution was measured with a scope for every backplane in the set-up connected to a cluster with L0 + L1 mezzanine. It was measured in the so-called UP direction, that is, from L1 trigger input at backplane to L1 trigger input at TIB fake module, and in the so-called DOWN direction, that is, from TIB fake L1 trigger input to backplane Camera Trigger output. In both cases the measurement was done with and without coarse delay set in the backplane.

IP	Ring	L1 Trigger Jitter (no coarse) ps	L1 Trigger Jitter (coarse) ps	Camera Trigger Jitter (no coarse) ps	Camera Trigger Jitter (coarse) ps
82	0	14	24	13	22
10	1	15	21,5	10	10
20	2	15,3	22	12,45	19,4
108	3	16,6	20,5	14	20
78	4	14,2	19,5	13,85	21,5
12	4	13,1	20,3	14,5	21,1
75	5	15,25	19,5	13,75	19,8
150	5	16,1	18,9	13,1	17,35
83	5	15,5	18,2	13,5	16,8
144	6	14,5	20,5	13	18,75
57	6	16,7	21	15,6	20,2
80	6	16,5	17,8	15,6	17,8
130	6	16,3	16,5	13,8	19,9
30	7	16,9	17,3	15,27	19,3
77	7	16,72	20,9	14	17,9
105	7	14,5	16,5	14,8	16,8
19	7	15,3	18,2	16,5	16,8
119	7	15,3	16,9	15	16,2
89	8	14,6	17,6	15,1	21
145	8	16	18,7	14,9	18,2
61	8	14,7	16,2	13,8	15,9
66	8	15,5	19	14,6	16,8

47	8	15,5	17,5	16,5	18,5
149	8	15,8	17,2	15,3	16,5
15	9	19,8	19,35	15,4	17,29
14	9	15	17	15,8	15,5
135	9	14,8	15,8	15,15	15,7
74	9	18,5	20,5	14,5	18,5
24	9	14,9	17,9	16	17
73	9	16,2	17,2	15,5	16,5

Table 3 Trigger distribution jitter

In the four cases (L1 Trigger jitter without coarse correction, L1 Trigger jitter with coarse correction, Camera Trigger jitter without coarse correction, and Camera Trigger jitter with coarse correction) jitter levels are very good. In addition, it can be observed that jitter does not depend on the position of the backplane in the camera. Some more jitter is measured when coarse correction is applied. Anyway, these levels of jitter are totally negligible since jitter will be dominated by time walk of L1 discriminator and TIB delay line during the operation of the camera.

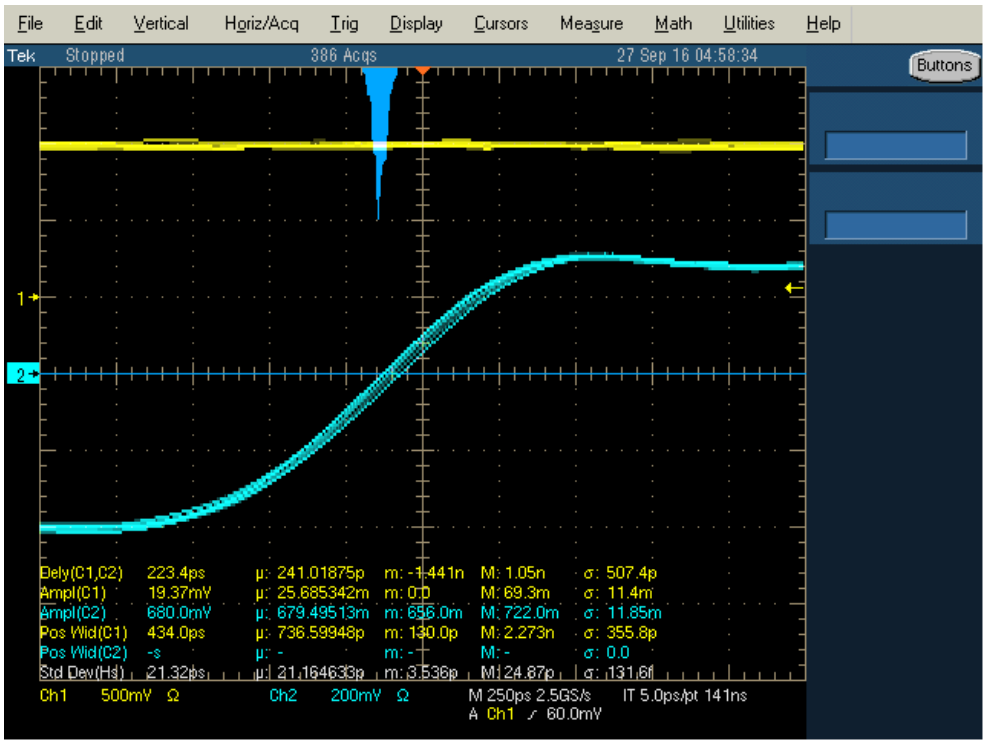

Figure 6 Camera Trigger jitter with respect to L1 at central backplane after coarse delay correction

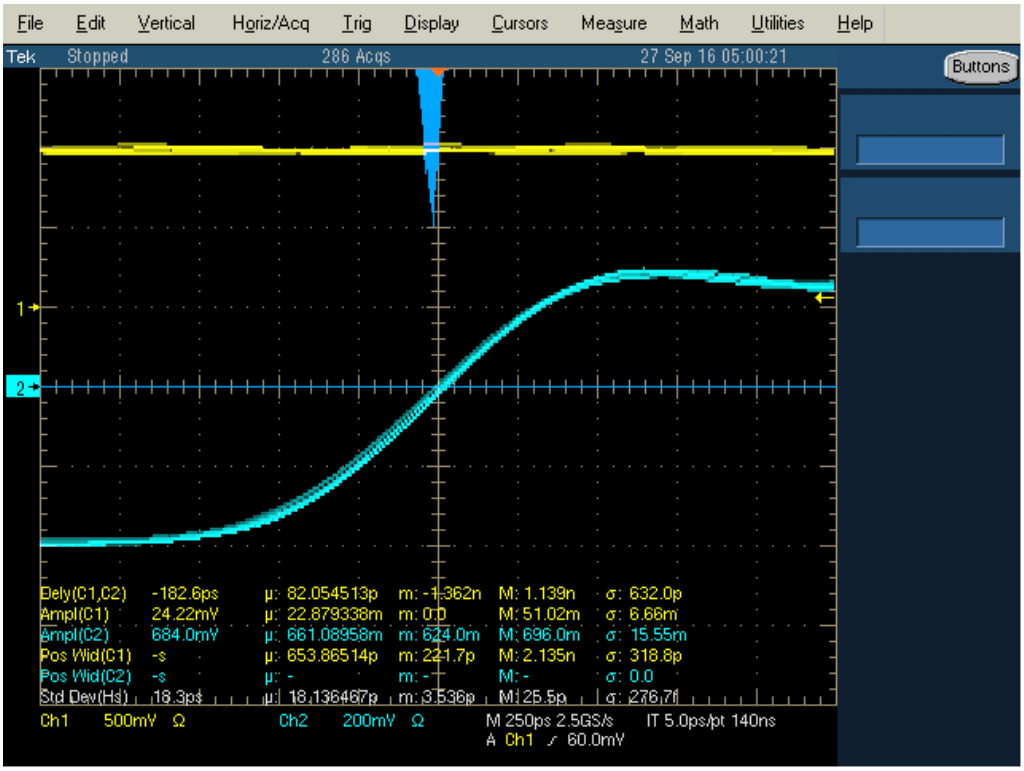

Figure 7 Camera Trigger jitter with respect to L1 at one outer ring backplane after coarse delay correction

3.2.3. Trigger counting

Trigger counting test goal is to check for trigger loose or spurious trigger generation in the trigger distribution. Test is based in generation of trigger in every cluster sequentially and reading of L1 Trigger and Camera Trigger counters implemented in backplanes FPGA. The test was successful since no trigger loose or spurious trigger generation was detected, apart from one trigger loose from time to time when the test pulse enabling is changed to a new Dragon. This still has to be understood but it seems more related with a configuration issue more than a trigger distribution failure.

3.3. Clock and PPS Distribution test

Jitter and delay of clock distribution was measured with the scope. Table 4 shows the results. A delay of about 24 ns is measured from clock in central backplane and clock in outer ring backplane. This value is higher than expected. Cycle to cycle jitter means the dispersion of clock period with time. Values are as expected and there is no difference depending on the

position of the backplane in the camera. Jitter from central means the phase dispersion of the clock in a backplane with respect to clock delivered to central backplane. In this case, values are higher than expected in the outer rings of the camera, getting a correlation of jitter and ring position of the backplane. For both phase correction and jitter optimization some firmware development is needed.

IP	Ring	Delay ns	Cycle to cycle Jitter ps	Jitter from Central ps
82	0	62,75	34	24
10	1	60	31	52
20	2	57,48	38	64
108	3	55,05	34	80
78	4	52,6	32	86
12	4	53	28	82
75	5	50,5	38	93
150	5	49,2	30	102
83	5	49,97	33	85
144	6	48,4	32	98
57	6	48,4	39	105
80	6	48,5	31	101
130	6	47	35	104
30	7	46	36	104
77	7	46	32	110
105	7	46,3	33	120
19	7	45,85	33	114
119	7	43,95	32	92
89	8	43,35	36	107
145	8	43,2	38	120
61	8	44	28	122
66	8	43,7	31	110
47	8	43,7	36	115
149	8	41,8	32	103
15	9	40,8	32	110
14	9	40,6	32	130
135	9	41,27	38	121
74	9	41,3	28	118
24	9	41	39	122
73	9	39,2	30	125

Table 4 Clock distribution delay and jitter

Figures 8, 9 and 10 show some examples of jitter measured with the scope. Regarding PPS distribution, since distributed PPS is sampled with distributed clock before delivery to Dragon board, it can be assumed that delay and jitter of PPS is very similar to delay and jitter of clock. One example is show in figure 11.

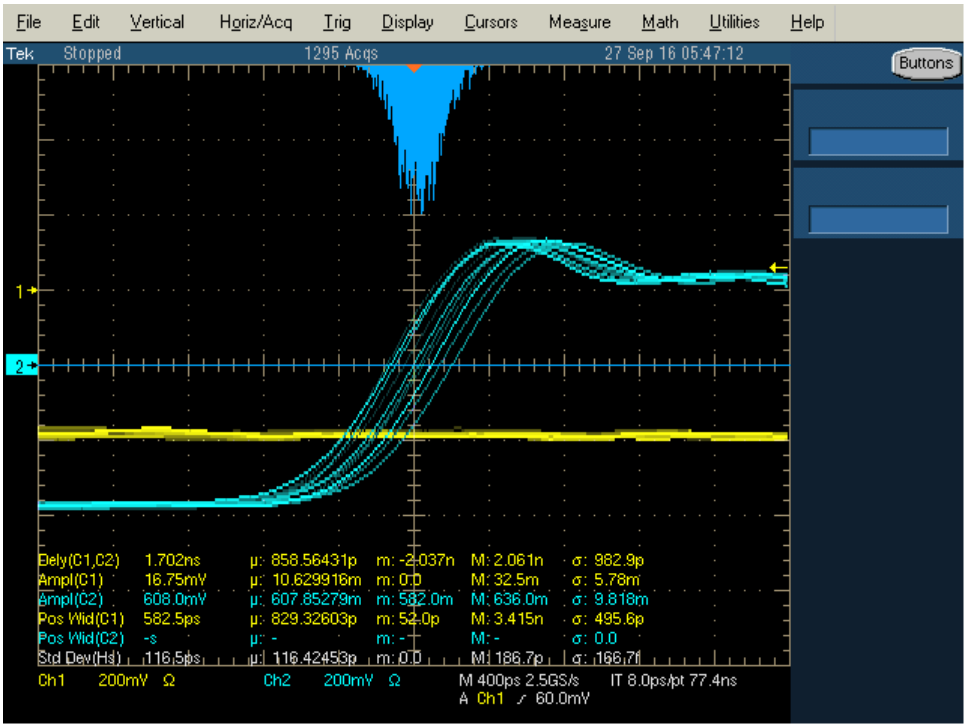

Figure 8 Jitter of clock delivered to Dragon in an outer ring backplane with respect to clock delivered to Dragon at central backplane, 116ps rms are measured.

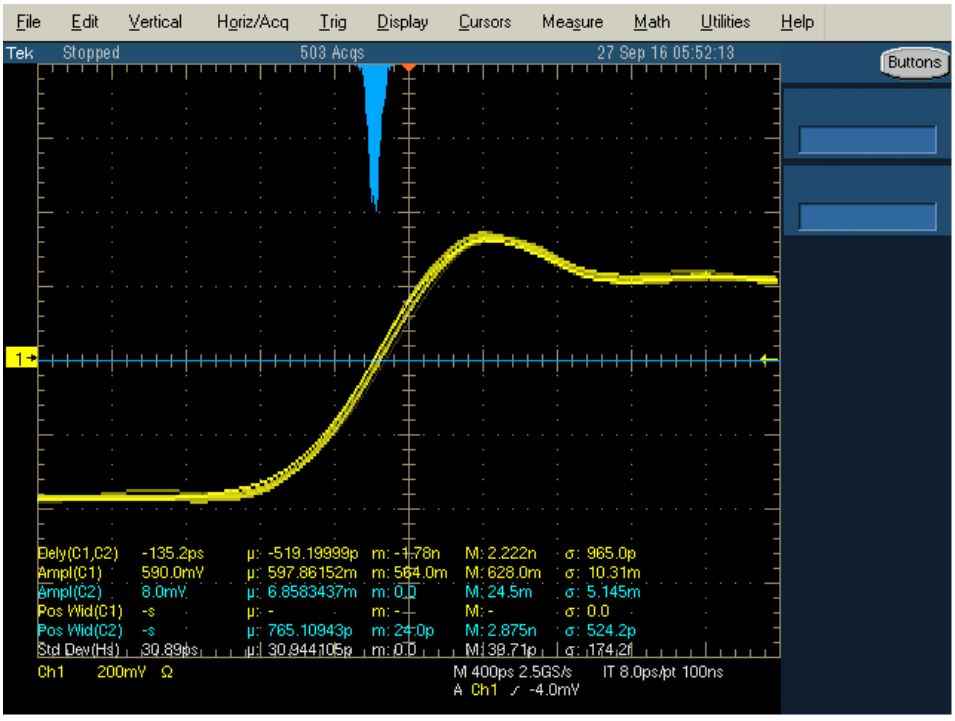

Figure 9 Cycle cycle jitter of clock delivered to Dragon at central backplane

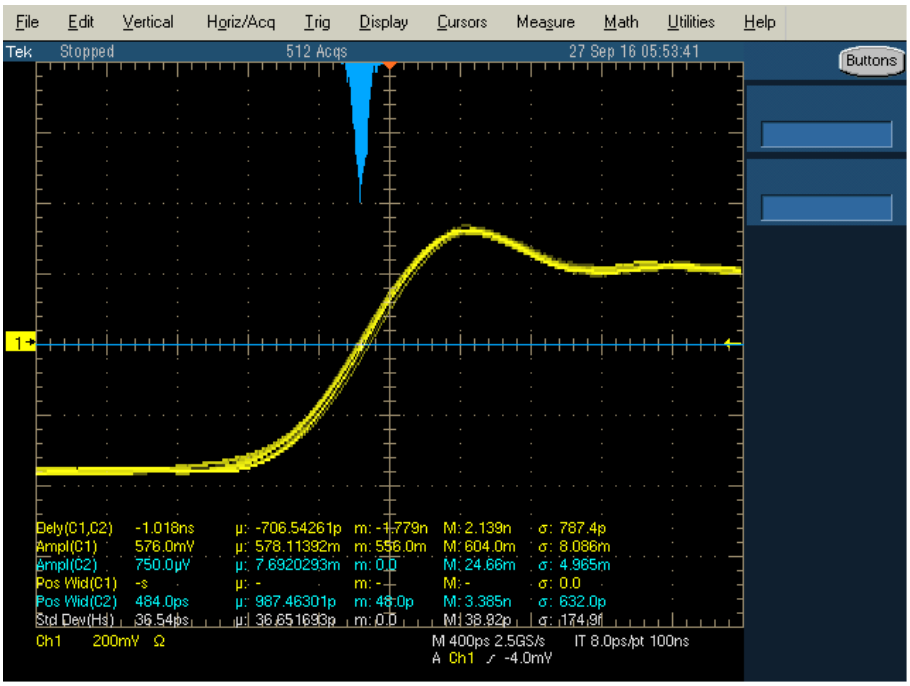

Figure 10 Cycle to cycle jitter of clock delivered to Dragon at one outer ring backplane

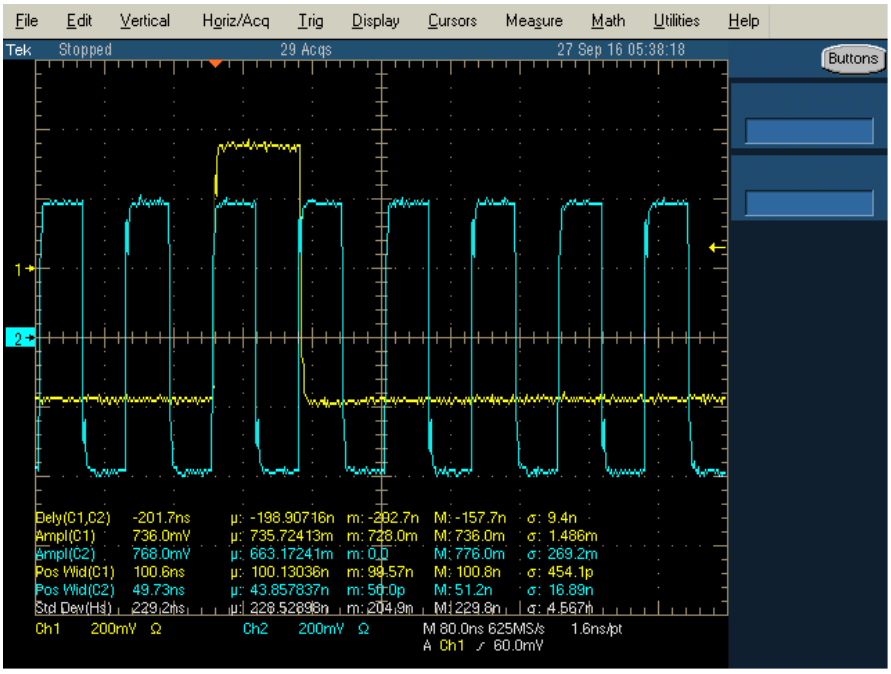

Figure 11 Clock and PPS delivered to Dragon by one backplane

3.4. L0 distribution test

L0 distribution test consisted in the characterization of L0 fanout circuit in backplane both in terms of delay and amplitude. Table 5 shows the propagation delay of all L0 replicas in three different backplanes. Table 6 shows the amplitude of different L0 replicas in one backplane. Table 7 shows time width of different replicas in the same backplane. An example of pulses observed with the scope is shown in Fig. 12.

IP	Delay Local (ns)	Delay N0 (ns)	Delay N2 (ns)	Delay N3 (ns)	Delay N4 (ns)	Delay N5 (ns)
75	**1,82**	**2,56**	**2,61**	**2,55**	**2,53**	**2,53**
144	**1,81**	**2,57**	**2,58**	**2,57**	**2,55**	**2,55**
30	**1,84**	**2,59**	**2,60**	**2,57**	**2,57**	**2,57**

Table 5 L0 fanout delays

Input Amplitude	Output Amplitude Local	Output Amplitude N0	Output Amplitude N2	Output Amplitude N3	Output Amplitude N4	Output Amplitude N5
354mV	**328mV**	**315mV**	**318mV**	**320mV**	**319mV**	**320mV**

Table 6 L0 fanout amplitudes

Input width	Output width Local	Output width N0	Output width N2	Output width N3	Output width N4	Output width N5
2,96ns	**3,24ns**	**3,16ns**	**3,13ns**	**3,09ns**	**3,11ns**	**3,09ns**

Table 7 L0 fanout time widths

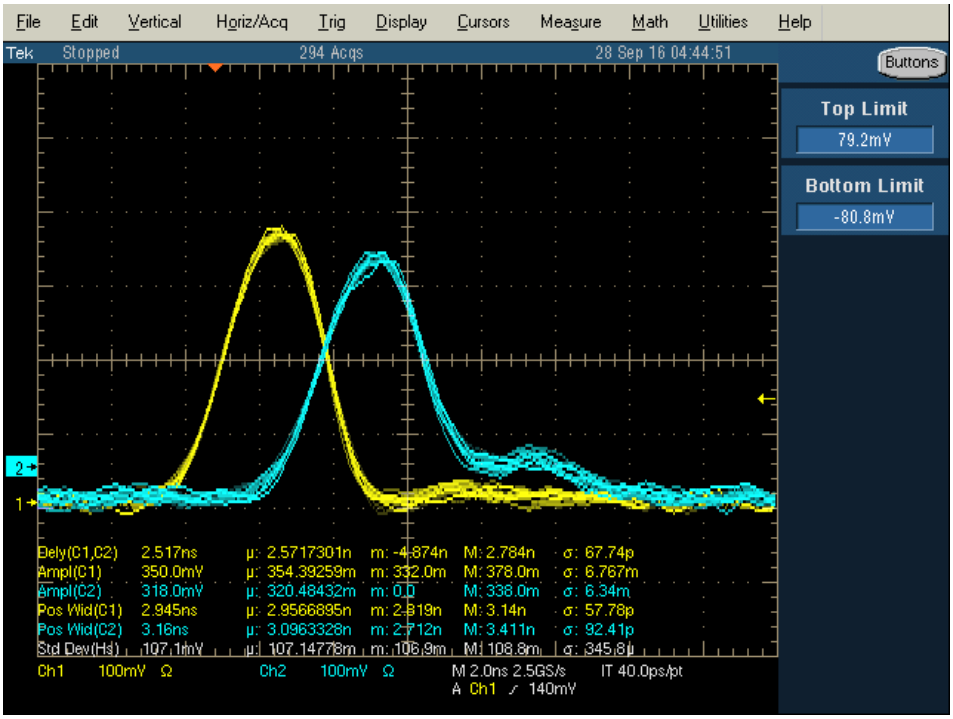

Figure 12 Channel 1 (yellow): L0 input to L0 fanout circuit at backplane. Channel 2 (blue): L0 fanout output corresponding to neighbor 3.

3.5. Busy logic test

Busy logic was tested with the scope just checking that every time a Camera Trigger is delivered to backplanes a Camera Busy is received at TIB, either real TIB or TIB fake board (Fig. 13). In addition, there are busy rate counter at backplanes that were crosschecked with trigger rate counters, being correlated most of the time. In some runs, and after a stable running period, a burst of busy pulses are detected without the corresponding camera trigger (Fig. 14), This effect is not understood and should be further studied.

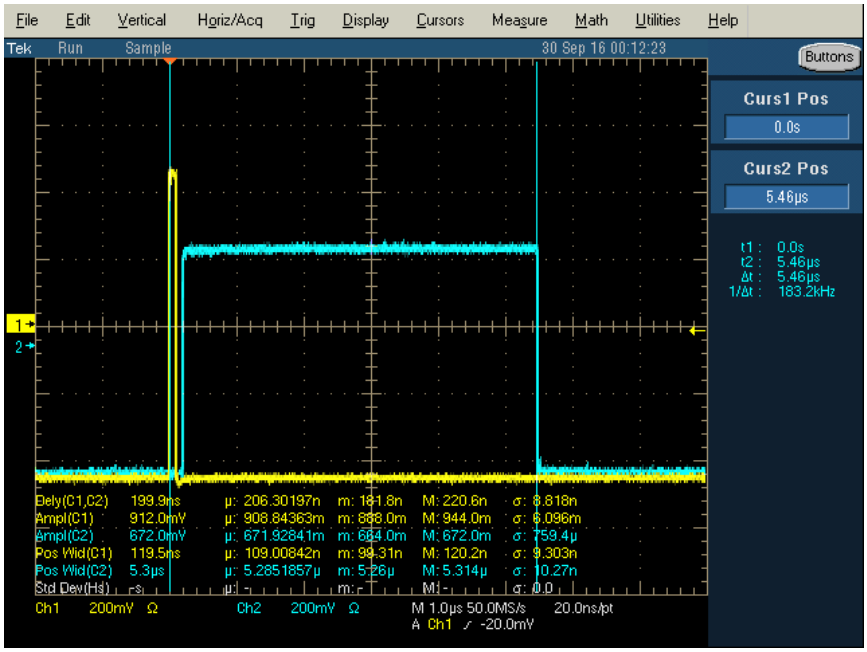

Figure 13 Channel 1 (yellow): Camera Trigger. Channel 2 (blue): Busy. Busy pulse after corresponding Camera Trigger. Both signals picked up at TIB level.

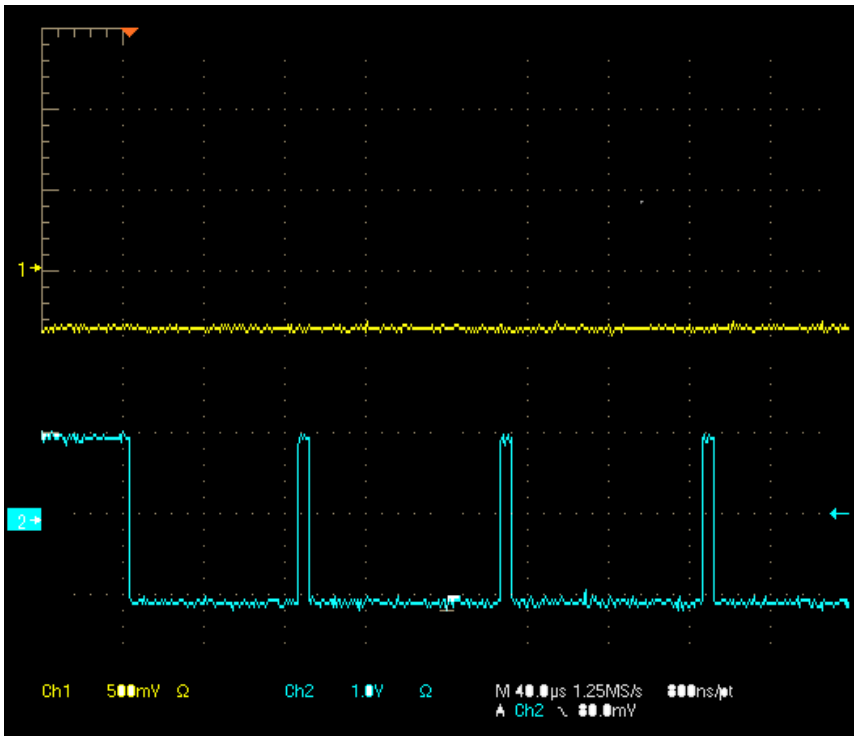

Figure 14 Channel 1 (yellow): Camera Trigger. Channel 2 (blue): Busy. Burst of Busy pulses without any Camera trigger.

When running with real TIB, a delay is set in order to have latency needed for stereo trigger operation. In such a case dead time goes up to 9,4 us from L1 received at TIB to Camera Busy falling edge (see Figure 15).

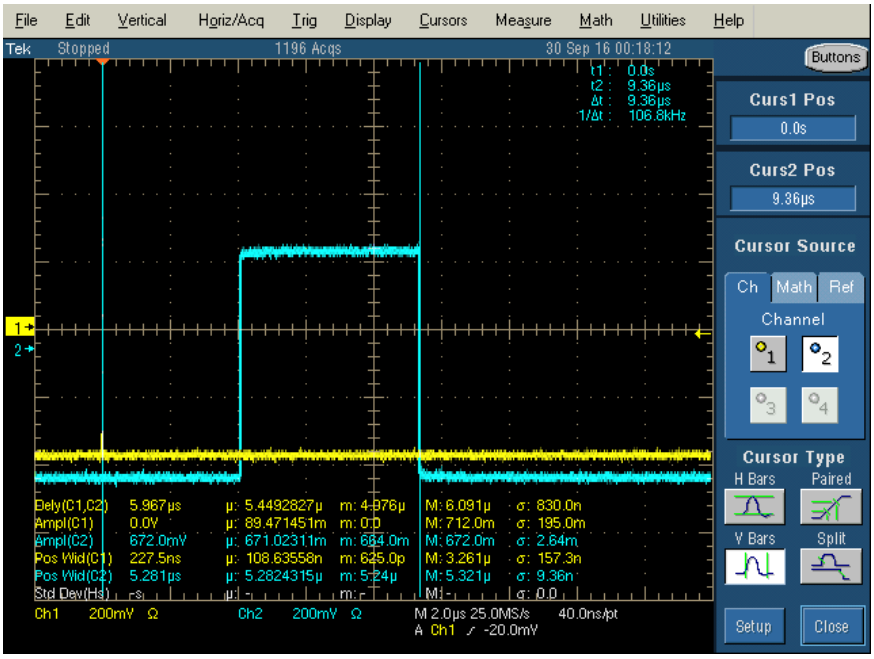

Figure 15 Channel 1 (yellow), Camera Trigger at TIB level.
Channel 2 (blue) Camera Busy at TIB level.

3.6. Time calibration test

Time calibration exercises where done in order to implement procedures without the need of flat fielding light, just using test pulse in Dragon board for L1 generation. Procedures where defined and tested both for Trigger distribution delay equalization and distributed Clock phase equalization. These procedures use TDCs at backplane FPGA to measure propagation delays along the backplane network. A pair of modules was successfully calibrated by using these procedures.

When extending the procedure to all the modules, an unexpected feature was observed in Dragon board. The propagation delay of L1 trigger pulse from L1 ASIC to Backplane FPGA through Dragon FPGA has a different value depending on the Dragon module itself with dispersion up to 1ns. This was confirmed by measuring L1 propagation in Dragon FPGA in several modules, using same L0+L1 mezzanine and backplane in the measurement. This feature can have an impact in the performance of the time calibration of backplane network.

3.7. Temperature test

Temperature test consisted in the measurement of Trigger distribution delay dependence with temperature. In order to do that, some temperature cycling was done by switching on and off the fan used to cool down backplanes operating at room temperature. L1 trigger is generated sequentially in every module by using the test pulse in Dragon. Propagation delays are measured with backplanes TDCs.

Figure 16 shows the linear fit of the propagation delays obtained for one module during the test. It can be observed that a drift of 222ps per degree is obtained for a latency of about 304ns, that is, 0,73% per degree. Figure 17 shows the gradient for all the modules in the set-up that have been obtained with the same linear fit of Figure 16. All gradients are compatible although there is some dispersion from backplane to backplane. These results are also compatible with the ones obtained in a dedicated backplane temperature characterization performed at Ciemat in a climate chamber. These results were presented in LST meeting in La Palma on July, 2016 [1].

Figures 18 and 19 show average latency and temperature measured along the test, a clear correlation is observed.

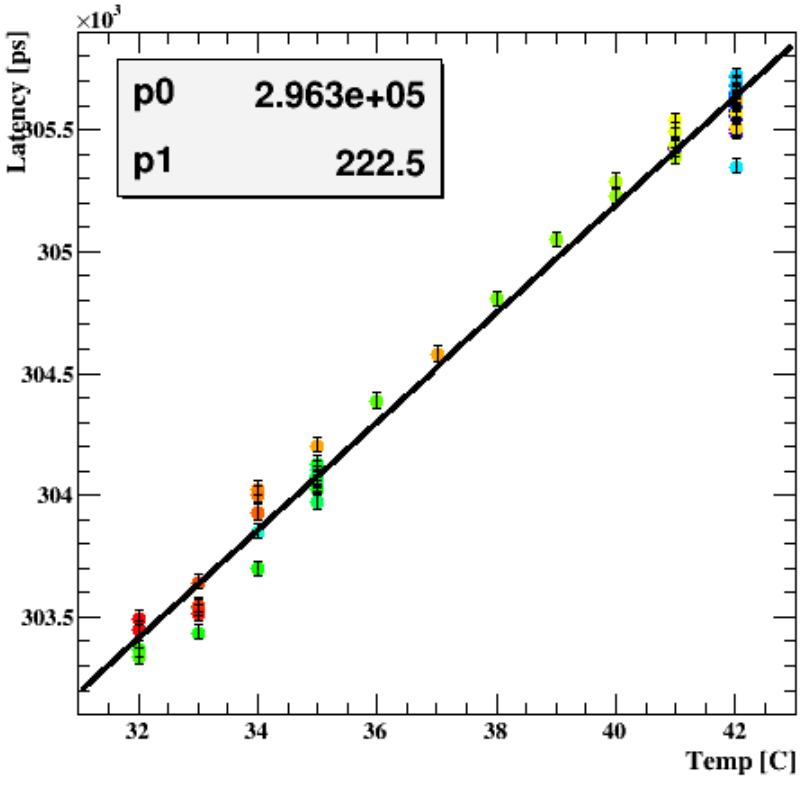

Figure 16 Trigger latency vs Temperature

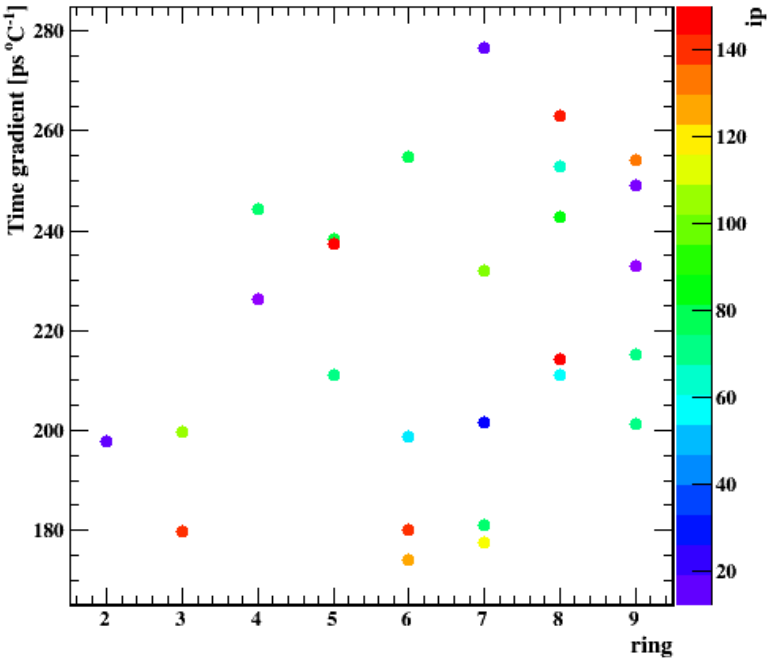

Figure 17 Time gradients per degree for all modules in the set-up

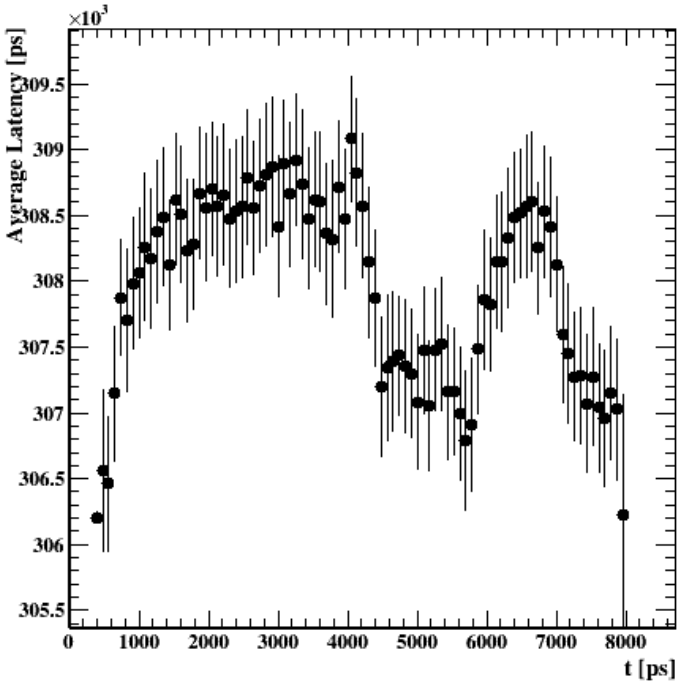

Figure 18 Average of measured latency vs time

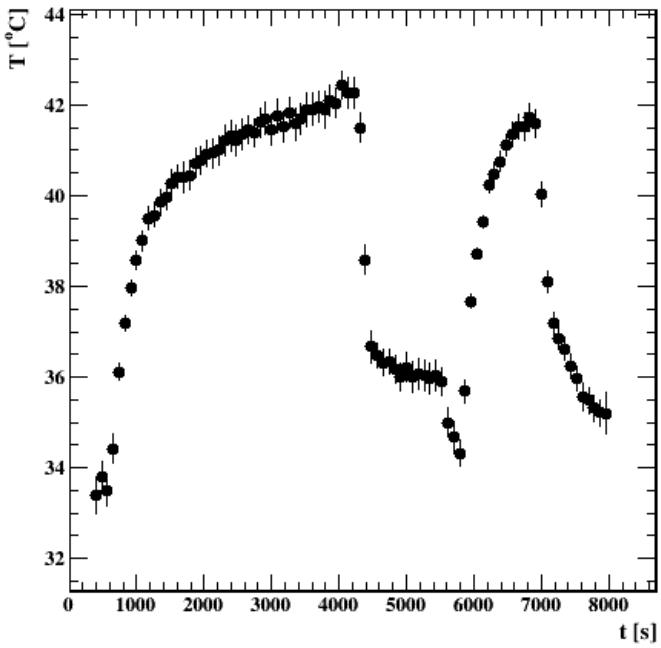

Figure 19 Average of measured temperature vs. time

4. Conclusions

Backplanes functionality and performance have been tested and measured in the C35 test set-up. The most of items where confirmed to be OK, although some of them need further study and firmware development. As conclusion a summary of items is shown below:

- Backplane general functionality: all functionalities where confirmed again (L0 trigger distribution, L1 and Camera Trigger distribution, Clock and PPS distribution, delay lines, TDCs, temperature sensor and slow control).
- Noise in power rails: it is compatible with the noise measured in the laboratory
- Trigger distribution latency: latency can be equalized in the entire camera with current delay lines. Some more delay maybe needed in order to have more backplane failure contingency. This can be achieved with a firmware change.
- Trigger distribution jitter: very good, measurement results are even better than expected.

- Trigger counting: no spurious trigger generation neither trigger loosing except for one L1 trigger lost from time to time when the enabled test pulse is changed from one Dragon board to other. Need to be understood although it is not critical.
- Clock distribution phase equalization: phase correction range it is not enough for equalization in the entire camera. Firmware change is required.
- Clock distribution jitter: clock jitter between some backplanes is higher than expected and there is a correlation with the position of the backplane in the camera. Some firmware development needed to correct this.
- L0 fanout: delay equalization in backplane tracks is OK for neighbor L0 replicas. L0 outputs time width as expected. Fanout outputs amplitude lower than expected. Maybe due to full load of six Dragon boards. To be studied in the laboratory. Amplitude uniformity among outputs is ok.
- Busy test: busy distribution logic is confirmed. An unexpected effect observed, busy pulses generated by at least one Dragon without the corresponding Camera Trigger before. To be understood. When real TIB board is in place, and full delay for stereo trigger operation is programmed, a dead time of 9,4us is measured.
- Time calibration of backplanes: and exercise of calibration both for Trigger delay and Clock phase by using Dragon board test pulse was done in a pair of modules. The procedure was not extended to the full set-up. More development needed. An unexpected feature about L1 propagation time in Dragon FPGA was observed. The impact of this feature in backplane time calibration should be studied in detail.
- Temperature test: some temperature cycling at room temperature was done in order to measure dependence between Trigger latency and temperature. The results are compatible with previous backplane temperature characterization performed at Ciemat in a climate chamber.

5. References

[1] https://www.cta-observatory.org/indico/getFile.py/access?contribId=39&sessionId=12&resId=0&materialId=slides&confId=1079