



A. The L1 Trigger System of the LST

A.1 Introduction

Imaging Atmospheric Cherenkov Telescopes (IACTs) work detecting the Cherenkov light produced by the interaction of γ -rays and other particles in the atmosphere. This Cherenkov photons must be distinguished from those of the Night Sky Background (NSB) that fill the atmosphere, and constantly reach the telescopes. An efficient trigger system is necessary to decide whether the light reaching the camera must be stored as a Cherenkov event, or discarded as background.

Typically this task is accomplished by recognizing a concentration of signal from several pixels both in space and time, because showers are produced in a time window of a few nanoseconds, reaching a group of near pixels, while NSB light is randomly distributed over the entire camera.

Two possible approaches for the detection of coincident light are used in IACTs, known as *majority trigger* or *sum trigger*. In majority trigger the light of each pixel is compared to a certain threshold. If the signal of several (the majority of) pixels in a certain region exceeds the threshold in a short time, the trigger is fired. This approach presents a disadvantage when detecting low energy photon showers, as happens in Large Size Telescope (LST). The problem is that as the pixels must overcome the threshold individually, if the signal is too low, it is possible that some of them do not exceed the threshold and therefore the event would be mislead as NSB.

On the other hand, the sum trigger approach takes into account the total signal coming to a group of several pixels. The light arriving to each pixel of the group is added and this sum is compared to a threshold to fire the trigger. If several close groups of pixels surpass the threshold at a given time window, then the event is recorded as a shower event.

In the LST, a multilevel trigger system is implemented, that guarantees the rejection

of the majority of the NSB.

The pixels in the LST camera are distributed in 265 hexagonal modules of 7 pixels, that are connected to each of its 6 neighbours. The first trigger level (L0) sums the signal of the pixels in each module, and if it is higher than the configured threshold, it sends the L0 signal to the neighbouring modules. In the second trigger level (L1), each module takes the trigger signal coming from its neighbours and compares it to another threshold to decide if the camera trigger is fired. Finally, the third level compares the camera trigger of several telescopes and if two or more telescopes have triggered in a certain time window, the event is recorded. A scheme of the trigger system of LST is shown in picture A.1. In the next sections, a detailed description of the three trigger levels is given.

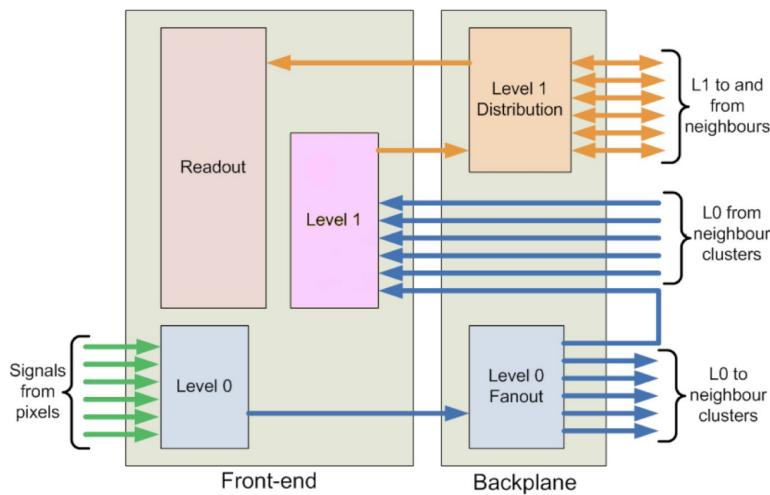


Figure A.1: Architecture of the analog trigger system of the LST.

A.2 Pixel Level: L0 trigger decision

The pixel level trigger, known as L0, takes into account the signals from the pixels in one module or cluster. If the trigger is fired, the signal is replicated and distributed by the L0 fan out to the local L1 and to the neighbouring modules. Both, the majority and sum trigger approaches have been implemented in LST.

A.2.1 Majority trigger

The majority approach counts the number of pixels in a module that have a signal over a certain threshold voltage, generating a digital signal. The signal from all the pixels is added, with a resulting amplitude proportional to the number of activated pixels, that goes to the local L1 trigger system, and to the neighbouring modules. This approach do not account for the number of photoelectrons that activated each

pixel, only for the number of pixels that have surpassed the threshold. This means that even if a large number of pixels in a region receive a flash of light, if in each pixel the amount of photoelectrons is not over the threshold, the event will not be recorded, possibly losing very low energy events.

A.2.2 Sum trigger

The sum trigger adds the signal received in each pixel of the module and the resulting signal is compared with a threshold voltage. If the threshold is surpassed, the signal is sent to local L1 and neighbouring modules. This way makes it possible to take into account the photoelectron contribution of all pixels of the module, raising the sensitivity to low energy events while still rejecting NSB events. After adding the signals of all pixels, a clipping is applied to overcome afterpulse effects in the photomultipliers. Afterpulses are sometimes produced after a real pulse in the photosensors, due to the ionization of residual gases, and can contribute with a very high amplitude to the sum.

A.2.3 Camera Level: L1 trigger decision

Camera level trigger decision system, known as L1, analogically adds the resulting signals of L0 trigger from neighbouring modules and compares the result with a threshold voltage. If the analog sum is over the configured threshold, a signal is sent to through the L1 distribution system to trigger the whole camera. Each module can combine the L0 fan-out signals from six neighbours, plus the local L1. To ensure that all modules are participating in the trigger and addings are made in an efficient way, it is possible to configure by slow control different modes where smart configurations of neighbouring signals are added. In figure A.2 the three possible modes are shown. These configurations make it possible, through combinations of two, three or four modules, to evaluate any trigger region.

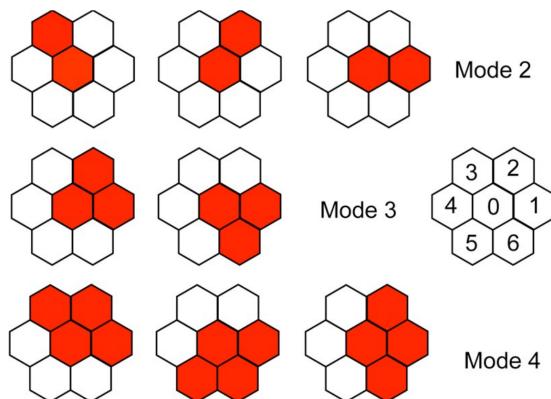


Figure A.2: Illustration of the three possible modes for adding signals of neighbouring modules. Each hexagon represents a group of seven photomultipliers.

The threshold voltages for each module should be calibrated, in order to find the threshold level which produce a trigger signal in a rate of the 50%. The calibration algorithm developed for LST camera, is described in appendix C.

L1 Trigger Distribution

The L1 trigger distribution system allows the L1 signal to reach the data adquisition systems of all the modules and start the digitalizing process. Every module can propagate the L1 signal to each of its six neighbours, being aware of its position in the camera. This way, when a module receives a L1 signal, it can be delayed depending on the position in the camera, and be sent to the appropriate neighbours following the preconfigured paths (See figure A.3). The distribution paths are firmware configurable and they can automatically be reconfigured to go through the full camera, even if one module is malfunctioning or deactivated. The algorithm developed for the time delay calibration of the L1 signal, depending on the camera position of the modules, is described in appendix D.

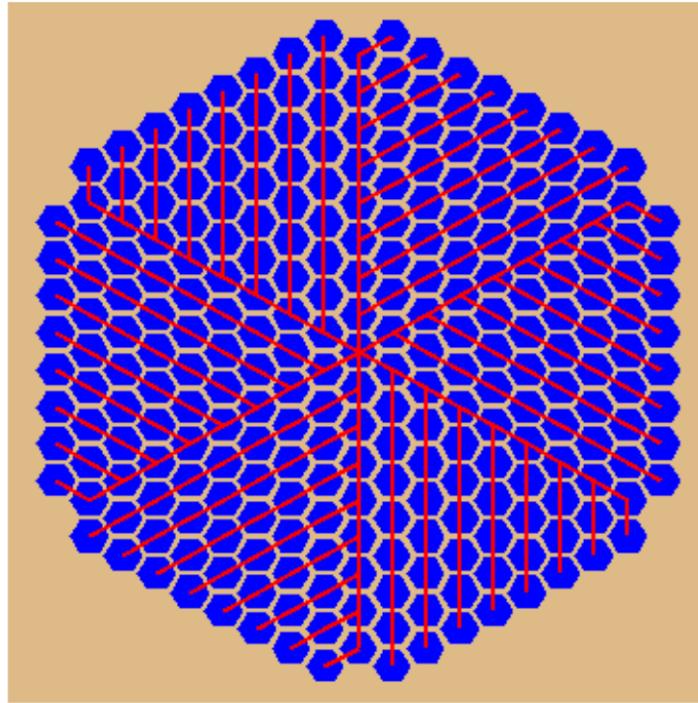
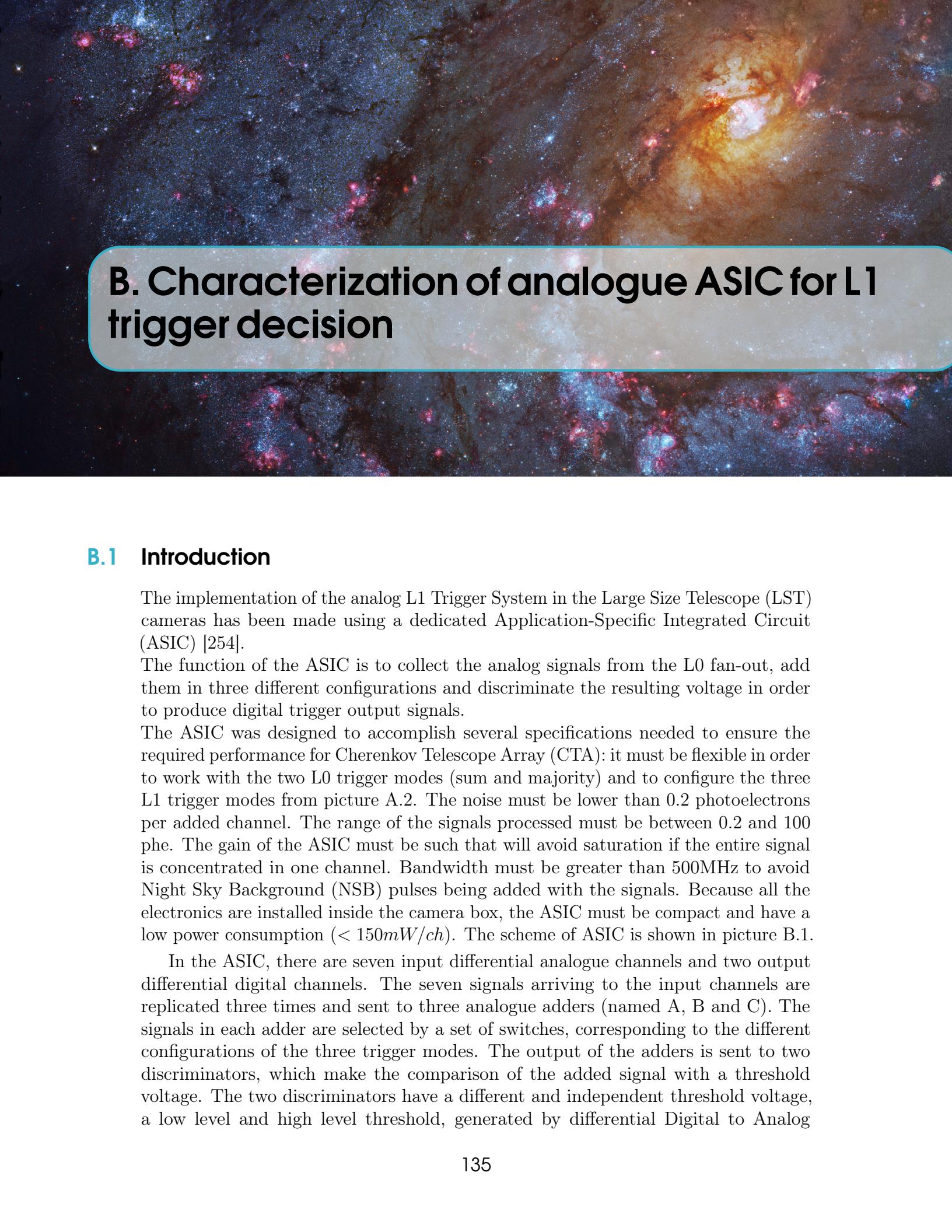


Figure A.3: Paths for trigger distribution over the entire camera.

A.2.4 Array Level trigger decision

Array level trigger looks for coincidences in events recorded by several telescopes. If more than one telescope produces a camera trigger in a certain time window, it is likely that the light is produced by a Cherenkov shower, so the event will be stored.

This level allows to reject the majority of NSB events that have overcomed the lower level triggers.



B. Characterization of analogue ASIC for L1 trigger decision

B.1 Introduction

The implementation of the analog L1 Trigger System in the Large Size Telescope (LST) cameras has been made using a dedicated Application-Specific Integrated Circuit (ASIC) [254].

The function of the ASIC is to collect the analog signals from the L0 fan-out, add them in three different configurations and discriminate the resulting voltage in order to produce digital trigger output signals.

The ASIC was designed to accomplish several specifications needed to ensure the required performance for Cherenkov Telescope Array (CTA): it must be flexible in order to work with the two L0 trigger modes (sum and majority) and to configure the three L1 trigger modes from picture A.2. The noise must be lower than 0.2 photoelectrons per added channel. The range of the signals processed must be between 0.2 and 100 phe. The gain of the ASIC must be such that will avoid saturation if the entire signal is concentrated in one channel. Bandwidth must be greater than 500MHz to avoid Night Sky Background (NSB) pulses being added with the signals. Because all the electronics are installed inside the camera box, the ASIC must be compact and have a low power consumption ($< 150\text{mW}/\text{ch}$). The scheme of ASIC is shown in picture B.1.

In the ASIC, there are seven input differential analogue channels and two output differential digital channels. The seven signals arriving to the input channels are replicated three times and sent to three analogue adders (named A, B and C). The signals in each adder are selected by a set of switches, corresponding to the different configurations of the three trigger modes. The output of the adders is sent to two discriminators, which make the comparison of the added signal with a threshold voltage. The two discriminators have a different and independent threshold voltage, a low level and high level threshold, generated by differential Digital to Analog

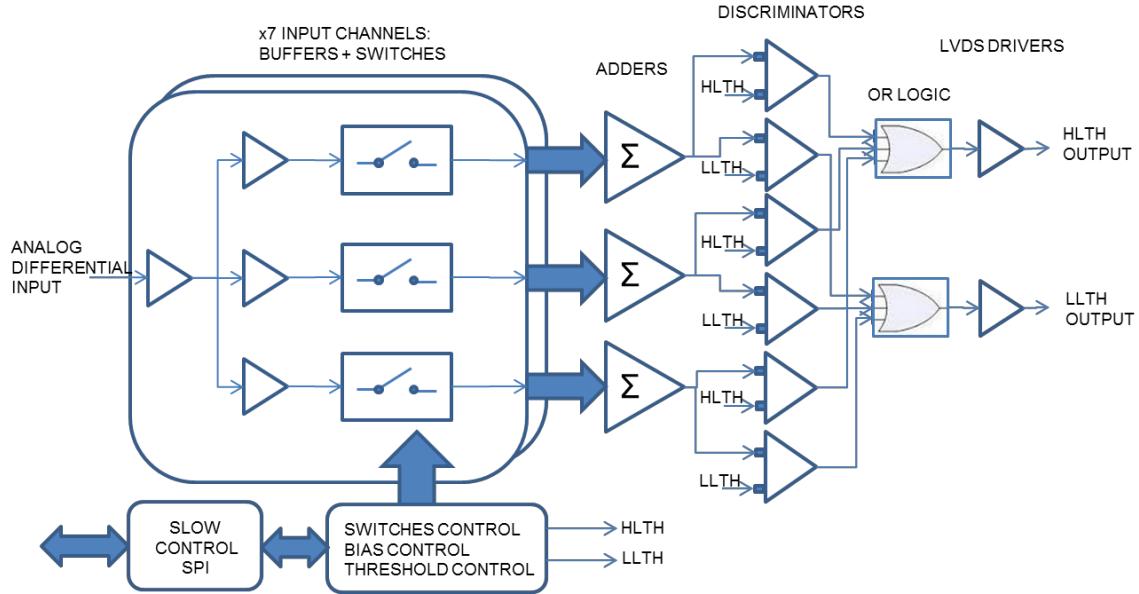


Figure B.1: L1 ASIC Block diagram

Converters (DACs). The discriminator outputs are connected to two OR gates which are in turn connected to Low-Voltage Differential Signalling (LVDS) transmitters that provide the trigger signal.

About 400 asics were produced at CIEMAT, passing a quality control to validate their performance. The quality control tests probed several characteristics of the ASICs, such as gain, noise and offset, for all the channels, adders and discriminators. From all the ASICs tested, 389 surpassed the quality control test and the results were analyzed to characterize the general behaviour of the ASIC. Averaging to all the ASIC analyzed, the result is an overall view of the features that a default ASIC would have, shown in table B.2. In this appendix, the results of the characterization of the L1 ASICs produced at CIEMAT are summarized, using the data from the quality control tests.

B.2 Quality control test

The quality control test consisted of several steps to qualify the behaviour of the ASIC in its different parts (seven input channels, three adders and two LVDS outputs).

The quality control provided a datasheet for each individual ASIC with the results of the tests which were analyzed to characterize the manufactured ASICs. Each combination of channel (7), adder (3) and discriminator(2) is accounted separately, having a proper gain, offset and noise. This procedure allows the detection of outliers that could imply the existence of a defect in a part of the ASIC. The quality control tests provided direct measures of offset and noise, but gain must be calculated from the rate scan results in the test voltage. This procedure also offers other way of

measuring the offset. The computation of gain and offset from the rate scan, described in section B.2.2, was performed considering a linear behaviour of the input voltage vs. threshold voltage for the 50% trigger rate. From a linear fit, the gain and offset are obtained. In the next sections, the different steps of the quality control test are described.

B.2.1 Test DAC

Measurement of the maximum and minimum voltage of the DAC was taken directly from the output pin of the ASIC by a multimeter. Each DAC set is composed by 2 DACs of 9 bits to get a final resolution of 10 bits (positive and negative parts). The measurement is made setting the code in the register with the maximum and minimum values for both positive and negative parts.

B.2.2 Voltage Test: Rate scan

The Voltage test measured the gain of all seven input single channels and the two outputs for 10 different voltages (from 100mV to 1000mV) using a rate scan methodology, consisting on the comparison of the input trigger rate from a generator on the evaluation setup and the ASIC trigger output rate. This computation is performed with scalers implemented in the FPGA board.

B.2.3 Test Adder Channels

The gain of different sum combinations was obtained by the same rate scan methodology. There are 3 different methods combining different channels of different adders.

B.2.4 Analog Offset test

The Analog offset test consisted in the measurement of the offset in the Analog Adder Output test, which is the output of a multiplexor that selects among the available analog output adder, plus a buffer for the output pins. The measurement is made directly from the differential output pin of the ASIC by a Multimeter.

B.2.5 Digital Offset test

The Digital offset test procedure measures the offset in the LVDS digital outputs, by the evaluation of the output status as a function of the threshold. The methodology consists in increasing the threshold from 0 Volts using the DAC values until finding the minimum value where the output goes from 1 to 0, and the maximum for which it goes from 0 to 1. The voltage difference between these two points is the noise of the digital output, and the mean point is the offset. Setting the Threshold to 0, three possible behaviours are observed:

- If the status of the digital output is a logic '1' (tagged as type 'Pos') it is possible to measure the minimum and the maximum points and therefore it is possible to calculate the offset and the noise.

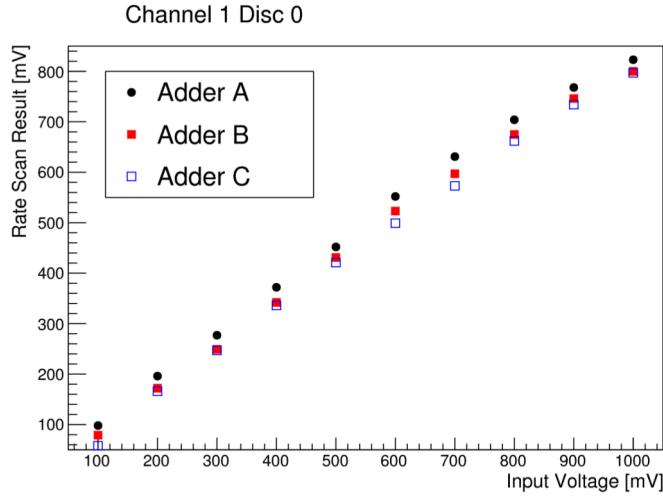


Figure B.2: Rate scan result from one of the voltage tests for ASIC #61. It can be observed a linear tendency which deteriorates at high voltages. Similar plots where obtained from the rest of channel-adder-discriminator combinations.

- If the status of the digital output is a logic '0' (tagged as type 'Neg'), it is not possible to measure neither the minimum nor the maximum point, and then a value of zero is assigned by the program both to the noise and the offset.
- If the status of the digital output is switching (tagged as type 'Com'), it is only possible to measure the maximum value, and the other is assigned to 0. In this case the noise is underestimated and the threshold is overestimated.

B.3 Characterization of the ASIC

In this section, the results from the quality control tests for all ASICs are analyzed and discussed.

B.3.1 Rate Scan Fit

For the calculation of the gain, the output of the Voltage test is used to perform a linear fit. If we assume a linear model, the relation between the input voltage and the rate scan result should be:

$$V_{rs} = Gain * V_{input} + Offset \quad (B.1)$$

In figure B.2 the rate scan result versus ten input voltages for a certain path (channel, adder, discriminator) of one ASIC is shown. The linearity can be easily appreciated, specially for low input voltages (under 500 mV).

Where V_{rs} represents the threshold voltage that gives a rate of 50% trigger, and V_{input} is the input voltage. The use of this method has the advantage of obtaining

Channel	Mean Gain	RMS
1	0.871	0.035
2	0.839	0.036
3	0.880	0.036
4	0.873	0.036
5	0.876	0.036
6	0.873	0.036
7	0.878	0.036

Table B.1: Mean gains for the seven channels, averaged to the sample of all asics, without the outliers.

not only the gain but also the offset of the ASIC without having to measure it with a multimeter. Since linearity seems to depend on the input voltage, it is necessary to consider a range for the fitting where the linearity is better. To do so, several ranges were fitted and the offset obtained was compared to the offset measured with the multimeter in the analog offset test. The range where the difference between the two offsets was lower was selected as the best range to fit the linear model. The resulting range was from 0 V to 300 V and so this range was used to calculate the gain and offset for every path of each ASIC.

B.3.2 Gain

The gain was calculated with the model fitting described in the previous section. Figure B.3 shows the distribution of gain values over the paths of the 389 asics. A clear gaussian profile is observed, centered in the characteristic gain of 0.87, the expected result according to the design specifications. Some outliers were identified having gain values that are too low for the requisites of the ASIC, which could mean a malfunctioning in the ASIC. Fitting the distribution to a gaussian, it is possible to see that the probability of an ASIC to have a gain lower than 0.7 in any of its paths is lower than 0.025%. There are some outliers with higher gain values, but the probability of any entry to have a gain over 1.05 is lower than 0.007%. The outliers are identified in image B.3 by their ASIC number.

Cleaning the outliers from the sample, the characteristic gain is 0.87 ± 0.038 , obtained from the gaussian fit. This is an average to all the possible paths of channel, adder and discriminator in the ASICs analyzed. A single path characterization is given in table B.2, each entry averaged to all ASICs. When observing the average gain for each channel separately in table B.1, and in image B.4 it can be observed that the second channel has a slightly lower gain than the others, and the third one a slightly higher gain. This effect comes out from the configuration used during the quality control tests. The third channel was connected directly to the pulse generator, while the second channel had to be fed with a cable of different length than the others.

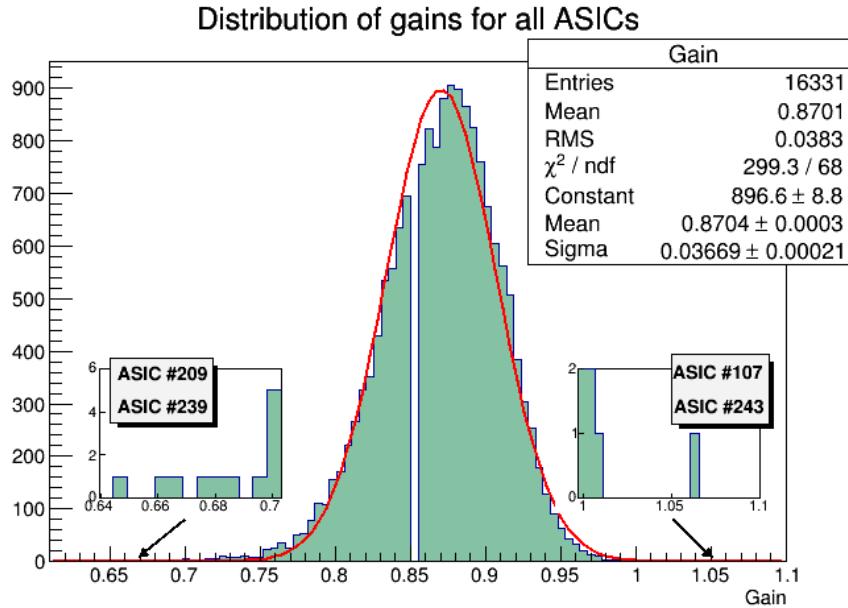


Figure B.3: Distribution of gains for all ASICs. Each entry represents the gain of one possible path (combination of channel-adder-discriminator). The red line represents a gaussian fit with mean 0,8704 and sigma 0,3669. The zoom-ins show several outliers with gains very deviated from the average.

To find if any part of the ASIC is dominating the fluctuations of the gain, correlation plots between channels, adders and discriminators were studied. A remarkable correlation is not observed in any of the elements of the ASIC, so we can conclude that all parts contribute to the final value of the gain in a similar way.

B.3.3 Offset

The offset has been measured in three different ways. In the tests, the analog offset was directly measured with a multimeter, the digital offset was measured using the procedure described in section B.2.5, and finally, from equation B.1 an offset value that will be called fit offset was calculated.

In figure B.5 the distribution of the analog and digital offsets are shown. It must be noted that it was not possible to measure the digital offset for all the configurations, only the ones with an output status tagged as “Pos”, so it’s not possible to measure negative values of digital offset. Some outliers were detected, with digital offset values very deviated from the mean, which has been removed from the sample at the final characterizaton. Those outiers correspond to ASICs 110, 209,248 and 437.

The averaged value of the analog offset is -6.138 mV with RMS of 13.01 mV while for the digital offset the mean is 8.41 mV with RMS of 6.17 mV. Plotting the correlation between the two measured offsets(B.6 it can be seen that there is a correlation between the two ways of measuring the offset. Regarding the fit offset, the

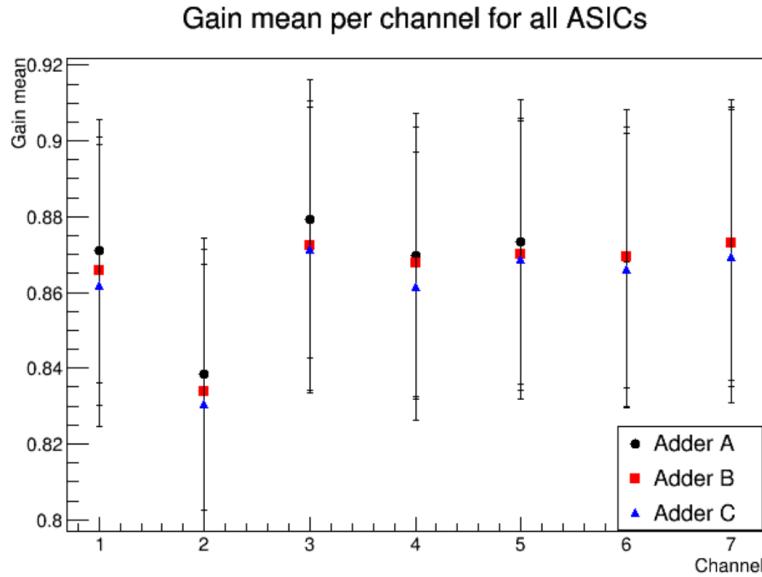


Figure B.4: Distribution of gains for all ASICs. Each entry represents the gain of one possible path (combination of channel-adder-discriminator). The red line represents a gaussian fit with mean 0,8704 and sigma 0,3669. The zoom-ins show several outliers with gains very deviated from the average.

distribution of the obtained values is shown in figure B.7. To check the validity of this method of obtaining the offset value, the difference between the fit offset and the analog offset has been studied. The averaged value of the fit offset is 0.1334 mV with RMS 13.75 mV. The mean difference between the analog offset and the fit offset is of 5.55 mV with RMS 8.06 mV. Checking the correlation between the two offset values (fig B.6) it can be observed that even there is a clear correlation between them, the fit offset is underestimating the analog offset measured. In figure B.8 the averaged offsets to all ASICs, separated by channels and adders are plotted. In general the offset takes similar values for all the channels and adders, without any remarkable outlier. In table B.2 the average offsets to all ASICs in every single path are shown.

To find out which part of the ASIC is responsible of the offset, correlation plots between channels, adders and discriminators were studied. Channels and discriminators show a clear correlation between pairs of them, but for adders, a real correlation is not observed. This implies that the offset do not depend on the channels or discriminators, but it is introduced by the adders. This result was expected from the original specifications of the ASIC.

B.3.4 Noise

The noise in the ASIC was measured during the Digital Offset test described in section B.2.5. The noise again can only be measured when the output status is tagged

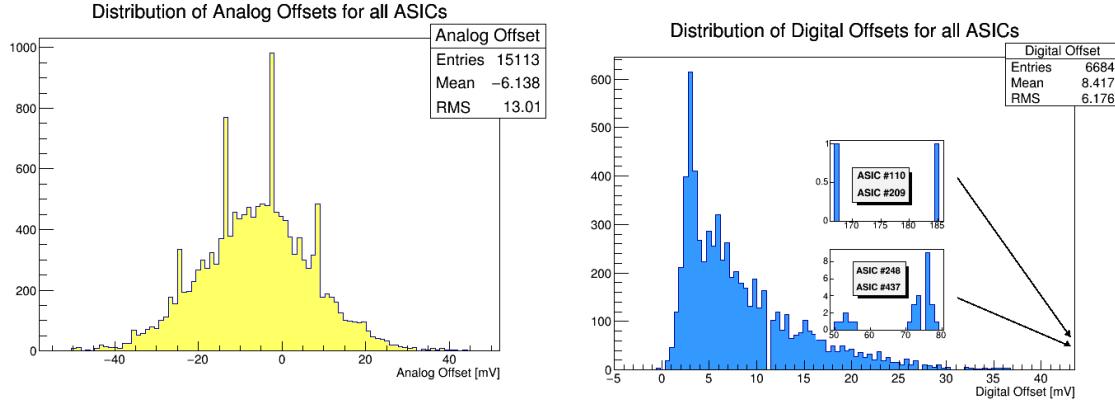


Figure B.5: Distribution of offsets for all ASICs. Each entry represents the offset of one possible path (combination of channel-adder-discriminator). *Top:* Analog offset. *Bottom:* Digital offset. The zoom-ins represent outliers in the digital offset.

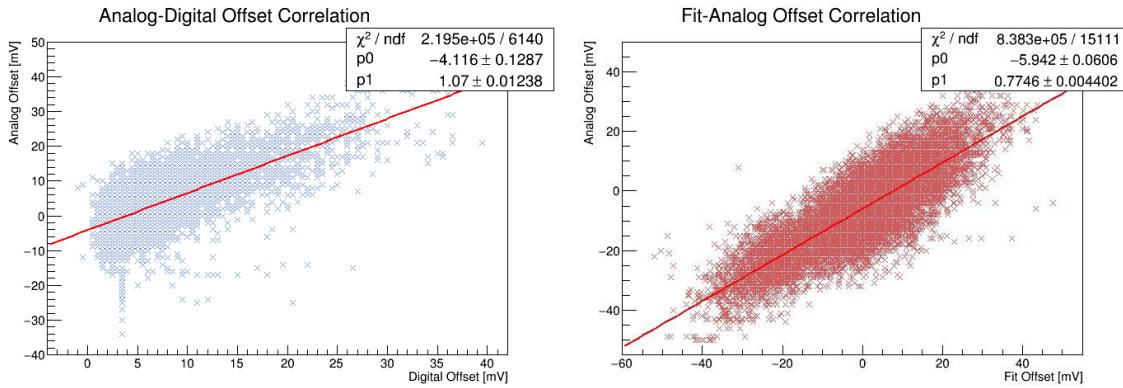


Figure B.6: *Left:* Correlation between analog offset and digital offset. *Right:* Correlation between analog offset and fit offset.

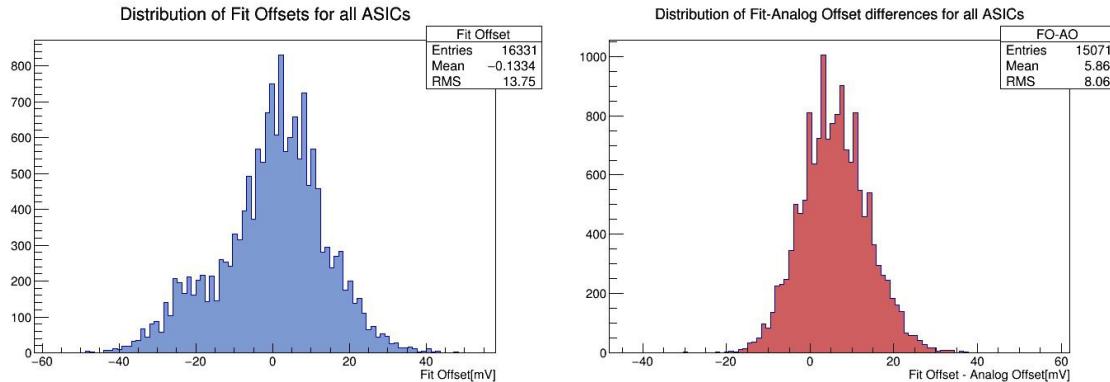


Figure B.7: *Left:* Distribution of offset calculated from the rate scan fitting. *Right:* Distribution of the difference between the analog offset and the fit offset.

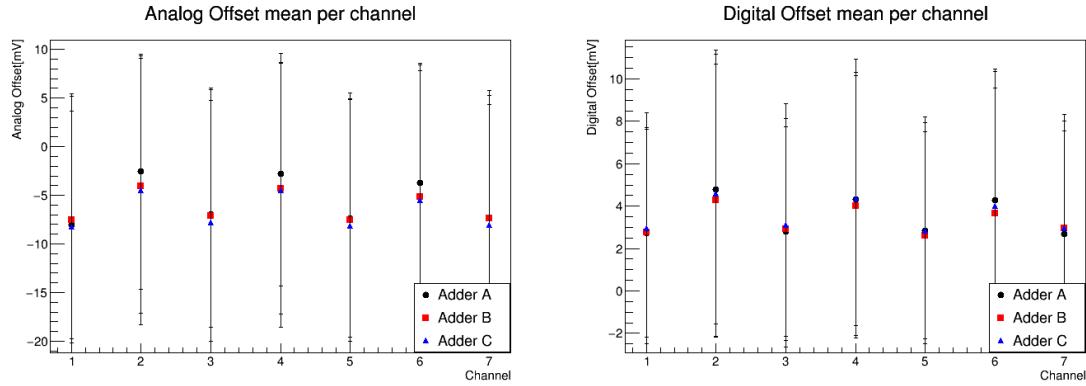


Figure B.8: *Left:* Analog offset averaged to all ASICs separated by channel and adder. *Right:* Digital offset averaged to all ASICs separated by channel and adder.

as “Pos”. In figure B.9 the total distribution of noise values is shown, having an average noise of 5.186 mV with RMS of 2.878 mV. Several outliers were spotted and are marked in the plot, with noises very deviated from the mean. If we fit a gaussian profile to the distribution, the probability of having an outlier with noise over 40 mV is 0% and over 10 mV is less than 1%. These outliers have been excluded from the general characterization.

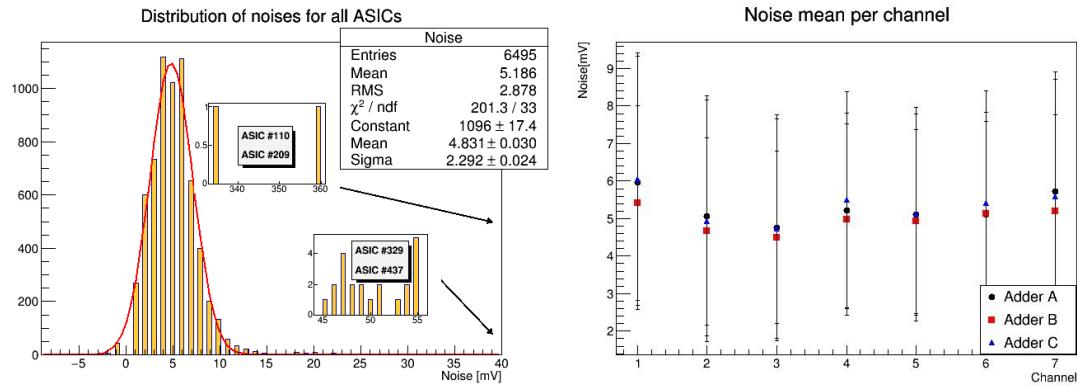


Figure B.9: *Left:* Distribution of noises measured for all ASICs. Each entry represent the noise in a certain path (channel-adder-discriminator combination). The zoom-ins show the outliers. *Right:* Noise averaged to all ASICs separated by channel and adder.

No correlation of the noise between pairs of channels, adders or discriminators have been observed, so the noise is being introduced in each part of the ASIC in a similar way.

In figure B.9 the average noise value separated by channels and adders show that its value is mostly uniform.

B.4 Characterization: Summary and discussion

The gain measured in the ASIC has a typical value of about $0,87 \pm 0,038$, having two channels that slightly differ from the rest. In the case of the channels (2 and 3), that for all ASICs seem to have a deviation from the general mean, this effect is explainable by the setup configuration of the rate scan test. There are two ASICs where gain has a very low value, under 0,7, in several of their channels. Relative to the correlation study, there is not a strong correlation for the gain in any part of the ASICs, having all of them a correlation coefficient below 0,5.

The analog offsets measured in the test have a negative mean value, while the digital offset, as the rate scan only can provide positive offsets, gives a positive mean value. In the correlation plots for the analog offset, it can be observed a positive correlation between channels, with correlation coefficients $\sim 0,8$. For the adders however, no significant correlation is observed, concluding that in the adders, the offset measured is independent from each other, so they are the part of the ASIC where the offset is introduced. In the case of the digital offset, no correlation is observed at all, with coefficients very close to 0. It is needed to take into account that the data of digital offset is biased by the rate scan conditions. From the correlation plot of digital and analog offset, we can say that both offsets have a correspondence and we are measuring the same feature, having a linear correlation with slope ~ 1 . In summary, the offset expected from a typical ASIC would be of -6 ± 13 mV.

A method to calculate the offset of the ASIC in an indirect way was applied assuming a model where the input signal and the rate scan result have a linear relation. The offset calculated by this method have in average, a difference with the analog offset of $5,86 \pm 8$ mV. The correlation between the fit offset and the analog offset showed that they have a linear correlation by a factor of 0,774. The study of the fit offset in the different parts of the ASICs supported the idea that the adders are responsible for introducing the offset in the ASIC.

Finally, in table B.2 are presented the values of gain, offset and noise, averaged to all the ASICs studied. This values represent the typical values that should be expected from a correctly functional ASIC. If deviations from this numbers are observed, it might point to a defect in the ASIC, meaning a bad performance that will not fit the specifications.

Disc.	Ch.	Add.	Gain	RMS	Analog Offset[mV]	RMS[mV]	Digital Offset[mV]	RMS[mV]	Fit Offset[mV]	RMS[mV]	Noise[mV]	RMS[mV]
0	1	0	0.870941	0.0347202	-8.04178	11.7013	7.6831	5.41629	0.237361	12.2547	5.86861	3.00563
0	1	1	0.865733	0.0354431	-2.56825	12.0754	9.26942	6.00255	5.42159	13.151	4.73869	2.65657
0	1	2	0.861889	0.0372319	-6.90529	11.6572	7.38961	5.61574	0.459297	13.2761	4.40559	2.48136
0	2	0	0.838466	0.035875	-2.82682	11.5199	8.88718	5.92886	4.81186	12.0241	5.08421	2.35825
0	2	1	0.833886	0.0374605	-7.35196	12.2333	7.90845	5.88134	0.506872	13.5916	5	2.55973
0	2	2	0.830387	0.0369065	-3.70752	12.1045	8.92932	6.18108	3.99229	12.8837	4.79679	2.44105
0	3	0	0.879369	0.0367518	-7.35933	11.7325	7.87132	5.64872	0.784061	13.1786	5.64662	3.484
0	3	1	0.872314	0.0381587	-7.52089	12.7001	7.58562	5.68263	-0.450728	13.1254	5.22917	2.54056
0	3	2	0.871234	0.0377928	-4.04735	13.1041	9.25946	6.80006	3.55013	14.3746	4.32	2.18838
0	4	0	0.869755	0.0373787	-7.07521	12.9157	8.36331	6.00024	0.205656	13.5603	4.19231	2.25012
0	4	1	0.867655	0.0359559	-4.30168	12.8884	8.9435	6.38963	2.65292	13.278	4.65497	2.18266
0	4	2	0.861649	0.0354134	-7.55153	12.4649	7.70956	5.78174	0.0951152	13.1499	4.81395	2.60223
0	5	0	0.873273	0.0374989	-5.17827	12.9837	8.79697	6.41468	1.78835	13.7437	4.80921	2.19069
0	5	1	0.870116	0.0359688	-7.37604	12.6522	8.36525	5.49044	-0.487576	13.7508	5.05839	2.46957
0	5	2	0.868586	0.0368392	-8.2312	13.7086	8.84926	6.51816	-0.999143	14.8268	5.9771	3.5693
0	6	0	0.86892	0.0393618	-4.48189	13.8268	9.7963	7.14917	3.15424	15.5242	4.8895	3.11456
0	6	1	0.869291	0.0343526	-7.76602	13.8442	8.83929	6.63897	-0.61611	14.7812	4.48462	2.61721
0	6	2	0.866015	0.0360581	-4.48324	14.1144	9.44624	6.93439	3.11168	14.9143	5.3587	2.9565
0	7	0	0.873033	0.0379731	-8.15042	13.6576	8.28777	6.33279	-0.973436	14.9387	4.92537	2.75526
0	7	1	0.872879	0.0360707	-5.50418	14.0574	9.41124	7.01801	1.49357	14.6893	5.28402	3.06379
0	7	2	0.869562	0.0386874	-8.07242	13.8974	8.32168	6.35307	-0.732647	14.9372	5.6383	2.63978
1	1	0	0.881697	0.0341451	-8.04178	11.7013	7.4927	5.56054	-3.03256	12.605	6.04444	3.70158
1	1	1	0.876093	0.0328864	-2.56825	12.0754	9	6.24797	2.56555	12.6045	5.40816	3.62626
1	1	2	0.872108	0.0318161	-6.90529	11.6572	7.15753	5.46745	-2.59383	12.1416	5.12057	3.43424
1	2	0	0.847899	0.0314701	-2.82682	11.5199	8.46073	5.71851	1.5189	11.4802	5.34737	2.79574
1	2	1	0.845232	0.0323591	-7.34819	12.2164	7.43103	5.58897	-3.17824	13.3383	5.1958	2.79425
1	2	2	0.838856	0.0329706	-3.70752	12.1045	8.5582	5.93878	0.9006	12.3124	5.41711	2.95009
1	3	0	0.890874	0.0358411	-7.35933	11.7325	7.37132	5.31715	-3.06684	12.7281	5.78195	2.88199
1	3	1	0.884409	0.0339822	-7.52089	12.7001	7.07483	5.47237	-3.13453	13.5406	5.6069	2.64522
1	3	2	0.883612	0.0325719	-4.04735	13.1041	8.89503	6.50563	0.259641	13.9549	5.01156	2.73066
1	4	0	0.882881	0.034909	-7.07521	12.9157	7.51034	5.7519	-2.88689	13.3739	4.77698	2.30121
1	4	1	0.878196	0.0336269	-4.30168	12.8884	8.66384	6.19265	-0.0876289	13.5648	5.28977	2.82262
1	4	2	0.875941	0.0309881	-7.55153	12.4649	7.20438	5.55088	-3.23393	13.001	5.03759	2.28893
1	5	0	0.887686	0.034171	-5.17827	12.9837	8.5122	6.00304	-0.83976	12.6118	5.41718	2.66956
1	5	1	0.881864	0.0329572	-7.37604	12.6522	7.61986	5.27637	-3.32048	12.9181	5.34028	2.65666
1	5	2	0.877262	0.0327925	-8.2312	13.7086	7.81071	5.98285	-3.39332	14.0924	6.13971	3.1557
1	6	0	0.880771	0.0354957	-4.48189	13.8268	9.3288	6.61699	0.871464	14.3059	4.99444	3.31913
1	6	1	0.878608	0.0332089	-7.76602	13.8442	8.63603	6.52525	-3.29734	13.35	4.96296	3.16791
1	6	2	0.87653	0.031666	-4.48324	14.1144	9.18362	6.59579	-0.118557	13.5596	5.63793	2.83065
1	7	0	0.887339	0.0345601	-8.15042	13.6576	7.87037	6.10918	-3.0437	13.7544	5.31579	2.9389
1	7	1	0.88383	0.033284	-5.50418	14.0574	8.97059	6.77424	-0.674379	13.6534	5.5503	2.8985
1	7	2	0.881967	0.0317656	-8.07242	13.8974	7.93478	5.91143	-3.7892	14.0832	5.56115	3.54846

Table B.2: Values of the gain, offset (measured by three different methods) and noise for the different parts of the typical ASIC, obtained averaging to all the ASICs tested.



C. Calibration method for the L1 analog trigger system of LST camera

C.1 Introduction

During the year 2016, a connectivity test took place at CIEMAT involving 35 modules of the Large Size Telescope (LST)¹ camera, to evaluate the integration of the electronics and mechanical structure. As explained in chapter 3, the modules of the LST are designed to be manipulated individually, allowing an easy removal and substitution in case of malfunctioning modules. The goals of the C35 test were to evaluate the interface between cluster mechanics and cluster holder, check the possible interference of modules during assembly, establish an assembly procedure, find potential problems during assembly and test assembly time. Also, it was dedicated to check the interfaces between the different parts of the electronics such as the Dragon boards and mezzanines, and the connection between the clusters and the backplanes. During this test, 35 modules were assembled in the camera plate in different configurations, and several connectivity tests were performed, such as tests on the clock, PPS, camera trigger and busy signals, power supply, trigger distribution along the camera and time delays configuration.

Within the scope of the C35 test, it was necessary to design a calibration method for the L1 transfer function, to find the threshold voltage which produces a trigger rate of 50%, depending on the input signal.

In the next sections the calibration algorithm developed for this task is described and results on the calibration are commented. Note that this is the calibration method currently implemented in the telescope.

C.2 L1 transfer function calibration

A method for the calibration of the L1 analog trigger system was developed and tested, based in a rate scan methodology. The goal of the calibration is to find the threshold voltage needed in each module to obtain a trigger rate of 50%. The calibration need to be performed for each one of the three adders and two discriminators of the L1 Application-Specific Integrated Circuit (ASIC). The 50% trigger rate threshold is obtained for several input signals in order to plot a curve that allows retrieving the gain and offset of the circuit, and compare them with the characterization of the ASICs.

The setup for the calibration consists on one module where a pulse with fixed amplitude and frequency can be injected in each of its seven pixels by the Slow Control Board (SCB). Increasing signal voltages are generated by adding the pulses injected in each of the seven channels of the module, meaning that in total it is possible to obtain up to 6 points for the calibration curve.

An algorithm based in a bisection method is applied to each input signal to calculate the 50% trigger rate threshold.

C.2.1 Calibration algorithm

The algorithm for this calibration has been implemented using a scripting language specially designed for the C35 test. It proceeds by configuring a fixed gain and frequency pulse in the SCB, in a fixed number of pixel lines. This way, the amplitude of the input pulse can be modified by adding more pixels. Once the initial pulse is configured, a bisection method is used to find the 50% trigger rate threshold. The threshold voltage in the ASIC is configured through a Digital to Analog Converter (DAC) with 8 bits, that can provide up to 255 different voltages from 0 to 1.2 V in steps of 4.8 mV. The algorithm initiates setting the threshold at the maximum voltage (setting the 8 bits to 1) and runs bit by bit, from the most significant bit, changing 1 to 0. If the new threshold voltage provide a trigger rate that is less than the target rate (in this case the target is 50%) then that threshold voltage is stored and the algorithm goes to the next bit. This way, only 8 steps are necessary to find the required threshold voltage. A diagram describing the algorithm is shown in figure C.1.

Once the loop is finished, the 50% trigger rate threshold is calculated following the formula:

$$50TH = \frac{(TargetRate - Baseline)}{(Baseline - Rate[CurrentThreshold - 1])} + CurrentThreshold \quad (C.1)$$

Being baseline the rate at current threshold, say the last threshold that was stored in the loop.

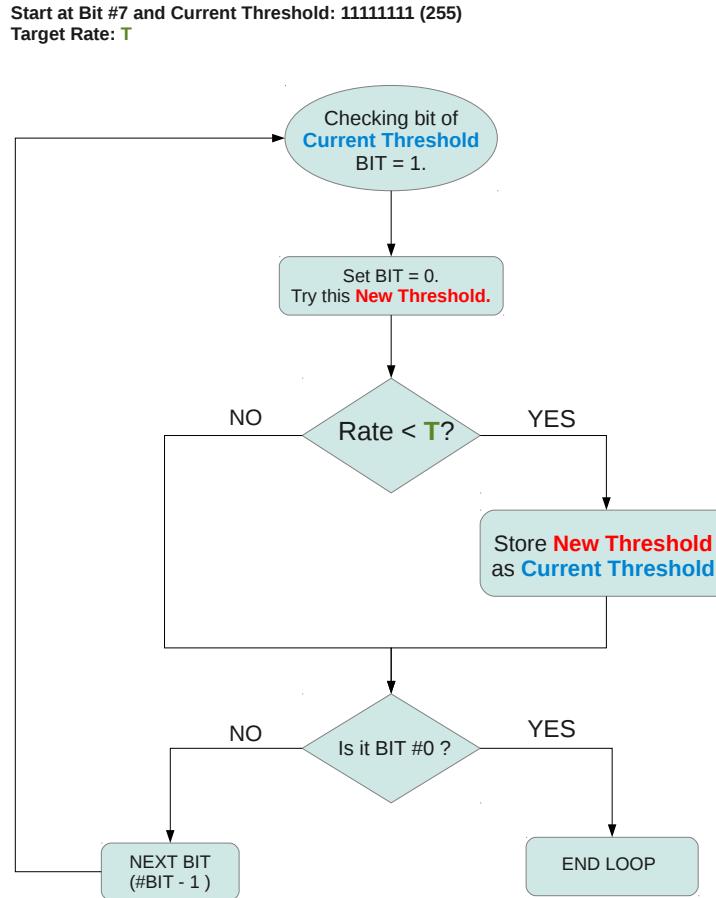


Figure C.1: Flux diagram of the calibration algorithm.

C.2.2 Calibration result

When the full algorithm ends and runs over the 6 possible input signals, the obtained 50% threshold can be plotted against the number of pixels added to see the calibration curve (see figure C.2).

If the initial pulse injected by the SCB is known and assuming that the adding is correct, the amplitude of each pulse is simply the multiplication of the initial pulse by the number of pixels added, being possible to obtain the gain and offset of the ASIC.

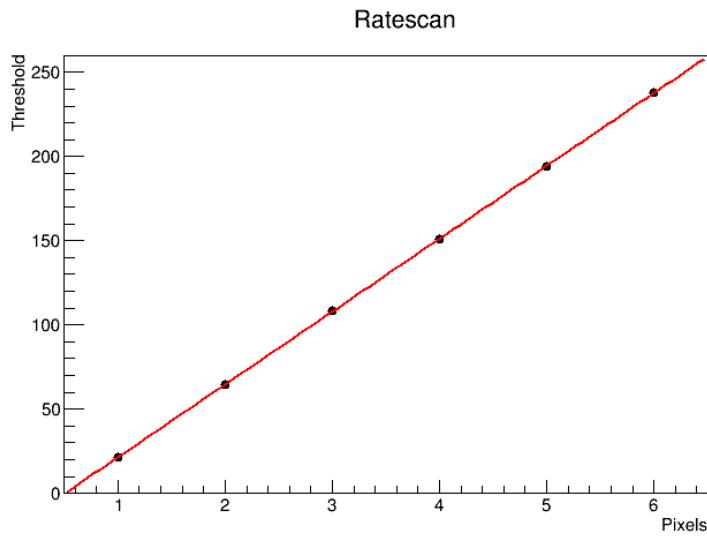
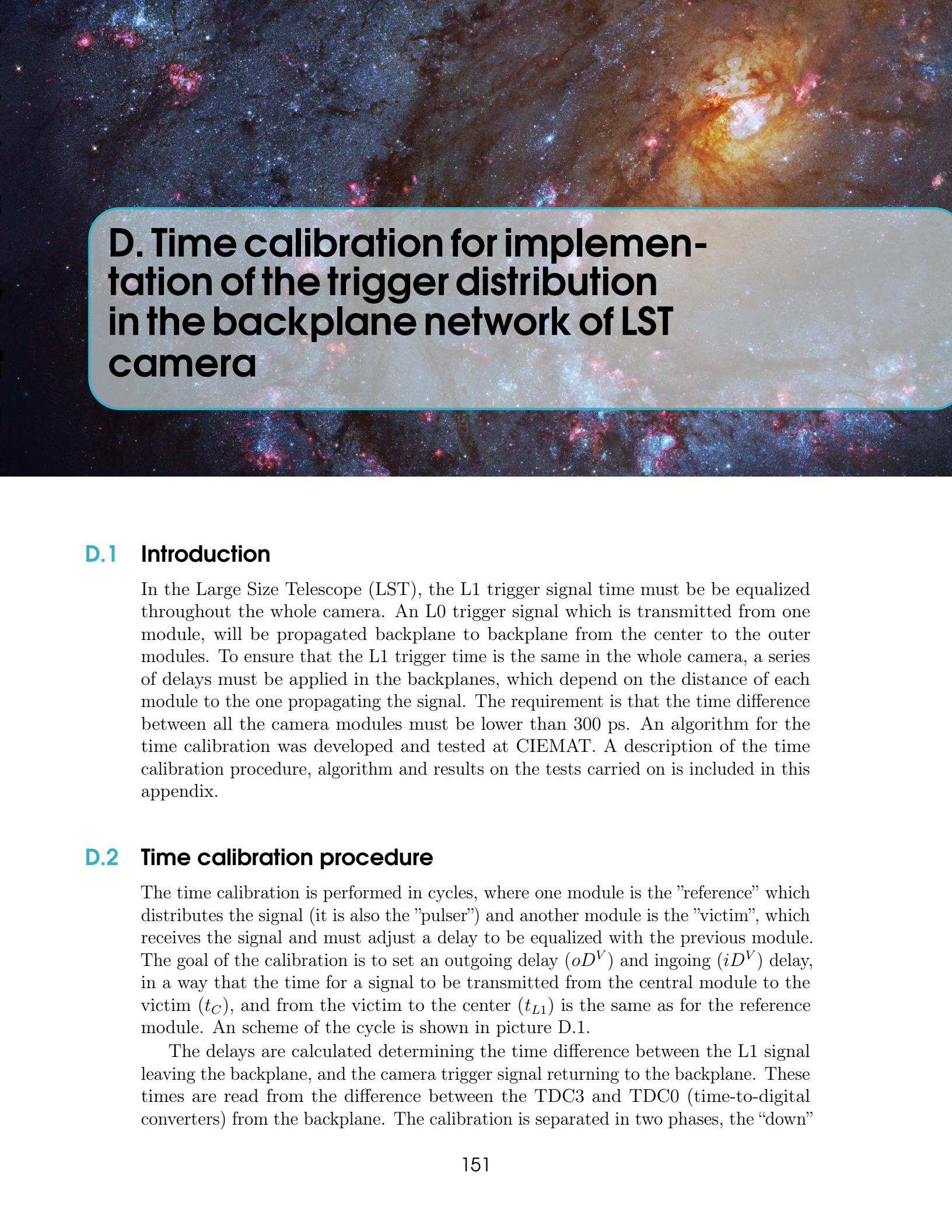


Figure C.2: Result of the rate scan for Adder A of one module.



D. Time calibration for implementation of the trigger distribution in the backplane network of LST camera

D.1 Introduction

In the Large Size Telescope (LST), the L1 trigger signal time must be equalized throughout the whole camera. An L0 trigger signal which is transmitted from one module, will be propagated backplane to backplane from the center to the outer modules. To ensure that the L1 trigger time is the same in the whole camera, a series of delays must be applied in the backplanes, which depend on the distance of each module to the one propagating the signal. The requirement is that the time difference between all the camera modules must be lower than 300 ps. An algorithm for the time calibration was developed and tested at CIEMAT. A description of the time calibration procedure, algorithm and results on the tests carried on is included in this appendix.

D.2 Time calibration procedure

The time calibration is performed in cycles, where one module is the "reference" which distributes the signal (it is also the "pulser") and another module is the "victim", which receives the signal and must adjust a delay to be equalized with the previous module. The goal of the calibration is to set an outgoing delay (oD^V) and ingoing (iD^V) delay, in a way that the time for a signal to be transmitted from the central module to the victim (t_C), and from the victim to the center (t_{L1}) is the same as for the reference module. A scheme of the cycle is shown in picture D.1.

The delays are calculated determining the time difference between the L1 signal leaving the backplane, and the camera trigger signal returning to the backplane. These times are read from the difference between the TDC3 and TDC0 (time-to-digital converters) from the backplane. The calibration is separated in two phases, the "down"

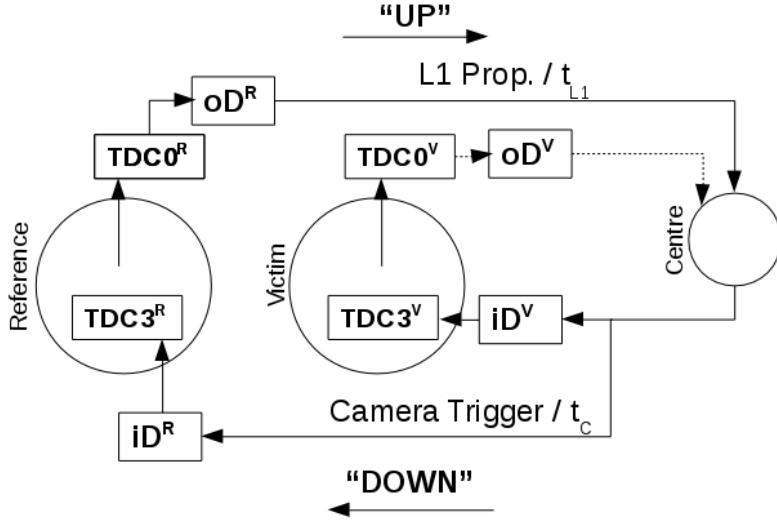


Figure D.1: Flux diagram of the calibration algorithm.

calibration and the “up” calibration, as shown in picture D.1.

- For the down calibration, the L1 signal distribution of the victim is deactivated, so the camera trigger signal is only triggered by the L1 of the reference. Because reference and victim are triggered by the same L0, the time at TDC0 for both modules will be the same. The difference $TDC3 - TDC0 = \Delta$ can be measured both in the reference and victim modules, therefore the incoming delay is simply:

$$iD_V = (TDC3 - TDC0)^r - (TDC3 - TDC0)^V = \Delta^R - \Delta^V \quad (\text{D.1})$$

Once the required delay value is calculated, it is set in two steps: a coarse delay in steps of 10ns and a fine delay in steps of 36 ps.

- For the up calibration, the L1 signal distribution of the victim is activated, and the one of the reference is deactivated. The goal of the up calibration is to set the outgoing delay in a way that the difference $(TDC3 - TDC0)^V$, which is the total time the signal needs to go from the victim module to the center and back to the victim. The delay therefore is:

$$oD^V = L - (TDC3 - TDC0)^V = L - \Delta^V \quad (\text{D.2})$$

Where L is the latency, and corresponds to the Δ^R measured in the down calibration. At the end of the cycle, the times t_C and t_{L1} will be the same both for reference and victim. At the start of the new cycle, the victim will be the new reference and other module is chosen as victim.

The calibration algorithm was implemented in a scripting language specifically designed for the communication with the different backplane registers.

D.3 Time calibration setup and tests

Two calibration setups were configured at CIEMAT, to implement the time calibration procedure. At first, four modules were set as shown in picture D.2, allowing to run three time calibration cycles as described in the previous section. The test consisted in setting initial default values in the delays, given by the position of the modules, and running the calibration several times for different initial values to ensure the reliability of the procedure. After the success of the first implementation, a second setup was prepared involving eight modules. The calibration procedure was performed several times, to check the stability of the final TDC values and that the deviations with every backplane were in the allowed range of 300 ps.

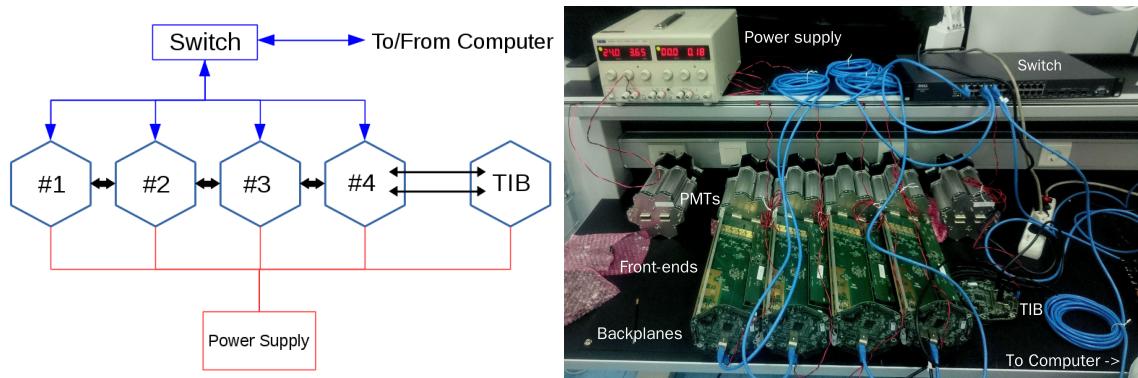


Figure D.2: *Left:* Diagram of the four modules setup. *Right:* Picture of the actual setup at CIEMAT clean room.

Thanks to these two setups, the time calibration procedure was successfully verified. The algorithm was then adapted to perform the calibration of the full camera, following the predefined paths of signal distribution as shown in picture A.3. This time calibration procedure must be run at least once every night of operation of the telescope.