L1 Analogue Sum Trigger ASIC for cameras of the Cherenkov Telescope Array

ABSTRACT

The level 1 (L1) trigger decision in cameras of the Cherenkov Telescope Array (CTA) is generally based in the detection of an accumulation of signal both in space and time among clusters of pixels. An application specific integrated circuit (ASIC), developed for the L1 trigger decisions in some of the cameras (analogue) proposed for CTA, comprises 7 input differential analogue channels and two low-voltage differential signalling (LVDS) digital output channels. The L1 ASIC computes the analogue sum of three configurable sets of inputs, and provides digital output signals when any of the sums is above a configurable voltage threshold, provided by an internal digital-to-analog converter (DAC). The analogue signal processing stage has been specifically developed for this application by means of a low noise differential architecture that provides a bandwidth of 500MHz.

The performance of the ASIC has been assessed using a rate scan methodology, consisting on the comparison of the input trigger rate from a generator on the evaluation setup and the ASIC trigger output rate.

The results of the characterization of the first version of the ASIC are very satisfactory. Improvements in its performances have been obtained with the current update version (2nd), using an internal individual DAC for each adder output that generates the threshold for each discriminator, instead of using one per each group of three adders as was done in the previous version, to correct the offset dispersion at the output. The second version was submitted last June 2014 for manufacture in a 350nm SiGe-BiCMOS. This version will be installed in the camera of the Large Size Telescope (LST) prototype for the CTA, and an automatic test system has been designed for the quality control of all the ASICs to be equipped.

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