Reconfigurable ASIC for Low Level Trigger System in Cherenkov Telescope Cameras

David Gascon[e], Juan Abel Barrio[a], Oscar Blanch[b], Joan Boix[b], Eric Delagnes[c], Carlos Delgado[d], Lluís Freixas[a], Fabrice Guilloux[c], Ruben López Coto[b], Gustavo Martínez[d], Oscar Martínez[b], Andreu Sanuy[e] and Luis Ángel Tejedor[a]

[a] *Universidad Complutense de Madrid (UCM),*
Ciudad Universitaria, Plaza Ciencias, s/n, 28040, Madrid, Spain
[b] *Institut de Física d'Altes Energies (IFAE)*
Edifici CN, Campus UAB, 08193, Bellaterra, Spain
[c] *IRFU, CEA, Université Paris-Saclay,*
F-91191 Gif-sur-Yvette, France
[d] *Centro de Investigaciones Energéticas, Medioambientales y Tecnológicas (CIEMAT)*
Av. Complutense, 40, 28040, Madrid, Spain
[e] *Dept. d'Estructura i Constitents de la Matèria, Institut de Ciències del Cosmos (ICCUB),*
Universitat de Barcelona (IEEC-UB), Martí Franquès 1, E08028 Barcelona, Spain

E-mail: dgascon@ecm.ub.edu

ABSTRACT: A versatile and reconfigurable ASIC implementing multiple concepts of low level trigger (L0) for Cherenkov telescopes is presented. Two different Level-0 approaches have been included in the L0 ASIC: the Majority trigger (sum of discriminated inputs) and the Sum trigger concept (analog clipped sum of inputs). Up to 7 input signals can be processed following one or both of the previous trigger concepts. Each differential pair output of the discriminator is also available as a LVDS output. Differential circuitry using local feedback allows high speed (500 MHz) to be achieved while maintaining good linearity in a 1 Vpp range. Experimental results are presented. First prototype cameras of Cherenkov Telescope Array (CTA) project under production, use this ASIC.

KEYWORDS: Integrated Circuit; ASIC; Trigger circuits; High energy physics instrumentation; gamma ray detectors; Telescopes; Nuclear Electronics.

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1. Introduction

The Cherenkov Telescopes are used to detect Very High Energy (VHE, E>10 GeV) gamma rays after their interaction with earth's atmosphere [1], [2], [3] and [4]. By detecting and processing Cherenkov light produced by gamma rays, it is possible to characterize the incoming photon in terms of direction and energy. Placing several telescopes (of different sizes) together results in a gamma-ray detector with enhanced sensitivity in a wide energy spectrum.

Detection of Cherenkov light is performed by means of cameras whose pixels are based on fast and sensible photo sensors; typically photomultiplier tubes (PMTs). Each photo sensor is coupled to an electronic readout chain for PMT waveform digitalization, and an electronic trigger chain to disentangle signals produced by incident VHE gamma rays and those induced by background due to the light of night sky.

Trigger decision electronics perform a fast signal processing in order to discriminate gamma-ray events from other events produced by light from Night Sky Background (NSB). In this paper an Application Specific Integrated Circuit (ASIC) designed specifically for camera trigger decision in Cherenkov Telescopes is presented. The ASIC can be configured to perform different triggering schemes: majority trigger, sum trigger and also provides interface for digital trigger systems. Section 2 describes a typical multilevel trigger approach used for Cherenkov telescope cameras [5]. Section 3 presents the architecture of a new versatile ASIC for the implementation of the low level trigger. Section 4 includes measurements of functionality and performance of the ASIC. Conclusions are included in section 5.

2. Trigger architecture

2.1 Analog trigger

Trigger decision in Cherenkov telescopes is based in the detection of a concentration of signal both in space and time. The photons coming from a Cherenkov shower will be detected by several close pixels in a time window of few ns. Therefore, a telescope trigger, requiring a given number of pixels of the camera with a minimum number of photons in a short time, will reject a sizeable amount of NSB induced events.

Two different strategies for triggering are used in current Cherenkov Telescopes [5]. Majority trigger architecture consists in the discrimination of the signals coming from pixels, in order to count the number of activated pixels in a region. After discrimination, the signal processing can be analog or digital. On the contrary, sum trigger strategy consists in the addition of the pulses from the pixels in a region, in order to be compared with a threshold defined for the whole region. In a typical multilevel architecture, these two strategies are used at lower level (L0) trigger, being possible to use the same high level (L1) trigger circuit for both.

The trigger system is designed for cameras made up by 7-pixel modules. One cluster consists of PMTs, front-end circuits, digitize and readout electronics and trigger decision and distribution electronics.

2.2 Architecture of the trigger

The signal of every pixel is amplified and feeds a fast readout digitizer like NECTAR [6] or DRAGON [7] developments. A two-level trigger scheme compatible with the actual hardware and mechanical architecture of some telescopes cameras proposed for CTA has been developed and is shown in Figure 1.

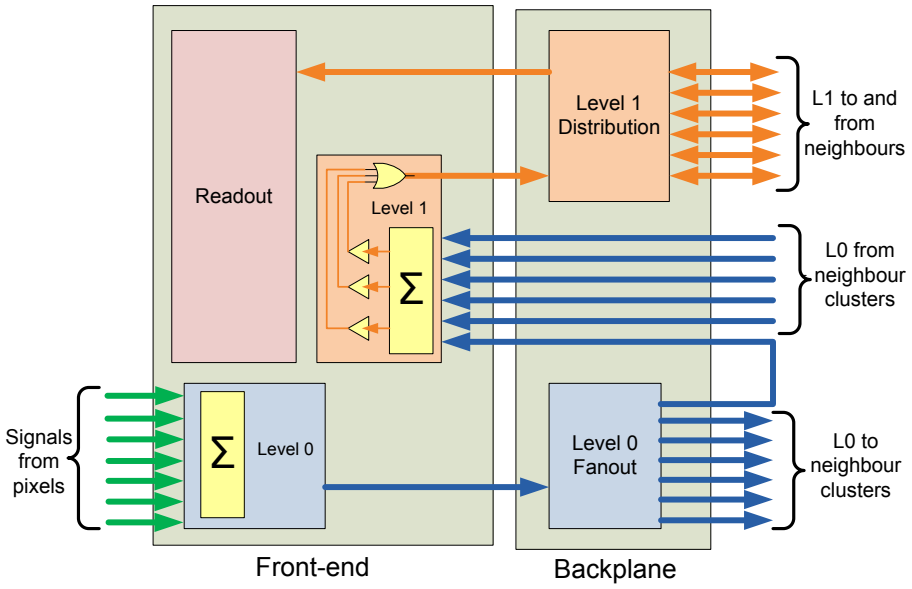

Figure 1. Block diagram of the analogue trigger

The first level, so-called L0, is module-based and combines the signals of the pixels in each module. In this level the trigger implements the Majority and Sum trigger strategies, as shown in Figure 2. The second level, called L1, is also implemented in each module and combines the L0 signals of neighbouring clusters with local L0 in specific trigger regions. The level 1 will generate a digital trigger pulse, which is distributed to the digitizers of all clusters in the camera

and is the final camera trigger, with different physical meaning depending on the strategy of L0. A detailed description of the ASIC implementing L0 subsystem is presented in section 3.

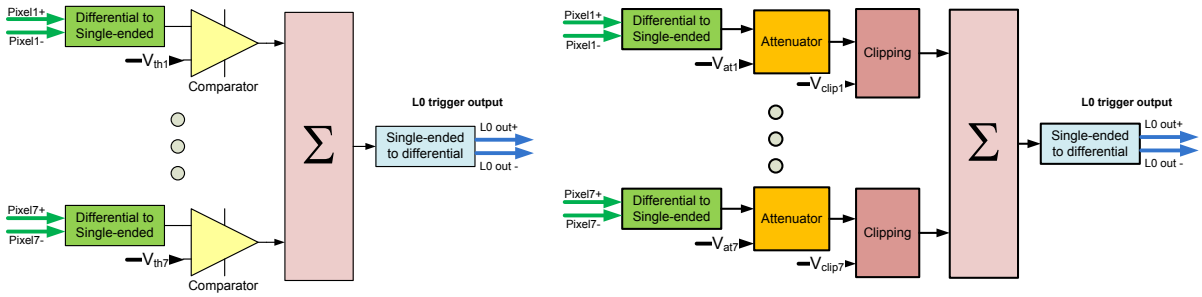

Figure 2. Block diagram of the L0 trigger: majority (left) and sum (right) schemes

3. ASIC design

A mixed signal ASIC is designed to implement several low level trigger functionalities. A block diagram is shown in Figure 3.

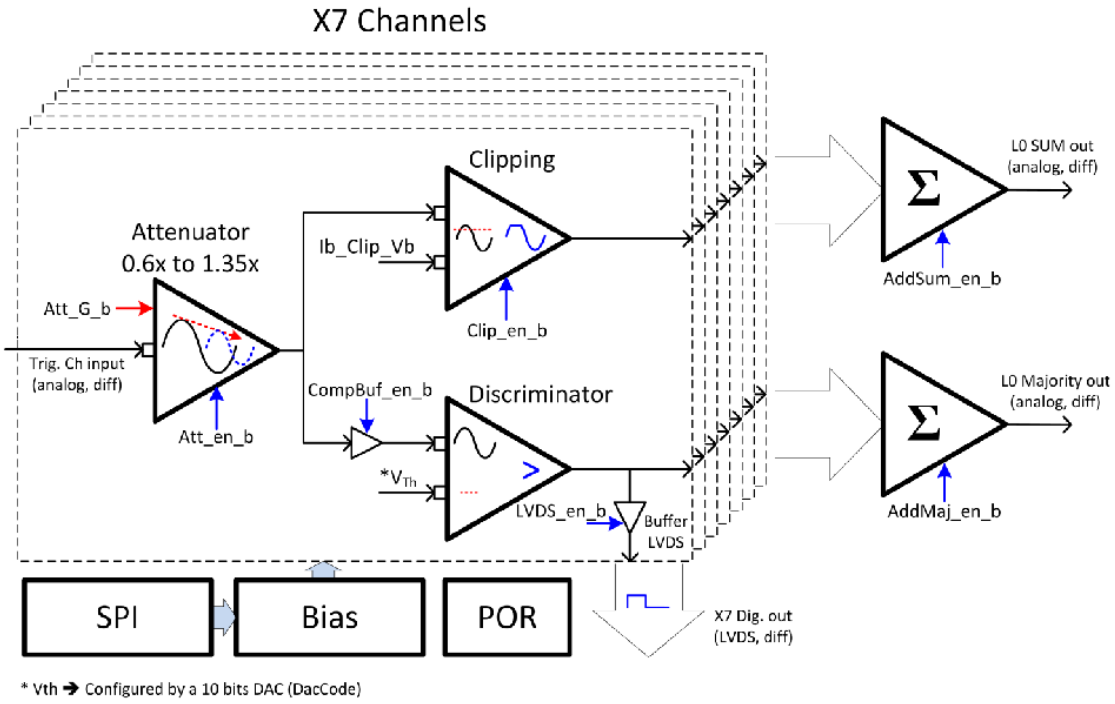

Figure 3. Block diagram of L0 ASIC

Both majority and sum trigger analogue schemes are implemented. The output of each majority discriminator is available, so the majority decision and high level trigger scheme can be implemented in a programmable logic device (FPGA or CPLD typically).

Requirements of the ASIC are summarized in Table 1. The L0 trigger receives the signal from each individual PMT after signal conditioning that is basically a preamplifier with a bandwidth larger than 350 MHz (see [9] and [10]). The input signal will have an amplitude of 20 mV per phe (photoelectron) with a signal to noise ratio (S/N) larger than 4 and the L0 should

be able to manage up to 20 phe per channel. A gaussian with 2.4 ns FWHM is a good approximation of the signal shape.

Dynamic range (input)	> 20 phe per channel
Bandwidth	> 500 MHz
Output noise (sum)	< 2 mV rms (with unconnected inputs)
Output noise (majority)	< 0.2 phe (with unconnected inputs)
Comparator DAC resolution	> 8 bits
Comparator efficiency	> 95%
Comparator purity	> 99.99%
Linearity error	< ± 5% or 0.25 phe
Gain adjustment	Reduce 25% RMS to 5%
Clipping DAC resolution	> 8 bits
Power consumption	< 150 mW/ch

Table 1. L0 trigger ASIC specifications

For the majority case, the input signal of each pixel should be passed through a comparator with a threshold programmable over a 8- bit range and then added to the other 6 pixels being part of the cluster. The comparator should be able to react fast enough to the rising edge of the input pulse, so that it triggers on the signal provided by one phe with efficiency larger than 95% keeping the probability to trigger on noise below 0.01%. The output of the comparator should be a window with time duration equal (± 15%) to the time the input signal was above the discriminator threshold. The linearity of the comparator, defined as (Mean-Fit)/Fit, should be at least the largest values between ±5% and ± one fourth of phe.

For the sum-trigger option, there should be a gain adjustment, which does not need to be continuous. The amplitude of the signal coming from the PMTs most likely will be calibrated with a RMS around 25%. The gain adjustment should be able to narrow down to 5% RMS the amplitude spread. The adjusted signal should go through a clipping module controlled by a DAC of 8-bit or more DAC.

Although both schemes are implemented, it is possible to power down the one that is not currently used.

3.1 Basic differential stage

Several building blocks are based on different versions of the open loop differential stage depicted in Figure 4. Those blocks comprehend the input attenuators, the clipping stage and a transconductance stage in the adders on Figure 3. An open loop fully differential architecture has been chosen to fulfil high speed and low power requirements. The main drawback of such an architecture is a moderate linearity compared with a closed loop solution however linearity requirements are moderate and closed loop (OTA/OPA based)solutions often suffer from linearity limitations due to slew rate problems.

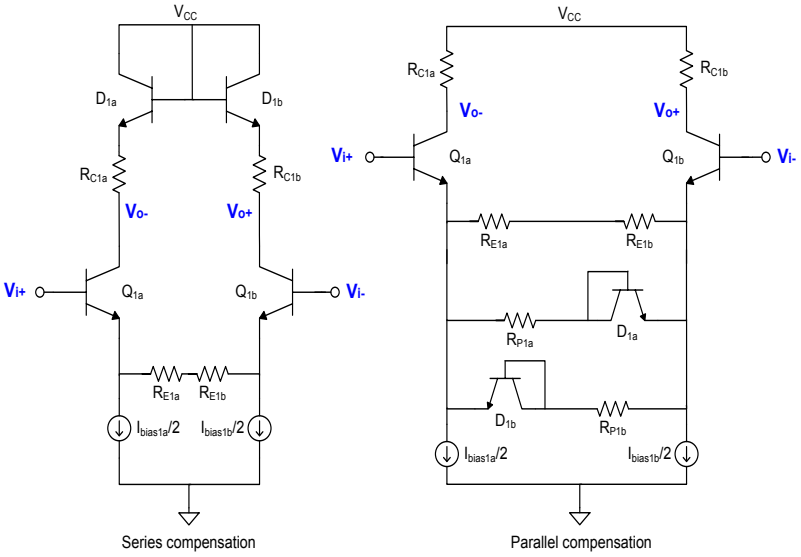

Figure 4. Open loop differential stage. Series (left) and parallel (right) linearity compensation.

The non-linearity of differential pair is due to the variation of the base-emitter voltage of the two transistors. It is often corrected by the addition of one diode (gain of 1) as shown in Figure 4, or two diodes (gain of 2) in the collector branches to obtain the same voltage drop in emitter and collector. However, the consequence of this "serial correction" is lower voltage headroom and that the compensation is dependent to the gain. This is problematic for low voltage operation and for circuits with variable gain as the ones required for this ASIC. In [11] a parallel correction scheme is presented. In this parallel correction, the loss of gain is compensated by decreasing the emitter generation in the opposite branch, as shown in Figure 4. The new linearity compensation scheme permits compensation of different gains and does not imply any penalty in voltage headroom.

3.2 Discriminators

The discriminator block for the majority trigger mode is based on a differential discriminator and a 10-bit digital to analogue converter (DAC) designed for SCOTT chip ([12] and [13]). In order to maximize the speed, the discriminator follows a multistage architecture followed by a digital restorer and a latch, as depicted in Figure 5.

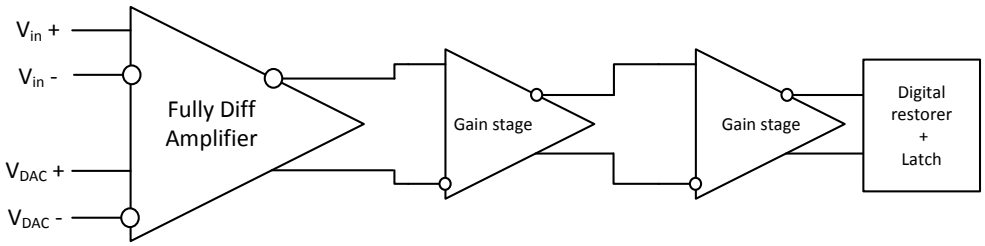

Figure 5. Architecture of the discriminator.

The DACs are differential and implement resistor string architecture [14] to guarantee their monotonicity.

3.3 Adders

Both the SUM and majority fully differential adders are designed as shown in Figure 6. Each adder consists on seven open loop transconductance stages (one per input) and a closed loop transimpedance amplifier based on a fully differential operational amplifier. The transconductor is based on a degenerated differential pair with the same parallel scheme for linearity compensation presented in in Figure 4.

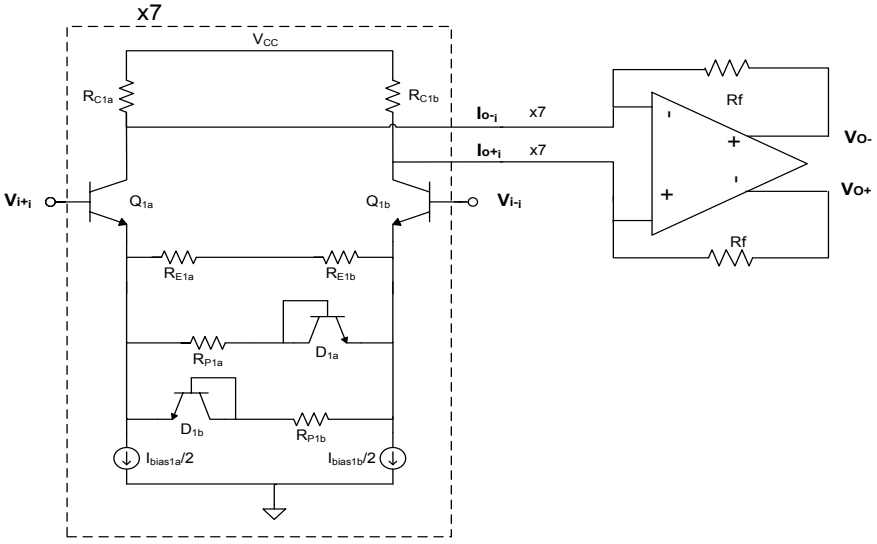

Figure 6. Schematic of the adder block.

Closed loop transimpedance amplifier of Figure 6 is based on high gain bandwidth product (GBP) operational amplifier. It is also used in other ASICs for CTA ([10]). A simplified schematic of fully differential operational amplifier is shown in Figure 7 left. It is a folded cascode amplifier, with a second Miller stage and a class AB output stage. Miller compensation is used, with nulling resistor. Input pair is degenerated to improve slew rate. Fast and accurate continuous time common mode feedback is provided by an error amplifier.

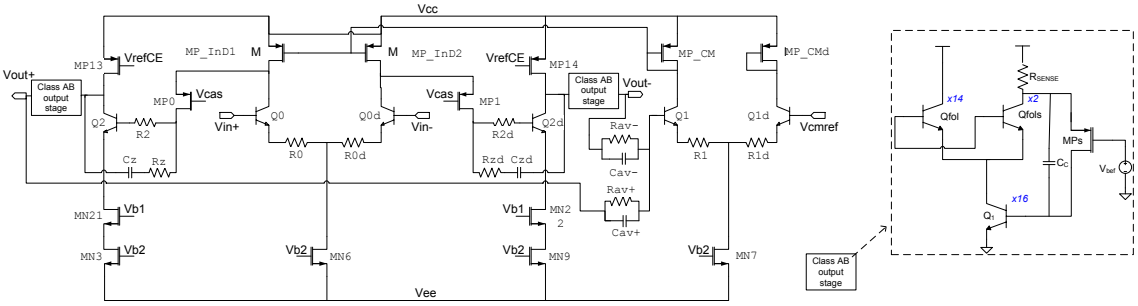

Figure 7. Simplified schematic of the fully differential operational amplifier (left) and of the class AB output stage (right).

The class AB output stage is shown in Figure 7 right. Lower voltage operation is achieved (by 1 Vbe), so the stage can be integrated in the operational amplifier of Figure 7. The push-pull operation is based on fast local feedback loop, which GBP exceeds 2 GHz with a PM exceeding 60 deg. This stage can provide more than 20 mA peak current, with a quiescent current of 5 mA. This allows driving low load impedances with AC coupling, i.e. the cable or transmission line impedance connecting L0 ASIC to the trigger backplane, as shown in Figure 1.

3.4 A 7-channel ASIC

The ASIC is implemented in a 0.35 µm BiCMOS technology with SiGe NPN HBTs. The use of HBT transistors is crucial because of several reasons:

- The BW of the signal processing in the ASIC must be higher than 500 MHz. It means that the bandwidth of each stage should be significantly higher, 700 MHz or more. Therefore, the use of high f_t active devices is crucial.
- The differential pair stages depicted in Figure 4 and Figure 6 rely on emitter degeneration to achieve the required linearity. Bipolar devices provide a very good transconductance over bias current ratio.

The layout and microphotograph of the ASIC are shown in Figure 8. The area is about 12 mm^2 and it is packaged in a QFN 56 package.

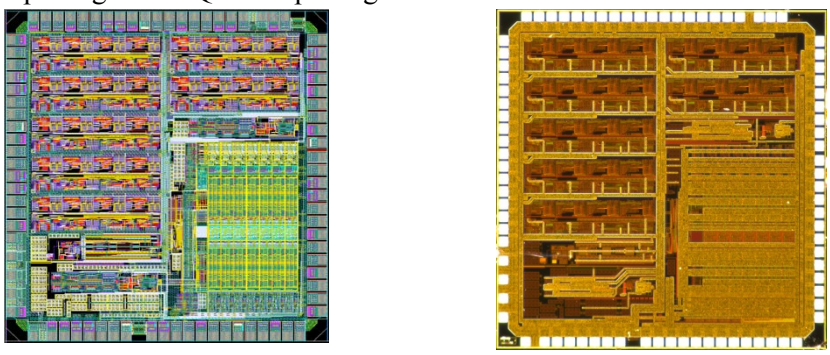

Figure 8. Layout (left) and microphotograph (right) of the ASIC

Three different simultaneous operation modes are possible: sum trigger, majority trigger and discriminated outputs (7 LVDS outputs). Each subsystem of each channel can be set in "power down mode. The chip can be reconfigured and the operating parameters (thresholds, attenuation factors, bias currents, etc) set by means of a Serial Peripheral Interface (SPI) bus.
The power consumption depends on the ASIC configuration but for a typical sum or majority trigger operation (not simultaneous) is about 90 mW per channel.

4. Results

The L0 ASIC has been integrated in NECTAr and DRAGON front end (FE) board, see [15]. A typical L0 ASIC sum trigger output for a 2 phe signal using DRAGON FE is shown in Figure 9.

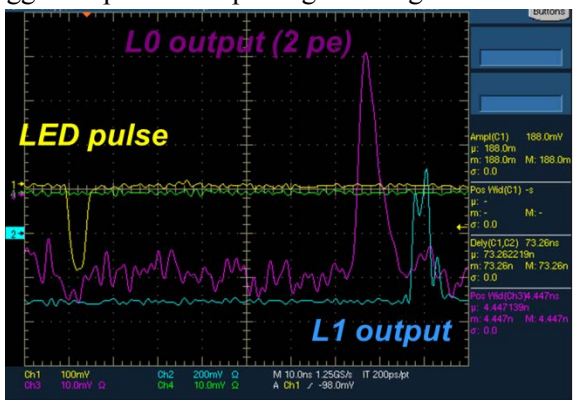

Figure 9. Typical L0 ASIC sum trigger output for a 2 phe signal using DRAGON FE.

The response of the sum trigger system for different clipping levels is depicted in Figure 10. The system is linear until a saturation or clipping level is reached. The clipping level is a configurable parameter.

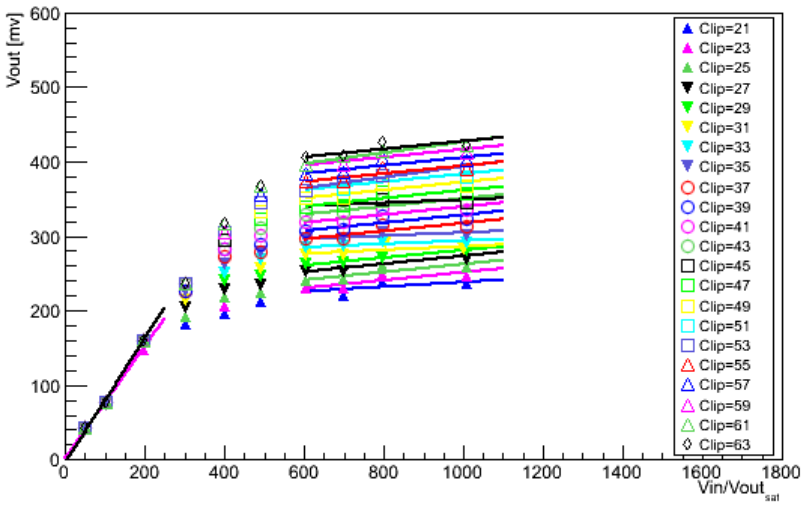

Figure 10. Sum trigger transfer function for different clipping levels.

The clipping level can be adjusted from 30 to 450 mV, as shown in Figure 11. Three different ranges can be selected by a coarse control (3 bit). A fine control (6 bit) sets the precise level clipping of each channel.

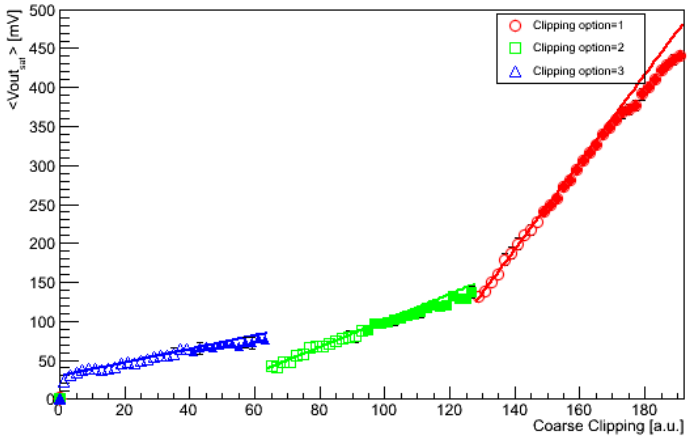

Figure 11. Clipping level as function of clipping control.

The performance of sum trigger adder is illustrated in Figure 12. The sum adder responses to an input voltage below (50 mV) and above (500 mV) clipping level are shown. In each case, the same signal is injected to different number of channels and the output is normalized to the number of channels which have been pulsed. For input levels below clipping, the behaviour is linear and the normalized output is around 40 mV for any combination. Of course, this condition does not hold when inputs are above clipping level.

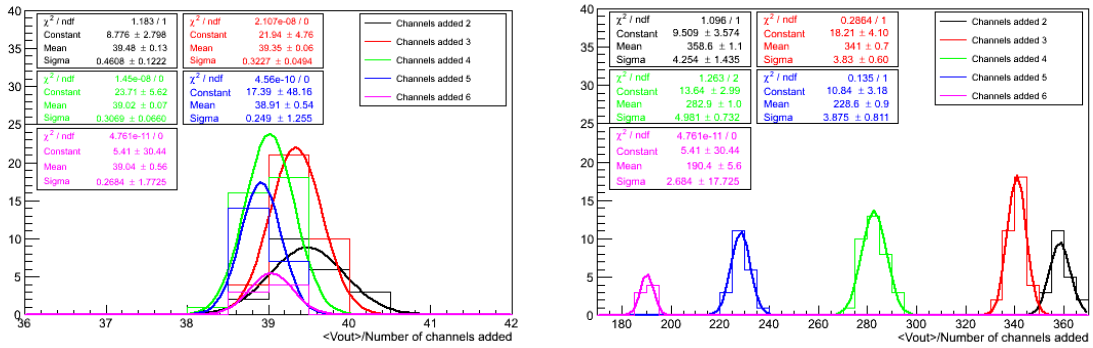

Figure 12. Sum adder response to an input voltage below (left) and above (right) clipping level.

Majority trigger dynamic range and thus discriminator linearity is shown in Figure 13. The discriminator transition level as function of input signal amplitude is obtained by a discriminator threshold scan. The noise of the majority chain can be inferred from the resulting curves (the so-called S-curves) as well. Noise is well below 2 mV rms.

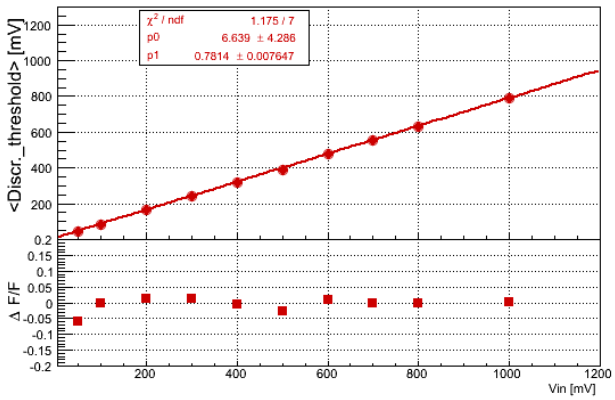

Figure 13. Discriminator transition for different input signal amplitude.

The majority trigger timing characteristics is shown in Figure 14. Relative delay (from input to output) variation and output pulse width are measured as function of input signal amplitude. The input pulse FWHM is about 3 ns. The threshold is set to about 6 phe and the approximate calibration is 20 mV/phe, at the input of the L0 ASIC. The discriminator propagation delay and time walk are well below 2 ns.

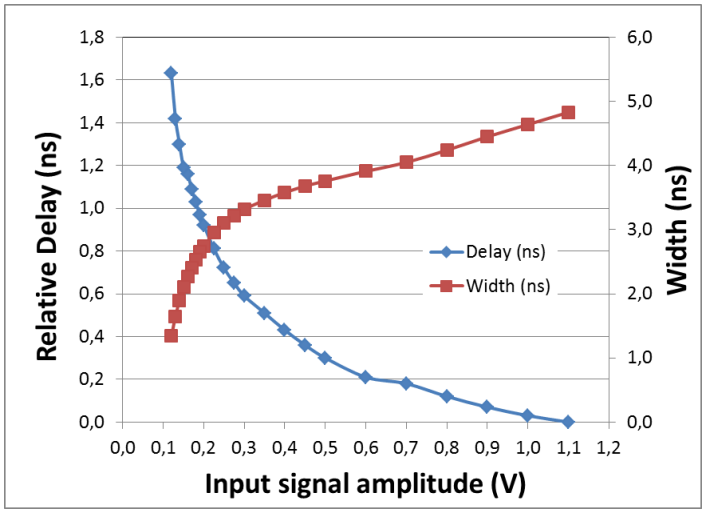

Figure 14. Majority trigger timing characteristics. Relative delay variation (blue) and output pulse width (red) as function of input signal amplitude (input FWHM of about 3 ns). The threshold is set to about 6 phe, with 20 mV/phe (at the input of the L0 ASIC).

The performance of majority adder is illustrated in Figure 15. In this case, the discriminator outputs are added. Therefore, clipping has no effect provided its value is above discriminator threshold. It can be noticed that a constant value of 100 mV is added for every active input.

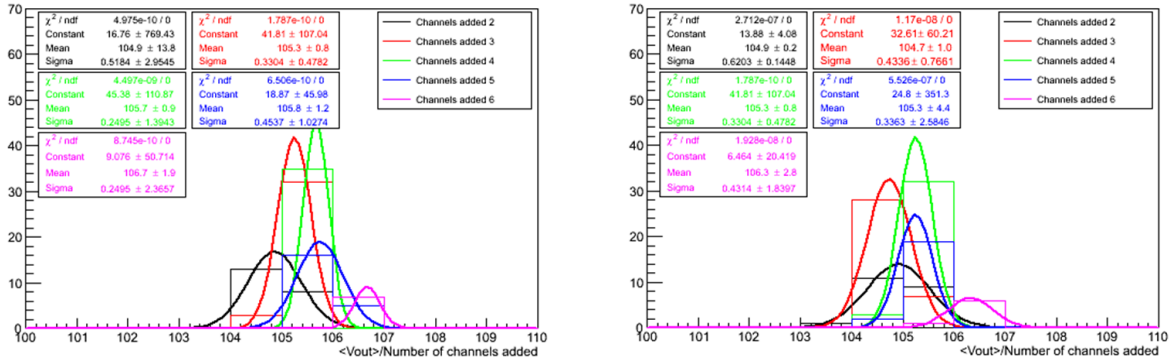

Figure 15. Majority adder response to an input voltage below (left) and above (right) clipping level.

5. Conclusions

A versatile and reconfigurable ASIC for implementing the trigger of Cherenkov telescope cameras has been presented. The chip implements two different trigger schemes: the sum and the majority trigger. Furthermore, the discriminator outputs are available as independent LVDS signals allowing the implementation of complementary trigger schemes such as a FPGA based "digital" trigger ([15]).

Unused blocks in a given operation mode can individually be set in standby mode, thus optimizing the power consumption which is a factor 5 smaller than equivalent solutions implemented with commercial off the shelf components ([5]).

A combination of open and closed loop design techniques is used to achieve high speed and minimize power consumption, while fulfilling linearity and noise requirements. Fully

differential design is used to increase power supply noise rejection and to increase dynamic range.

Acknowledgments

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