Characterization of analogue ASIC for L1 trigger decision.

Abstract

A test for the quality control of the L1 trigger system ASIC has been performed to characterize its behaviour and features. Different parts of the ASIC were tested and the information obtained has been analyzed in order to obtain data about the gain, offset and noise. A number of 389 ASICs that surpassed the quality control are included in this analysis.

In addition to the characterization, an alternative method to calculate the offset in an indirect way has been developed, as a result of a voltage rate scan. If this method is reliable, it would offer the possibility to measure the offset directly from the camera.

1. Introduction

A characterization and analysis of the features of the ASIC for the L1 trigger system, is useful to be familiar with its response, for calibration or for interpretation of the data retrieved by the camera.

Its mandatory to check for every ASIC that its performance is valid and inside the specifications required by the quality control. For that reason, an automatic quality test has been designed, which is able to measure features such as gain, offset and noise coming from different part of the ASIC.

In section 3, those features are presented for the 389 ASICs that passed the test.
In section 4, an alternative way to calculate the offset of the ASIC, using a lineal fit of an input voltage rate scan, is discussed and applied.
In section 5, analysis and conclusions substracted from the previous sections are commented.

2. Quality Control Test

The quality control test consisted in different checks that evaluate the behaviour of the ASICs in its different parts (such as the 7 input channels, three adders and the two LVDS discriminator outputs).

The Voltage test measured the gain of all seven input single channels and the two outputs for 10 different voltages (from 100mV to 1000mV) using a rate scan methodology, consisting on the comparison of the input trigger rate from a generator on the evaluation setup and the ASIC trigger output rate. This computation is performed with scalers implemented in the FPGA board.

The Analog offset test consisted in the measurement of the offset in the Analog Adder Output test, which is the output of a multiplexor that selects among the available analog output adder, plus a buffer for the output pins. The measurement is directly from the differential output pin of the ASIC by a Multimeter.

The Digital offset test procedure was the measurement of the offset in the LVDS digital outputs, 0 and 1, by the evaluation of the outputs status as a funtion of the threshold.

The methodology consist on increasing the threshold from 0 Volts using the DAC's values until find the minimum value that the output crosses from 1 to 0, and the maximum cross from 0 to 1. The voltage between this two points is the noise of the digital output, and the mean point is the offset. Setting the Threshold to 0 it is possible 3 different behaviors:

If the status of the digital output is always a logic "1" (tagged as type "Pos") it is possible to

measure the minimum and the maximum points and therefore it is possible to calculate the Offset and the noise.

If the status of the digital ouput is always a logic '0' (tagged as type "Neg"), it is not possible to measure neither the minimum nor the maximum point, and then a value of zero is assigned by the program both to the noise and the offset.

Finally, if the status of the digital ouput is switching (tagged as type "Com"), it is only possible to measure the maximum value, and the other is assigned to 0. In this case the noise is understimated and the threshold is overstimated.

3 Characterization

3.1 Gain.

From the test voltage, it was possible to measure the gain for the seven input channels, the three adders and two output discriminators. In *figure 1* is presented the distribution of the gains for the 389 ASICs for a certain combination of channel-adder-discriminator. In general, gains for all combinations are quite uniform with a mean value of ~0,87 mV and a RMS of ~0,04.

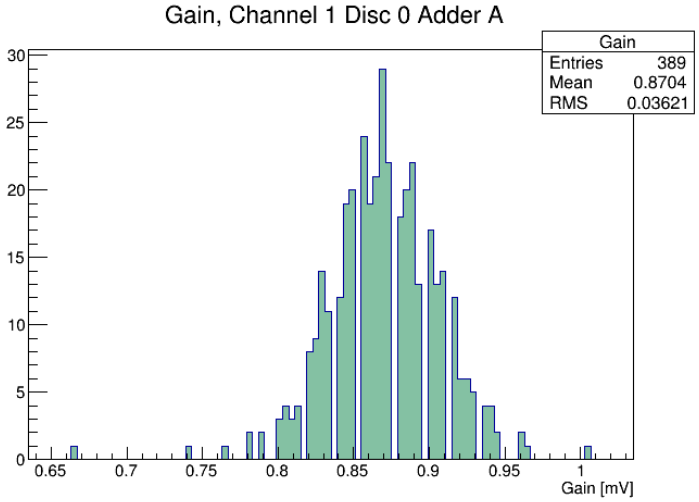

Figure 1: *Gain distribution for all ASICs in a certain combination of channel-adder-discriminator. All possible combinations were plotted, being similar to this one.*

An overview of the gains for all the ASICs, was made in order to analyze the behaviour of every independent channel. It was required to check if there is a channel that could dominate over the others or on the other part, a channel with too low gain that could be supressed.

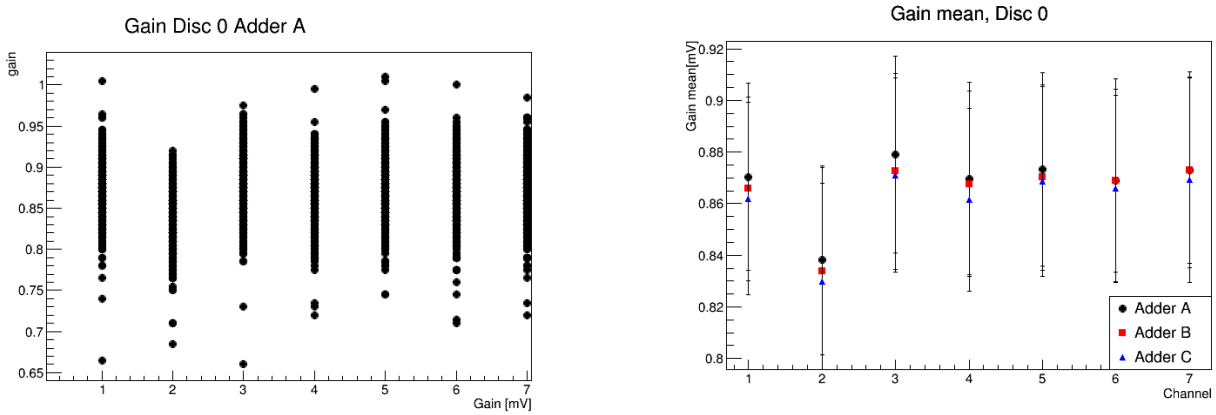

Figure 2: *Gains per channel for 389 ASICs for fixed discriminator and adder (left) and the gain mean of all ASICs per*

channel, for one discriminator and the three adders.Vertical bars represent the RMS.

In *figure 2* it can be observed that the second channel has for all the ASICs, a lower gain than the others. The third channel seems to have a slightly higher gain. This effect could overcome from the fact that this two channels are fed with a different kind of signal than the others.
The rest of the channels present a mainly uniform gain for all the ASICs.

Several low gains have been spotted in some channels of certain ASICs. Having too low gain could be a criteria to discard units that would have a bad performance, therefore, the ASICs with a gain measured lower than 0,7 were identified in *table 1*.

#Asic	Disc	Ch	Adder	FO	Gain
209	0	2	B	37.3333	0.7
209	1	2	A	14.3333	0.68
209	1	2	B	32.6667	0.7
329	0	1	A	29	0.665
329	0	2	A	23	0.685
329	0	2	B	-9.66667	0.7
329	0	2	C	23	0.645
329	0	1	A	31	0.66
329	0	6	B	3	0.7
329	0	7	C	21	0.695
329	1	4	A	30.3333	0.7
329	1	6	B	16	0.675

Table 1: *Asics with gain equal or lower than 0,7 mV for the corresponding combination of channel-adder-discriminator. Values of the offset from the fit (FO) are also presented.*

To study how the different parts of the ASIC are related, correlation plots have been generated, studying correlation between channels, adders and discriminators.

First of all, the channel-channel correlation was plotted. In this case gains from pairs of channels were presented keeping the adder and the discriminator fixed. There were 252 combinations from where a linear fit was performed to analyze the possible correlation.

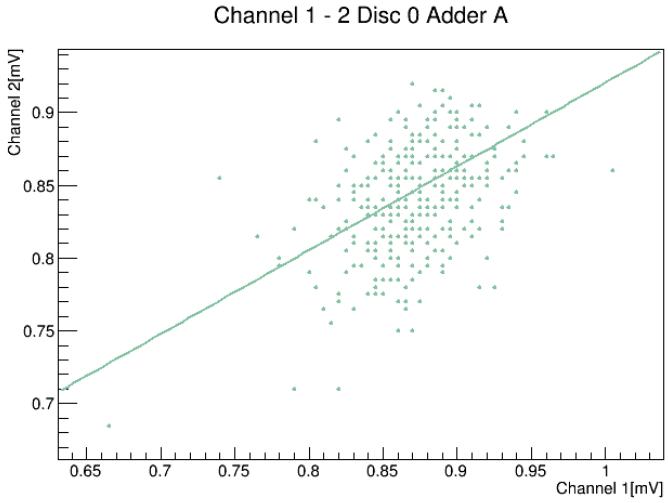

Figure 3: *Correlation of the gain between channels for fixed adder and discriminator. All possible combinations of*

channel pairs were plotted.

The same case was done for the three adders, presenting the gain from different adders keeping the channel and discriminator fixed. There were 126 possible combinations.

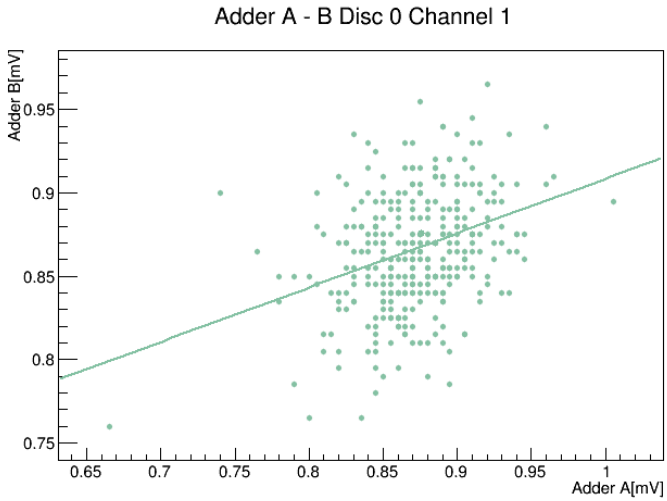

Figure 4: *Correlation of the gain between adders for fixed channel and discriminator. All possible combinations of adder pairs were plotted.*

For correlation between output discriminators, 21 combinations were plotted.

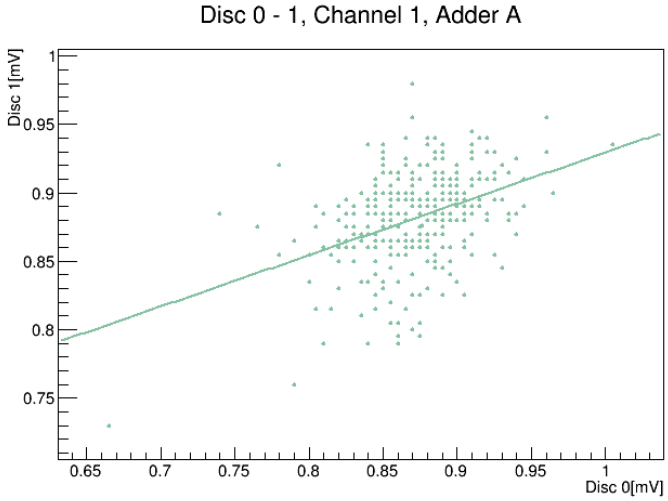

Figure 5: *Correlation of the gain between discriminators for fixed channel and adder.*

The pearson correlation coefficient for each plot was calculated trhough a linear fit to quantify such correlation. In *table 2* are presented the mean values of the coefficents, together with each RMS and chi2 value.

3.2 Offset.

The offset of the ASICs was measured in the quality control test by two different techniques. First of all, an analog offset was measured directly at the output of the adders using a multimeter. In this case, discriminators are not taken into account for the analysis.
Secondly a digital offset was measured at the outpus of the discriminators, using a rate scan methodology described in section 1. Note that with the rate scan methodology, offset cannot be

measured for all the adders in certain ASICs, only the ones with an output status tagged as “Pos” have calculated values of the offset. The rest of them are assigned a value of “0”, therefore they have been excluded from the distribution plots.

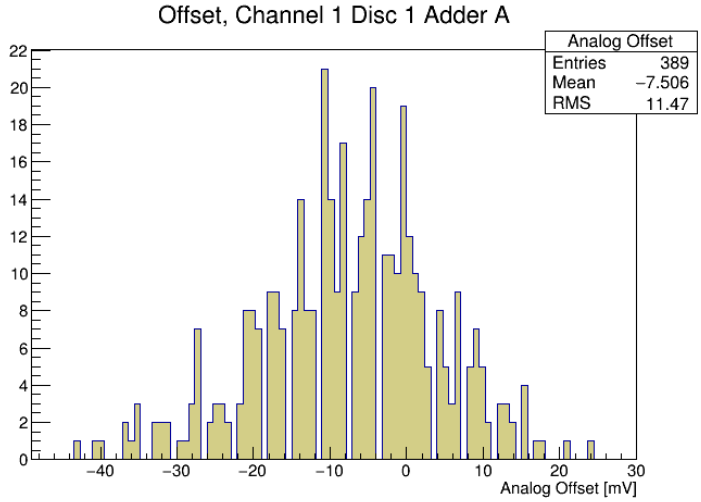

Figure 6: *Analog offset distribution for all ASICs in a certain combination of channel-adder-discriminator. All possible combinations were plotted, being similar to this one.*

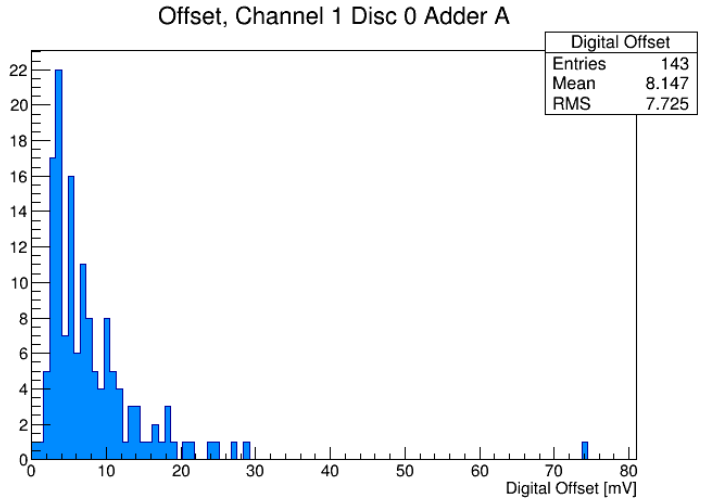

Figure 7: *Digital offset distribution for all ASICs in a certain combination of channel-adder-discriminator. All possible combinations were plotted, being similar to this one.*

For the analog offset, the mean value of all distributions is -5,68 mV with RMS of 12,65 mV. For the digital offset the mean value is 3,28 mV with RMS of 6,353. Note that due to the conditions of the rate scan methodology, it is not possible to measure negative values for digital offset.

Correlation plots has been made also for the offsets and the results of the mean values for the pearson correlation coefficient are presented in table 2.

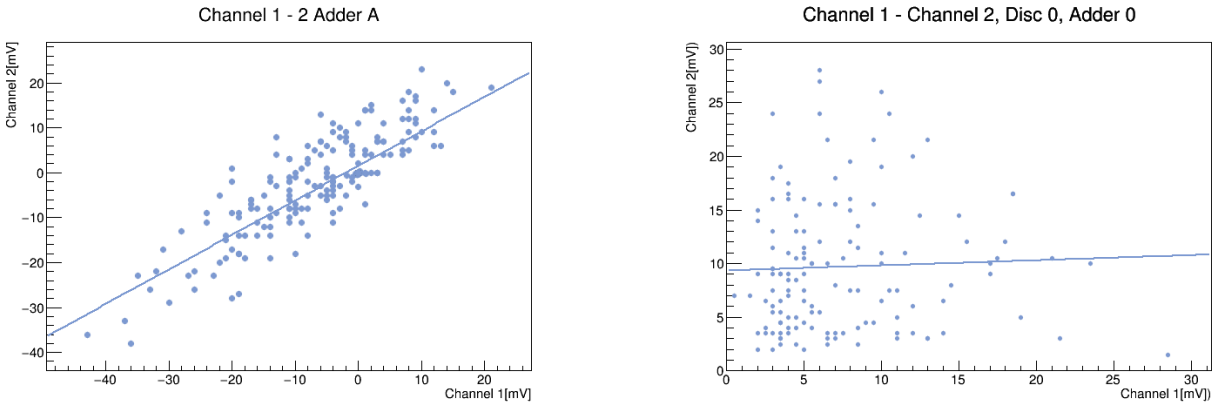

Figure 8: *Correlation plots for analog offset (left) and digital offset (right) between channels for fixed adder and discriminator in the case of digital offset. All possible combinations of channel pairs were plotted.*

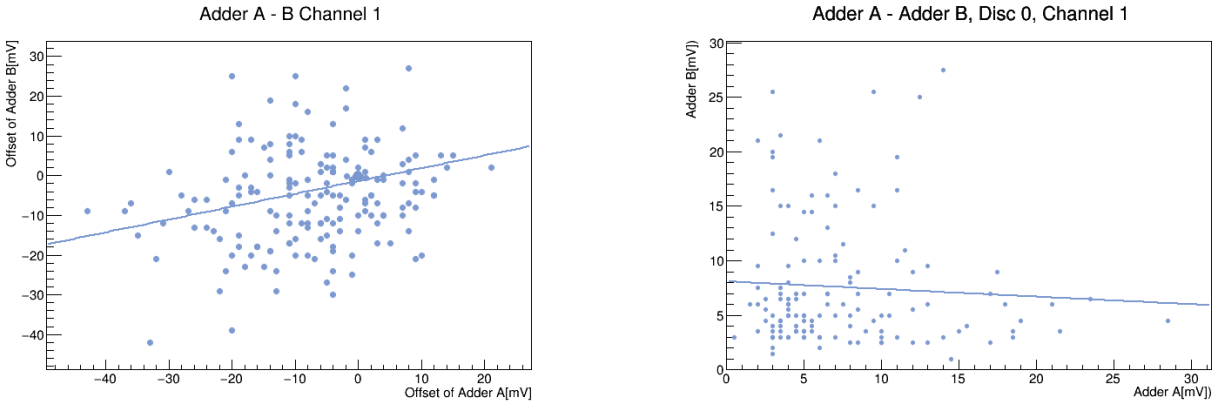

Figure 9: *Correlation plots for analog offset (left) and digital offset (right) between adders for fixed channel and discriminator in the case of digital offset. All possible combinations of adder pairs were plotted.*

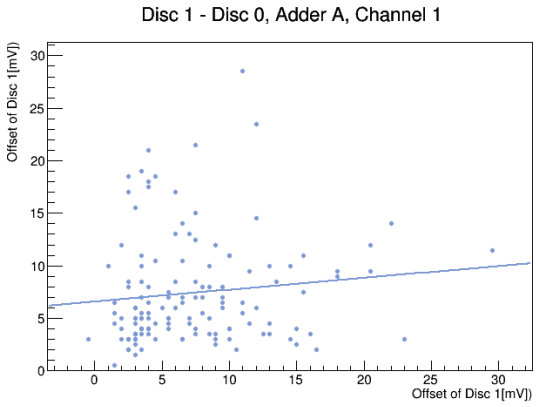

Figure 10: *Correlation plot for digital offset between discriminators for fixed adder and channel.*

3.3 Noise

The noise introduced in the ASIC signals has been measured thanks to the digital offset test of the quality control. Similar to the digital offset, only the adders which output status was tagged as “Pos” has measured values of noise. The rest of them were assigned a value of “0” and are excluded from the distribution analysis.

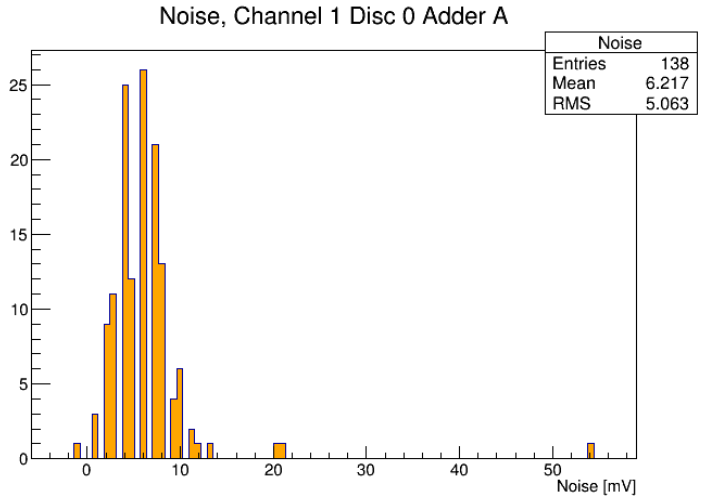

Figure 11: *Noise distribution for all ASICs in a certain combination of channel-adder-discriminator. All possible combinations were plotted, being similar to this one.*

The mean value of all the distributions of noise is 2,71 mV, with RMS of 5,24 mV.

Noise correlation in the different parts of the ASIC has laso been studied. In table 2 the resulting pearson correlation coefficients means are presented.

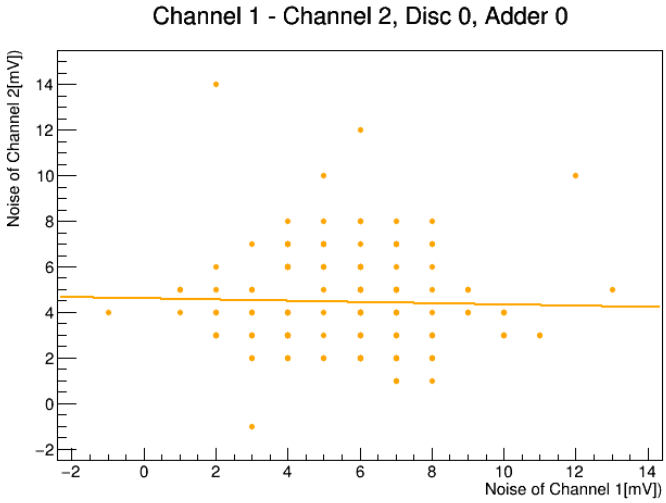

Figure 12: *Correlation plot for noise, between channels for fixed adder and discriminator. All possible combinations of channel pairs were plotted.*

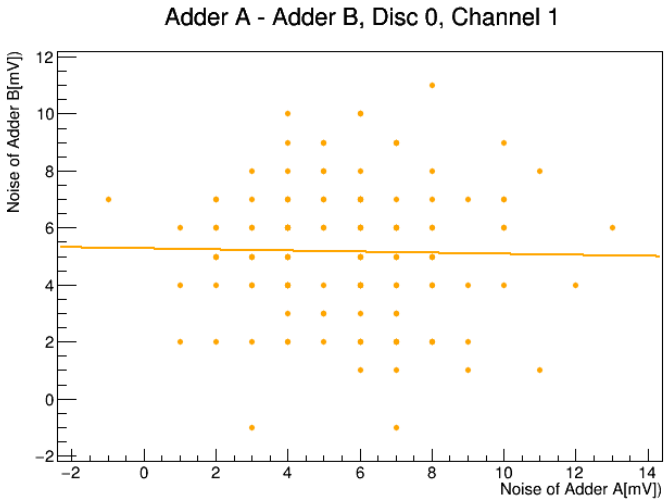

Figure 13: *Correlation plot for noise, between adders for fixed channel and discriminator. All possible combinations of adder pairs were plotted.*

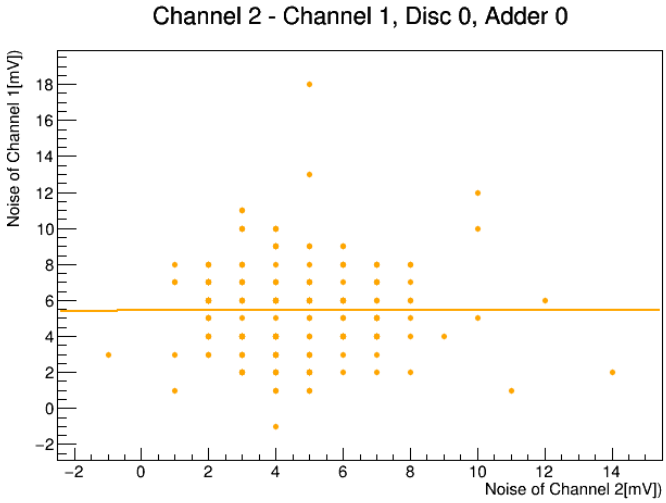

Figure 14: *Correlation plot for noise, between discriminators, for fixed adder and channel.*

	Corr. Factor Mean	**Corr. Factor RMS**	**Chi2 Mean**	**Chi2 RMS**	**NDF**
Analog Offset Ch-Ch	0.83787	0.0797831	9510.95	5298.51	387
Analog Offset Add-Add	0.402399	0.090969	26058.7	3447.51	387
Digital Off Ch-Ch	0.0402217	0.0977128	5662.46	1132.02	151.762
Digital Off Add-Add	0.0159922	0.090079	5694.98	1630.13	153.571
Digital Off Disc-Disc	0.152429	0.160245	5432.6	1560.36	151.762
Noise Ch-Ch	0.0210633	0.0885024	925.045	249.055	151.762
Noise Add-Add	-0.00218032	0.102373	845.033	205.65	153.571
Noise Disc-Disc	0.0471226	0.118144	917.351	209.484	151.762
Gain Ch-Ch	0.449329	0.144733	2.19479	8.43908	387
Gain Add-Add	0.438699	0.114398	2.05874	7.70398	387
Gain Disc-Disc	0.438699	0.114398	2.05874	7.70398	387
Fit Offset Ch-Ch	0.668336	0.192364	159124	556521	387
Fit Offset Add-Add	0.114982	0.0962141	189410	537969	387
Fit Offset Disc-Disc	0.760724	0.222289	144667	541227	387
Offsets diff. Ch-Ch	0.510537	0.147869	152528	594981	387
Offsets diff. Add-Add	0.410999	0.0861314	147804	557192	387
Offsets diff. Disc-Disc	0.568198	0.0779438	135010	520831	387

Table 2: *Mean value of the pearson correlation factor and Chi square for all the correlation plots done regarding the different features of the ASICs.*

4. Offset calculation from fitting the rate scan result.

As described in section 2, in the quality control test a rate scan of ten input pulses was performed in order to measure the gain of the ASICs. Plotting the input voltage versus the rate scan result voltage it can be observed that the relation is quite lineal, specially for low voltages under 500 mV (see *figure 15*).

We are going to assume a model where the input voltage is linearly related to the rate scan voltage through the expression:

(1) $V_{rs} = V_{in} * Gain + Offset.$

Where V_{rs} represents the voltage for the rate scan response, and V_{in} represent the input voltage. Therefore, if we control the input signal and measure the rate scan voltage, we will be able to obtain the offset without having to measure it directly in the ASIC.

In order to find a good fitting to calculate the offset, it is needed to find a range of input voltages where linearity is optimal.

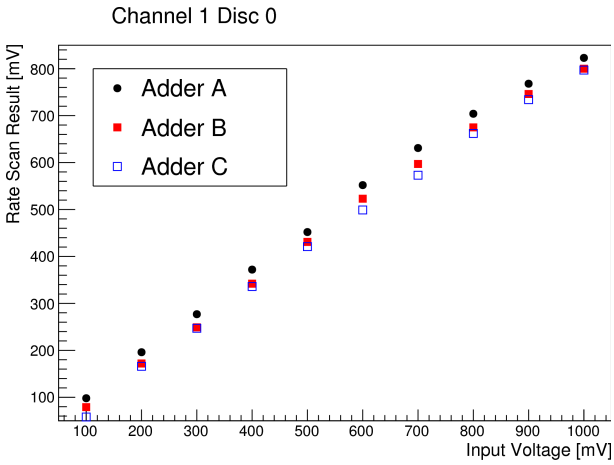

Figure 15: *Rate scan result from one of the voltage tests for ASIC #61. It can be observed a linear tendency which deteriorates at high voltages. Similar plots where obtained from the rest of channel-adder-discriminator combinatios.*

To do so, using data from one of the ASICs (#61), the offset obtained from the fit has been compared with the analog offset measured during the authomatic test.

We assume that the range with the best linearity would be the one where the difference between the offset from the fit and the analog offset measured directly in the test, is minimun.

In *figure 16* plots of the offsets for different ranges are presented where it can be observed the difference between fit and analog offset.

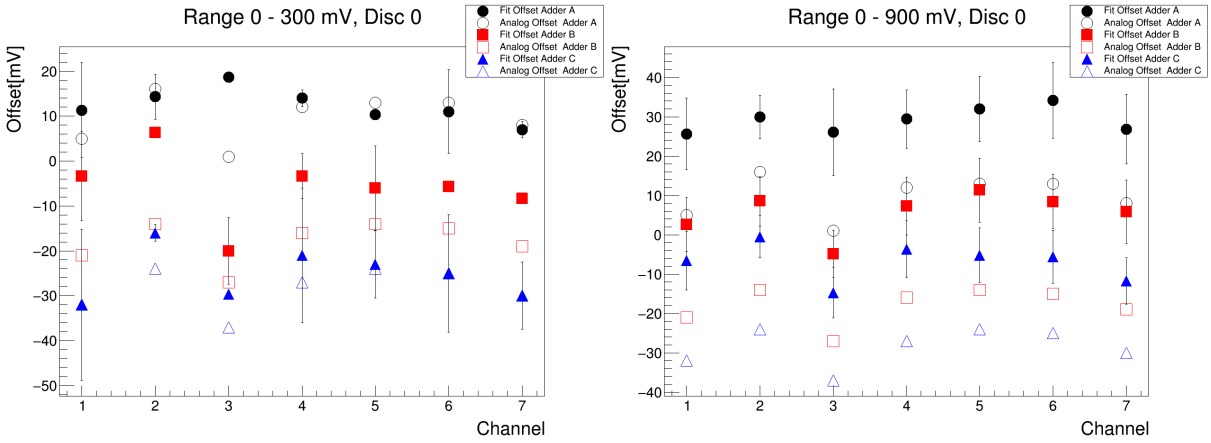

Figure 16: *Offset calculated from the fit(empty icons) and offset measured directly in the test for ASIC #61(filled icons). The difference in mV between them increases for ranges that include higher voltages, so we assume that the best linearity is reached at the minimun possible range, which is 0-300 mV.*

Ten different ranges were tested measuring the offsets differences, including intermediate ranges not starting from 0mV. Finally the range from 0 to 300 mV was selected as the one with better linearity and therefore the minimun difference.

Once selected the range, using the result of the fit, the offset (FO) for all the ASICs was computed, and also the difference of such offset with the analog offset(AO) was calculated and presented in distribution histograms.

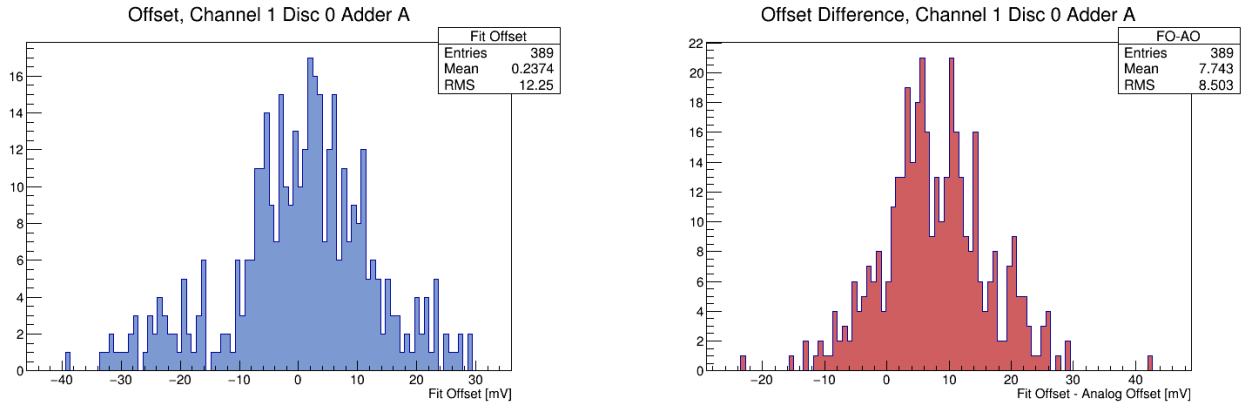

Figure 17: *Distribution of fit offsets (left) and offsets difference (right) for 389 ASICs in a certain combination of channel-adder-discriminator. Similar distributions were plotted for all combinations.*

From all the distributions,the mean of the FO-AO difference is of 5,55 mV with an RMS of ~8,71 mV. The mean of the FO is of -0,133 mV and the RMS is 13,75 mV.

To find if there is a relation between the offset and the offsets difference, for different channels, adders or discriminator, correlation plots were made.

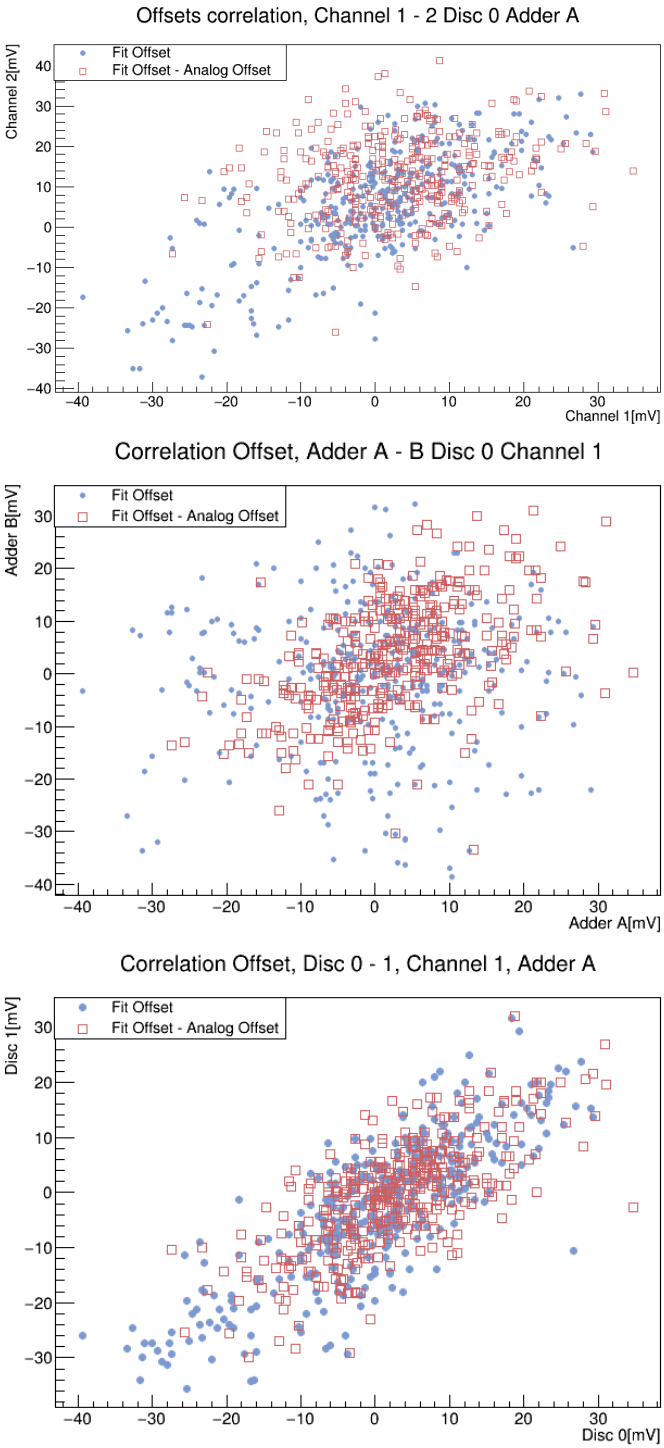

Figure 4: *Plots of correlations of the offset calculated from the fit of the rate scan(blue dots), together with the difference with the analog offset (red squares). On top is presented the correlation between two channels for fixed adder and discriminator. Middle plot is the correlation between two adders for fixed channel and discriminator. Bottom plot corresponds to the correlation between the two discriminators for fixed channel and adder. All possible combinations for correlations were plotted and the results are similar to these.*

The pearson correlation coefficients for these corerlation plots are presented in table 2.

5. Discussion and conclusions.

5.1 Gain.

Regarding the gain measured for the ASICs, in general it seems to have a very uniform value. In the case of the channels (2 and 3) that for all ASICs seem to have a deviation from the general mean, this effect is explanable by the differences in the way they are fed.

There are two ASICs where gain has a very low value, under 0,7, in several of their channels. This two ASICs probably should be discarted since signals coming into low gain channels could be supressed by the signals from the other channels and neglected in the final trigger response.

Relative to the correlation study, there is not a strong correlation for the gain in any part of the ASICs, having all of them a correlation coefficient under 0,5.
A curious effect observed in the correlation plots is that the gain seems to be quantized. This behaviour could arise due to the rate scan methodology.

5.2 Offset.

The analog offsets measured in the test have a negative mean value, while the digital offset, as the rate scan only can provide possitive offsets, gives a positive mean value.

In the correlation plots for the analog offset, it can be observed a positive correlation between channels , with correlation coefficients ~0,8 which means that for a high offset in one channel it is also high in all the rest, and therefore, the channels are not the part responsible for the offset. For the adders however, no correlation is observed in the plot, and the correlation coefficient is under 0.5 , concluding that the adders must be the elements that introduce the offset into the ASIC.

In the case of the digital offset, no correlation is observed at all, with coefficients very close to 0. It is needed to take into account that the data of digital offset is biased by the rate scan conditions.

5.3 Noise

The mean value measured for the noise fits into the 0,2 phe noise described in the ASICs requierements. Again the distribution of noises is biased because of the rate scan.

No correlation is observed for the noise in any part of the ASIC, it seesm to be introduced everywhere. Similar to the gain plots, quantization of the noise values is observed, that again could arise due to the rate scan.

5.4 Offset calculated from fitting the rate scan.

The model assumed to calculate the offset directly from the rate scan result has given values of offsets that differ from the analog offset directly measured in the ASIC in ~ 5 mV with RMS of ~9. Taking into account that 1 phe corresponds to 10 mV, the error commited when calculating the offset by this method would be mostly of the order of 1 phe.

Regarding the correlation studied, again is confirmed that are the adders the responsible for introducing an offset in the ASICs and not the channels nor the discriminators.