Analog trigger L1 ASIC Package and Pin out

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List of Abbreviations			

History		
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Distribution	

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1 Introduction

This document contains a preliminary description of the second version of the Analog Trigger L1 ASIC (CTA_L1_R2).

The ASIC has been sent to manufacture on 10th of June of 2014 and is packaged in a QFN48 package.

The second version of the analog trigger L1 ASIC has 7 differential analog inputs and 2 differential LVDS digital outputs. It is controlled by a serial link that controls the DACs values for the discriminators thresholds, the switches to enable the inputs and other internal configurations. It has different input/output test pins to test the ASIC properly.

Fig. 1 shows a basic block diagram of the ASIC. The two basic functionalities of the circuit are the calculation of the analog sum of the input channels and the discrimination of the resulting voltage in order to generate digital L1 LVDS outputs. All the analog circuits in the ASIC have been designed following a fully differential approach, from input pins to discriminator inputs.

The ASIC comprises three independent fully differential 7-input analog adders. All input channels are replicated three times and connected to one input of each analog adder through a low impedance differential switch. Thus, there are 21 switches, which are controllable in an independent way by the slow control circuit. This symmetric architecture provides high flexibility for defining different trigger modes and ensures all input channels are processed in the same way inside the ASIC in order to minimize differences from channel to channel. The overall gain of the analog circuit is near to 1 and the linear range of the adder and any of its inputs is around 1.2V. Therefore, the ASIC is able to process signals up to 120phe assuming a gain of 10mV/phe in the previous stage in the trigger chain (i.e. L0 circuits plus L0 fanout). The bandwidth of the analog circuit chain, that is, input buffers, switches and adders, has been designed to be greater than 500MHz. All circuits in the analog stage have been designed specifically for this application.

The output of the three adders are connected to two group of discriminators (two groups of 3 discriminators [x6]), with independent threshold definition each discriminator, in order to generate a High Level Threshold Trigger (HLTH) output and a Low Level Threshold Trigger (LLTH) output. Threshold voltages are generated by six independent differential DACs of 9 bits of resolution, which are controllable by slow control. Each DAC is composed by 2 DAC's (One for the positive part P and another for the negative part N) of 9 bits in a common mode of 1,4V to a proper working condition of the Discriminator. The DAC P range is from 1,4V to 2V and the DAC N range is from 0,8V to 1,4V. The Output threshold of the DAC is the difference between the DAC P and DAC N. It can get the maximum range of 1,2V with the maximum value of DAC P (2V) and the minimum value of DAC N (0,8V). Contrarily with the minimum value of DAC P (1,4V) and the maximum value of DAC N (1,4V) it obtained the minimum output threshold of 0V. The outputs of the discriminators are combined in two OR gates and then send to LVDS transmitters, which provide the digital trigger outputs of the ASIC.

The slow control circuit is based in a serial link that uses CMOS electrical standard. It comprises a set of seven 16-bit registers (96 to 102) that can be written and read by the serial link. The registers contain the data used to control the input stage switches, the DAC used to

define the bias current of the differential pairs in the ASIC, the DACs for trigger threshold generation, the multiplexor to select the adder analog output test point, the enable of the buffer of the adder analog output test point and the enable of LVDS transmitters. The power supply is 3.3 V (Analog VDDA and digital VDDD).

2 Functional Block Diagram

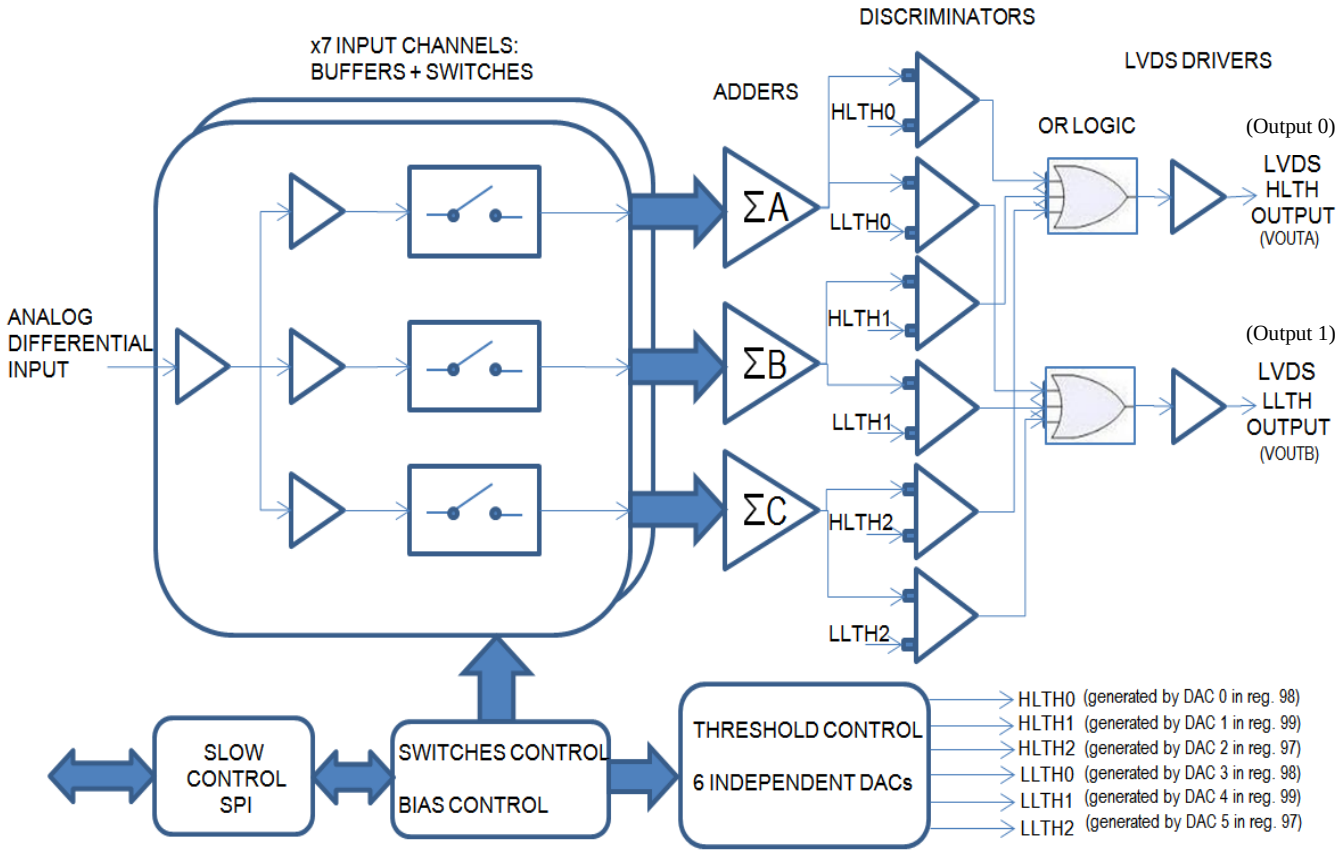

Fig. 1 – Block diagram of L1 ASIC

3 L1 ASIC Pin Configuration

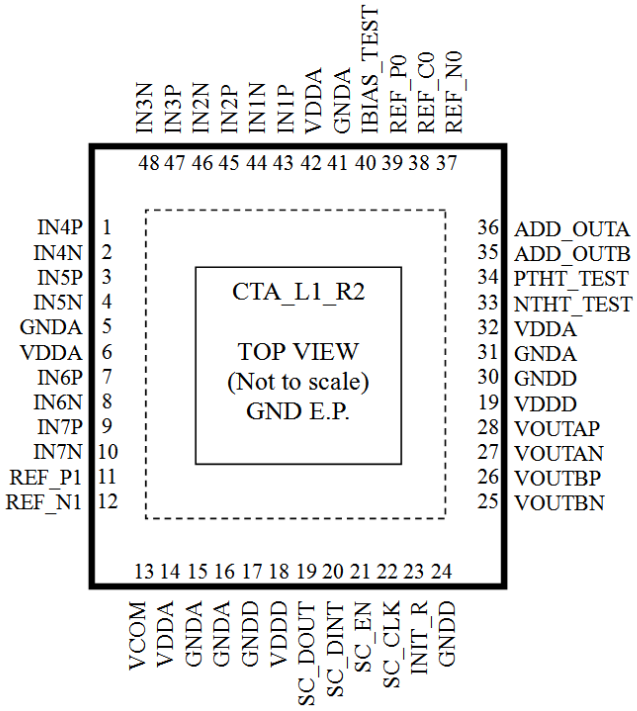

Fig. 2 – L1 ASIC pinout diagram

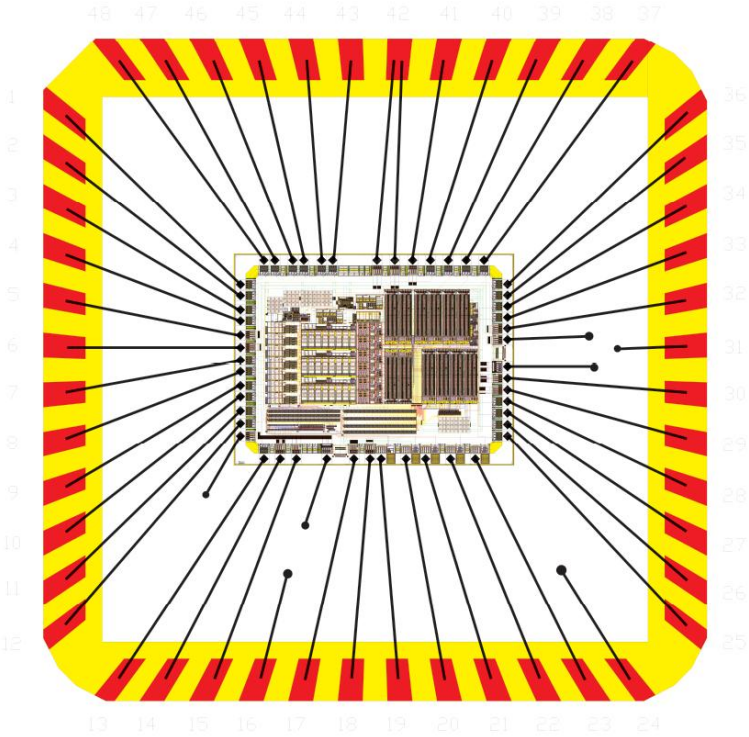

Fig. 3 – L1 ASIC bonding diagram

4 L1 ASIC pin out table

PIN NAME	PIN NUMBER	SIGNAL DESCRIPTION
IN4P	1	Positive Input Voltage
IN4N	2	Negative Input Voltage
IN5P	3	Positive Input Voltage
IN5N	4	Negative Input Voltage
GNDA	5	Analog GND
VDDA	6	Analog VDD
IN6P	7	Positive Input Voltage
IN6N	8	Negative Input Voltage
IN7P	9	Positive Input Voltage
IN7N	10	Negative Input Voltage
REF_P1	11	Voltage Input/output test signal to references of DAC
REF_N1	12	Voltage Input/output test signal to references of DAC
VCOM	13	Input/Output Reference signal test
VDDA	14	Analog VDD
GNDA	15	Analog GND
GNDA	16	Analog GND
GNDD	17	Digital GND
VDDD	18	Digital VDD
SC_DOUT	19	Digital Output data
SC_DINT	20	Digital input data
SC_EN	21	Digital input enable
SC_CLK	22	Digital input clock
INIT_R	23	Digital input reset
GNDD	24	Digital GND
VOUTBN	25	LVDS Negative Voltage Output
VOUTBP	26	LVDS Positive Voltage Output
VOUTAN	27	LVDS Negative Voltage Output
VOUTAP	28	LVDS Positive Voltage Output
VDDD	29	Digital VDD
GNDD	30	Digital GND
GNDA	31	Analog GND
VDDA	32	Analog VDD
NTHT_TEST	33	Voltage Input/output test signal of Threshold from DAC to DISC
PTHT_TEST	34	Voltage Input/output test signal of Threshold from DAC to DISC
ADD_OUTB	35	Voltage Output test signal from ADDER output
ADD_OUTA	36	Voltage Output test signal from ADDER output
REF_N0	37	Voltage Input/output test signal to references of DAC
REF_C0	38	Voltage Input/output test signal to references of DAC
REF_P0	39	Voltage Input/output test signal to references of DAC
IBIAS_TEST	40	Voltage Input/output test signal from drain of current mirror
GNDA	41	Analog GND
VDDA	42	Analog VDD
IN1P	43	Positive Input Voltage
IN1N	44	Negative Input Voltage
IN2P	45	Positive Input Voltage
IN2N	46	Negative Input Voltage
IN3P	47	Positive Input Voltage
IN3N	48	Negative Input Voltage

Table 1- Analog Trigger L1 ASIC PINOUT Table

5 L1 ASIC OUTLINE DIMENSIONS

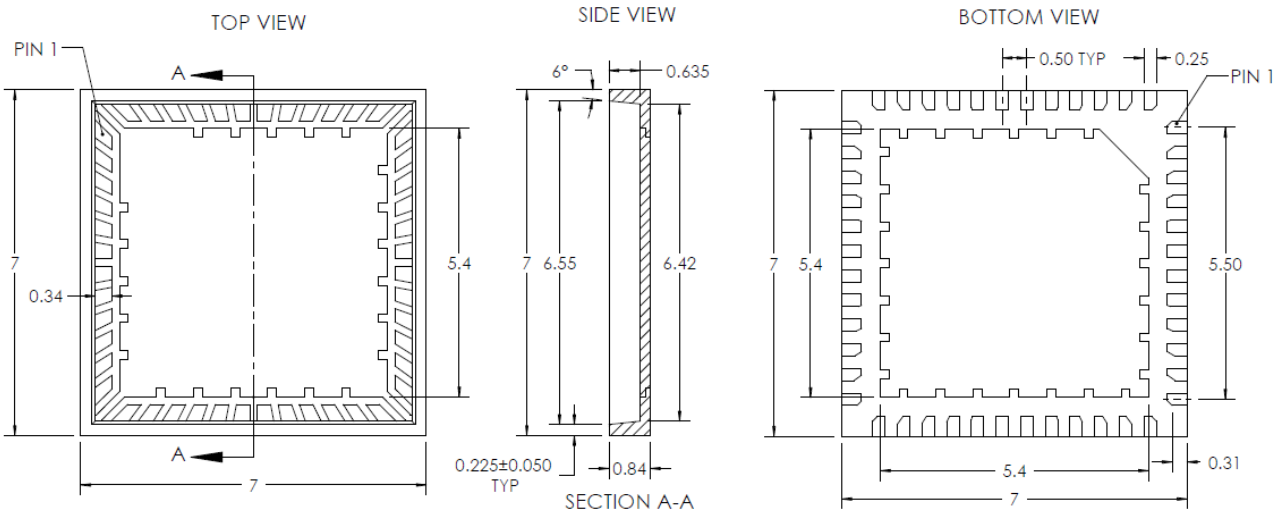

Fig. 4 - QFN48 outline dimensions

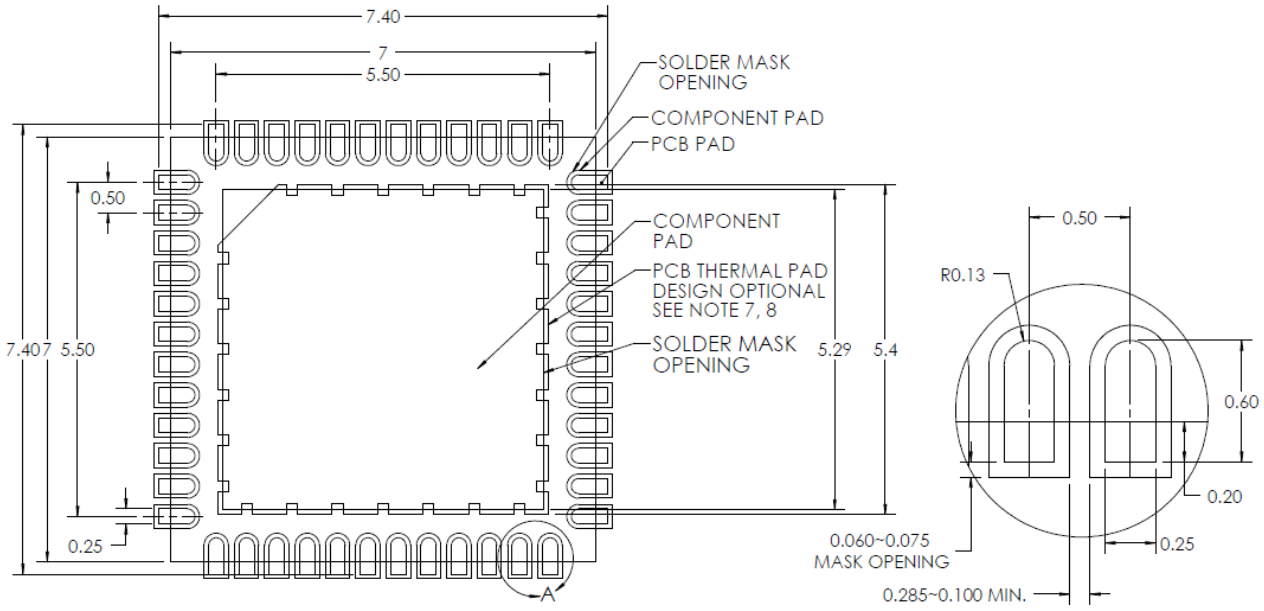

Fig. 5 - Recommended PCB footprint for QFN48 package

6 L1 ASIC SLOW CONTROL MAP

The Slow Control of analog trigger level 1ASIC is based in a serial link interface controlled by a master (typically an FPGA), where the ASIC act as slave. The electrical standard is 3.3V LVCMOS.

6.1 Control signals from/to the front-end FPGA

The serial link consists of the following signals:

- SC_EN: master output enable (active high)
- SC_CLK: master output clock
- SC_DIN: master output data (data input ASIC)
- SC_DOUT: master input data (data output from ASIC)

The maximum speed for clock is still not specified. A reasonable value for operation is around 1MHz. In Figs. 5, 6, 7 and 8, several chronogram examples are shown. Notice the extra clock cycles before and after the enable window, they are required for the logic to work properly.

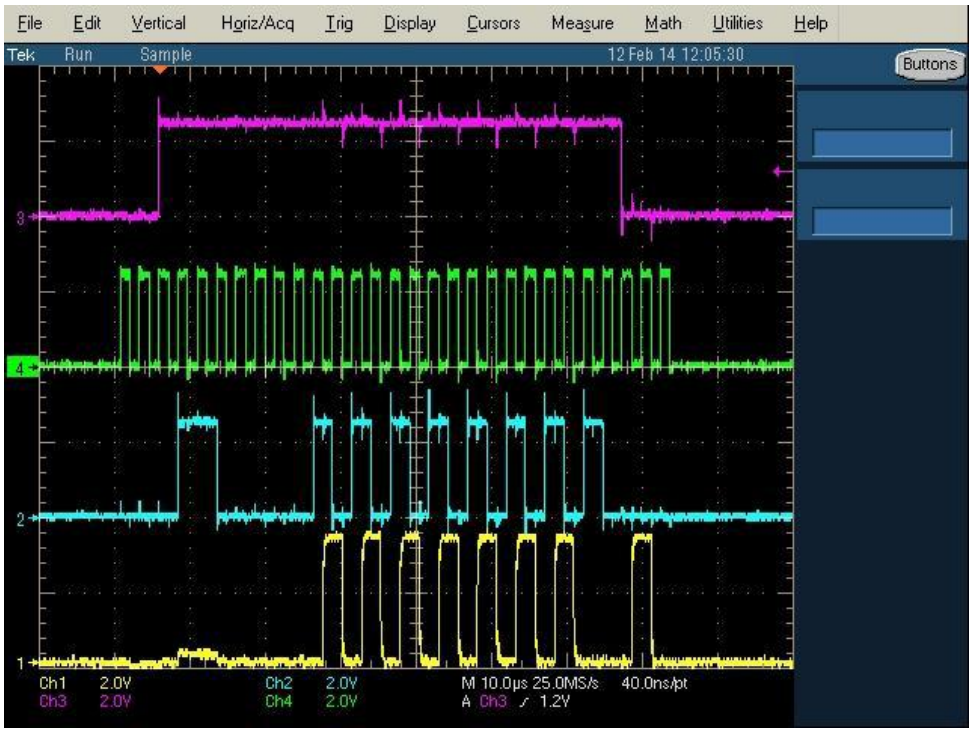

Fig. 6 - Writing sequence of 0xAAAA data into register number 0x60 (d96).
CH3 SC_EN, CH4 SC_CLK, CH2 SC_DIN, CH1 SC_DOUT

Fig. 7 _ Reading sequence of 0xAAAA data from register number 0x60 (d96).
CH3 SC_EN, CH4 SC_CLK, CH2 SC_DIN, CH1 SC_DOUT

Fig. 8 _ Writing sequence of 0x00AA data to register number 0x64(d100).
CH3 SC_EN, CH4 SC_CLK, CH2 SC_DIN, CH1 SC_DOUT

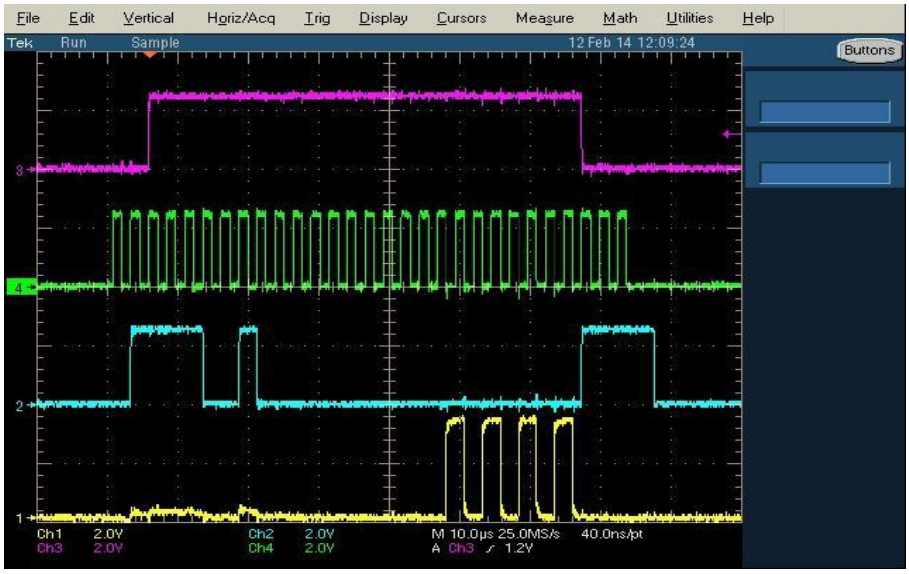

Fig. 9 - Reading sequence of 0x00AA data from register number 0x64(d100). CH3 SC_EN, CH4 SC_CLK, CH2 SC_DIN, CH1 SC_DOUT

In addition, there is a reset line (INIT_R), active high. When the reset is activated, the internal registers are initialized to the default values shown in next section. After power-up, the content of the registers are unknown, so, a reset is recommended before operation, in order to set the ASIC into a known status.

6.2 Register map

There are 7 registers with addresses numbered from 96 to 102. Registers from 96 to 99 are devoted to store the threshold code for the six DACs. In order to save number of registers, and therefore ASIC area, the negative part (DAC N) of the code is generated automatically in the ASIC from the positive part, just inverting all the bits of the positive part of the DAC P, therefore only the positive part of the DAC P is stored in the register. Additionally, from the 9 bits of the 6 DAC's, 8 MSB of all of them are combined in three 16-bit registers (97, 98 and 99), and all LSBs are combined in another 16-bit register (96). Register 99 stores the positive thresholds codes for DAC1 and DAC4 (threshold of the discriminators from adder B). Register 98 stores the positive thresholds codes for DAC0 and DAC3 (threshold of the discriminators from adder A). Register 97 stores the positive thresholds codes for DAC2 and DAC5 (threshold of the discriminators from adder C).

To set the minimum value of the DAC (a threshold of 0V), is just to set the 8 MSB code for the minimum value of DAC P (1,4V) to 0 (00x in hexadecimal), and automatically is set the maximum value of DAC N (1,4V). Contrarily, to set the maximum value of the DAC (a threshold of 1,2V), it is necessary to set the maximum value of DAC P (2V), and automatically is set the minimum value of DAC N (0,8V), with "1" in the 8 MSB code (FFx in hexadecimal) in the right register.

The register 96 stores the negative and positive LSB of the 6 DACs and the bits to enable the output of the multiplexor to check the thresholds. In the Annex of this datasheet there are a table with all possible values of the DAC's. In the first column there is the value in hexadecimal in green, then the 8 MSB of this hexadecimal value, followed by the voltage in DAC N and DAC P of this code. In red there is the voltage threshold in the DAC's output for this code and finally there are the voltages of the output according to the LSB of the register 96 of each DAC, than can be 00, 01, 10 or 11. The default value is 49x, that corresponds a voltage of 1,22V in DAC N, 1,57V in DAC P and a output of 350mV that can be tested in the test point pin of the ASIC of the DAC's multiplexor.

Registers 100 and 101 are used to store the switches enables values. These switches are used to connect input channels with the adders. The enable value "0"of a particular switch means that the channel input signal participate in the corresponding adder. Register 101 is also used to store enables for LVDS transmitter's outputs, the bit to enable the analog test point of the multiplexor of the adder's outputs and the enable of the analog buffer in this output after the multiplexor.

Finally the register 102 is used to store the code for the Ibias DAC. The code is in inverted logic, that is, code b"111111" provides minimum Ibias current.

SLOW CONTROL MAP ASIC CTA_L1_R2

				1AAA
Reg address 96	**DAC_TH_LSBs_MUX**			
Bit 0	DAC_TH0_P0		0	A
Bit 1	DAC_TH0_N0		1	
Bit 2	DAC_TH1_P0		0	
Bit 3	DAC_TH1_N0		1	
Bit 4	DAC_TH2_P0		0	A
Bit 5	DAC_TH2_N0		1	
Bit 6	DAC_TH3_P0		0	
Bit 7	DAC_TH3_N0		1	
Bit 8	DAC_TH4_P0		0	A
Bit 9	DAC_TH4_N0		1	
Bit 10	DAC_TH5_P0		0	
Bit 11	DAC_TH5_N0		1	
Bit 12	DAC_MUX_ENA0		1	1
Bit 13	DAC_MUX_ENA1		0	
Bit 14	DAC_MUX_ENA2		0	
Bit 15	Reserved	Unused	0	

DAC_MUX ENA 2, 1, 0	DAC	Adder + Output of this DAC's threshold
001	0	Adder A – Output 0 (reg 98)
010	1	Adder B – Output 0 (reg 99)
011	2	Adder C – Output 0 (reg 97)
100	3	Adder A – Output 1 (reg 98)
101	4	Adder B – Output 1 (reg 99)
110	5	Adder C – Output 1 (reg 97)

				4949
Reg address 97	**DAC_TH5/2_P**			
Bit 0	DAC_TH5_P1		1	9
Bit 1	DAC_TH5_P2		0	
Bit 2	DAC_TH5_P3		0	
Bit 3	DAC_TH5_P4		1	
Bit 4	DAC_TH5_P5		0	4
Bit 5	DAC_TH5_P6		0	
Bit 6	DAC_TH5_P7		1	
Bit 7	DAC_TH5_P8		0	
Bit 8	DAC_TH2_P1		1	9
Bit 9	DAC_TH2_P2		0	
Bit 10	DAC_TH2_P3		0	
Bit 11	DAC_TH2_P4		1	
Bit 12	DAC_TH2_P5		0	4
Bit 13	DAC_TH2_P6		0	
Bit 14	DAC_TH2_P7		1	
Bit 15	DAC_TH2_P8		0	

				4949
Reg address 98	**DAC_TH3/0_P**			**HEXA**
Bit 0	DAC_TH3_P1		1	9
Bit 1	DAC_TH3_P2		0	
Bit 2	DAC_TH3_P3		0	
Bit 3	DAC_TH3_P4		1	
Bit 4	DAC_TH3_P5		0	4
Bit 5	DAC_TH3_P6		0	
Bit 6	DAC_TH3_P7		1	
Bit 7	DAC_TH3_P8		0	
Bit 8	DAC_TH0_P1		1	9
Bit 9	DAC_TH0_P2		0	
Bit 10	DAC_TH0_P3		0	
Bit 11	DAC_TH0_P4		1	
Bit 12	DAC_TH0_P5		0	4
Bit 13	DAC_TH0_P6		0	
Bit 14	DAC_TH0_P7		1	
Bit 15	DAC_TH0_P8		0	

				4949
Reg address 99	**DAC_TH4/1_P**			**HEXA**
Bit 0	DAC_TH4_P1		1	9
Bit 1	DAC_TH4_P2		0	
Bit 2	DAC_TH4_P3		0	
Bit 3	DAC_TH4_P4		1	
Bit 4	DAC_TH4_P5		0	4
Bit 5	DAC_TH4_P6		0	
Bit 6	DAC_TH4_P7		1	
Bit 7	DAC_TH4_P8		0	
Bit 8	DAC_TH1_P1		1	9
Bit 9	DAC_TH1_P2		0	
Bit 10	DAC_TH1_P3		0	
Bit 11	DAC_TH1_P4		1	
Bit 12	DAC_TH1_P5		0	4
Bit 13	DAC_TH1_P6		0	
Bit 14	DAC_TH1_P7		1	
Bit 15	DAC_TH1_P8		0	

Slow Control Map. Switches are enabling with 0, these means that participate in the adder.

				7770
Reg address 100	**SW_ENA0**			**HEXA**
Bit 0	IN0_adderA		0	0
Bit 1	IN0_adderB		0	
Bit 2	IN0_adderC		0	
Bit 3	IN1_adderA		0	
Bit 4	IN1_adderB		1	7
Bit 5	IN1_adderC		1	
Bit 6	IN2_adderA		1	
Bit 7	IN2_adderB		0	
Bit 8	IN2_adderC		1	7
Bit 9	IN3_adderA		1	
Bit 10	IN3_adderB		1	
Bit 11	IN3_adderC		0	
Bit 12	IN4_adderA		1	7
Bit 13	IN4_adderB		1	
Bit 14	IN4_adderC		1	
Bit 15	Reserved	Unused	0	

				017F
Reg address 101	**SW_ENA1**			**HEXA**
Bit 0	IN5_adderA		1	F
Bit 1	IN5_adderB		1	
Bit 2	IN5_adderC		1	
Bit 3	IN6_adderA		1	
Bit 4	IN6_adderB		1	7
Bit 5	IN6_adderC		1	
Bit 6	MUX_ENA0		1	
Bit 7	MUX_ENA1		0	
Bit 8	LVDS_ENA0		1	1
Bit 9	LVDS_ENA1		0	
Bit 10	BUFF_ENA		0	
Bit 11	Reserved	Unused	0	0
Bit 12	Reserved	Unused	0	
Bit 13	Reserved	Unused	0	
Bit 14	Reserved	Unused	0	
Bit 15	Reserved	Unused	0	

MUX_ENA 1, 0	Adder in the Output
00	-
01	A
10	B
11	C

DAC Ibias Code is in inverted logic

				3400
Reg address 102	**DAC_IB**			**HEXA**
Bit 0	Reserved	Unused	0	0
Bit 1	Reserved	Unused	0	
Bit 2	Reserved	Unused	0	
Bit 3	Reserved	Unused	0	
Bit 4	Reserved	Unused	0	0
Bit 5	Reserved	Unused	0	
Bit 6	Reserved	Unused	0	
Bit 7	Reserved	Unused	0	
Bit 8	Reserved	Unused	0	4
Bit 9	Reserved	Unused	0	
Bit 10	DAC_IB0		1	
Bit 11	DAC_IB1		0	
Bit 12	DAC_IB2		1	3
Bit 13	DAC_IB3		1	
Bit 14	DAC_IB4		0	
Bit 15	DAC_IB5		0	

7 SEQUENCES TO START

First of all it is recommended a reset in order to initialize the internal registers to the default values after the power-up and before operations.

Then, with a know status, it can select the switches with the 100 and 101 registers, remembering that a “0” of a particular bit enable the connection of the input channel with the adder in order to this channel participate in the corresponding adder.

For example, to enable just the channel 0 in the adder A in both LVDS output and disabling the multiplexor and the buffer of the analog output, the code needed is:

Register 100: FFFEx

Register 101: 033Fx

Next registers to set is 97, 98 and 99 to modify the value of the DAC depending of the adder and output used. The 96 register it is not necessary to modify with the default values. It is important to remember that if we want that some adder don’t participate in the summing, the corresponding registers has to be in the maximum threshold (FFx)

For example to set a 100mV threshold in just adder A and the output A:

Register 98: 15FFx

Registers 97 and 99: FFFFx

The register 102 it is not necessary to modify because de default value of the Ibias DAC it is OK.

8 ANNEX

	1	2	4	8	16	32	64	128		1,2mV	VoD (mV)	PN	PN
HEXA	<1>	<2>	<3>	<4>	<5>	<6>	<7>	<8>	VoN (V)	VoP (V)	01	00/11	10
00	0	0	0	0	0	0	0	0	1,4	1,4	0,0	1,2	2,4
01	1	0	0	0	0	0	0	0	1,3976	1,4024	4,8	6,0	7,2
02	0	1	0	0	0	0	0	0	1,3952	1,4048	9,6	10,8	12,0
03	1	1	0	0	0	0	0	0	1,3928	1,4072	14,4	15,6	16,8
04	0	0	1	0	0	0	0	0	1,3904	1,4096	19,2	20,4	21,6
05	1	0	1	0	0	0	0	0	1,388	1,412	24,0	25,2	26,4
06	0	1	1	0	0	0	0	0	1,3856	1,4144	28,8	30,0	31,2
07	1	1	1	0	0	0	0	0	1,3832	1,4168	33,6	34,8	36,0
08	0	0	0	1	0	0	0	0	1,3808	1,4192	38,4	39,6	40,8
09	1	0	0	1	0	0	0	0	1,3784	1,4216	43,2	44,4	45,6
0A	0	1	0	1	0	0	0	0	1,376	1,424	48,0	49,2	50,4
0B	1	1	0	1	0	0	0	0	1,3736	1,4264	52,8	54,0	55,2
0C	0	0	1	1	0	0	0	0	1,3712	1,4288	57,6	58,8	60,0
0D	1	0	1	1	0	0	0	0	1,3688	1,4312	62,4	63,6	64,8
0E	0	1	1	1	0	0	0	0	1,3664	1,4336	67,2	68,4	69,6
0F	1	1	1	1	0	0	0	0	1,364	1,436	72,0	73,2	74,4
10	0	0	0	0	1	0	0	0	1,3616	1,4384	76,8	78,0	79,2
11	1	0	0	0	1	0	0	0	1,3592	1,4408	81,6	82,8	84,0
12	0	1	0	0	1	0	0	0	1,3568	1,4432	86,4	87,6	88,8
13	1	1	0	0	1	0	0	0	1,3544	1,4456	91,2	92,4	93,6
14	0	0	1	0	1	0	0	0	1,352	1,448	96,0	97,2	98,4
15	1	0	1	0	1	0	0	0	1,3496	1,4504	100,8	102,0	103,2
16	0	1	1	0	1	0	0	0	1,3472	1,4528	105,6	106,8	108,0
17	1	1	1	0	1	0	0	0	1,3448	1,4552	110,4	111,6	112,8
18	0	0	0	1	1	0	0	0	1,3424	1,4576	115,2	116,4	117,6
19	1	0	0	1	1	0	0	0	1,34	1,46	120,0	121,2	122,4
1A	0	1	0	1	1	0	0	0	1,3376	1,4624	124,8	126,0	127,2
1B	1	1	0	1	1	0	0	0	1,3352	1,4648	129,6	130,8	132,0
1C	0	0	1	1	1	0	0	0	1,3328	1,4672	134,4	135,6	136,8
1D	1	0	1	1	1	0	0	0	1,3304	1,4696	139,2	140,4	141,6
1E	0	1	1	1	1	0	0	0	1,328	1,472	144,0	145,2	146,4
1F	1	1	1	1	1	0	0	0	1,3256	1,4744	148,8	150,0	151,2
20	0	0	0	0	0	1	0	0	1,3232	1,4768	153,6	154,8	156,0
21	1	0	0	0	0	1	0	0	1,3208	1,4792	158,4	159,6	160,8
22	0	1	0	0	0	1	0	0	1,3184	1,4816	163,2	164,4	165,6
23	1	1	0	0	0	1	0	0	1,316	1,484	168,0	169,2	170,4
24	0	0	1	0	0	1	0	0	1,3136	1,4864	172,8	174,0	175,2
25	1	0	1	0	0	1	0	0	1,3112	1,4888	177,6	178,8	180,0
26	0	1	1	0	0	1	0	0	1,3088	1,4912	182,4	183,6	184,8
27	1	1	1	0	0	1	0	0	1,3064	1,4936	187,2	188,4	189,6
28	0	0	0	1	0	1	0	0	1,304	1,496	192,0	193,2	194,4
29	1	0	0	1	0	1	0	0	1,3016	1,4984	196,8	198,0	199,2
2A	0	1	0	1	0	1	0	0	1,2992	1,5008	201,6	202,8	204,0
2B	1	1	0	1	0	1	0	0	1,2968	1,5032	206,4	207,6	208,8
2C	0	0	1	1	0	1	0	0	1,2944	1,5056	211,2	212,4	213,6
2D	1	0	1	1	0	1	0	0	1,292	1,508	216,0	217,2	218,4
2E	0	1	1	1	0	1	0	0	1,2896	1,5104	220,8	222,0	223,2
2F	1	1	1	1	0	1	0	0	1,2872	1,5128	225,6	226,8	228,0
30	0	0	0	0	1	1	0	0	1,2848	1,5152	230,4	231,6	232,8
31	1	0	0	0	1	1	0	0	1,2824	1,5176	235,2	236,4	237,6
32	0	1	0	0	1	1	0	0	1,28	1,52	240,0	241,2	242,4

33	1	1	0	0	1	1	0	0	1,2776	1,5224	244,8	246,0	247,2
34	0	0	1	0	1	1	0	0	1,2752	1,5248	249,6	250,8	252,0
35	1	0	1	0	1	1	0	0	1,2728	1,5272	254,4	255,6	256,8
36	0	1	1	0	1	1	0	0	1,2704	1,5296	259,2	260,4	261,6
37	1	1	1	0	1	1	0	0	1,268	1,532	264,0	265,2	266,4
38	0	0	0	1	1	1	0	0	1,2656	1,5344	268,8	270,0	271,2
39	1	0	0	1	1	1	0	0	1,2632	1,5368	273,6	274,8	276,0
3A	0	1	0	1	1	1	0	0	1,2608	1,5392	278,4	279,6	280,8
3B	1	1	0	1	1	1	0	0	1,2584	1,5416	283,2	284,4	285,6
3C	0	0	1	1	1	1	0	0	1,256	1,544	288,0	289,2	290,4
3D	1	0	1	1	1	1	0	0	1,2536	1,5464	292,8	294,0	295,2
3E	0	1	1	1	1	1	0	0	1,2512	1,5488	297,6	298,8	300,0
3F	1	1	1	1	1	1	0	0	1,2488	1,5512	302,4	303,6	304,8
40	0	0	0	0	0	0	1	0	1,2464	1,5536	307,2	308,4	309,6
41	1	0	0	0	0	0	1	0	1,244	1,556	312,0	313,2	314,4
42	0	1	0	0	0	0	1	0	1,2416	1,5584	316,8	318,0	319,2
43	1	1	0	0	0	0	1	0	1,2392	1,5608	321,6	322,8	324,0
44	0	0	1	0	0	0	1	0	1,2368	1,5632	326,4	327,6	328,8
45	1	0	1	0	0	0	1	0	1,2344	1,5656	331,2	332,4	333,6
46	0	1	1	0	0	0	1	0	1,232	1,568	336,0	337,2	338,4
47	1	1	1	0	0	0	1	0	1,2296	1,5704	340,8	342,0	343,2
48	0	0	0	1	0	0	1	0	1,2272	1,5728	345,6	346,8	348,0
49	1	0	0	1	0	0	1	0	1,2248	1,5752	350,4	351,6	352,8
4A	0	1	0	1	0	0	1	0	1,2224	1,5776	355,2	356,4	357,6
4B	1	1	0	1	0	0	1	0	1,22	1,58	360,0	361,2	362,4
4C	0	0	1	1	0	0	1	0	1,2176	1,5824	364,8	366,0	367,2
4D	1	0	1	1	0	0	1	0	1,2152	1,5848	369,6	370,8	372,0
4E	0	1	1	1	0	0	1	0	1,2128	1,5872	374,4	375,6	376,8
4F	1	1	1	1	0	0	1	0	1,2104	1,5896	379,2	380,4	381,6
50	0	0	0	0	1	0	1	0	1,208	1,592	384,0	385,2	386,4
51	1	0	0	0	1	0	1	0	1,2056	1,5944	388,8	390,0	391,2
52	0	1	0	0	1	0	1	0	1,2032	1,5968	393,6	394,8	396,0
53	1	1	0	0	1	0	1	0	1,2008	1,5992	398,4	399,6	400,8
54	0	0	1	0	1	0	1	0	1,1984	1,6016	403,2	404,4	405,6
55	1	0	1	0	1	0	1	0	1,196	1,604	408,0	409,2	410,4
56	0	1	1	0	1	0	1	0	1,1936	1,6064	412,8	414,0	415,2
57	1	1	1	0	1	0	1	0	1,1912	1,6088	417,6	418,8	420,0
58	0	0	0	1	1	0	1	0	1,1888	1,6112	422,4	423,6	424,8
59	1	0	0	1	1	0	1	0	1,1864	1,6136	427,2	428,4	429,6
5A	0	1	0	1	1	0	1	0	1,184	1,616	432,0	433,2	434,4
5B	1	1	0	1	1	0	1	0	1,1816	1,6184	436,8	438,0	439,2
5C	0	0	1	1	1	0	1	0	1,1792	1,6208	441,6	442,8	444,0
5D	1	0	1	1	1	0	1	0	1,1768	1,6232	446,4	447,6	448,8
5E	0	1	1	1	1	0	1	0	1,1744	1,6256	451,2	452,4	453,6
5F	1	1	1	1	1	0	1	0	1,172	1,628	456,0	457,2	458,4
60	0	0	0	0	0	1	1	0	1,1696	1,6304	460,8	462,0	463,2
61	1	0	0	0	0	1	1	0	1,1672	1,6328	465,6	466,8	468,0
62	0	1	0	0	0	1	1	0	1,1648	1,6352	470,4	471,6	472,8
63	1	1	0	0	0	1	1	0	1,1624	1,6376	475,2	476,4	477,6
64	0	0	1	0	0	1	1	0	1,16	1,64	480,0	481,2	482,4
65	1	0	1	0	0	1	1	0	1,1576	1,6424	484,8	486,0	487,2
66	0	1	1	0	0	1	1	0	1,1552	1,6448	489,6	490,8	492,0
67	1	1	1	0	0	1	1	0	1,1528	1,6472	494,4	495,6	496,8

68	0	0	0	1	0	1	1	0	1,1504	1,6496	499,2	500,4	501,6
69	1	0	0	1	0	1	1	0	1,148	1,652	504,0	505,2	506,4
6A	0	1	0	1	0	1	1	0	1,1456	1,6544	508,8	510,0	511,2
6B	1	1	0	1	0	1	1	0	1,1432	1,6568	513,6	514,8	516,0
6C	0	0	1	1	0	1	1	0	1,1408	1,6592	518,4	519,6	520,8
6D	1	0	1	1	0	1	1	0	1,1384	1,6616	523,2	524,4	525,6
6E	0	1	1	1	0	1	1	0	1,136	1,664	528,0	529,2	530,4
6F	1	1	1	1	0	1	1	0	1,1336	1,6664	532,8	534,0	535,2
70	0	0	0	0	1	1	1	0	1,1312	1,6688	537,6	538,8	540,0
71	1	0	0	0	1	1	1	0	1,1288	1,6712	542,4	543,6	544,8
72	0	1	0	0	1	1	1	0	1,1264	1,6736	547,2	548,4	549,6
73	1	1	0	0	1	1	1	0	1,124	1,676	552,0	553,2	554,4
74	0	0	1	0	1	1	1	0	1,1216	1,6784	556,8	558,0	559,2
75	1	0	1	0	1	1	1	0	1,1192	1,6808	561,6	562,8	564,0
76	0	1	1	0	1	1	1	0	1,1168	1,6832	566,4	567,6	568,8
77	1	1	1	0	1	1	1	0	1,1144	1,6856	571,2	572,4	573,6
78	0	0	0	1	1	1	1	0	1,112	1,688	576,0	577,2	578,4
79	1	0	0	1	1	1	1	0	1,1096	1,6904	580,8	582,0	583,2
7A	0	1	0	1	1	1	1	0	1,1072	1,6928	585,6	586,8	588,0
7B	1	1	0	1	1	1	1	0	1,1048	1,6952	590,4	591,6	592,8
7C	0	0	1	1	1	1	1	0	1,1024	1,6976	595,2	596,4	597,6
7D	1	0	1	1	1	1	1	0	1,1	1,7	600,0	601,2	602,4
7E	0	1	1	1	1	1	1	0	1,0976	1,7024	604,8	606,0	607,2
7F	1	1	1	1	1	1	1	0	1,0952	1,7048	609,6	610,8	612,0
80	0	0	0	0	0	0	0	1	1,0928	1,7072	614,4	615,6	616,8
81	1	0	0	0	0	0	0	1	1,0904	1,7096	619,2	620,4	621,6
82	0	1	0	0	0	0	0	1	1,088	1,712	624,0	625,2	626,4
83	1	1	0	0	0	0	0	1	1,0856	1,7144	628,8	630,0	631,2
84	0	0	1	0	0	0	0	1	1,0832	1,7168	633,6	634,8	636,0
85	1	0	1	0	0	0	0	1	1,0808	1,7192	638,4	639,6	640,8
86	0	1	1	0	0	0	0	1	1,0784	1,7216	643,2	644,4	645,6
87	1	1	1	0	0	0	0	1	1,076	1,724	648,0	649,2	650,4
88	0	0	0	1	0	0	0	1	1,0736	1,7264	652,8	654,0	655,2
89	1	0	0	1	0	0	0	1	1,0712	1,7288	657,6	658,8	660,0
8A	0	1	0	1	0	0	0	1	1,0688	1,7312	662,4	663,6	664,8
8B	1	1	0	1	0	0	0	1	1,0664	1,7336	667,2	668,4	669,6
8C	0	0	1	1	0	0	0	1	1,064	1,736	672,0	673,2	674,4
8D	1	0	1	1	0	0	0	1	1,0616	1,7384	676,8	678,0	679,2
8E	0	1	1	1	0	0	0	1	1,0592	1,7408	681,6	682,8	684,0
8F	1	1	1	1	0	0	0	1	1,0568	1,7432	686,4	687,6	688,8
90	0	0	0	0	1	0	0	1	1,0544	1,7456	691,2	692,4	693,6
91	1	0	0	0	1	0	0	1	1,052	1,748	696,0	697,2	698,4
92	0	1	0	0	1	0	0	1	1,0496	1,7504	700,8	702,0	703,2
93	1	1	0	0	1	0	0	1	1,0472	1,7528	705,6	706,8	708,0
94	0	0	1	0	1	0	0	1	1,0448	1,7552	710,4	711,6	712,8
95	1	0	1	0	1	0	0	1	1,0424	1,7576	715,2	716,4	717,6
96	0	1	1	0	1	0	0	1	1,04	1,76	720,0	721,2	722,4
97	1	1	1	0	1	0	0	1	1,0376	1,7624	724,8	726,0	727,2
98	0	0	0	1	1	0	0	1	1,0352	1,7648	729,6	730,8	732,0
99	1	0	0	1	1	0	0	1	1,0328	1,7672	734,4	735,6	736,8
9A	0	1	0	1	1	0	0	1	1,0304	1,7696	739,2	740,4	741,6
9B	1	1	0	1	1	0	0	1	1,028	1,772	744,0	745,2	746,4
9C	0	0	1	1	1	0	0	1	1,0256	1,7744	748,8	750,0	751,2

9D	1	0	1	1	1	0	0	1	1,0232	1,7768	753,6	754,8	756,0
9E	0	1	1	1	1	0	0	1	1,0208	1,7792	758,4	759,6	760,8
9F	1	1	1	1	1	0	0	1	1,0184	1,7816	763,2	764,4	765,6
A0	0	0	0	0	0	1	0	1	1,016	1,784	768,0	769,2	770,4
A1	1	0	0	0	0	1	0	1	1,0136	1,7864	772,8	774,0	775,2
A2	0	1	0	0	0	1	0	1	1,0112	1,7888	777,6	778,8	780,0
A3	1	1	0	0	0	1	0	1	1,0088	1,7912	782,4	783,6	784,8
A4	0	0	1	0	0	1	0	1	1,0064	1,7936	787,2	788,4	789,6
A5	1	0	1	0	0	1	0	1	1,004	1,796	792,0	793,2	794,4
A6	0	1	1	0	0	1	0	1	1,0016	1,7984	796,8	798,0	799,2
A7	1	1	1	0	0	1	0	1	0,9992	1,8008	801,6	802,8	804,0
A8	0	0	0	1	0	1	0	1	0,9968	1,8032	806,4	807,6	808,8
A9	1	0	0	1	0	1	0	1	0,9944	1,8056	811,2	812,4	813,6
AA	0	1	0	1	0	1	0	1	0,992	1,808	816,0	817,2	818,4
AB	1	1	0	1	0	1	0	1	0,9896	1,8104	820,8	822,0	823,2
AC	0	0	1	1	0	1	0	1	0,9872	1,8128	825,6	826,8	828,0
AD	1	0	1	1	0	1	0	1	0,9848	1,8152	830,4	831,6	832,8
AE	0	1	1	1	0	1	0	1	0,9824	1,8176	835,2	836,4	837,6
AF	1	1	1	1	0	1	0	1	0,98	1,82	840,0	841,2	842,4
B0	0	0	0	0	1	1	0	1	0,9776	1,8224	844,8	846,0	847,2
B1	1	0	0	0	1	1	0	1	0,9752	1,8248	849,6	850,8	852,0
B2	0	1	0	0	1	1	0	1	0,9728	1,8272	854,4	855,6	856,8
B3	1	1	0	0	1	1	0	1	0,9704	1,8296	859,2	860,4	861,6
B4	0	0	1	0	1	1	0	1	0,968	1,832	864,0	865,2	866,4
B5	1	0	1	0	1	1	0	1	0,9656	1,8344	868,8	870,0	871,2
B6	0	1	1	0	1	1	0	1	0,9632	1,8368	873,6	874,8	876,0
B7	1	1	1	0	1	1	0	1	0,9608	1,8392	878,4	879,6	880,8
B8	0	0	0	1	1	1	0	1	0,9584	1,8416	883,2	884,4	885,6
B9	1	0	0	1	1	1	0	1	0,956	1,844	888,0	889,2	890,4
BA	0	1	0	1	1	1	0	1	0,9536	1,8464	892,8	894,0	895,2
BB	1	1	0	1	1	1	0	1	0,9512	1,8488	897,6	898,8	900,0
BC	0	0	1	1	1	1	0	1	0,9488	1,8512	902,4	903,6	904,8
BD	1	0	1	1	1	1	0	1	0,9464	1,8536	907,2	908,4	909,6
BE	0	1	1	1	1	1	0	1	0,944	1,856	912,0	913,2	914,4
BF	1	1	1	1	1	1	0	1	0,9416	1,8584	916,8	918,0	919,2
C0	0	0	0	0	0	0	1	1	0,9392	1,8608	921,6	922,8	924,0
C1	1	0	0	0	0	0	1	1	0,9368	1,8632	926,4	927,6	928,8
C2	0	1	0	0	0	0	1	1	0,9344	1,8656	931,2	932,4	933,6
C3	1	1	0	0	0	0	1	1	0,932	1,868	936,0	937,2	938,4
C4	0	0	1	0	0	0	1	1	0,9296	1,8704	940,8	942,0	943,2
C5	1	0	1	0	0	0	1	1	0,9272	1,8728	945,6	946,8	948,0
C6	0	1	1	0	0	0	1	1	0,9248	1,8752	950,4	951,6	952,8
C7	1	1	1	0	0	0	1	1	0,9224	1,8776	955,2	956,4	957,6
C8	0	0	0	1	0	0	1	1	0,92	1,88	960,0	961,2	962,4
C9	1	0	0	1	0	0	1	1	0,9176	1,8824	964,8	966,0	967,2
CA	0	1	0	1	0	0	1	1	0,9152	1,8848	969,6	970,8	972,0
CB	1	1	0	1	0	0	1	1	0,9128	1,8872	974,4	975,6	976,8
CC	0	0	1	1	0	0	1	1	0,9104	1,8896	979,2	980,4	981,6
CD	1	0	1	1	0	0	1	1	0,908	1,892	984,0	985,2	986,4
CE	0	1	1	1	0	0	1	1	0,9056	1,8944	988,8	990,0	991,2
CF	1	1	1	1	0	0	1	1	0,9032	1,8968	993,6	994,8	996,0
D0	0	0	0	0	1	0	1	1	0,9008	1,8992	998,4	999,6	1000,8
D1	1	0	0	0	1	0	1	1	0,8984	1,9016	1003,2	1004,4	1005,6

D2	0	1	0	0	1	0	1	1	0,896	1,904	1008,0	1009,2	1010,4
D3	1	1	0	0	1	0	1	1	0,8936	1,9064	1012,8	1014,0	1015,2
D4	0	0	1	0	1	0	1	1	0,8912	1,9088	1017,6	1018,8	1020,0
D5	1	0	1	0	1	0	1	1	0,8888	1,9112	1022,4	1023,6	1024,8
D6	0	1	1	0	1	0	1	1	0,8864	1,9136	1027,2	1028,4	1029,6
D7	1	1	1	0	1	0	1	1	0,884	1,916	1032,0	1033,2	1034,4
D8	0	0	0	1	1	0	1	1	0,8816	1,9184	1036,8	1038,0	1039,2
D9	1	0	0	1	1	0	1	1	0,8792	1,9208	1041,6	1042,8	1044,0
DA	0	1	0	1	1	0	1	1	0,8768	1,9232	1046,4	1047,6	1048,8
DB	1	1	0	1	1	0	1	1	0,8744	1,9256	1051,2	1052,4	1053,6
DC	0	0	1	1	1	0	1	1	0,872	1,928	1056,0	1057,2	1058,4
DD	1	0	1	1	1	0	1	1	0,8696	1,9304	1060,8	1062,0	1063,2
DE	0	1	1	1	1	0	1	1	0,8672	1,9328	1065,6	1066,8	1068,0
DF	1	1	1	1	1	0	1	1	0,8648	1,9352	1070,4	1071,6	1072,8
E0	0	0	0	0	0	1	1	1	0,8624	1,9376	1075,2	1076,4	1077,6
E1	1	0	0	0	0	1	1	1	0,86	1,94	1080,0	1081,2	1082,4
E2	0	1	0	0	0	1	1	1	0,8576	1,9424	1084,8	1086,0	1087,2
E3	1	1	0	0	0	1	1	1	0,8552	1,9448	1089,6	1090,8	1092,0
E4	0	0	1	0	0	1	1	1	0,8528	1,9472	1094,4	1095,6	1096,8
E5	1	0	1	0	0	1	1	1	0,8504	1,9496	1099,2	1100,4	1101,6
E6	0	1	1	0	0	1	1	1	0,848	1,952	1104,0	1105,2	1106,4
E7	1	1	1	0	0	1	1	1	0,8456	1,9544	1108,8	1110,0	1111,2
E8	0	0	0	1	0	1	1	1	0,8432	1,9568	1113,6	1114,8	1116,0
E9	1	0	0	1	0	1	1	1	0,8408	1,9592	1118,4	1119,6	1120,8
EA	0	1	0	1	0	1	1	1	0,8384	1,9616	1123,2	1124,4	1125,6
EB	1	1	0	1	0	1	1	1	0,836	1,964	1128,0	1129,2	1130,4
EC	0	0	1	1	0	1	1	1	0,8336	1,9664	1132,8	1134,0	1135,2
ED	1	0	1	1	0	1	1	1	0,8312	1,9688	1137,6	1138,8	1140,0
EE	0	1	1	1	0	1	1	1	0,8288	1,9712	1142,4	1143,6	1144,8
EF	1	1	1	1	0	1	1	1	0,8264	1,9736	1147,2	1148,4	1149,6
F0	0	0	0	0	1	1	1	1	0,824	1,976	1152,0	1153,2	1154,4
F1	1	0	0	0	1	1	1	1	0,8216	1,9784	1156,8	1158,0	1159,2
F2	0	1	0	0	1	1	1	1	0,8192	1,9808	1161,6	1162,8	1164,0
F3	1	1	0	0	1	1	1	1	0,8168	1,9832	1166,4	1167,6	1168,8
F4	0	0	1	0	1	1	1	1	0,8144	1,9856	1171,2	1172,4	1173,6
F5	1	0	1	0	1	1	1	1	0,812	1,988	1176,0	1177,2	1178,4
F6	0	1	1	0	1	1	1	1	0,8096	1,9904	1180,8	1182,0	1183,2
F7	1	1	1	0	1	1	1	1	0,8072	1,9928	1185,6	1186,8	1188,0
F8	0	0	0	1	1	1	1	1	0,8048	1,9952	1190,4	1191,6	1192,8
F9	1	0	0	1	1	1	1	1	0,8024	1,9976	1195,2	1196,4	1197,6
FA	0	1	0	1	1	1	1	1	0,8	2	1200,0	1201,2	1202,4
FB	1	1	0	1	1	1	1	1	0,7976	2,0024	1204,8	1206,0	1207,2
FC	0	0	1	1	1	1	1	1	0,7952	2,0048	1209,6	1210,8	1212,0
FD	1	0	1	1	1	1	1	1	0,7928	2,0072	1214,4	1215,6	1216,8
FE	0	1	1	1	1	1	1	1	0,7904	2,0096	1219,2	1220,4	1221,6
FF	1	1	1	1	1	1	1	1	0,788	2,012	1224,0	1225,2	1226,4