Inrush current test with 35 clusters at Ciemat

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List of Abbreviations			

History		
Version	Date	Observation
0	12/09/2016	Draft

Distribution	

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1 Introduction

This document contains a description of the inrush current test performed with 35 clusters at Ciemat. The main goal of the test is to measure the current that power supplies to be used in CTA cameras (PULS Q40.241) are able to provide at power-up when they are loaded with 35 clusters. These tests were performed during the second week of September at Ciemat as part of the C35 test with the final cluster holder.

2 Inrush current test

2.1 Setup description

Figure 1 shows a diagram of the setup used in the test. Two power supplies PULS Q40.241 are powered with three phase power cable. The ouput of the power supplies are combined in a PULS YR80.241 redundancy module. The output of the redundancy module is connected to the bus bars using a twisted pair power cable with Faston connectors. From the busbar there are individual power cables to each cluster for a maximum load of 35 clusters. One cluster consists of PMTs, Slow Control Board, Dragon Board, L0 + L1 mezzanine and Backplane, although some of the clusters are not equipped with L0+L1 mezzanines.

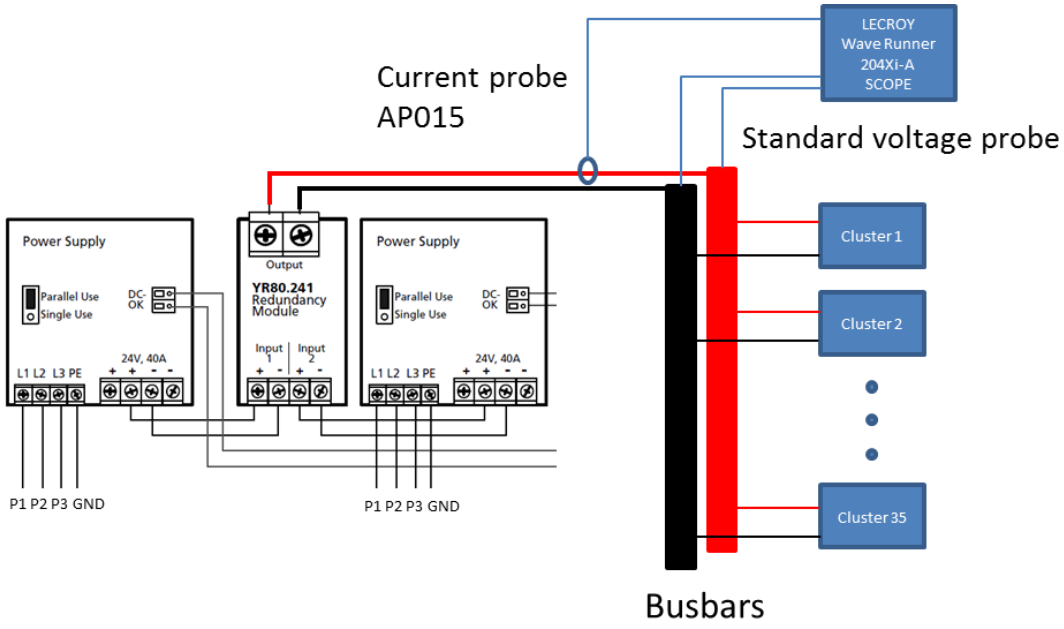

Fig. 1 Diagram of power distribution Setup used in the test

2.2 Results of the test

The test consisted in several power up cycles where the transient current and voltage is registered with a Wave Runner LeCroy Scope. For measuring the current an active current probe AP015 is used. In the following figures the current and voltage time evolution is shown with different cluster loads and time scales.

Figures 2 and 3 show current and voltage transients for 1 cluster load. After power up there is a current peak of ~1,5A amplitude probably produced by the load of decoupling capacitors that are placed in the first stage of the power distribution circuits on each board. After this peak, current consumption remains unstable during some miliseconds, probably due to the load of several power circuits in the boards. After 20 ~ 30ms from the power up both current and voltage become stable. From this moment on configuration of FPGAs starts.

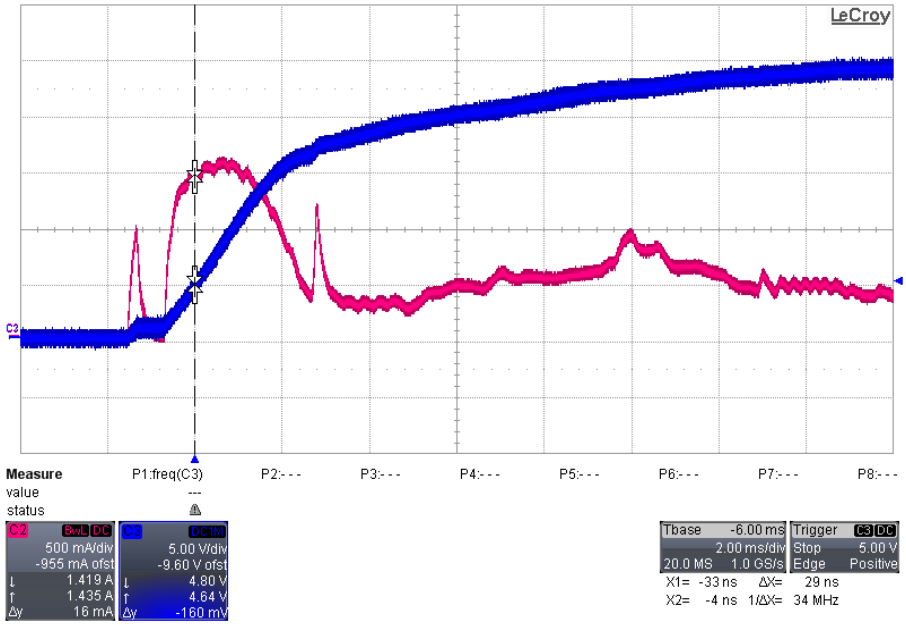

Fig. 2 Power on current and voltage with 1 cluster load. Red waveform: input current to busbar, 500mA/div. Blue waveform: busbar voltage, 5V/div. Time scale: 2ms/div.

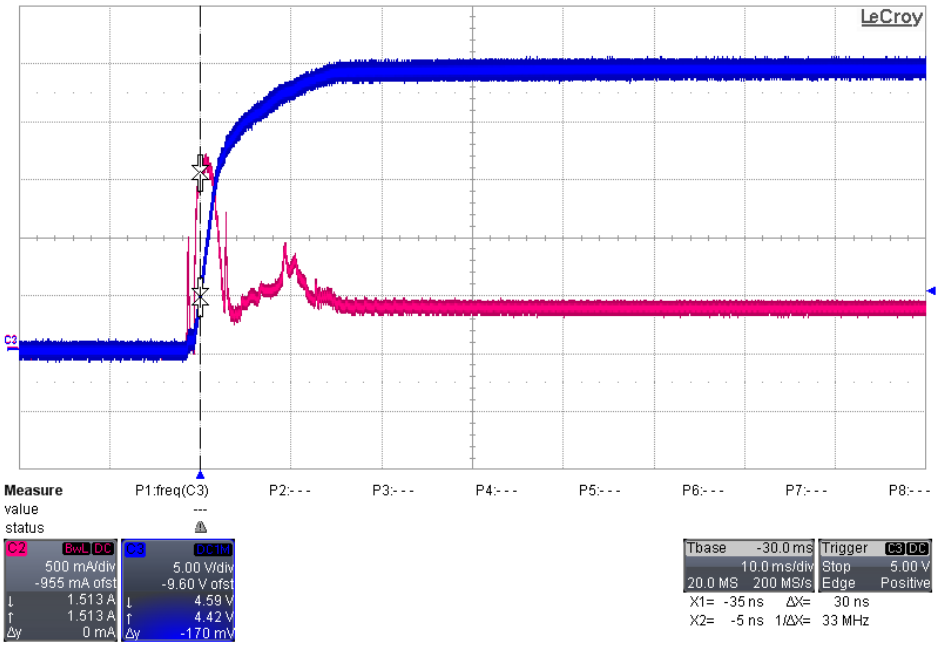

Fig 3 Power on current and voltage with 1 cluster load Red waveform: input current to busbar, 500mA/div. Blue waveform: busbar voltage, 5V/div. Time scale: 10ms/div.

Figures 4 and 5 show current and voltage transients for 9 clusters load. The first current peak has amplitude of around ~13,5 A in this case, ~1,5A per module. Time needed for current and voltage stabilization is again of ~ 30ms from power on. Fig 5 shows the current evolution with a time scale of 1ms/div so it can be observed the effect of the end FPGA configuration processes. Maybe also other initialization processes in Ethernet circuit and RAM memory are performed during this period. After 6 seconds, the modules seem to be ready for operation.

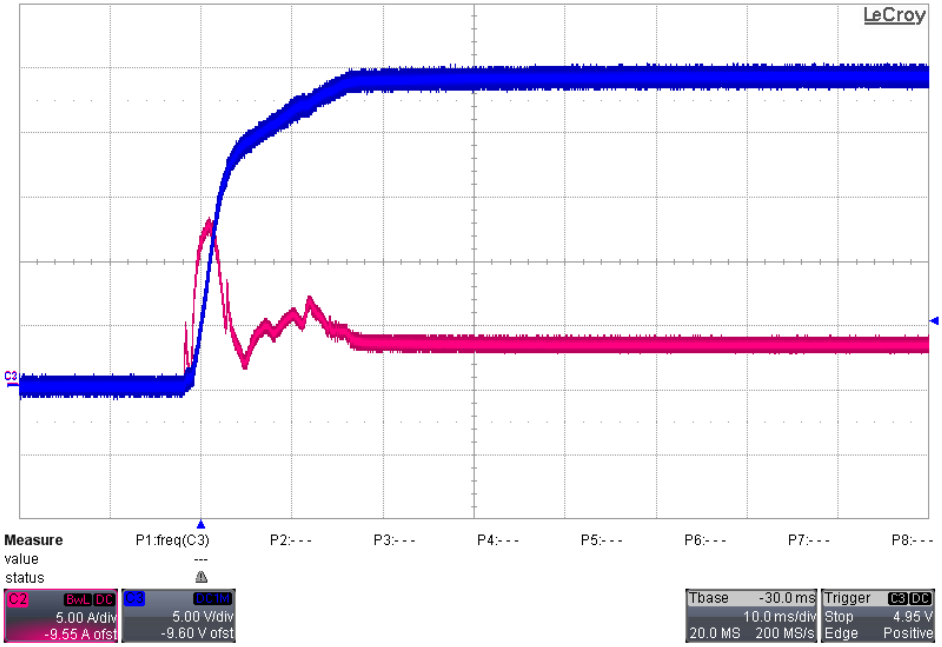

Fig 4 Power on current and voltage with 9 clusters load. Red waveform: input current to busbar, 5A/div. Blue waveform: busbar voltage, 5V/div. Time scale: 10ms/div.

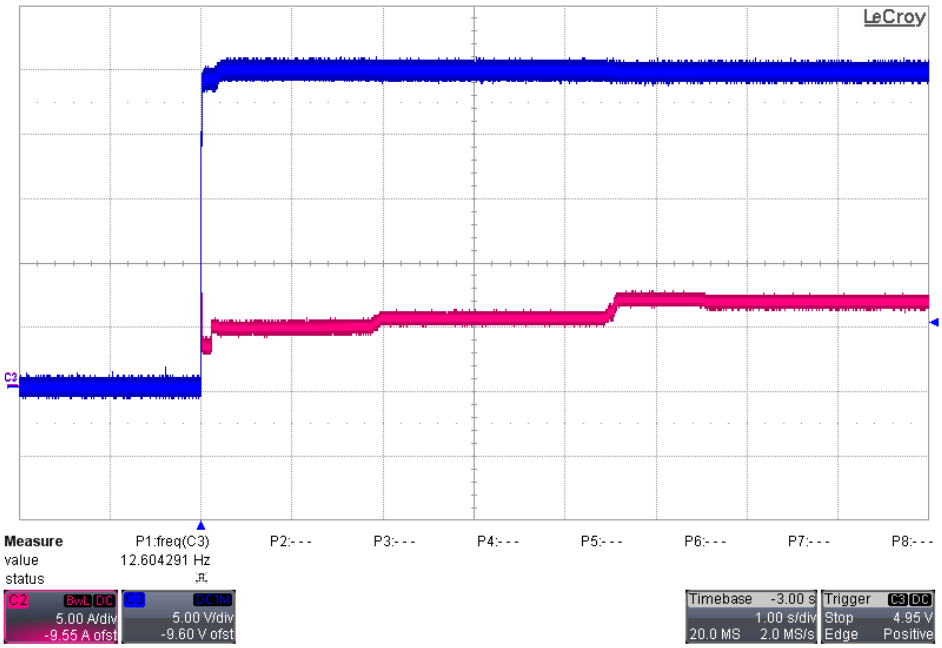

Fig 5 Power on current and voltage with 9 clusters load. Red waveform: input current to busbar, 5A/div. Blue waveform: busbar voltage, 5V/div. Time scale: 1s/div.

Figures 6 and 7 show current and voltage transients for 17 clusters load. The first current peak has amplitude of around 23 A in this case, that is, ~ 1.3A per module. Reduction of current amplitude per

module maybe related with power supply output current capabilities or with slightly different time constants in each module. Time needed for current and voltage stabilization is again of ~ 30ms from power on.

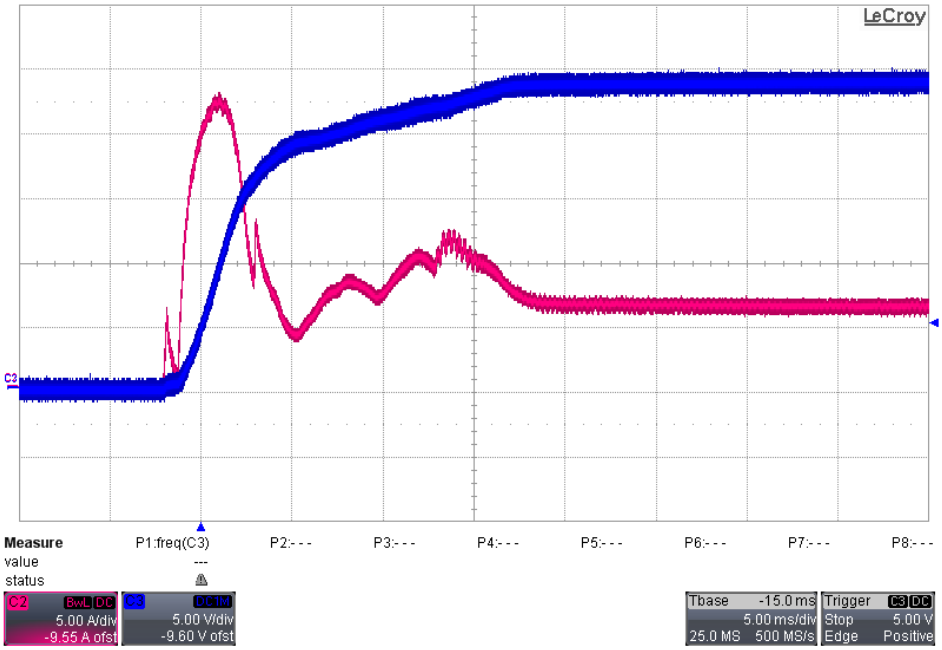

Fig 6 Power on current and voltage with 17 clusters load. Red waveform: input current to busbar, 5A/div. Blue waveform: busbar voltage, 5V/div. Time scale: 5ms/div.

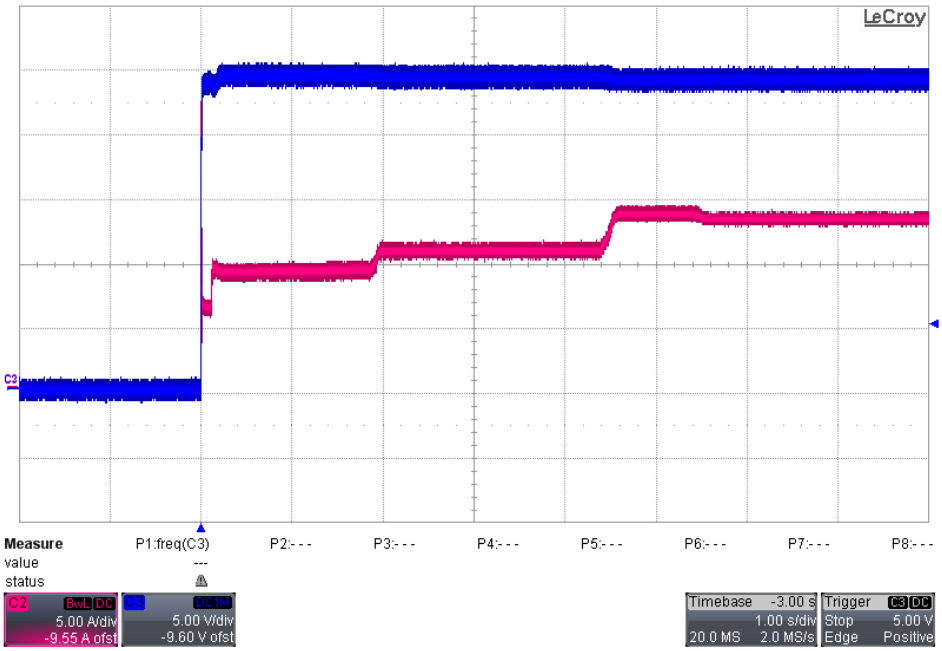

Fig 7 Power on current and voltage with 17 clusters load. Red waveform: input current to busbar,

5A/div. Blue waveform: busbar voltage, 5V/div. Time scale: 1s/div.

Finally figures 8 and 9 show current and voltage transients for 35 clusters load. The first current peak has amplitude of around 37 A, about 1A per module. Again, the reason for a reduction in the current amplitude per module can be due to power supply limitation or load time constant. Time needed for current and voltage stabilization is again of ~ 30ms from power on. Consumption becomes nominal after 6 seconds from power on.

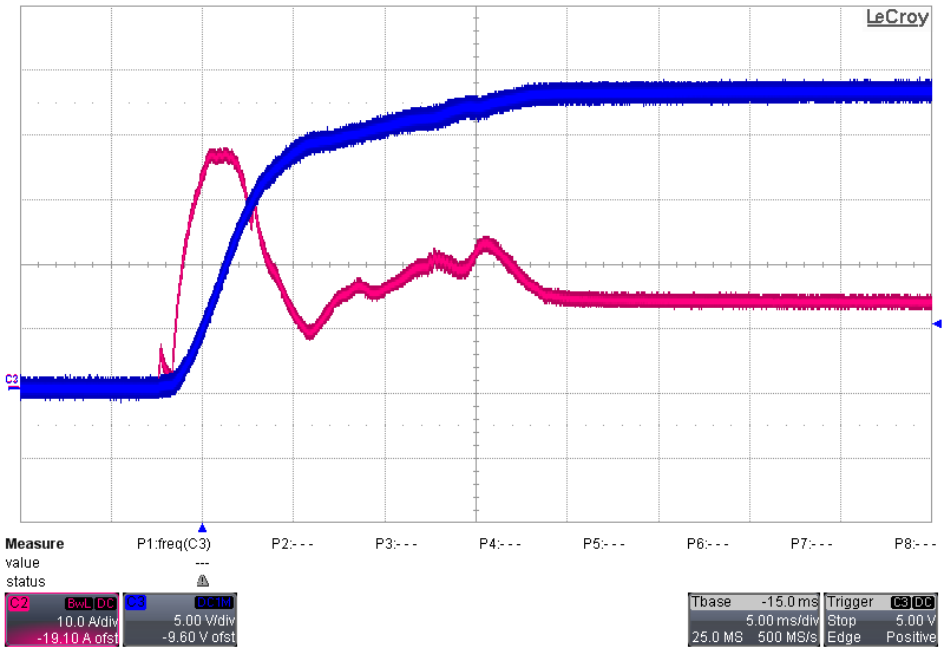

Fig 8 Power on current and voltage with 35 clusters load. Red waveform: input current to busbar, 10A/div. Blue waveform: busbar voltage, 5V/div. Time scale: 5ms/div.

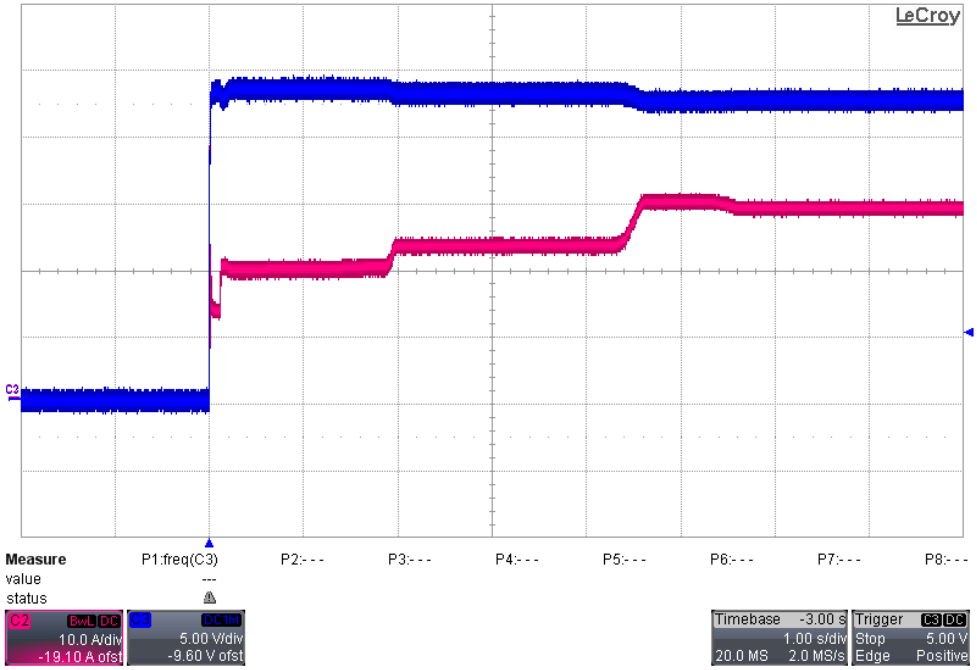

Fig 9 Power on current and voltage with 35 clusters load. Red waveform: input current to busbar, 10A/div. Blue waveform: busbar voltage, 5V/div. Time scale: 1s/div.

3 Conclusions

Main conclusion of the test is that power supply configuration used in this case is suitable for powering 35 clusters. Power supply arrangement is able of provide inrush current demanded by 35 clusters load. In addition, FPGAs of both Dragon and backplane finish their configuration cycles without problems.

There are three stages in the inrush current waveform at power up. In the first stage, a high peak is observed, probably due to the loading of first capacitors in the power distribution circuits in the boards. This first peak last around 5ms with an amplitude from 1,5A to 1A per module, depending on the number of modules connected to the power supply.

Second stage starts when input voltage reaches around 20 volts. At this moment switching regulators are activated and start demanding current in order to load capacitors and power circuits of parts powered by them. Therefore there is some time of unstable current that lasts around 20 ~ 30ms. After this, input voltage remains stable.

During the third stage different current consumption levels are observed due to different operations in the initialization processes of the boards. These processes may include FPGAs configuration, Ethernet PHY, DR4 and ADC initialization and maybe some RAM memory testing. After 6 seconds current consumption reaches its nominal value and the modules seem ready for operation.