

RJ45 connectors between the clock board and the TIB, and the ones of the RJ45 connectors of the links between the TIB and the backplanes, are assigned as it is shown in table 7.1. The signal named as CABLE\_DETECT, not yet mentioned, is used to ensure that the plug is connected properly and just consists on a  $1\ k\Omega$  resistor to ground in the reception side, and an input pin of the FPGA with a weak pull-up in the transmission side. So, the FPGA detects if it is properly connected or not.

	to clock board	from clock board	to/from central backplane	to-from not central backplane
Pin	Signal	Signal	Signal	Signal
1	CAMERA_TRIGGER_+	CLK_10MHZ_+	L1_TRIGGER_+	TRGTYPE_CLK_+
2	CAMERA_TRIGGER_-	CLK_10MHZ_-	L1_TRIGGER_-	TRGTYPE_CLK_-
3	TRGTYPE0_+	SOFT_ARRAYTRIG_+	CAMERA_TRIGGER_+	TRGTYPE_DATA_+
4	TRGTYPE1_+	SPARE_1+	BUSY_+	RES_TOPO1_+
5	TRGTYPE1_-	SPARE_1-	BUSY_-	RES_TOPO1_-
6	TRGTYPE0_-	SOFT_ARRAYTRIG_-	CAMERA_TRIGGER_-	TRGTYPE_DATA_-
7	CABLE_DETECT	CABLE_DETECT	SPARE_+	RES_TOPO2_+
8	GND	GND	SPARE_-	RES_TOPO2_-

Table 7.1: Pinout definition of the RJ45 connectors between the TIB and the clock board and the central backplane

Apart from these RJ45 connectors, others will be available in the TIB as spares, or with the aim to be used to implement advanced features like the ones explained in section 7.3. It is important to point out that the TIB is compatible with two different front-end boards (NECTAr and Dragon), two different clock boards (MUTIN and White Rabbit) and will work in LSTs and MSTs. A lot of coordination work has been required to achieve this compatibility.

## 7.2 Hardware stereo trigger

As was explained in section 3.2.8.1, the hardware stereo trigger function consists of looking for simultaneous triggers in neighbour telescopes, inside a time window of a few tens of nanoseconds, with the aim to readout only the events which triggered more than one telescope. As the probability of having more than one telescope triggered by NSB inside this short time window is rather low, the stereo trigger detects most of the events caused by Cherenkov showers, while rejecting most of the NSB events. The rejected events are never digitized, not contributing to the dead time. Thus, the telescope readout rate is reduced, so it is possible to reduce the Level 1 thresholds and increase the sensitivity to low energy  $\gamma$ -rays<sup>4</sup>.

### 7.2.1 Timing restrictions

In order to look for coincidences inside the mentioned time window (typically 50 ns), the TIB in each LST camera must receive the Level 1 trigger signals from its neighbour LSTs plus its local Level 1 trigger. However, as the neighbour LSTs are far away (at distances of around 100 m), their trigger signals will reach the TIB some time after the local Level 1 trigger. In this way, the local trigger must be delayed a time equivalent to the propagation delay before looking for coincidences. The situation

<sup>4</sup>To optimize the sensitivity to low energy  $\gamma$ -rays, the thresholds must be as low as possible, while maintaining a sustainable readout rate.

becomes more complicated if we take into account that each neighbour LSTs can be separated a different distance. Moreover, the time of flight of the Cherenkov light is different depending on the pointing direction. At the end, all these delays mean that the data must be stored in the analog memory buffers until all the triggers from the neighbour LSTs reach the local telescope, the TIB decides if there has been a coincidence or not and, in the positive case, the camera trigger signal is distributed to all the clusters in the camera. Therefore, the analog memory buffer must be long enough to keep the signal stored until the trigger arrives.

The Dragon front-end boards are equipped with four DRS4 [56] chips with 1024 analog memory cells in each channel, which means that it is able to store up to 4096 ns with a sample frequency of 1 GHz. This is required to implement the hardware stereo trigger in the LST subarray, and thus achieving the best sensitivity to low energy  $\gamma$ -rays. In the next subsections the different sources of time delay are analyzed and how the Dragon front-end board buffer can cope with them.

### **7.2.1.1 Compensation of the fixed delays**

The approximate fixed delays which contribute to the minimum length of the memory buffers, considering optical fibers with a refraction index of 1.5, are the following:

- 220 ns corresponding to Level 0, Level 1 and the distribution through the clusters until reaching the TIB (break down in table 3.1).
- 500 ns for the 100 m optical fiber between the TIB and the LST basement (see figure 7.5).
- 500 ns if the neighbour LST is placed at 100 m from the local one, or 700 ns if it is 141 m away (see figure 7.6).
- 500 ns for the 100 m optical fiber between the LST basement and the TIB.
- 170 ns for the trigger distribution of the camera trigger signal down to the clusters

This means that all the inputs must wait for the trigger from the furthest telescope, which needs at least 2090 ns to reach the telescope which we are considering as local.

### **7.2.1.2 Compensation of the Cherenkov light time of flight**

The Cherenkov showers are generated at ca. 10 km height, which is far enough to consider the photons as forming a plane wave front. Thus, if all the telescopes are pointing to the zenith, the wave front will reach them at the same time and only the fixed delays explained in section 7.2.1.1 need to be taken into account. However, in real operation the telescopes will not be generally pointing to the zenith, but to a certain location defined by specific azimuth and elevation angles. In this conditions the distance travelled by the photons is not the same for each telescope, and therefore the shower images will be formed at different times. The delay differences due to the different time of flight of the Cherenkov photons must be compensated in order to perform the coincidences of the images caused by the same shower.

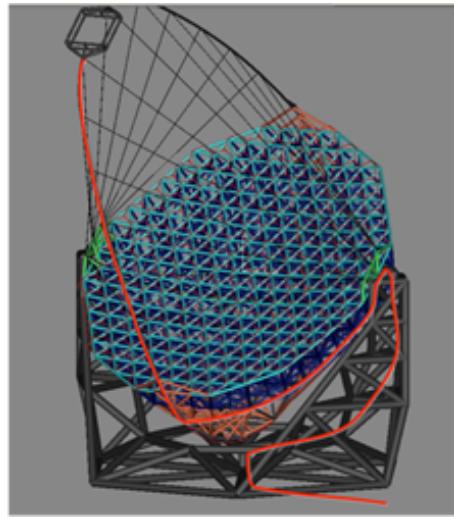


Figure 7.5: Sketch of the optical fiber from the camera to the basement, with an estimated length of 100 m

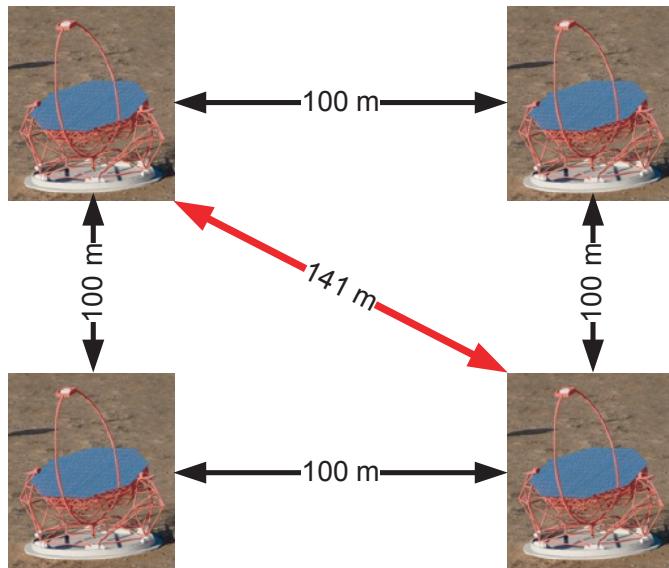


Figure 7.6: Expected LST layout, in a 100 m square rectangular grid

As it is easy to understand from picture 7.7, when two telescopes are aligned with the pointing direction, the different distances travelled by the Cherenkov photons depends on the elevation angle  $\theta$  as defined by equation 7.1:

$$\Delta d = d \cos \theta \quad (7.1)$$

However, as the telescopes are not usually aligned with the pointing direction, the additional distance at ground level that the Cherenkov photons must travel through ( $d$  in equation 7.1) depends on the azimuth angle  $\varphi$ .

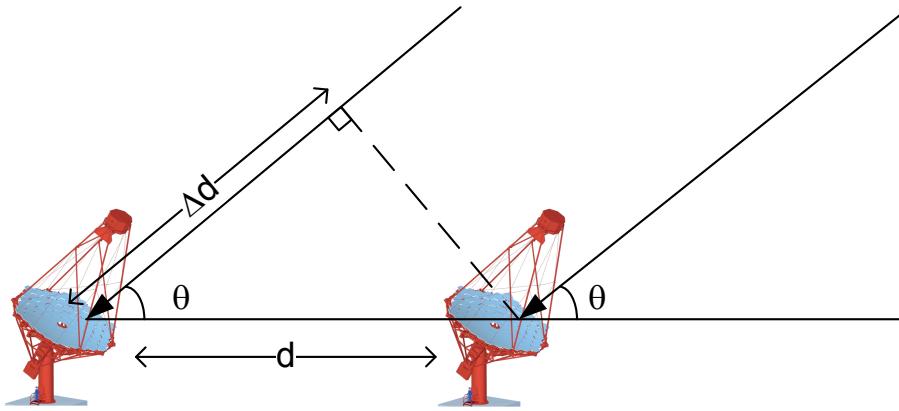
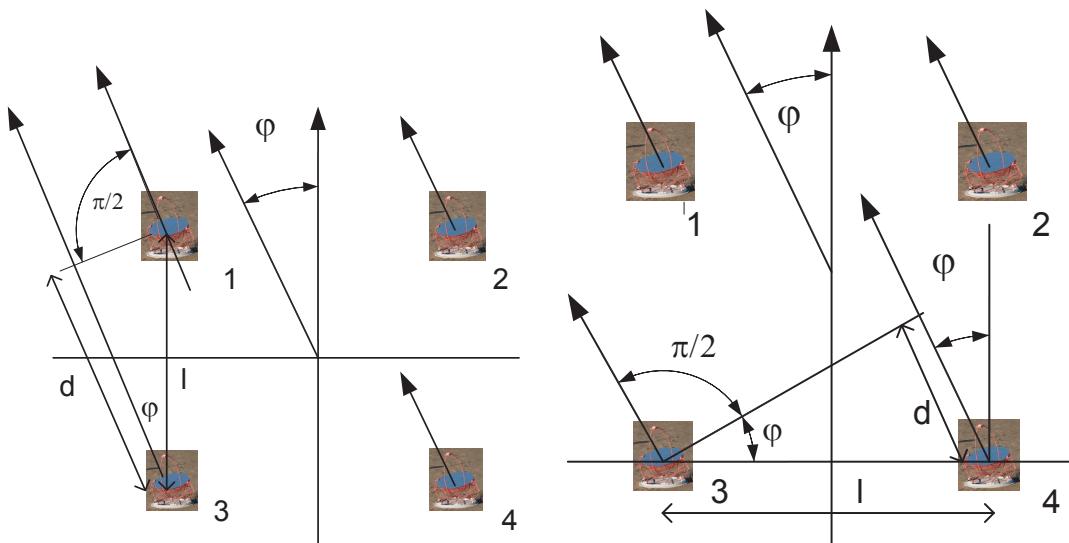


Figure 7.7: Different distance travelled by the Cherenkov photons depending on the elevation angle  $\theta$



(a) Light path difference between IACTs aligned parallel to the axis  $\varphi = 0$  (b) Light path difference between IACTs aligned parallel to the axis  $\varphi = \pi/2$

Figure 7.8: Different time of flight depending on the azimuth angle

Considering four LSTs placed at the corners of a square, and oriented with respect to the coordinate system as shown in figure 7.8, the distance  $d$  used in equation 7.1 for telescopes 3 and 4 with respect to 1 and 2 respectively, are defined by equation 7.2, for  $\varphi < \pi/2$ .

$$d = l \cos \varphi \quad (7.2)$$

On the other hand, the distance  $d$  for LSTs 2 and 4 with respect to LSTs 1 and 2, is given by equation 7.3, for  $\varphi < \pi$ .

$$d = l \sin \varphi \quad (7.3)$$

Thus, for  $\theta < \pi/2$  and  $\varphi < \pi/2$ , the different time of flight of the Cherenkov photons coming to LST 3 with respect to LST 1 will be given by equation 7.4, while for LST 4 with respect to LST 3 it will be given by 7.5.

$$\Delta\text{time of flight}_{31} = \frac{l}{c} \cos \varphi \cos \theta \quad (7.4)$$

$$\Delta\text{time of flight}_{43} = \frac{l}{c} \sin \varphi \cos \theta \quad (7.5)$$

Similar equations can be obtained in a similar way for any two pair of telescopes. It is easy to see that the maximum time difference to be compensated in the TIB will be the one required by the photons to travel a distance equivalent to the maximum telescope separation in ground, i.e. 141 m. In fact, the telescopes will never point at elevation angles lower than  $15^{\circ}$ <sup>5</sup>, so the maximum distance difference is 136 m, corresponding to 454 ns. This time should be added to the 2090 ns due to fixed delays, so a buffer of at least 2544 ns is required. Moreover, some more time should be added to perform the logic operations in the TIB, generate the optical pulses, send the different signals through the RJ45 cables in the camera or just as a safety margin. Therefore 3  $\mu\text{s}$  can be considered as the minimum time difference required<sup>6</sup>, so the 4096 cells of the Dragon front-end board, operating at 1 GHz sampling rate, should be enough.

It is worth to mention that in normal operation the IACTs will be tracking the  $\gamma$ -ray sources through the sky during some time, from several minutes to hours. During this time the azimuth and elevation angles change, and therefore the delay differences to be compensated. Thus, the pointing direction must be updated quite often and the compensation times must be recalculated. As an example, in order to compensate time errors lower than 2 ns, the pointing direction should be updated for every change of  $0.34^{\circ}$ , corresponding to 82 s in the worst case, when the IACTs are pointing near the zenith. The pointing direction is provided by the slow control system.

### 7.2.1.3 Synchronization with local trigger

The delay adjustments explained in sections 7.2.1.1 and 7.2.1.2 are useful to verify if the Level 1 triggers generated in the local LST and its neighbours are happening inside the coincidence window, and thus fulfilling the stereo trigger condition. Due to statistical fluctuations in the shower development, there is a certain jitter in the arrival times of the Cherenkov photons, which makes the optimum duration of the coincidence window to be around 50 ns. This effectively means that, for every single event, the stereo condition can be accomplished at any time during inside the window, with an uncertainty of several tens of nanoseconds. Due to this uncertainty, it is rather inconvenient to generate the camera trigger signal synchronized with the time at which the trigger condition is fulfilled (see figure 7.9). As it was briefly mentioned in the introduction of chapter 3, one of the targets of the trigger system is to minimize the jitter to reduce the amount of samples required for each event (and, as a consequence, the dead time) and to allow the calibration of the DRS4 cells. Therefore, a jitter of up to 50 ns in the trigger time is not acceptable.

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<sup>5</sup>For lower angles, the length of the path in the atmosphere which the Cherenkov photons must travel through, is very long and the telescope response is degraded.

<sup>6</sup>CTA consortium specified 3500 ns

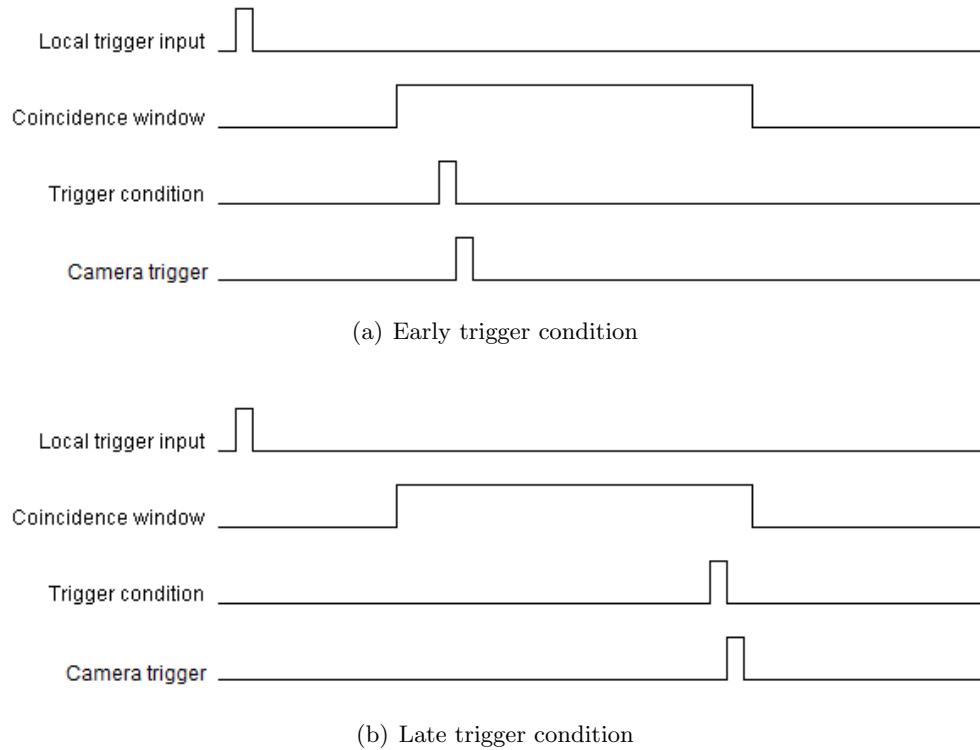


Figure 7.9: If the camera trigger signal is synchronized with the trigger condition, the time required to generate the trigger command is variable

Nevertheless, the time uncertainty in the compliance with the trigger condition is not a real problem. In fact, every LST has to read its local data, and these local data are synchronized with the local trigger, not with the trigger condition. So, the camera trigger signal must be generated a fixed and precise time after the local trigger, as shown in figure 7.10, whenever the trigger condition was satisfied. This fixed time must be somewhat longer than the longest time required to compensate the delay differences and to finish the coincidence window.

### 7.3 Advanced features

Interfacing with the other trigger generating subsystems and implementing the hardware stereo trigger for four LSTs are the two basic functionalities of the trigger interface board. However, there are other interesting features that can be implemented in the trigger interface board, which are described in this section.

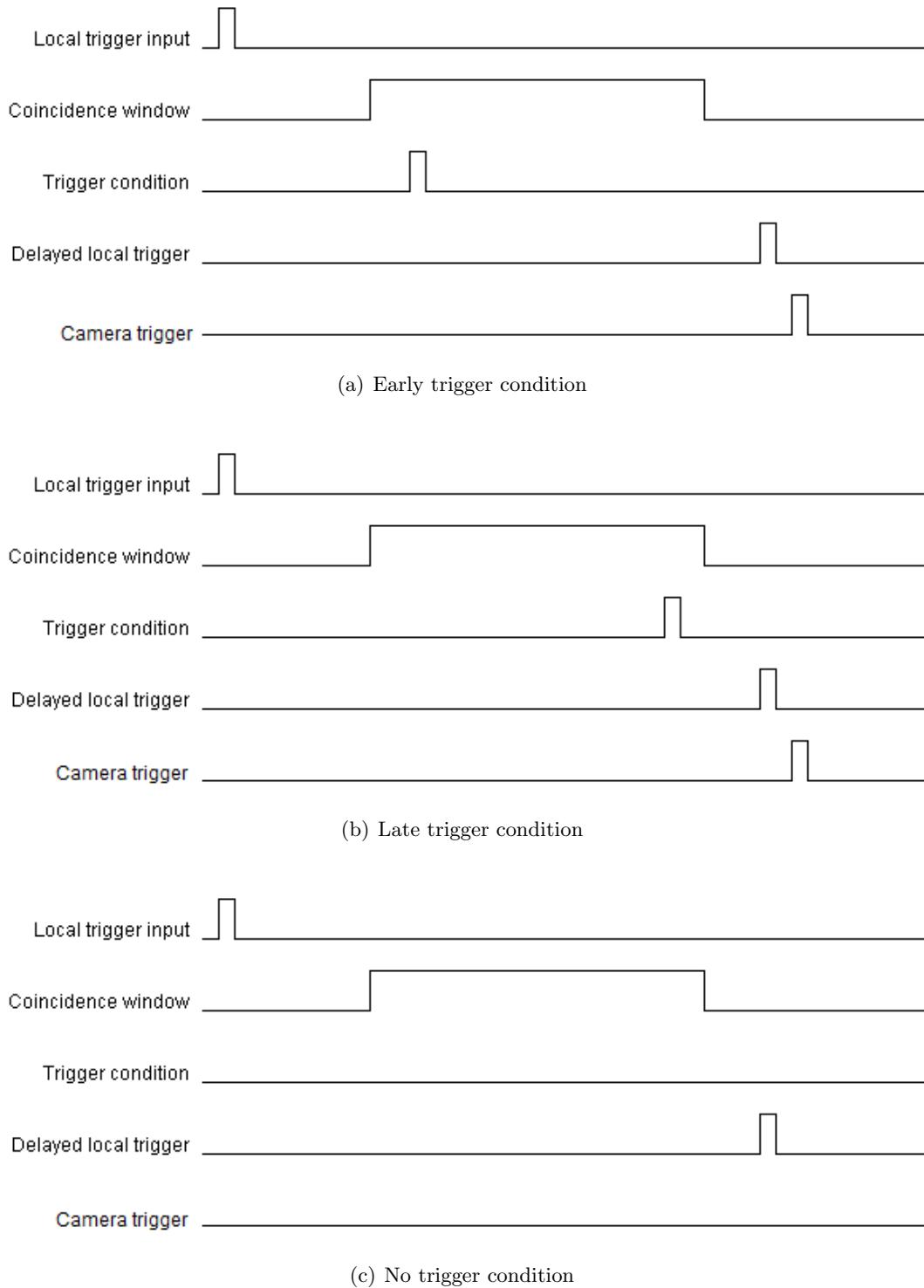


Figure 7.10: If the trigger command is synchronized with the local trigger, the time required to generate the camera trigger signal is fixed

### 7.3.1 More LSTs

In principle, there will be four LSTs in the CTA array, both in the north and south hemispheres. However, in the future more LSTs could be built if there were a special interest in improving even more the sensitivity or reducing the observation time at low energies<sup>7</sup>. In anticipation of this possible enlargement, the trigger interface board is able to handle up to nine LSTs and perform the stereo trigger algorithm with all its inputs.

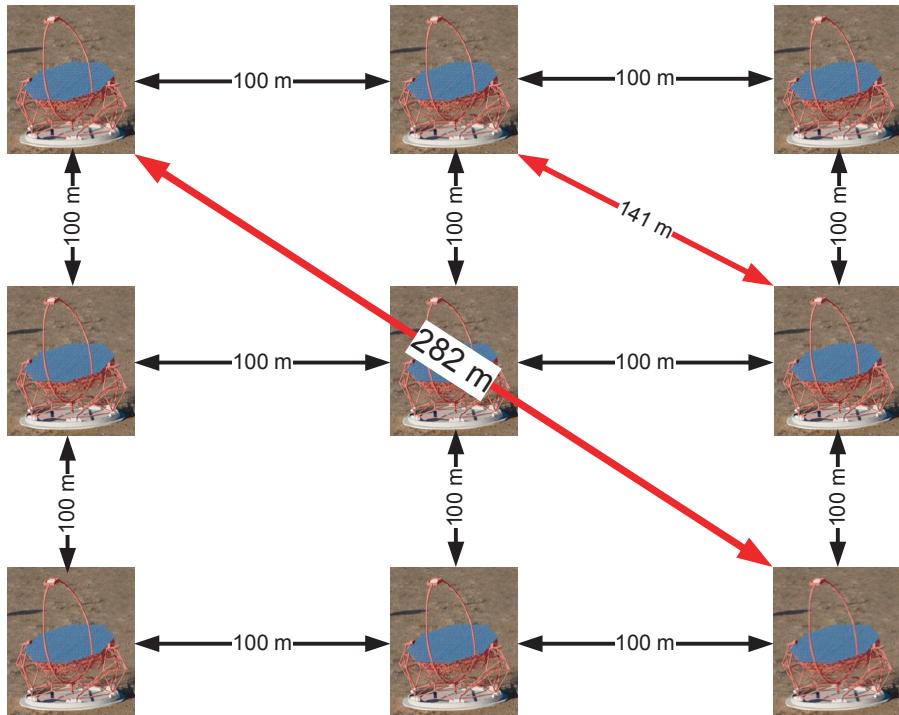


Figure 7.11: 9 LST possible layout

With a layout like the one showed in figure 7.11, the required buffer size needs to be increased in 700 ns corresponding to the additional 141 m of optical fiber between the most separated LSTs (eq. 7.6), plus 470 ns corresponding to the increment in the time of flight (eq. 7.7). Thus, the buffer must be able to store at least 3714 ns of signal, and there would be 382 ns of margin for the TIB logic operations, distribution, etc, considering 4096 memory cells and a sampling frequency of 1 GHz.

$$\Delta t_{\text{optical fiber}} = \frac{141\text{m}}{\frac{c}{1.5}} = 700 \text{ ns} \quad (7.6)$$

$$\Delta t_{\text{maximum time of flight}} = \frac{141\text{m}}{c} = 470 \text{ ns} \quad (7.7)$$

<sup>7</sup>The higher the number of LSTs, the larger the number of recorded low energy events and, at the end, the shorter the time required to obtain statistics and scientific results.

### 7.3.2 MSTs contributing to the LST stereo trigger

The readout of the MSTs will be based on NECTAr chips<sup>8</sup>, which only have 1024 memory cells, so it cannot store more than 1024 ns in its buffer if sampling at 1 GHz. This means that the MST cameras can not wait for the trigger information from the neighbour IACTs, nor be triggered in a hardware stereo mode. However, they can contribute to the stereo trigger algorithms running on their LST neighbours, as sketched in figure 7.12. Provided that the distances are short enough, the MSTs can use their trigger interface boards to broadcast their local Level 1 trigger pulses to their neighbour LSTs, which can wait for them and thus take this information into account in their stereo trigger algorithms. This idea can take advantage from the TIB capability to handle up to 9 trigger inputs, without requiring to build more expensive LSTs. Nevertheless, as the MSTs and LSTs are optimized for different  $\gamma$ -ray energy ranges, the gain in performance of the LST will be minor.

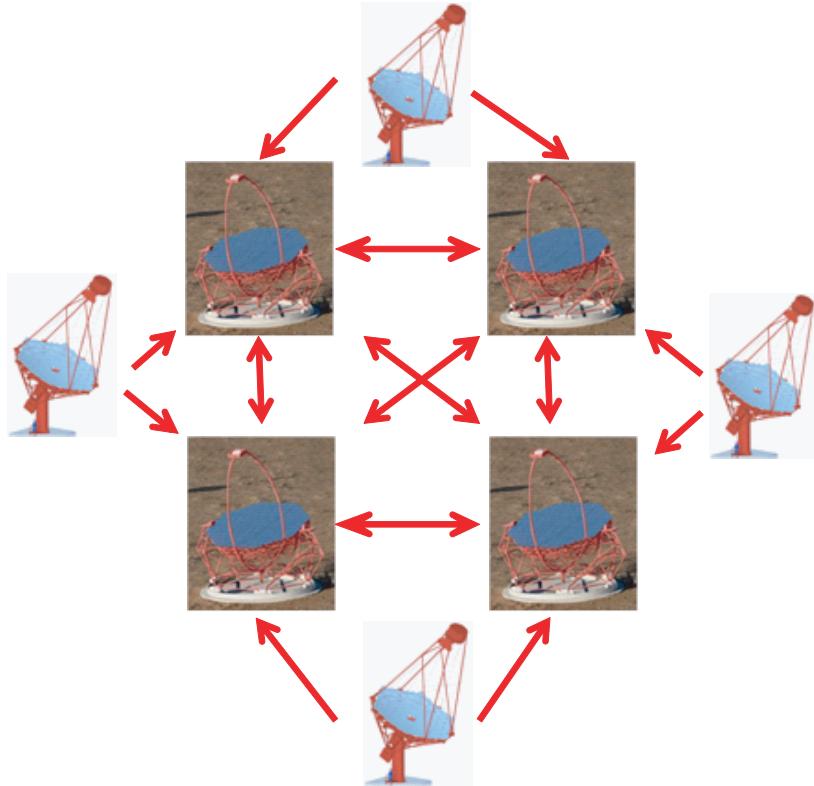


Figure 7.12: A possible stereo trigger scheme with LSTs and MSTs

### 7.3.3 Slow controllable functionalities

As will be described in section 7.4, the TIB is a flexible system essentially implemented in an FPGA and with a micro-PC used for slow control. This architecture makes possible to implement additional functionalities in a straightforward way, as well as to control important parameters dynamically. For instance:

<sup>8</sup>In fact, only some MSTs will be based on NECTAr, while others will follow different architectures. Anyway, if the TIB would be used in this other MSTs, the situation would be the same.

- The duration of the coincidence window can be changed by the slow control system.
- The trigger condition can be changed, in order to choose to look for coincidences of 2, 3, 4 or even more telescopes. Disabling the stereo mode and triggering only in mono mode is also an option.
- The local Level 1 trigger rate, stereo trigger rate and the trigger rates from the neighbours can be monitored by the slow control system, which can take decisions based on this information (change Level 1 thresholds, change Level 1 trigger region size, change stereo trigger condition, etc.).
- The temperature and the status of the optical links can also be monitored, generating alarms if a failure is detected.

#### **7.3.4 Busy state**

One of the additional functionalities foreseen in the TIB is a busy state, to avoid distributing new camera trigger signals to the clusters while the readout is still digitizing. This can be required if the readout system is not able to discard these triggers by itself, and it would be as simple as ignoring all the triggers produced during the dead time started after a trigger command.

This scheme could be more complex if different dead times among clusters are considered. For instance, if a scheme like Colibri is used, only the clusters which are effectively read-out would suffer dead time and, as they would start digitizing at slightly different times, their dead times would also finish at slightly different times. In this case, a BUSY signal (already considered in section 7.1), obtained as the global OR of the busy state of all the clusters, would be required.

#### **7.3.5 Topologic stereo trigger**

The next step to improve the stereo trigger performance and the noise rejection in an stereo scheme consists on using not only the information about when an IACT was triggered but also what part of the camera caused the trigger. This information can be used by the stereo system to check if the local triggers are compatible with the expected patterns for single  $\gamma$ -ray-like events or, on the contrary, they correspond to different events which occurred at the same time just by chance. In the last case, it is very likely that some of these events were caused by NSB, so they should be discarded[143]. Figure 7.13 show several examples of stereo trigger patterns compatible with Cherenkov showers or not.

The implementation of a topologic stereo trigger working as described in the previous paragraph is much more complex than the basic functionality, requiring to send to the neighbours not just the trigger pulse, but also a piece of information containing which cluster was fired, or at least in which part of the camera was placed the cluster that was fired. Nevertheless, the optical links between telescopes can be used to broadcast this information, and the FPGA firmware can be improved to handle it, so in principle it is not impossible to implement the topologic stereo scheme with the TIB. An important difficulty would be how to send the number of the local fired cluster to the TIB. The discussion about this is still an open issue, and the topologic stereo trigger will be an important line of work during the next years.

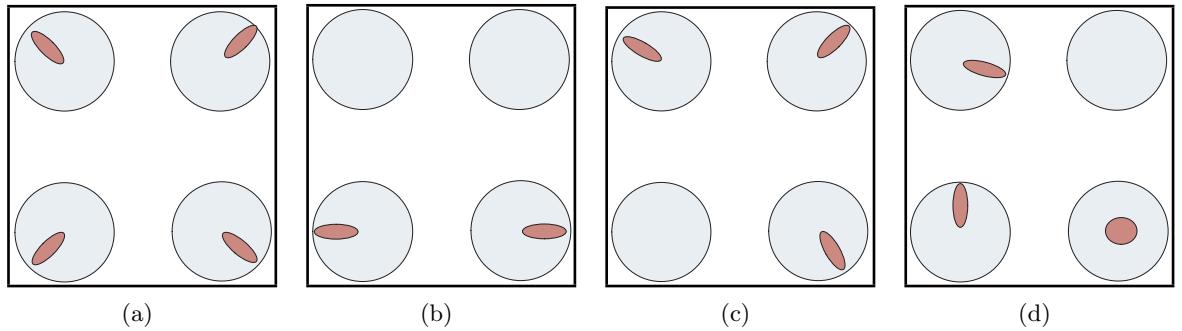


Figure 7.13: Several topologic stereo trigger patterns. 7.13(a), 7.13(b) and 7.13(c) would fire the stereo trigger, but not 7.13(d)

## 7.4 Technical description

### 7.4.1 General architecture

The TIB is implemented in a single PCB housed inside a 19" 1U rack box, as shown in figure 7.14. This rack box will be placed inside the camera, connected to the central backplane, the slow control unit, the clock board, the calibration box, the TIBs in other neighbour IACTs and the power supply unit, as was described in section 7.1. At the same time, the Trigger Interface Board is composed of several electronic subsystems, most of them handled by an FPGA as it is shown in figure 7.15.

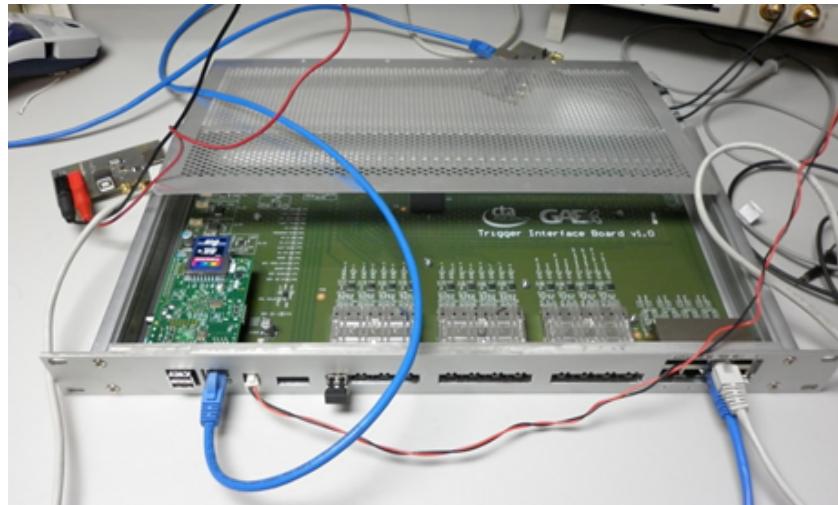


Figure 7.14: Trigger Interface Board prototype inside the 1U rack box

The different subsystems are described in the following subsections.

### 7.4.2 Optical links

Some essential hardware elements of the Trigger Interface Board are the optical links. Even in the case of MSTs triggering in mono, where no communication with neighbours would be required, some

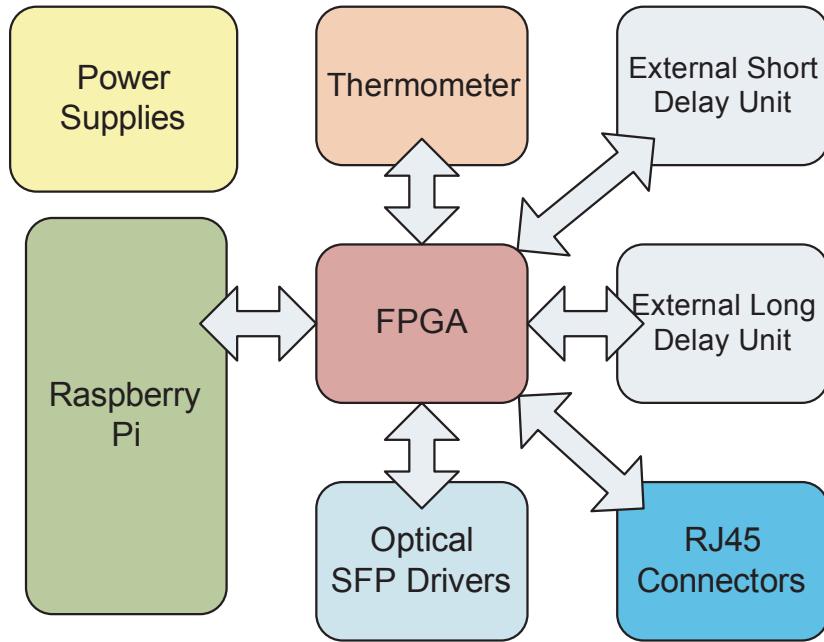


Figure 7.15: Internal block diagram of the Trigger Interface Board

optical links are needed for the communication with the calibration box (calibration and pedestal triggers), or as an alternative possibility to implement fixed delays with optical fibers. The main components of the optical links are described in the following subsections.

#### 7.4.2.1 Optical fibers

Between every two modules connected (TIBs of neighbouring telescopes, calibration boxes, etc.), there will be a cable containing two multimode optical fibers 50/125 OM3 [144] [145]. This kind of optical fibers are suitable for links of up to 550 m length, handling bit rates of up to 10 Gbps, corresponding to pulses as short as 100 ps. As the distance between telescopes will never be longer than 182 m (supposing an unlikely 9 LST subarray), and the transmitted trigger signals are expected to be around 5 ns width, this kind of optical fibers are very appropriate for our system. Additionally, as this kind of optical fiber cables are very common in LANs, they are quite cheap, with prices around 0.50 €/m.

The optical fiber cables are terminated with standard LC multimode duplex connectors, like the one shown in figure 7.16.

#### 7.4.2.2 Transceivers

Two options were considered to implement the optical transceivers: Using standard SFP modules, or using discrete VCSELs and PiN photodiodes mounted inside LC housings.



Figure 7.16: Duplex LC connector

#### 7.4.2.2.1 SFP modules

The first option considered for the transceivers was to use a standard SFP module like the AFBR-5715ALZ from Avago Technologies which is shown in figure 7.17(a). These transceivers consist of a transmitter section based on a 850 nm VCSEL (Vertical Cavity Surface Emitting Laser) and a receiver section containing a PiN photodiode, together with their drivers, amplifiers and other ancillary electronics [146]. One of the optical fibers in the cable is connected to the transmitter and other to the receiver, in order to build the bidirectional link.

The transceiver mentioned above is suitable for OM3 optical fibers, reaching a maximum data rate of 1.25 Gbps. These means that the shortest pulses will be 0.8 ns wide, still shorter than the expected pulses (around 5 ns). Apart from the transmitted and received trigger signals, the transceivers generate two control electronic signals named *TX\_Fault* and *LOS* to indicate possible failures in the transmission or the reception respectively, and receive one signal *TX\_Disable*, which switches off the transceiver when it is set to high level. Subsection 7.4.4.7 explains how these signals are handled by the FPGA.

Regarding the mechanics, the transceivers comply with the Small Form Factor Pluggable (SFP) standard. This allows to use housings from different suppliers, like the one shown in figure 7.17(b), able to house up to 4 transceivers inside. When some link is not in use, the transceiver can be pull out from the box, or just never being installed, saving resources.



(a) Transceiver AFBR-5715ALZ

(b) 4x SFP box

Figure 7.17: Transceiver and housing for 4 SFP transceivers

Nevertheless, the SFP transceivers have a minor difficulty: the transmitter must be driven by LVPECL signals, and the receiver also provides LVPECL output signals. This logic standard can not be managed directly by the FPGA, requiring an intermediate stage for translating the LVPECL

signals to LVDS or other standard supported by the FPGA. This translation can be implemented with the differential translators SN65LVDS100 and SN65LVDS101, from Texas Instruments [147]. SN65LVDS100 performs the conversion of the LVPECL signals into LVDS ones, while SN65LVDS101 is used in the LVDS to LVPECL translation.

In spite of this inconvenient, the AFBR-5715ALZ SFP transceivers were selected to be mounted in the first TIB prototype due to their simplicity and with the aim to use standard solutions.

#### 7.4.2.2.2 Discrete VCSELs and PiN photodiodes

Due to some problems found during the tests of the first TIB prototype (see section 7.5.9), an ad hoc design for the transceivers has also been considered. Designing the optical transmitter and receiver with discrete VCSELs and PiN photodiodes is an option which provides with great flexibility to optimize the bandwidth, the cost or the power consumption. The drawback is that some analog processing stages need to be designed in order to feed the VCSEL with a signal inside its input range, and to recover an LVDS signal from the analog output of the photodiode. The most critical characteristic is the bandwidth, which must be as large as possible in order to have pulses with very sharp edges, thus maintaining the timing information.

The design of the transmitter is shown in figure 7.18. The VCSEL chosen emits at 850 nm and has 1 GHz bandwidth. It was provided by AFE ltd. [148] who also assembled it in an LC plastic housing. Considering a single-ended input signal between 0 and 3.3 V from the FPGA, the AD8009 [149] operational amplifier is used to adjust the voltage range of the signal and to avoid overloading the FPGA. The AD8009 is a very fast operational amplifier ( $5500 \text{ V}/\mu\text{s}$  and 1 GHz bandwidth), able to drive the VCSEL. Finally the pulses are injected through a decoupling capacitor used to separate the bias.

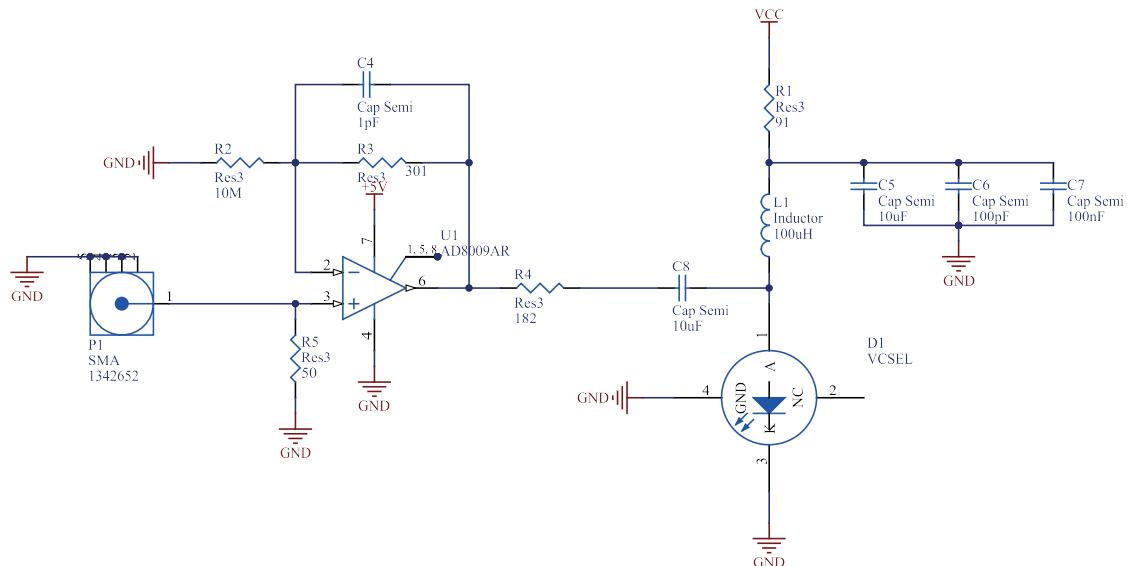


Figure 7.18: Schematic of the optical transmitter implemented with a discrete VCSEL

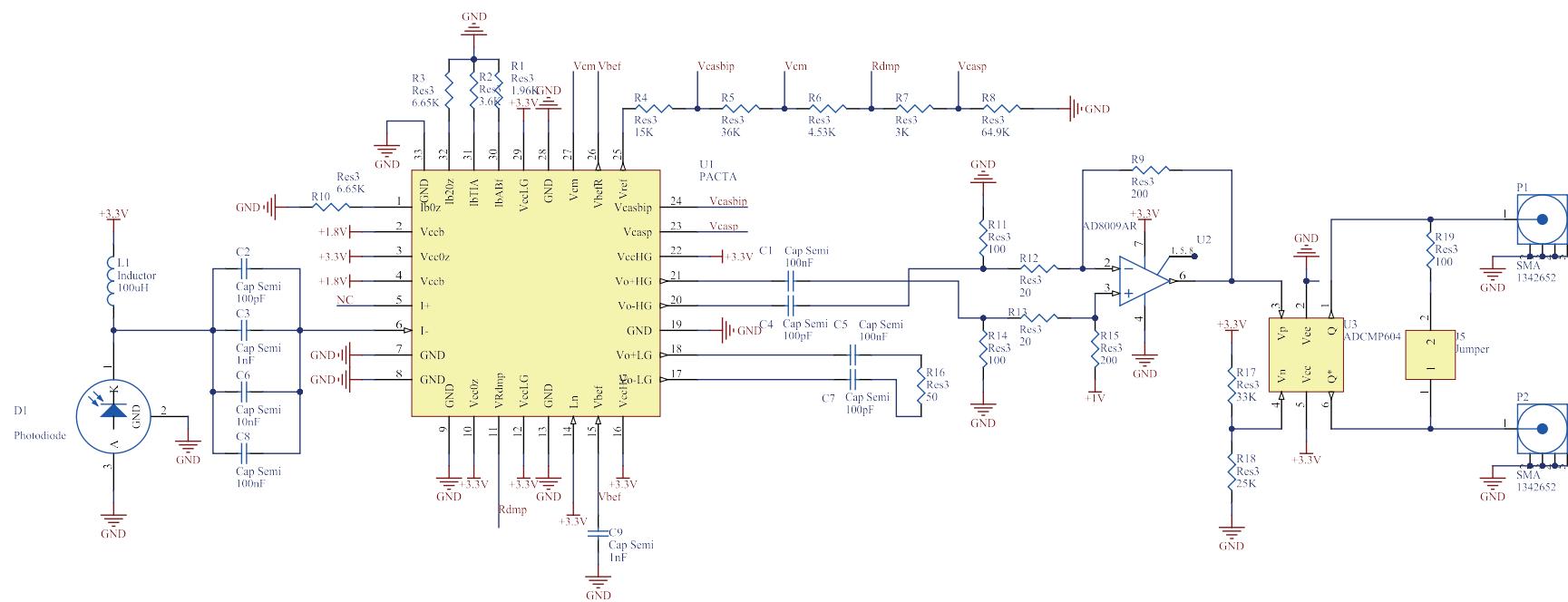


Figure 7.19: Schematic of optical receiver designed with a discrete photodiode

The design of the receiver is somewhat more complicated. The photodiode chosen was the S5973-01 from Hamamatsu [150], also with 1 GHz bandwidth and assembled into the LC housing by AFE. First the current signal from the photodiode is introduced into a PACTA [95] transimpedance amplifier. The output of the PACTA is a differential voltage signal, which is converted into single-ended with an AD8009 configured as a subtractor (the scheme is similar to the one described in section 4.2). Then the single-ended output is compared with a threshold with an ADCMP604, which generates the LVDS output. All the receiver circuit is shown in figure 7.19

### 7.4.3 External delays

As it was previously explained in sections 7.2.1.3 and 7.4.4.1, the camera trigger at the output of the TIB must be generated a long<sup>9</sup> and fixed time after the local Level 1 trigger arrives. This delay must be as accurate as possible to know in which cells of the analog memory buffer the signal is. These requirements for the *Delayed\_local* signal make inadvisable to delay it with the flip-flop chains described in 7.4.4.2: first because the accuracy with those delay lines can not be better than 2.5 ns, and second because it would be a waste of logic resources for a delay which, in principle, does not need to be programmable.

Several options have been tested to implement the long asynchronous delay:

- The most obvious way to implement a long delay is to use a long transmission line. Using an optical link like the ones described in section 7.4.2 and a long optical fiber, it should be possible to obtain a very accurate fixed delay. However, this solution would be very bulky because a reel of around 500 m of optical fiber would be required for each telescope.
- The programmable delay line 3D3428-15 from Data Delay Devices inc. [151] can add delays of up to 3825 ns in steps of 15 ns, in a single chip.
- The chip DS1123L-200, from Maxim Integrated [152], is able to add a delay of 512 ns in steps of 2 ns. So, a chain of 8 of this chips connected in cascade, should be able to add up to 4  $\mu$ s.

The possibility to use external chip delays was studied in depth during the first steps of the TIB design. Both delay chips were found to introduce long delays, with a fine precision, high accuracy, low jitter and good stability, according to their data sheets. The 3D3428-15 was preferred, but there were no stock in Europe for this chip, so a chain of 8 DS1123L-200 was included in the first prototype of the TIB. Whatever the solution, it must be tested and characterized, specially in which respects to jitter, as shown in section 7.5.10.

### 7.4.4 FPGA and firmware

Both the interfacing and the stereo trigger functions consist of properly managing fast digital trigger pulses: replicating, delaying, looking for coincidences, counting, etc. These kind of functions are the typical ones which can be performed by an FPGA, so this technology appeared as the natural option to develop the logic of the TIB. As the FPGAs are programmable devices, they do not only provide with a high performance, but also with a great flexibility. Thus, the firmware installed in

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<sup>9</sup>around 3  $\mu$ s

the FPGA can evolve with the aim of improving or implementing new functionalities as the ones commented in section 7.3.

The FPGA chosen for the TIB was the Xilinx Artix-7 X7A100T-3FGG676 (figure 7.20, [153]) for several reasons:

- It belongs to the newest FPGA Series at the moment of developing the TIB, which means more time until it will become obsolete. As the CTA telescopes will have to work during 20 years, this is an important point.
- The Artix 7, being the less powerful FPGA family of the 7 Series, is the most suitable for the TIB, which does not require very high computing power. On the other hand, Artix 7 family is optimized to reduce its power consumption, which is important for all the systems installed in the camera.
- Despite the TIB does not need high computing power, it requires high speed, specially to implement accurate programmable delays as will be described in subsection 7.4.4.2. The standard synchronous logic inside the selected FPGA can work with clock frequencies as high as 500 MHz.
- The selected FPGA has 676 pins, which can be very useful to manage additional interfaces to implement advanced features.

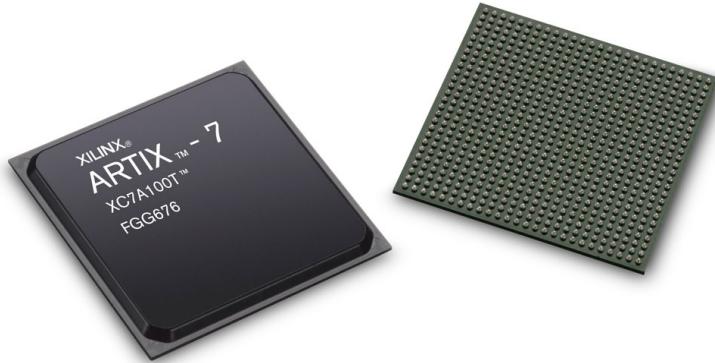


Figure 7.20: Xilinx Artix-7 FPGA

The firmware running in the FPGA contains several logic modules implemented in VHDL. The code can be consulted in [154], but in the following subsections a high level description of the most important modules is presented.

#### 7.4.4.1 High level architecture

Figure 7.21 shows a general scheme of the firmware modules implemented in the FPGA. Some functions are programmed directly using libraries provided by Xilinx [155]. For instance, the local Level 1 trigger input is replicated to be sent to the neighbours by using the FPGA input and output buffers. In a similar way, the internal clock frequencies (4 KHz, 50 MHz, 100 MHz and 400 MHz) are obtained from the external 10 MHz input clock by means of the internal PLLs [156], properly

configured with the Xilinx Core Generator [157] and one simple frequency divider. Nevertheless most of the specific functions of the TIB require the development of specific firmware modules.

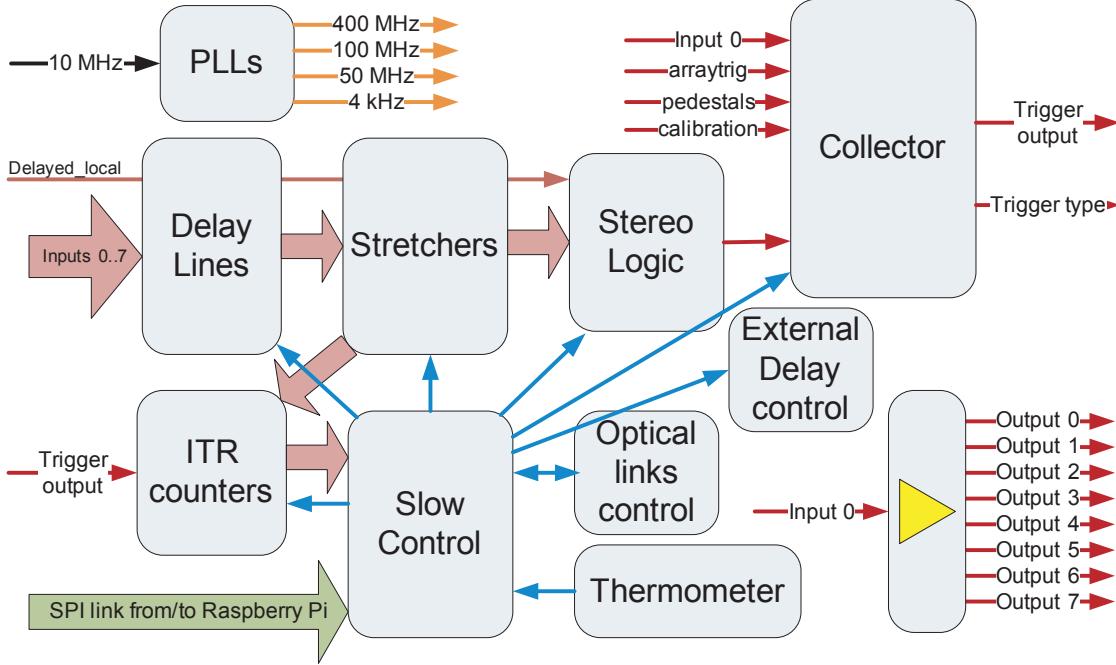


Figure 7.21: TIB firmware architecture

The stereo logic involves 3 logic modules. First, the local Level 1 trigger input from the central backplane and the inputs from the neighbour telescopes (up to 8) are delayed a programmable number of clock cycles to compensate the delays due to the cable lengths and the pointing direction, as was mentioned in section 7.2.1. The 9 delayed signals are then connected to 9 programmable stretchers, which extend the duration of the trigger pulses until making them as wide as the coincidence window. Then, the delayed and stretched trigger inputs are sent to the stereo logic module which has a counter which is able to provide the number of active inputs for every rising edge of the 400 MHz clock. If the count is greater than a programmable trigger condition, a stereo trigger will be generated. However, to be consistent with what was explained in section 7.2.1.3, the camera trigger pulse is not generated just when the condition is accomplished but it is synchronized with a delayed copy of the local input named “Delayed\_local” in figure 7.21.

Once the stereo trigger is generated in the stereo logic module, it is sent to the collector, which is essentially an OR gate that generates a trigger output when the stereo trigger or other input is active. Depending on the input that caused the trigger output, the collector module generates the corresponding trigger type which is sent to the central backplane and to the clock board as described in section 7.1.1. With the aim of being also able to work only with local triggers in mono mode, or to disable the different trigger inputs, the collector also receives a mask to enable/disable each input.

The delay for each input, the coincidence window, the trigger condition and other parameters are configured by the slow control module, which receives these parameters from the Raspberry Pi through an SPI link. Additionally, the trigger inputs and the trigger output are sent to a set of counters which monitor the trigger rates. These rates can be read by the slow control module,

providing with valuable feedback to select the thresholds, choose a suitable trigger condition or to detect failures. Finally, the slow control module is also able to monitor and control the status of the optical links, to configure the external delay and to monitor also the temperature from a chip thermometer.

The following subsections explain some technical details of the most complex modules:

#### 7.4.4.2 Programmable delay lines

The programmable delay lines used to delay each input a different amount of time, are based on chains of flip-flops as the one shown in figure 7.22. With every clock cycle, the signal present at the input of each flip-flop passes to the output. So an input pulse requires as many clock cycles as flip-flops in the chain to go through all the flip-flops and reach the output. This means that, with this structure, the amount of delay is as accurate as one clock cycle, so high clock frequencies are required to get a fine delay tuning. A clock frequency of 400 MHz was chosen, obtaining a resolution of 2.5 ns in the delay adjustment. Additionally, the input pulses do not reach the output exactly after  $N \cdot T_{clk}$  ns, but introducing certain jitter. This jitter results from the fact that the flip-flop outputs can only be updated synchronously with the clock leading edge, while the input pulses can happen at any time. Thus, the input pulse will reach the output of the first flip-flop after an unknown amount of time between 0 and 2.5 ns depending on the arrival time of the input pulse with respect to the rising edge of the clock. Nevertheless, as the delayed outputs from the delay lines are only used to check for coincidences inside a time window of several tens of nanoseconds, and the camera trigger output is synchronized with the local Level 1 trigger, an uncertainty lower than 2.5 ns is not very harmful for the trigger performance. It is also worth to mention that the input pulses will never be narrower than 2.5 ns, so they will always be captured by at least one leading edge of the clock.

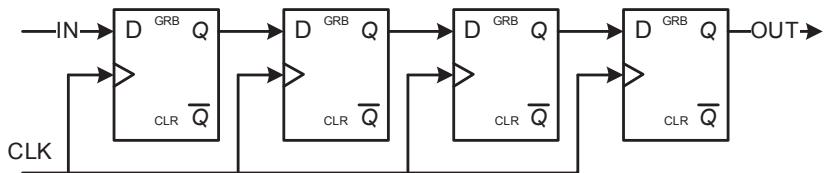


Figure 7.22: Delay line implemented with a chain of flip-flops

The delays introduced by the delay lines can be as long as 4000 ns, which means that the chains should have at least 1600 flip-flops. The first obvious solution to be able to select every possible amount of delay is to connect each flip-flop output to the input of a 1600-input multiplexer. Such a multiplexer does not exist inside the FPGA, so it should be implemented as a multilevel hierarchy of 8 and 4-input multiplexers. A complicated structure like that is not a good solution from a timing point of view, because the output signal from the selected flip-flop would have to go through many multiplexers in cascade and reach its destination in a single clock cycle. So in order to avoid the 1600-input multiplexer, a logarithmic structure like the one shown in figure 7.23 was designed.

The amount of delay which should be added by the delay line is configured by the slow control module by means of a 12 bits word. So, every bit set to “1” introduces a delay correspondent to  $2^p$  clock cycles, being  $p$  the position of the bit in the 12 bits word. If the flip-flops in the chain are set

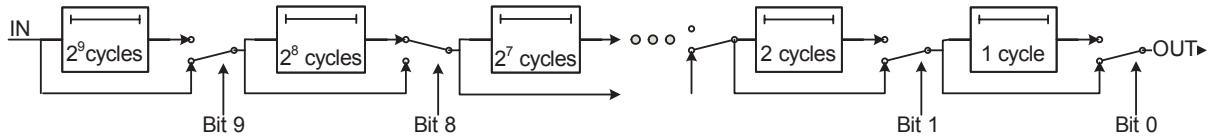


Figure 7.23: Logarithmic delay line

in subchains of powers of 2 units as shown in figure 7.23 and the bits of the control word are used to connect these subchains to the signal path or to bypass them, the output of the chain provides with the desired delayed output, just with 11 2-inputs switches. Only 11 from the 12 bits of the delay word are used, providing with an adjustment capability of up to 2048 clock cycles (i.e. 5120 ns at 400 MHz). Moreover, as the longest delays can only be applied to the local input (the inputs from the neighbours have an inherent delay due to the travel through the optical fibers), the delay lines used in the neighbour inputs only use 10 bits and comprise 1024 flip-flops instead of 2048, saving logic resources.

#### 7.4.4.3 Stretchers

The stretchers are used to make the pulses coming from the delay lines as wide as the coincidence window. The duration of the coincidence window is programmable by means of a 6 bit number configured by the slow control module, which expresses the duration in clock cycles. The stretchers use the same 400 MHz clock used for the delay lines, so the finest resolution is limited to 2.5 ns. In fact, the stretchers use a delay line like the ones described in section 7.4.4.2 to produce the stretching, but with 6 bits instead of 10 or 11. A copy of the input pulses is sent to the input of this delay line, obtaining at the output a delayed signal. Both the delayed signal and the original input feed the state machine shown in figure 7.24.

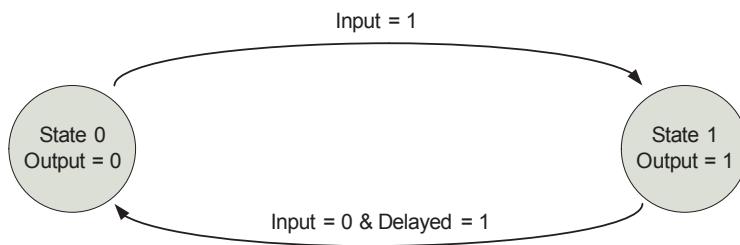


Figure 7.24: Diagram of the state machine running in the stretcher modules

After the FPGA reset, the state is 0, as well as the output of the stretcher. When the input changes to “1”, the state machine changes to State 1, and the output changes immediately to “1”. This situation remains until the delayed input coming from the delay line changes to “1” and only if the non-delayed input has already changed to “0”. This means that:

- If the input is narrower than the coincidence window (as usually expected), the output pulse width is the coincidence window duration.
- If the input is wider than the coincidence window, the output width is similar to the input width.

If the input pulses arrive at the stretchers separated by less than the coincidence window width, this scheme does not work properly, so that the system can consider several close input triggers as a single one, or to produce outputs shorter than the coincidence window. This situation would mean that a high pulse rate is present at the output of the stretchers, which will be detected by the ITR counters (see section 7.4.4.6), which in turn will be read by the slow control system, which will take the appropriate measures.

#### 7.4.4.4 Stereo Logic

The delayed and stretched inputs from the local and the neighbour telescopes are sent to the Stereo Logic module, which generates a stereo output if the trigger condition is accomplished. The trigger condition consists of having coincident triggers in the local telescope and in one or more neighbours during the coincidence window. This is implemented by connecting the inputs to a fast counter which provides, with every leading edge of the 400 MHz clock, the number of inputs which are set to “1”. The result of the counter is expressed as a 4 bits number, which is compared with the number of coincident triggers required to satisfy the trigger condition. The trigger condition can be reconfigured in a very simple way, just modifying this number by slow control. If, besides satisfying the required number of coincidences, one of the coincident inputs is the local one, the signal named “*Stereo\_trigger*” in figure 7.25 is generated.

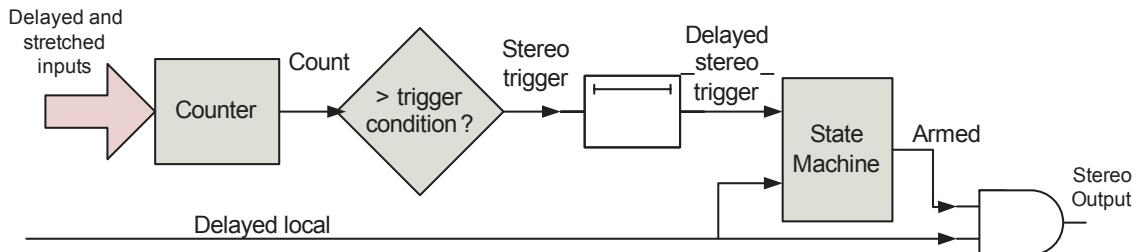


Figure 7.25: Stereo logic block diagram

However, as was previously said in subsections 7.4.4.1 and 7.2.1.3, the Stereo Output cannot be simply generated when the stereo trigger condition is accomplished. Instead, it must be generated a fixed time after the local trigger, i.e. synchronized with the signal named “*Delayed\_local*” in figures 7.21 and 7.25. To do this, the *Stereo\_trigger* signal is sent to a programmable delay line as the ones described in section 7.4.4.2 and, once delayed it feeds a state machine which generates an “*Armed*” output. When this *Armed* signal is set to “1”, a stereo output is generated when *Delayed\_local* appears.

The delay line is required to set *Armed* = 1 only some tens of nanoseconds before the expected arrival of *Delayed\_local*. Of course it is impossible to know accurately when the stereo trigger condition is going to be accomplished and therefore when *Armed* is going to be set to one (it can happen at any time inside the coincidence window). However, what it is possible is to know how much time the local trigger is being delayed in the Programmable Delay Lines module to compensate the neighbour’s delays before checking for coincidences and how much delay is introduced in the *Delayed\_local* path. Thus, introducing an additional delay of  $T_{stereotigger}$  ns, calculated according to equation 7.8, it is possible to ensure that *Armed* will be set to “1” between  $T_{coincidencewindow} + T_{securitymargin}$  ns and  $T_{securitymargin}$  ns before the arrival of *Delayed\_local*.

$$T_{stereotigger} = T_{delayedlocal} - T_{coincidences} - T_{coincidencewindow} - T_{securitymargin} \quad (7.8)$$

Figure 7.26 illustrates this calculation. If *Stereo\_trigger* is not delayed, *Armed* could be activated a long time before the arrival of the corresponding *Delayed\_local* pulse and this could cause the acceptance of previous local triggers which did not comply with the coincident condition as stereo ones. On the contrary, if *Armed* is set to “1” just a few nanoseconds before the time at which *Delayed\_local* is expected, is very unlikely that a local trigger different from the one which caused the coincidence could be accepted.

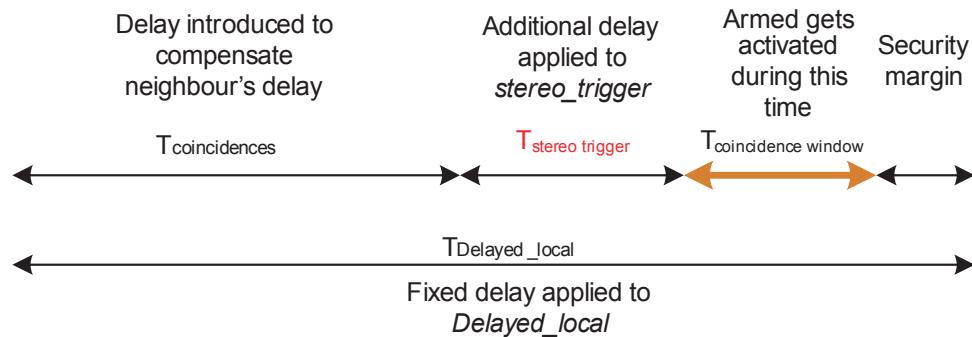


Figure 7.26: Stereo trigger delay scheme

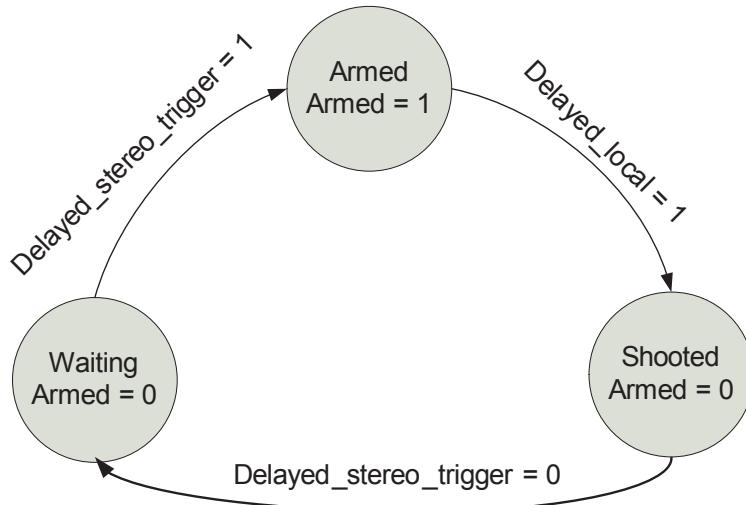


Figure 7.27: State machine which controls the generation of the *Armed* signal

Regarding the state machine which controls the activation of the *Armed* signal, its scheme is shown in figure 7.27. It is more complicated than just setting *Armed* to “1” when *Delayed\_stereo\_trigger* arrives, with the aim to produce only one stereo trigger when the trigger condition is accomplished during a long time. Thus, starting from the *waiting* state, it changes to *armed* when *delayed\_stereo\_trigger* appears. Then, when *Delayed\_local* arrives and generates the Stereo Output the state changes to *shoted*, setting *Armed* to “0”. In this state, *Delayed\_stereo\_trigger* must be “0” to make the state machine go back to *waiting* state and then being ready to get armed again.

So, if the trigger condition is fulfilled during a long time, the state machine remains in *shooteed* state, avoiding several triggers to be generated for a single long event.

#### 7.4.4.5 Collector

The Collector module implements the interfacing function with the different trigger origins, generating the *trigger\_output* signal every time a trigger comes from any of the inputs. Thus, the trigger output is implemented in a simple way with a 5 input OR gate and an AND gate, as it is shown in figure 7.28.

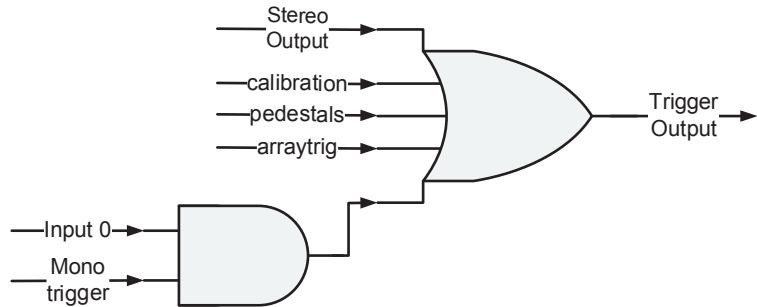


Figure 7.28: Trigger output generation in the collector module

The AND gate allows to generate a trigger output directly from the local telescope trigger (*Input 0* signal), whenever the mono trigger mode is selected, as will be the case in the MSTs. It is important to notice that, whatever the input, the trigger output is generated in a completely asynchronous way, keeping the timing information in the leading edge of the trigger output and introducing very low (24ps RMS). For the trigger type generation, the input trigger signals are copied and stretched in order to work with them synchronously with the state machine of figure 7.29.

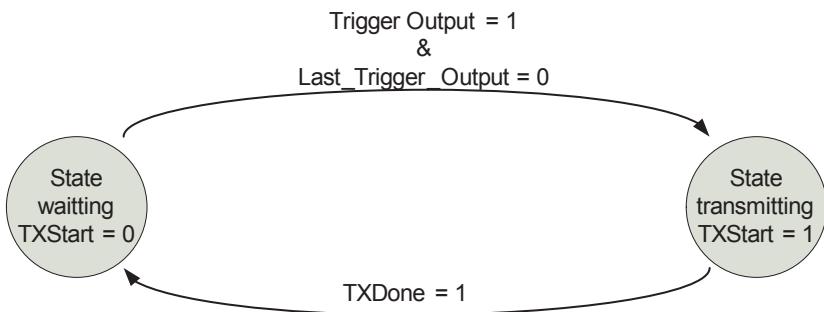


Figure 7.29: State machine which controls the generation and transmission of the trigger type information

When the stretched copy of the trigger output signal changes from “0” to “1”, the 3 bits of the trigger type corresponding to the effective triggering input are calculated, and then a signal called *TXStart* is set to “1”, indicating to the SPI module<sup>10</sup> that there are data to transmit. From this moment, the state machine ignores the possible new triggers, remaining in the *transmitting* state

<sup>10</sup>The SPI module is a free implementation.

until the SPI module finishes transmitting the trigger type. Then, The SPI sets to “1” a signal named *TXDone*, indicating to the collector module that it is ready to accept new transmissions. It is worth to say that the collector state machine works with the 400 MHz clock, evaluating the different variables every 2.5 ns, while the SPI module receives a 50 MHz clock for its state machine, sending the bits at 10 MHz.

#### 7.4.4.6 ITR counters

The Individual Telescope Rate (ITR) counters are a set of counters in charge of counting the number of input triggers from each telescope (local and neighbours), as well as output triggers, during a certain period of time, with the aim to provide the slow control module with information to calculate the trigger rates. The trigger rate monitoring is very important to set the Level 1 thresholds and the trigger condition to the lowest possible levels, while maintaining the trigger rate below the maximum telescope readout rate<sup>11</sup>.

The design of digital counters entails a compromise between the number of bits of the counter and the maximum counting speed. As it has been represented in figure 7.30, the counter is composed by a chain of 2 bit adders. The time between one addition and the next one must be long enough to allow a carry bit to ripple through the whole chain of full adders and to have the result ready at the input of the counters to start the next addition. Thus, the more bits in the counter, the longer the time required to propagate the carries and the lower the maximum frequency at which the counter can work<sup>12</sup>.

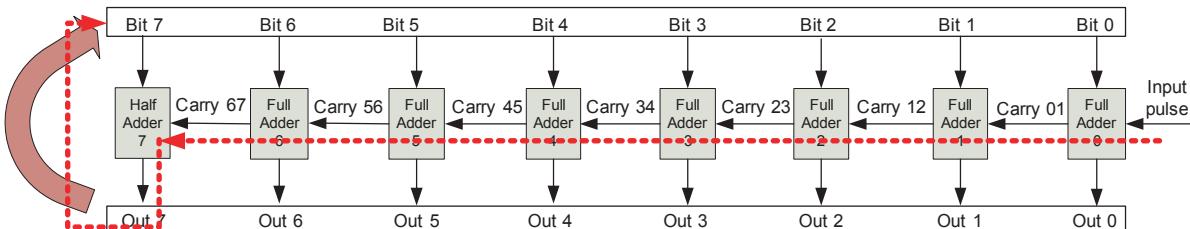


Figure 7.30: Structure of an 8 bit ripple-carry counter

In the particular case of the ITR counters, the inputs will be separated by some  $\mu$ s during normal operation (i.e. the expected trigger rates are below 1 MHz). If the counters are fed with the input pulses after going through the stretchers, the pulses to be counted will be long enough to allow the counters to work at lower frequencies, and therefore to reach higher ranges. The coincidence window, and the correspondent pulse width of the stretched pulses will be around 50 ns, but it is programmable so, in order to have some safety margin, a minimum pulse width of 10 ns has been considered. Assuming this condition, the counters have been designed to have 8 bits and being updated at 100 MHz. Every 10 ns each counter checks if its input has changed from “0” to “1”. If so, they increment the account, otherwise they do nothing.

In principle, the counters are read-out and reset to 0 every 250  $\mu$ s (4 kHz rate), so they are useful to monitor rates between 4 kHz and around 1 MHz. If the rate is higher, the counters maintain their

<sup>11</sup>Limited by the dead time

<sup>12</sup>For this reason it is not possible to implement the delay lines described in section 7.4.4.2 by counting the number of clock cycles.

maximum value ( $2^8 - 1 = 255$ ), so the slow control module will know that the rate is too high and it will take the appropriate actions. If it were required to measure higher or lower trigger rates, it would be possible to do it just by changing the frequency at which the counters are read and reset.

#### 7.4.4.7 SFP control

The optical links used to send and receive triggers to/from the neighbours, as well as the calibration and pedestal signals, are implemented in the first TIB prototype by means of TX/RX SFP modules [146], which provide with several bits to monitor and control the link status:

- ***TX\_Disable***: When the FPGA sets this bit to “1”, the optical transmitter is switched off.
- ***TX\_Fault***: If a laser fault happen, the SFP module sets *TX\_Fault* to “1”, and disables the laser.
- ***RX\_LOS***: A Loss of Signal (LOS) bit indicates that the received optical power is too low to recover the signal, due to a disconnected or broken fiber, switched off transmitter or other reason.

The SFP control module simply gathers all these bits from all the SFP modules, forming words which can be read by the slow control module. Additionally, it generates a generic alarm signal directly connected to the Raspberry Pi if any of the control bits is indicating a failure. In this way, the slow control module does not need to read the SFP status periodically, but only when a problem is detected.

#### 7.4.4.8 External delay control

In the first TIB prototype, the external delays described in section 7.4.3 are implemented with a chain of Maxim DS1123LE-200 [152] programmable delay chips. These chips need to be configured by sending an 8-bits word to each chip through an SPI link. All the chips share the clock, MISO and MOSI lines, while they have independent chip selects. With the aim to handle these links and send the configuration information properly, a firmware module was implemented. This module receives from the slow control nine 8-bit words (one for each chip) and a signal indicating when the configuration of all the chips must be updated (*Write\_ex\_dels*). When the updating command arrives, the module sends the 8-bit word to one chip after the other until programming all of them. Figure 7.31 shows the state machine of the firmware module.

The process of updating the configuration uses a variable  $n$  to select each chip. Thus, when coming from *Waiting* state, the chip corresponding to  $n=0$  is updated in the *Writing* state ( $TX\_start=1$  starts the SPI communication). Then, when that message has been sent, *TX\_done* changes to “1” and the state changes to *Handshaking*. This state increments  $n$  and in the next step the state changes to *Writing* again to send the configuration message to the next chip. The process is repeated until programming all the delay chips. Then the state comes back to *Waiting*.

With the aim to initialize all the chips with a known value after the reset of the system, the state is set to *Writing* instead of *Waiting*, so the initial values are loaded.

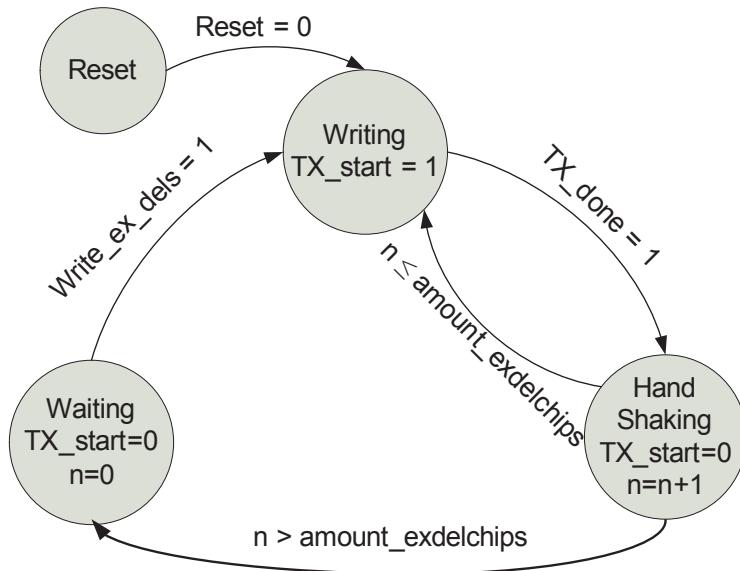


Figure 7.31: External delay control state machine

#### 7.4.4.9 Thermometer

The trigger interface board is equipped with a TC77 [158] chip thermometer, readable by a SPI interface. The thermometer firmware module is in charge of controlling this SPI interface, reading the temperature every  $250 \mu\text{s}$  and writing the data in a register accessible by the slow control module.

#### 7.4.4.10 Slow control module

The Slow Control firmware module implements an slave SPI interface which allows the Raspberry Pi to read and write 32 bit words. These words are composed of an 8-bit prefix which defines what information is being read or written and 24 data bits. Table 7.2 contains the different codes and the data corresponding to each one.

Prefix	Data bits	Information	Read/written by the Raspberry Pi
0x00			
0x01	12 LSB	Local trigger delay, in clock cycles	Written
0x02	12 LSB	Neighbour 1 trigger delay, in clock cycles	Written
0x03	12 LSB	Neighbour 2 trigger delay, in clock cycles	Written
0x04	12 LSB	Neighbour 3 trigger delay, in clock cycles	Written
0x05	12 LSB	Neighbour 4 trigger delay, in clock cycles	Written
0x06	12 LSB	Neighbour 5 trigger delay, in clock cycles	Written
0x07	12 LSB	Neighbour 6 trigger delay, in clock cycles	Written
0x08	12 LSB	Neighbour 7 trigger delay, in clock cycles	Written
0x09	12 LSB	Neighbour 8 trigger delay, in clock cycles	Written
—	—	—	—

0x11	12 LSB	Output trigger duration, in clock cycles	Written
—	—	—	—
0x20	7 LSB	Coincidence window, in clock cycles	Written
0x21	4 LSB	Trigger condition, in number of coincidences	Written
0x22	8 LSB	If =0xFF, mono trigger enabled	Written
0x23	12 LSB	Additional delay $T_{stereotigger}$ , in clock cycles	Written
—	—	—	—
0x30	8 LSB	Stereo count, for rate monitoring	Read
0x31	8 LSB	Local trigger count, for rate monitoring	Read
0x32	8 LSB	Neighbour 1 trigger count, for rate monitoring	Read
0x33	8 LSB	Neighbour 2 trigger count, for rate monitoring	Read
0x34	8 LSB	Neighbour 3 trigger count, for rate monitoring	Read
0x35	8 LSB	Neighbour 4 trigger count, for rate monitoring	Read
0x36	8 LSB	Neighbour 5 trigger count, for rate monitoring	Read
0x37	8 LSB	Neighbour 6 trigger count, for rate monitoring	Read
0x38	8 LSB	Neighbour 7 trigger count, for rate monitoring	Read
0x39	8 LSB	Neighbour 8 trigger count, for rate monitoring	Read
—	—	—	—
0x40	10 LSB	SFP enables	Read
0x41	10 LSB	SFP TX_Fault	Read
0x42	10 LSB	SFP LOS, Loss of Signal	Read
—	—	—	—
0x50	13 LSB	Temperature	Read
—	—	—	—
0xF0	8 LSB	Unknown prefix	Read

Table 7.2: Slow control registers

When an SPI message is received and its prefix does not correspond to a defined one, the slow control module sets an alarm line directly connected to the Raspberry Pi to “1”, and writes the unknown received prefix in the 0xF0 address. In this way, the Raspberry Pi can read what was received, which can be useful for debugging.

Another useful function of the slow control module is to write the initial values of the different parameters, before receiving them from the Raspberry Pi. This allows to test the different functionalities, even without the Raspberry Pi (see section 7.4.5.2). With the aim to have the updated information about the slow control always accessible, a wiki page has been created [159].

#### 7.4.5 Raspberry Pi

The TIB contains a Raspberry Pi micro-computer (figure 7.32), which is in charge of the FPGA configuration during the booting of the system and the slow control communication. In spite of its small size and very low price<sup>13</sup>, the Raspberry Pi is a complete PC running a Linux operating

<sup>13</sup>Around 30 €at the time when this thesis was written.

system<sup>14</sup> which is stored in an SD card used as hard disk [160]. It has several buses: two USBs, one RJ45, several general purpose pins, one audio connector and even an HDMI. In the case of the TIB, the Ethernet interface will be used to communicate with the camera slow control system, while the General Purpose Input/Output (GPIO) pins are used to interface with the FPGA.



Figure 7.32: Photograph of a Raspberry Pi micro-computer

#### 7.4.5.1 Interface with the FPGA

The Raspberry Pi have 26 pins in its GPIO interface, assigned to different signals as shown in table 7.3.

The signals can be divided in several groups:

- SPI MOSI, SPI MISO, SPI clock, SPI Chip Select 0 (CS0) and SPI Chip Select 1 (CS1) constitute an SPI interface able to control two SPI devices. In fact, all the lines are connected to the FPGA: CS0 is active during the transmission of the FPGA configuration file in the initialization (see section 7.4.5.2), while CS1 is used during the transmission of the slow control parameters. In both cases the Raspberry Pi is the master, while the FPGA is the slave device, which means that the clock is generated by the micro PC.
- I2C serial data (SDA) and I2C clock implement an I2C standard link connected to the FPGA. This interface is not currently used, but the lines are reserved for future uses.
- UART TX and UART RX can be used to implement a serial communication interface between the Raspberry Pi and the FPGA. As in the case of I2C, it is not currently used but reserved for future uses.

---

<sup>14</sup>We choose the most popular distribution optimized for Raspberry Pi, called Raspbian [161]

Pin	Function	Pin	Function
1	+3.3 V Power supply	2	+5 V Power Supply
3	I2C[162] Serial Data	4	+5 V Power Supply
5	I2C Clock	6	Ground
7	SPI error	8	UART <sup>15</sup>
9	Ground	10	UART receiver
11	Reset out	12	Program B
13	Temperature alarm	14	Ground
15	SFP_alarm	16	INIT B
17	+3.3 V Power supply	18	DONE
19	SPI MOSI	20	Ground
21	SPI MISO	22	RESET
23	SPI clock	24	SPI Chip Select 0
25	Ground	26	SPI Chip Select 1

Table 7.3: Raspberry Pi GPIO pinout

- PROGRAM B, INIT B, RESET and DONE are used during the initialization. See section 7.4.5.2
- Programmable inputs are used for managing alarms.
- Pin 11 is a programmable output used for resetting the default values in the FPGA.
- +5 V is an input power supply, while +3.3 V is an output power supply for low power demanding devices.

#### 7.4.5.2 FPGA-initialization

The Xilinx Artix 7 FPGAs can be configured in different ways. Taking advantage of the presence of the Raspberry Pi, the so called “slave serial mode” has been chosen [163]. According to this configuration scheme, the Raspberry Pi sends the firmware to the FPGA during the initialization by means of an SPI interface. Figure 7.33 shows the connections between the Raspberry Pi (labeled as *Microprocessor or CPLD*), the FPGA and the JTAG connector. *CCLK*, *DIN* and *PROGRAM\_B* correspond to the 3 typical SPI lines, clock, data and chip select respectively. The Raspberry Pi plays the role of master in this communication, generating the clock.

The JTAG connector provides with an alternative and effective way to load the firmware in the FPGA and run tests. In the first prototypes of the TIB an external JTAG connector is present in the front of the box with the aim to debug problems. In the final Trigger Interface Boards it will be an internal connector.

#### 7.4.5.3 Interface with the slow control unit

The Raspberry Pi is in charge of communicating with the central camera slow control unit, using the Ethernet camera network. This interface requires coordination with several CTA teams working

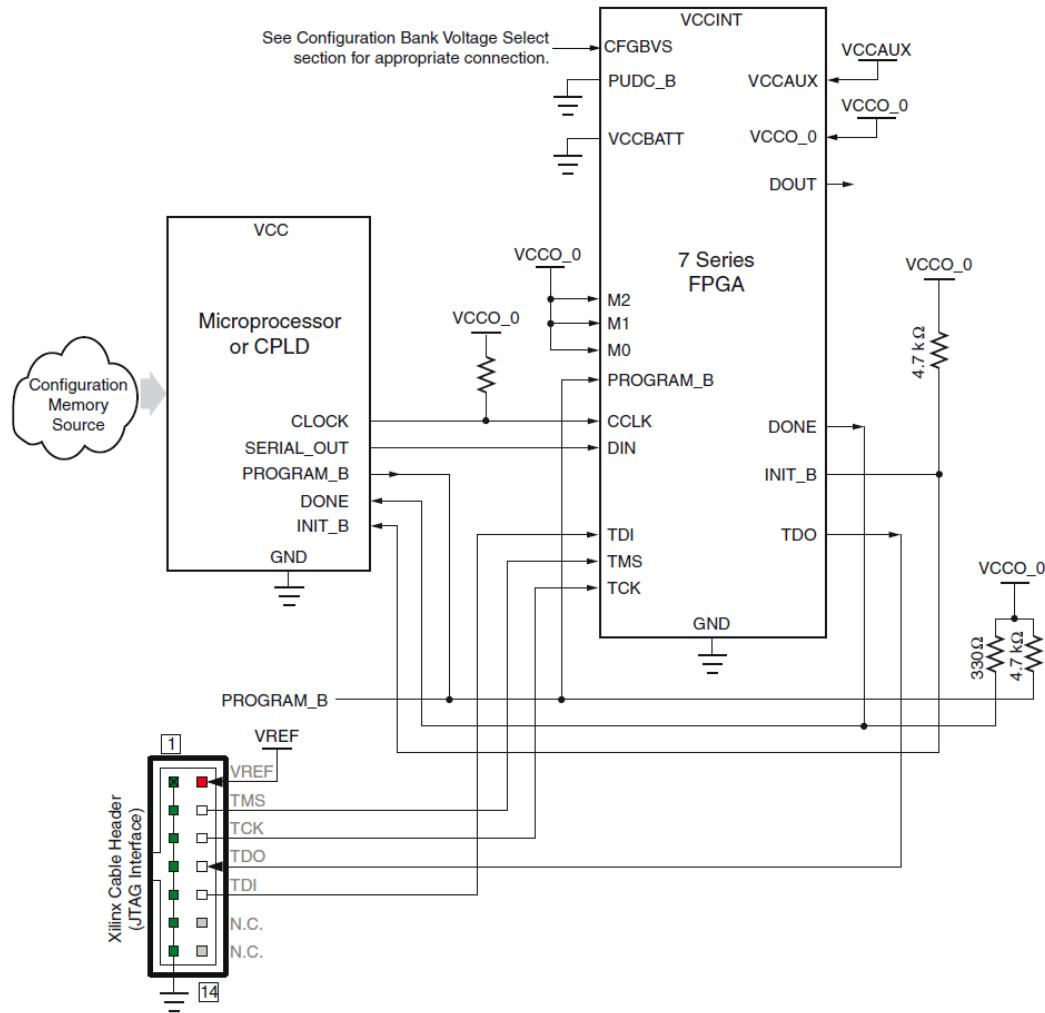


Figure 7.33: Slave serial mode FPGA configuration scheme [163]

on this issue and it was still under definition by the time this thesis was written. However, some guidelines have been given to develop the slow control software. The most important decision has been to use OPC-Unified Architecture [164] as the base communication architecture. OPC-UA works efficiently to control different parts, whether they are simple or complex, and is multiplatform, offering different APIs for software development. The Raspberry Pi will run an OPC-UA server implementation for the Java virtual machine.

#### 7.4.5.4 Other functions in the Raspberry Pi

Apart from interfacing the FPGA and the camera slow control system, the computing power of the Raspberry Pi is very useful to perform certain functions and calculations locally, reducing the workload of the camera slow control. Some of these additional functionalities are:

- Calculation of the number of clock cycles that every trigger input must be delayed, depending

on the pointing direction. The camera slow control can send the pointing direction or directly the delay in ns, and the Raspberry Pi calculates the delays in clock cycles.

- Centralization of the alarms. The Raspberry Pi checks periodically the trigger rates, the status of the optical links and the temperature, warning the central slow control only if necessary.
- SSH accessibility, useful for debugging.

#### 7.4.6 Power supply

The Trigger Interface Board receives a single +24 V DC power supply from the camera power supply system. From this voltage, the power must be provided to the different subsystems, which require different supply voltages. Table 7.4 shows the power consumption requirements of the different active hardware elements. In order to satisfy the power requirements efficiently, a two levels power supply system has been designed, according to the diagram shown in figure 7.34.

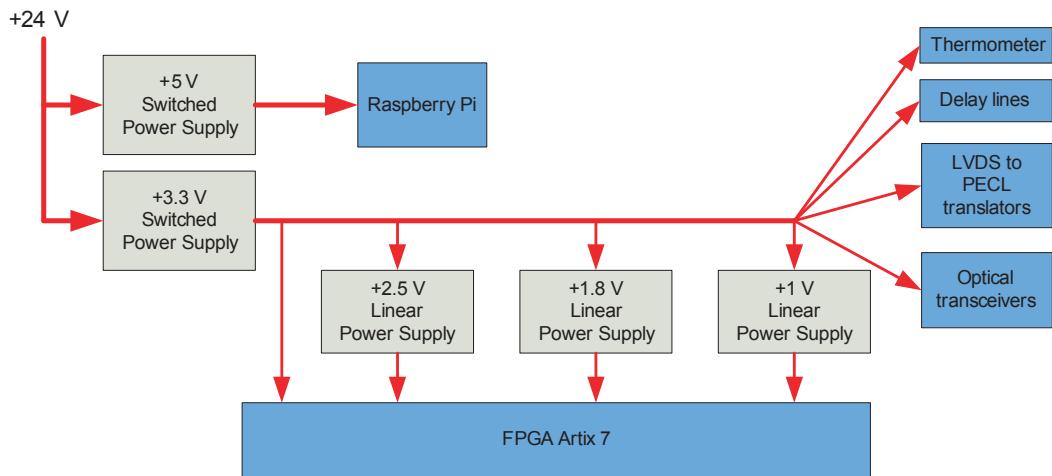


Figure 7.34: Block diagram of the TIB power supply system

As the most demanding power supply voltages are the +5 V and the +3.3 V, two switched DC-DC modules have been used to generate them from the +24 V general supply. This first step from +24 V must be done with switched DC-DCs because the voltage drop is too high to use linear regulators efficiently. On the other hand, the +2.5 V, +1.8 V and + 1 V are generated from +3.3 V by means of less noisy linear regulators. The Trigger Interface Board is not very sensitive to the noise in the power supply because it is a digital design where the most important signals are differential, so the switched noise introduced by the DC-DCs is not critical. Nevertheless, the noise in the power supplies has been measured and the results are shown in section 7.5.1.

The different power supply modules have been designed with the Webench Power Designer online tool from Texas Instruments [165]. Their schematics, as well as the schematics of all the TIB hardware modules can be seen in appendix A.2. Table 7.5 summarizes the most important characteristics of the designed power supplies.

<b>Component</b>	<b>+5V</b>	<b>+3.3V</b>	<b>+2.5V</b>	<b>+1.8V</b>	<b>+1V</b>	<b>Quantity</b>	<b>+5V</b>	<b>+3.3V</b>	<b>+2.5V</b>	<b>+1.8V</b>	<b>+1V</b>
Raspberry Pi	700 mA					1	700 mA				
Artix 7		21 mA	393 mA	191 mA	73 mA	1		21 mA	393 mA	191 mA	73 mA
Transceiver		220 mA				12		2460 mA			
SN65LVDS100		35 mA				12		420 mA			
SN65LVDS101		61 mA				12		732 mA			
DS1123L		30 mA				9		270 mA			
TC77		0.4 mA				1		0.4 mA			
<b>Total current flowing (mA)</b>							700 mA	4083 mA	393 mA	191 mA	73 mA
<b>Total power consumption (mW)</b>							3500 mW	13475 mW	982 mA	239 mA	73 mA

Table 7.4: Expected power consumption according to datasheets and FPGA simulations

Output power voltage	Type	Maximum output current	Efficiency
+5 V	Switched	1 A	84 %
+3.3 V	Switched	6 A	93 %
+2.5 V	Linear	500 mA	75 %
+1.8 V	Linear	300 mA	54 %
+1 V	Linear	250 mA	30 %

Table 7.5: Characteristics of the power supplies modules

Taking into account the efficiencies of table 7.5 and the power demands of table 7.4, the global power consumption of the TIB can be estimated according to equation 7.9.

$$\text{Power consumption} = \left( \frac{I_{2.5} \cdot 2.5V}{\eta_{2.5}} + \frac{I_{1.8} \cdot 1.8V}{\eta_{1.8}} + \frac{I_1 \cdot 1V}{\eta_1} \right) \cdot \frac{1}{\eta_{3.3}} + \frac{I_{3.3} \cdot 3.3V}{\eta_{3.3}} + \frac{I_5 \cdot 5V}{\eta_5} = 21.009 \text{ W} \quad (7.9)$$

#### 7.4.7 Temperature monitoring

The Trigger Interface Board includes a TC77 thermometer chip [158], which is read by the FPGA as was explained in subsection 7.4.4.9. Contrary to what it could be expected, the components with the most restrictive operating temperature range are not the transceivers (which have a VCSEL) but the Raspberry Pi [160], the FPGA [153] and the programmable delay lines DS1123LE [152]. Table 7.6 gathers the operating temperature range of the different components, showing an overall temperature range between 0 and +70 °C. The delay line is the most restrictive element, but it is still not clear if the DS1123L will be present in the final versions of the Trigger Interface Board.

Taking into account the temperature limits from table 7.6 and the temperature measured with the sensor, it will be possible to operate the camera cooling system [108] between safety margins.

#### 7.4.8 TIB PCB design

The TIB is a complex board which needs to handle many input and output signals, which in many cases consist of differential pairs. First, there are 24 differential pairs to and from the optical links, and other 32 differential pairs connected to the RJ45 connectors. Additionally, there are single-ended lines for the optical links monitoring, 15 lines for the communication with the Raspberry Pi, 12 for the control of the external delays implemented with the DS1123L and still some more for the JTAG interface and the reading of the thermometer. So many lines connected to the 676 pads FPGA, together with the different power supply rails described in section 7.4.6 required a complex 16 layer PCB design (figure 7.35) which was developed with Altium Designer [166].

The PCB design considered several restrictions such as the delay equalization of the lines coming from the neighbours, the controlled impedance of the differential pairs, the coupling between adjacent lines or the noise from the power supplies. Additionally a 3D model of the board (figure 7.36(b))

Component	Minimum Temperature (°C)	Maximum temperature (°C)
Raspberry Pi	0	+85
Avago AFBR5715 ALZ	-40	+85
SN65LVDS100/101	-40	+85
Xilinx Artix 7 FPGA	0	+100
TC77 thermometer	-55	+125
LP36890DT-2.5	-40	+125
LM22672MR-5.0	-40	+125
CDCV304PWRG4	-40	+85
DS1123L-200	0	+70
LP38691DT-1.8	-40	+125
CSD18534Q5A	-55	+150
B240A-13-F Schottky Diode	-65	+150
LP3878SD-ADJ	-40	+125
LM3151MHE-3.3	-40	+125
Ceramic Capacitors	-30	+ 85
Leds	-55	+85
Fuses	-55	+125
Inductors	-40	+85
Resistors	-55	+125
Electrolitic capacitors	-40	+85
Tantalum capacitors	-55	+105
<b>Global temperature range</b>	<b>0</b>	<b>+70</b>

Table 7.6: Operating temperature range of the electronic components in the TIB

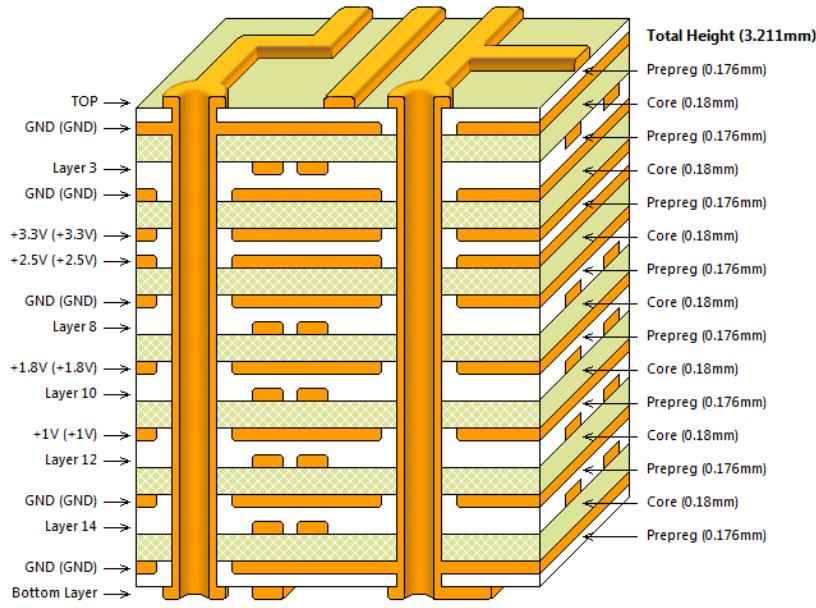
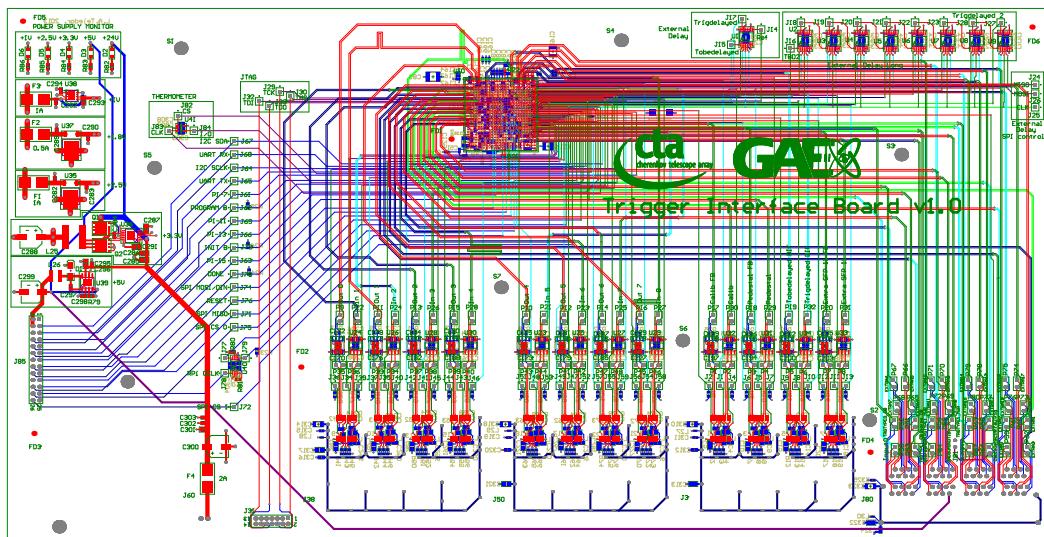
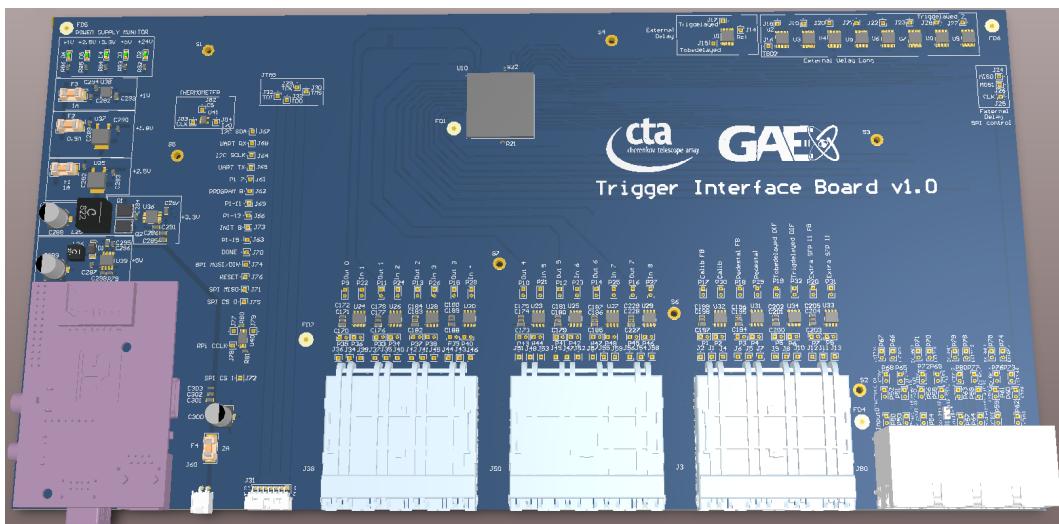


Figure 7.35: TIB prototype PCB stack-up

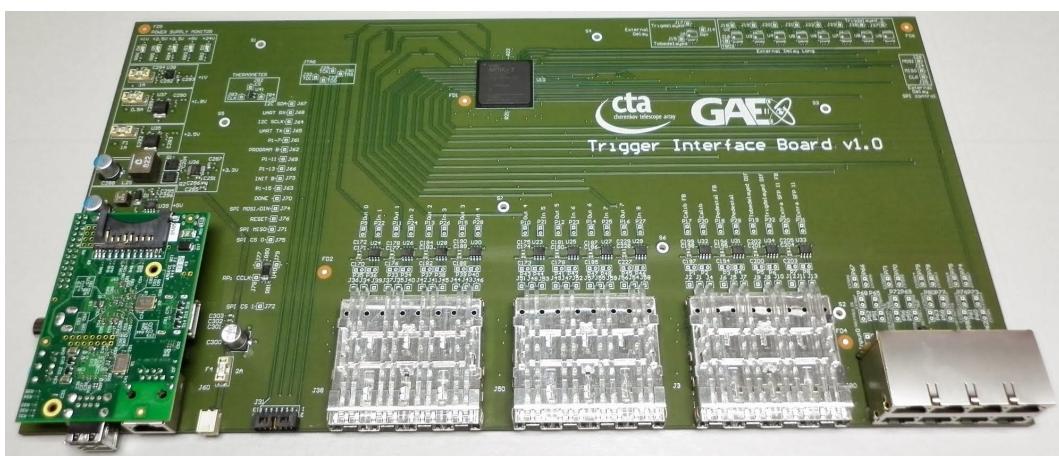
was used to ensure the mechanical compatibility with the rack box. Figure 7.36 shows two views of the board design and a photo of the manufactured prototype.



(a) PCB layout, with the different color lines corresponding to different PCB layers



(b) 3D design



(c) Photo

Figure 7.36: Views of the TIB design and first prototype

## 7.5 TIB measurements

Two boards of the first prototype of the TIB have been manufactured and tested. The goal of this prototype is to test the different functionalities, to improve the FPGA firmware, to develop the slow control software which will run in the Raspberry Pi and finally to provide with a TIB for several CTA camera integration tests which will take place during 2014. In order to perform the tests, the auxiliary boards shown in figure 7.37 were manufactured.

- Board in figure 7.37(a) simulates the central backplane interface.
- Board in figure 7.37(b) mimics the clock board.
- Board in figure 7.37(c) simulates an optical interface.
- Board in figure 7.37(d) is a generic adapter from RJ45 into SMA connectors.

The first three boards include an MCP2200 chip [167] each one, which can generate input pulses controlled by a computer through an USB interface.

The results obtained from these tests and the new requirements requested by the LST and MST camera developers will be taken into account for a second, upgraded, version which should be the one finally installed in the LST and MST cameras. The next sections show the main features tested in the TIB.

### 7.5.1 Power supplies

The first systems to be tested were the power supplies. They work as expected, providing with enough current for the different subsystems. Table 7.7 contains the measured DC voltage levels and the noise, measured as the AC coupled RMS voltages, corresponding to the different power rails (figure 7.38). The table shows that the measured DC levels are very close to the nominal ones and the noise power is very low. Looking at the numbers it is possible to notice that the RMS voltages is higher in the +5 V and +3.3 V power supplies. This is because these two power supplies are switched ones, in contrast to the others which are generated by means of linear regulators. The only problem related with the power supplies is that the +1 V LED indicator does not shine (figure 7.38(d)) because it was not selected properly and its threshold voltage is higher than 1 V.

Nominal voltage	Measured DC (V)	Measured AC RMS (mV)
+5 V	+5.01	4.15
+3.3 V	+3.36	5.37
+2.5 V	+2.55	1.97
+1.8 V	+1.78	2.68
+1 V	+1.09	3.74

Table 7.7: Measured DC voltage and AC coupled RMS voltage for the different voltage rails present in the TIB

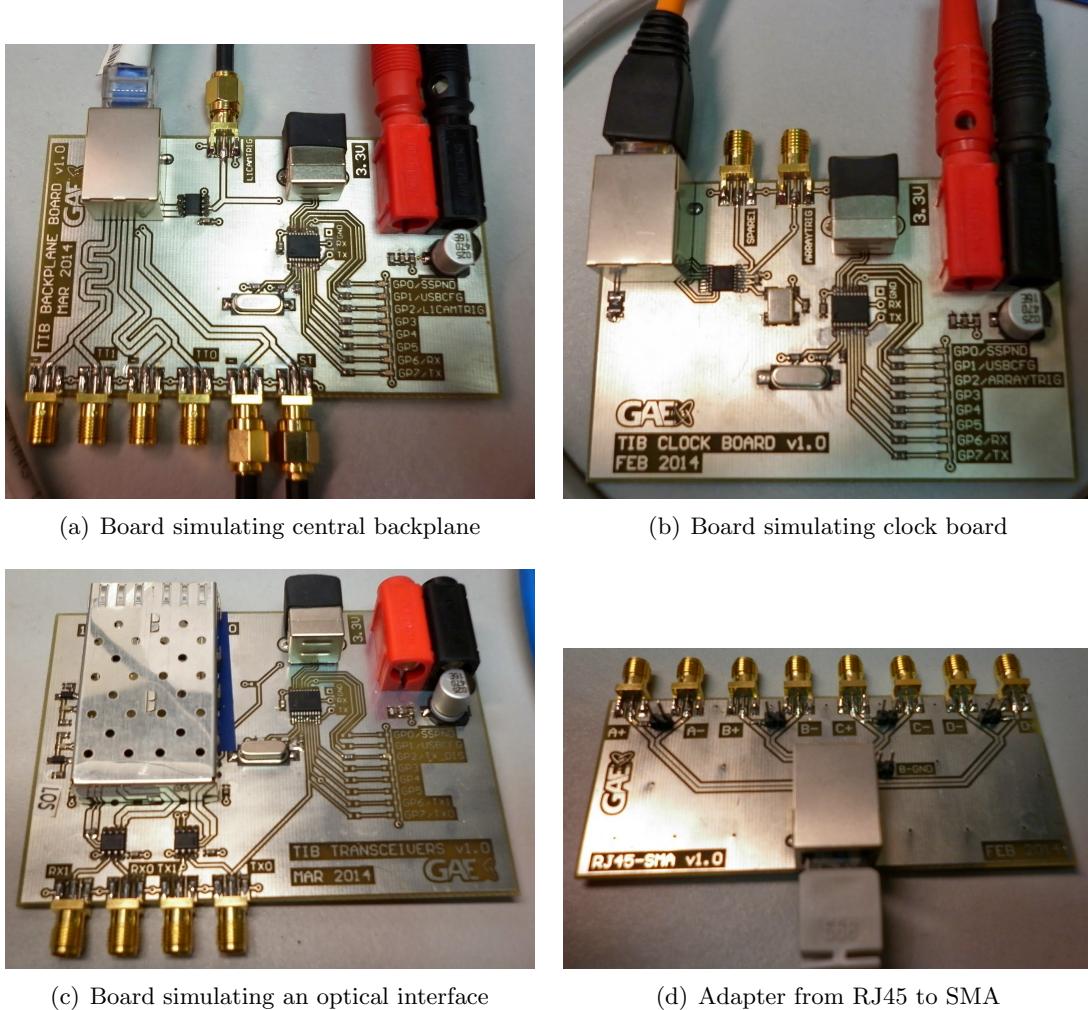


Figure 7.37: Auxiliary boards used for the tests of the Trigger Interface Board

### 7.5.2 FPGA configuration

The next system to be tested was the FPGA. First it was tested through the JTAG interface, observing that the FPGA was properly installed and the communication was possible. The next step was to configure the FPGA with the Raspberry Pi, and this target was also accomplished.

### 7.5.3 Clock generation in the PLLs

In order to test the different firmware modules running in the FPGA, different frequencies must be generated in the PLLs from the original 10 MHz input clock. In the first tests a problem with the matching of the input clock was found, which made the PLL to consider clock reflections as clock cycles and at the end to generate higher output frequencies than expected. The problem was caused because the Xilinx core generator does not activate the internal termination of the input buffer, represented in figure 7.39. Once the problem was found, it was corrected by activating the termination explicitly in the VHDL code and the output frequencies were the expected ones.

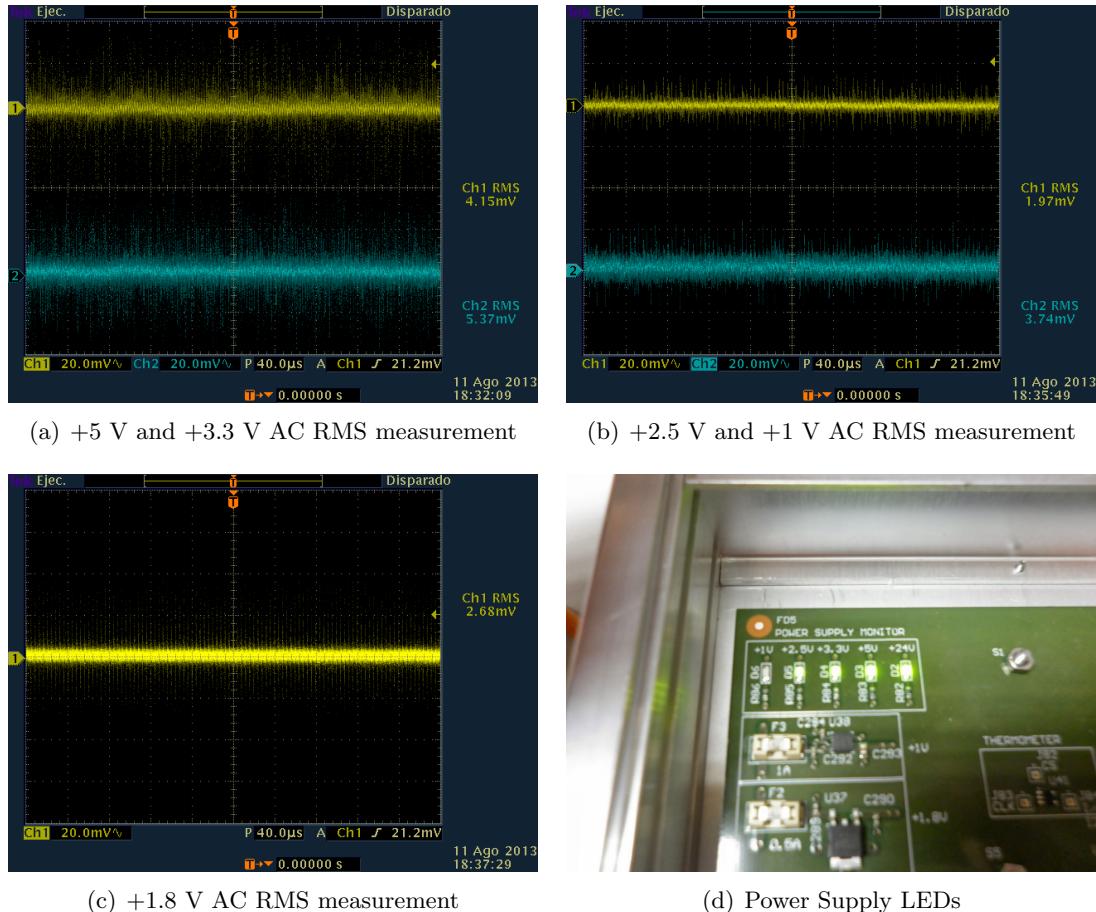


Figure 7.38: Measurements of the noise in the power supplies and photo of the failing LED

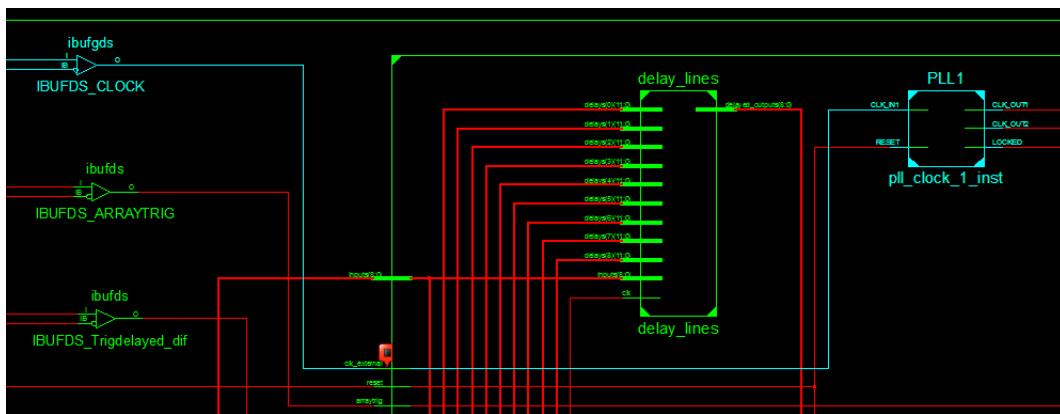


Figure 7.39: Internal differential clock input buffer and first PLL, in blue

#### 7.5.4 FPGA delay lines

Once the high clock frequencies were available, it was possible to test the other firmware modules. The next ones were the flip-flop based delay lines described in section 7.4.4.2. In order to test them,

a copy of the input and the output of a delay module were directly connected to two spare RJ45 pairs which, after an adapter board like the one shown in figure 7.37(d), were connected to an oscilloscope. Delays from 0 to 1600 cycles ( $4 \mu\text{s}$ ) were tested, observing a minimum delay of 6.2 ns corresponding to 0 cycles, which behaves as an offset added to the configured delay. This offset is due to propagation inside the TIB, and it does not mean any trouble. Regarding the maximum jitter, it was always limited to around 2.5 ns for all the delays tested, which corresponds to the minimum clock period, just as expected. Figures 7.40 and 7.41 show several delay measurements.

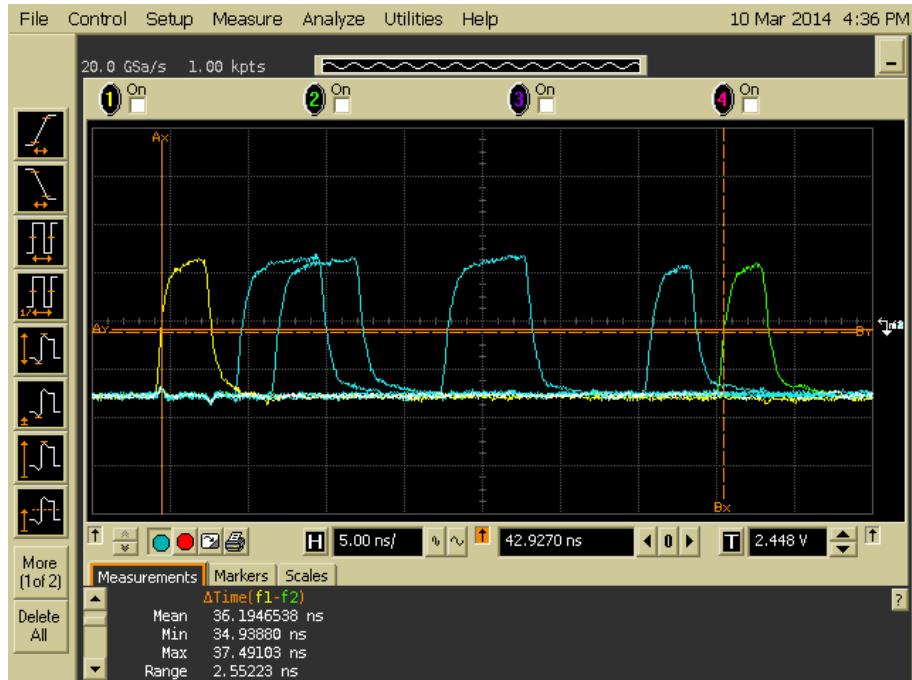


Figure 7.40: 0, 2.5, 12.5, 25 and 30 ns delayed outputs (blue and green) and input (yellow)

### 7.5.5 Stretchers

The next module to test were the stretchers. As in the case of the delay lines, the output of the stretchers was connected to an spare RJ45 connector in order to measure the width of the pulses. Figure 7.42 contains several measurements showing that the stretcher modules work as expected, i.e. stretching the pulse up to the configured width when the pulse is narrower than the coincidence window, and not changing the output width when the input pulse is wider than the coincidence window width, as it was described in section 7.4.4.3.

## 7. Trigger Interface Board.



Figure 7.41: 4  $\mu$ s delayed output (green) and input (yellow)

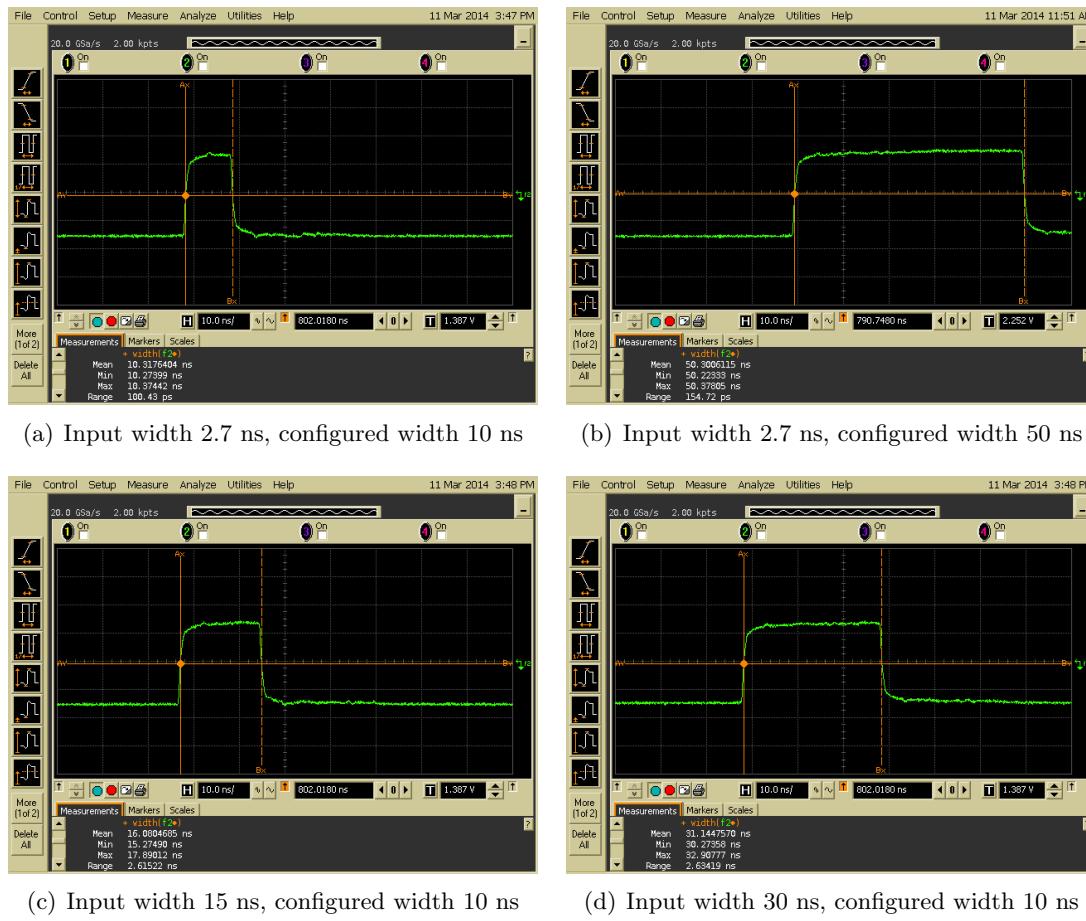


Figure 7.42: Several pulse width measurements at the output of the stretchers

### 7.5.6 Stereo Logic

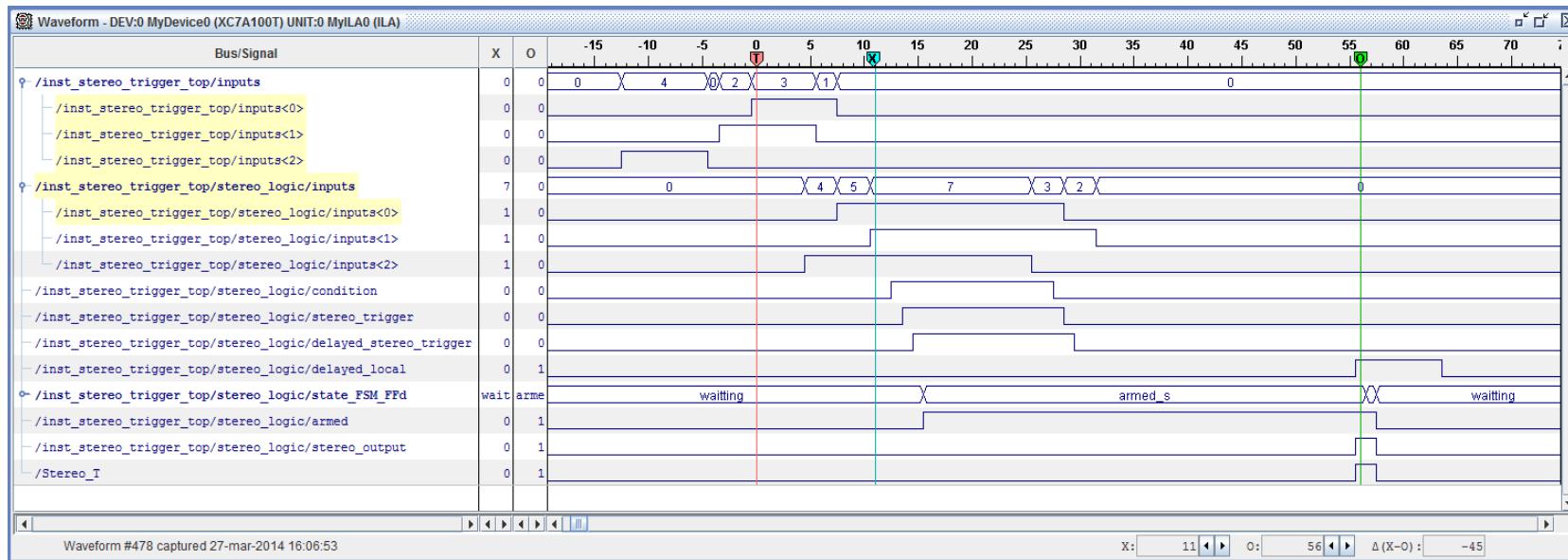
The tests of the stereo logic were difficult to perform with the oscilloscope because there are many signals involved, and not all of them can be represented in the screen at the same time. The available oscilloscope only have 4 channels and the outputs from the RJ45 connectors consist of differential pairs, so only 2 signals could be simultaneously represented without using the memories. Additionally, measuring the signals involved in the stereo logic outside the FPGA adds additional delays due to the cables, connectors, etc. which can distort the real situation when looking for coincidences. In this situation, it was preferred to use a Xilinx tool named ChipScope [168]. This tool uses the spare resources in the FPGA to implement a virtual logic analyzer, which can be used to see the internal signals, sampling them with an internal existing clock (the 400 MHz one was chosen), triggering with a selectable signal (the local trigger input was chosen) and storing the samples in the RAM blocks existing in the FPGA. By means of this powerful tool, all the internal signals participating in the logic could be represented in a PC like in a logic analyzer. The figures 7.43 and 7.44, in the following pages show several typical situations.

Figure 7.43(a) shows a typical situation where a trigger output is generated. The 2nd, 3rd and 4th rows in the figure (*inputs< 0 >*, *inputs< 1 >* and *inputs< 2 >*) correspond to the Level 1 trigger signal coming from the backplane and two Level 1 trigger inputs coming from neighbour telescopes<sup>16</sup>. These input trigger pulses are delayed and stretched, so 6th, 7th and 8th rows represent the signals coming into the stereo logic module. In real conditions the inputs would show a longer separation in time and the delays required to compensate them would be longer too. For these tests, short delays have been selected in order to see all the signals which are important for the logic in the same screen. In this way, the 9th signal (*condition*) is set to “1” when the trigger condition is accomplished, which in figure 7.43(a) happens for 3 coincident inputs. The 10th row, named *stereo\_trigger* requires *condition* to be set to “1” and also checks that one of the active inputs is the local one. If this is the case, the *stereo\_trigger* signal can be delayed, as will be shown in figure 7.44(b), or not delayed as shown in figure 7.43(a), generating in any case the 11th signal, labelled as *delayed\_local*. This signal changes the state of the state machine shown in figure 7.27, which is represented by the signal *state\_FSM\_FFd*, changing from *waiting* to *armed*, which means that a stereo trigger output will be generated when the delayed copy of the local input will arrive. This delayed copy is named as *delayed\_local* in figures 7.43 and 7.44. When it arrives, the stereo output signal (*stereo\_output*) is generated, changing the state from *armed* to *shooited* during the trigger output duration and, finally changing to *waiting* again. The last signal, named *Stereo\_T*, represents the trigger output from the FPGA.

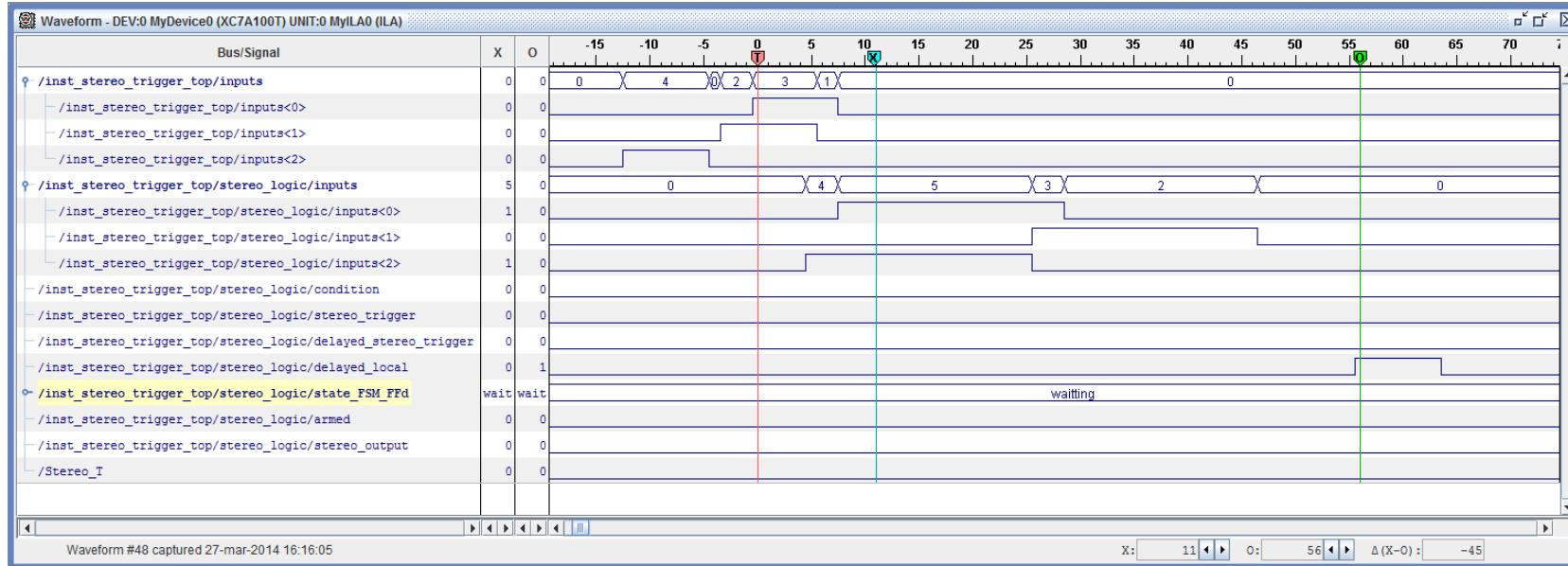
Figure 7.43(b) shows the signals in a case in which the trigger condition is not fulfilled because there are never 3 coincident signals, and therefore *condition* is never set to “1”. On the other hand, figure 7.44(a) shows a situation in which the trigger condition requires 2 coincident telescopes, but *stereo\_trigger* is shorter than *condition* because the local trigger is only active during part of the time. Finally, figure 7.44(b) shows a case in which *delayed\_stereo* is delayed with the aim to reduce the time during which *armed* is enabled, reducing the probability of generating a trigger output due to a previous non-coincident local Level 1 trigger.

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<sup>16</sup>1st and 5th signals (*stereo\_trigger\_top/inputs* and *../stereo\_logic/inputs* are 3-bit buses containing the decimal representation of signals 2nd, 3rd and 4th or 6th, 7th and 8th respectively



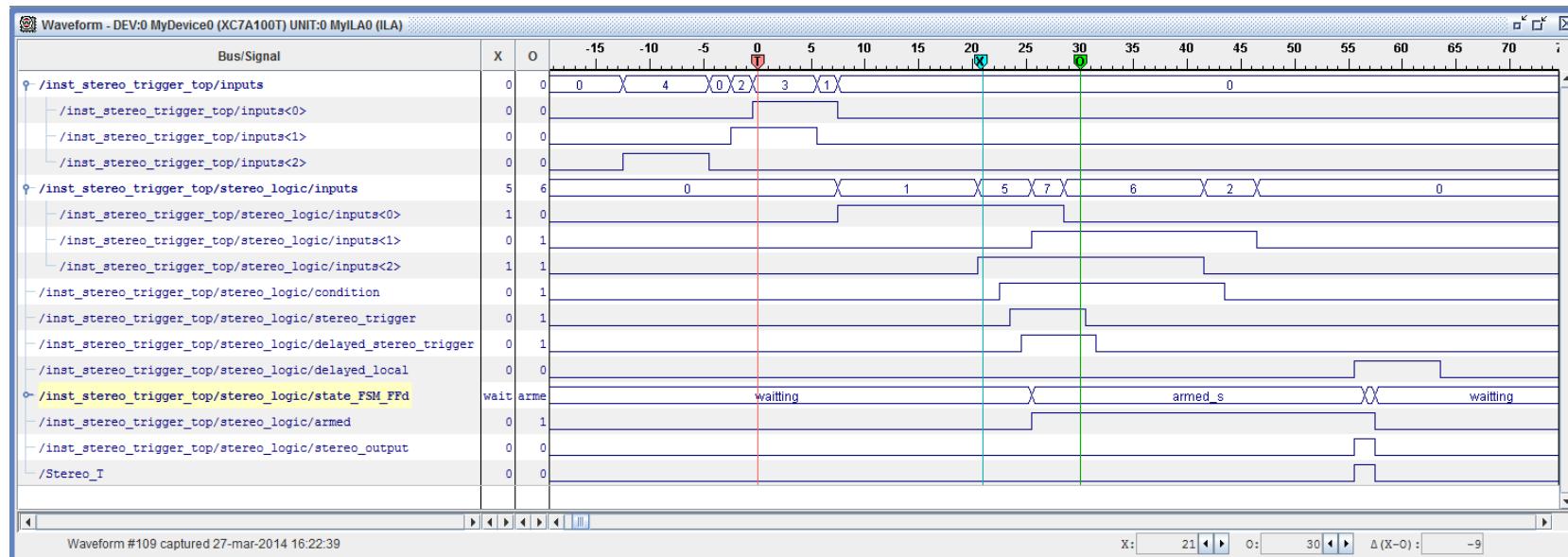
(a) Complying condition of 3 coincident trigger inputs



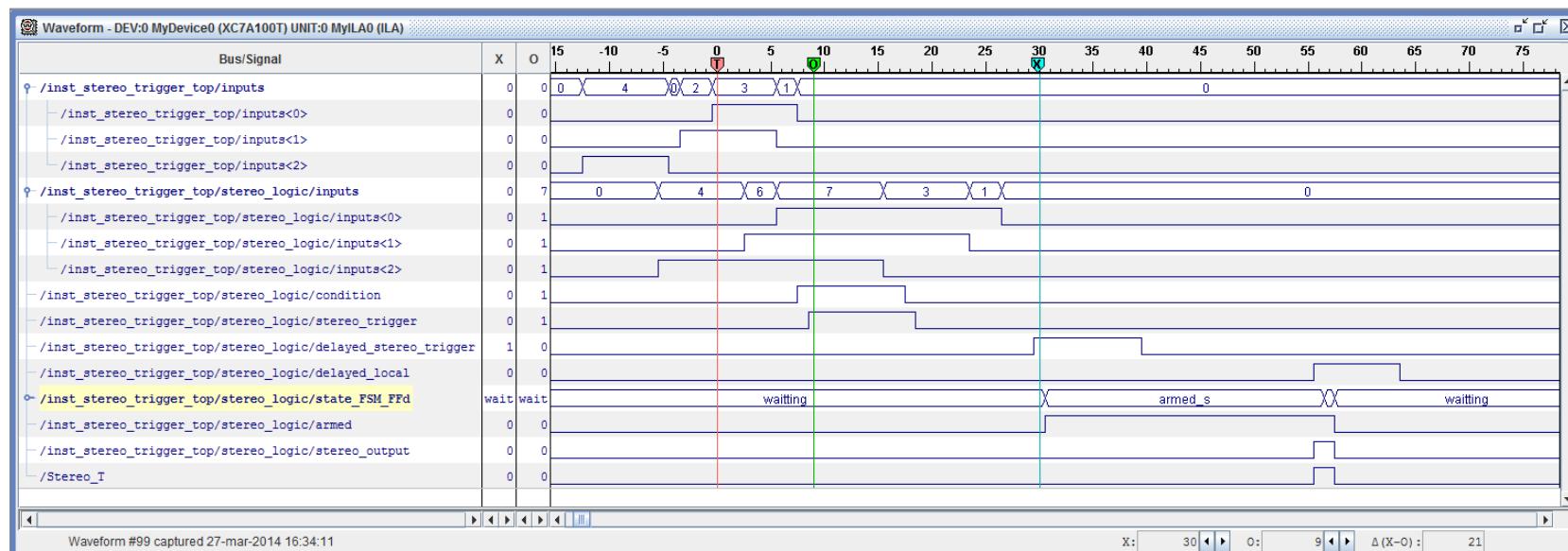
(b) Not complying condition of 3 coincident trigger inputs

Figure 7.43: Measurements of the signals involved in stereo logic, requiring 3 coincident trigger inputs.

## 7. Trigger Interface Board.



(a) Complying condition of 2 coincident trigger inputs, but requiring also local trigger



(b) Delayed stereo used to reduce the armed time

Figure 7.44: Measurements of the signals involved in stereo logic, showing local trigger requirement and utility of delayed stereo.

### 7.5.7 Collector

The collector module inside the FPGA was also tested, obtaining output triggers corresponding to the different trigger inputs. The mask allows to enable or disable the trigger inputs, and the trigger type is generated correctly. Figure 7.45 shows the output corresponding to a software trigger coming from the clock board. The corresponding code “101” is read in the leading edges of the 10 MHz clock. As it was required to represent 3 differential signals with a 4-channel oscilloscope, the trigger output was stored in memory (blue line) and, using it as trigger, the clock and data lines are represented with the yellow and green lines respectively.

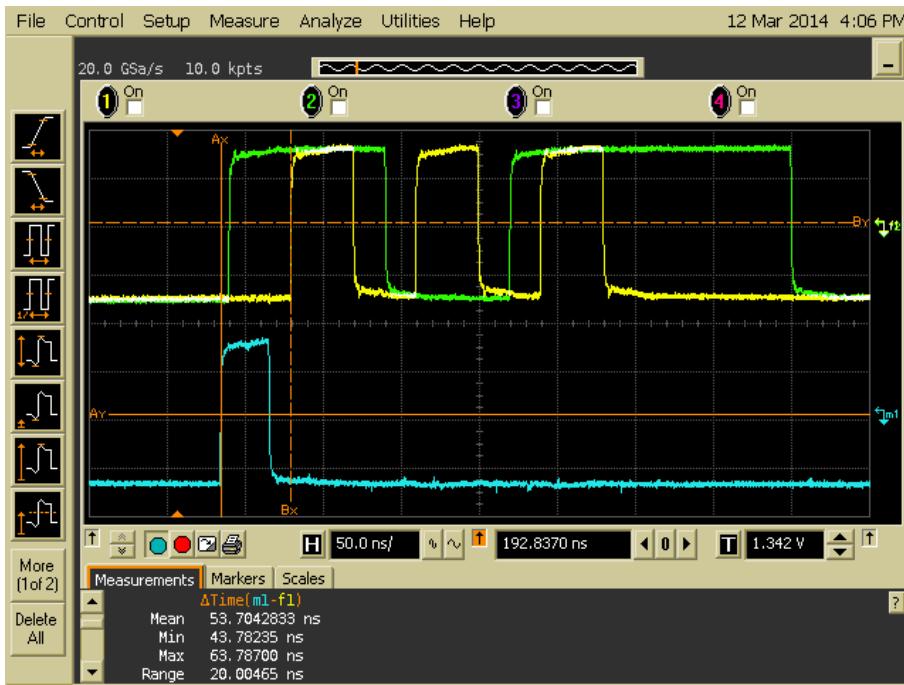


Figure 7.45: Trigger output pulse (blue) and trigger type clock (yellow) and data (green).

### 7.5.8 ITR counters

The ITR counters were also measured, just by setting different input trigger frequencies and reading the accounts, which are updated every  $250 \mu\text{s}$  as it was explained in section 7.4.4.6. The results are gathered in table 7.8, showing that the counters work as expected:

As it was expected from their implementation, the ITR counters cannot measure rates with an accuracy better than 4 kHz (because of the updating period), or to measure rates higher than 1.02 MHz, (because they are 8-bit counters). Nevertheless, the current characteristics of the counters are suitable for the expected rates to be measured in CTA.

### 7.5.9 Optical links

The optical links were implemented in the first prototype with SFP transceivers, like the ones used in optical Gigabit Ethernet networks [146]. These transceivers are easy to control, and very

Input rate (kHz)	Counts in a period of 250 $\mu$ s	Measured rate (kHz)
2	0	0
4	1	4
10	2	8
12	3	12
20	5	20
40	10	40
100	25	100
200	50	200
300	75	300
500	125	500
800	200	800
1000	250	1000
1500	255	1020

Table 7.8: Measured rates using the ITR counters

adequate for data transmission through cheap OM3 optical fibers in distances of up to 550 m length. However the tests showed that the SFP transceivers were not a suitable option for sending trigger pulses.

When testing an optical link, it was observed a high level of noise in the received signal. This was caused because, in the transmitter, the differential LVPECL inputs are AC coupled as shown in figure 7.46. If the signal is changing very fast, like it is the case in the Ethernet signals<sup>17</sup>, it works properly but, this is not the case of the digital trigger pulses. These trigger pulses sent by the camera telescopes consists of pulses of a few nanoseconds width (around 10 ns), which are sent at a maximum rate of some hundreds of kHz. This means that the baseline is set to “0” during most of the time. Looking at the scheme of figure 7.46, it is easy to understand that the DC levels of such a differential signal are removed by the capacitors, so the DC voltage is the same in the positive and negative inputs of the receiver (points marked as *TD+* and *TD-* in the figure). In this situation, the slightest noise fluctuations are recognized by the transmitter as “0s” or “1s”, sending noisy pulses. Real pulses are effectively sent, but together with thousands of noise pulses.

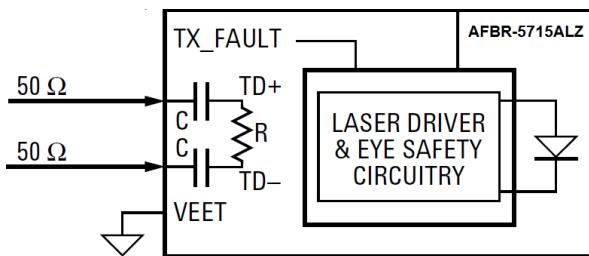


Figure 7.46: Emitter part of an SFP, transceiver, AC coupled [146].

The solution to this problem will consist of replacing the SFP transceivers of the first TIB

<sup>17</sup>Optical Gigabit Ethernet uses 8b/10b encoding, which achieves DC balance by mapping 8 bit symbols in 10 bit symbols, where there are never more than 5 consecutive zeros or ones [169].

prototype by analog optical links implemented with discrete VCSELs and PIN photodiodes, as was described in section 7.4.2.2.2. The transceivers have been implemented in test boards and tested with two optical fibers of 2 and 500 m. Figure 7.47 shows the measured signals corresponding to the 2 m link. The purple line was measured with a probe<sup>18</sup> with the aim to show that this kind of links can handle pulsed signals properly. On the other hand, figure 7.48 shows the input and output with a 500 m optical fiber, demonstrating that the optical power and the sensibility of the receptor are adequate. The bandwidth is large enough to allow sharp edges and, as a result, the jitter is very low: only 77 ps with the 500 m optical fiber.

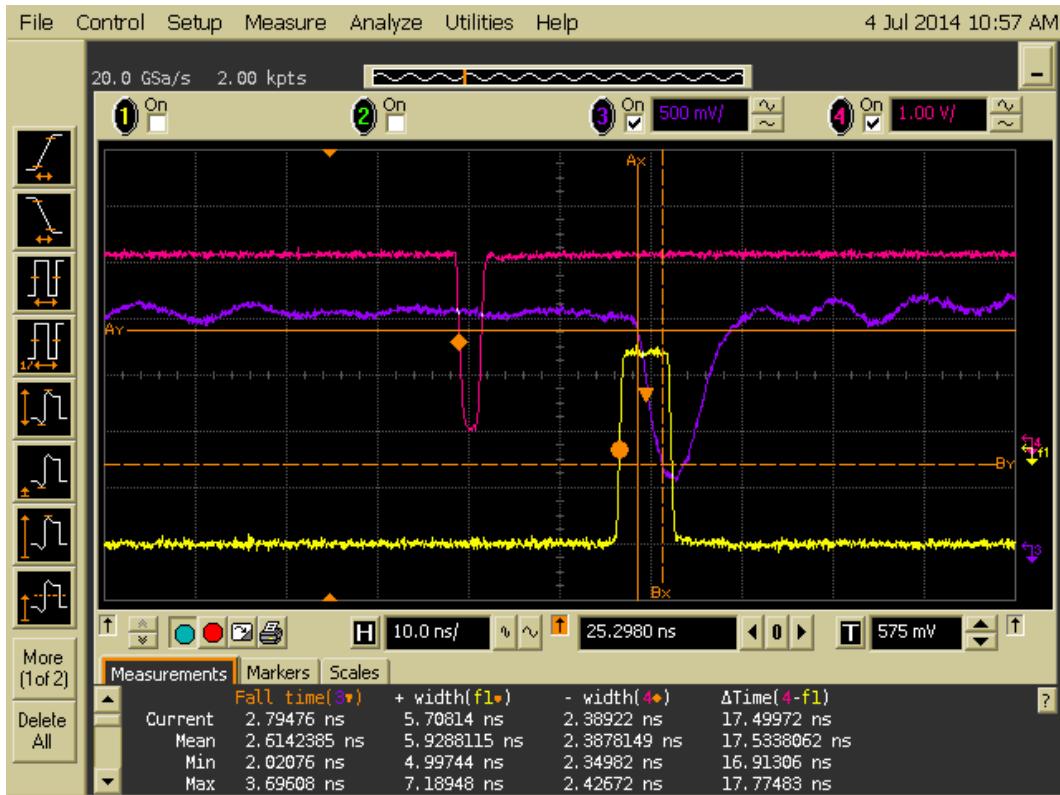


Figure 7.47: Inverted copy of the input signal (magenta), received analog signal at the input of the comparator (purple) and LVDS output (yellow) of the analog optical link, with a 2 m optical fiber

### 7.5.10 External delays

The different ways to implement the external delays described in section 7.4.3 have been tested:

#### 7.5.10.1 Delays with DS1123LE-200

The external delays implemented with the Maxim DS1123LE-200 chips [152] were the option chosen for the first TIB prototype. They were tested and, in fact, used to delay the local trigger

<sup>18</sup>The length of the probe cable is longer than the one of the cable which connects the LVDS output to the oscilloscope. This is why the LVDS output appears before the analog pulse.

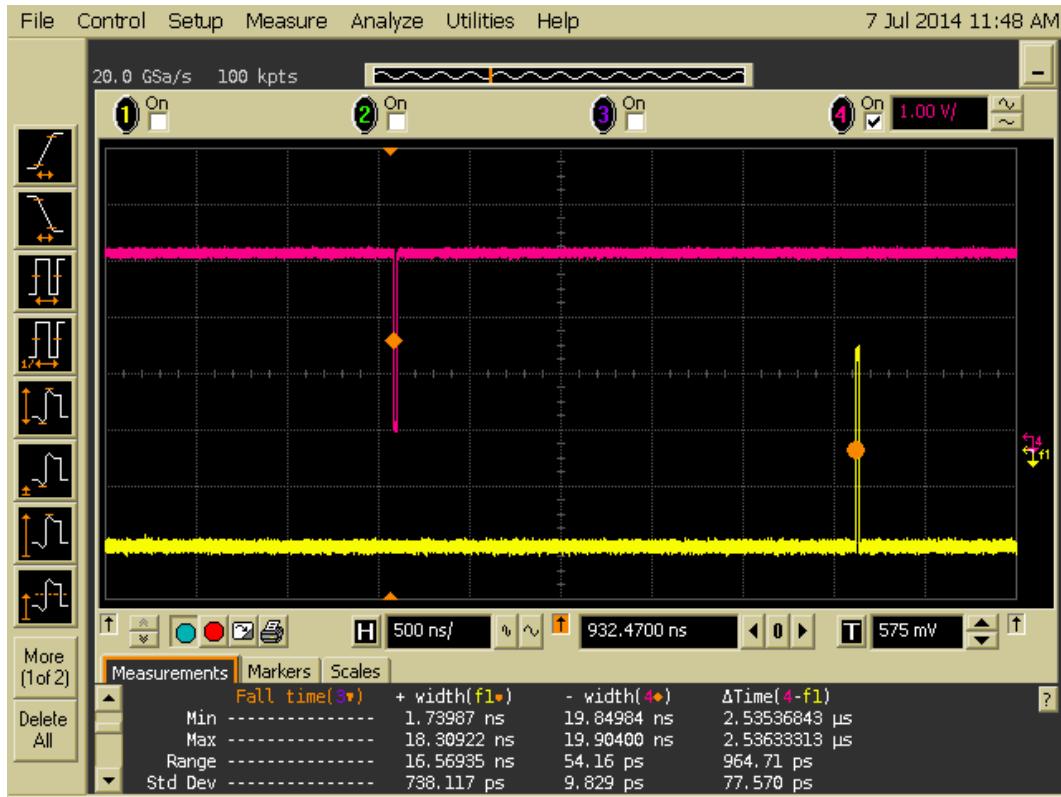


Figure 7.48: Inverted copy of the input signal (magenta) and received LVDS output (yellow) of the analog optical link, with a 500 m optical fiber

and generate the *delayed\_local* signals shown in figures 7.43 and 7.44. Figure 7.49 shows the result of delaying an input pulse 0, 50, 100, 150 and 200 steps of 2 nanoseconds with only one delay chip, and it can be seen that the delay accuracy is very good and the standard deviation of the jitter is around 20 ps.

However, when longer delays were implemented with a chain of 8 chips in cascade the results were not so good. For a delay of  $2.6 \mu s$ , a standard deviation of the jitter of 1.4 ns was measured. This jitter is too high, and discards these chips as an option to implement the asynchronous delay of the local input which at the end is used to read the camera, and which should have a jitter lower than 1 ns.

### 7.5.10.2 Delays with 3D3428

In spite of the difficulties with the supply of this chip, it was finally possible to get a sample and test it. The measurement corresponding to the expected required delay is shown in figure 7.50. As it can be see in the figure, the jitter is much lower than with the Maxim device: for a  $2.7 \mu s$  delay, the std. deviation of the jitter is 606 ps. Therefore this chip will be the chosen one for the upcoming version of the TIB.

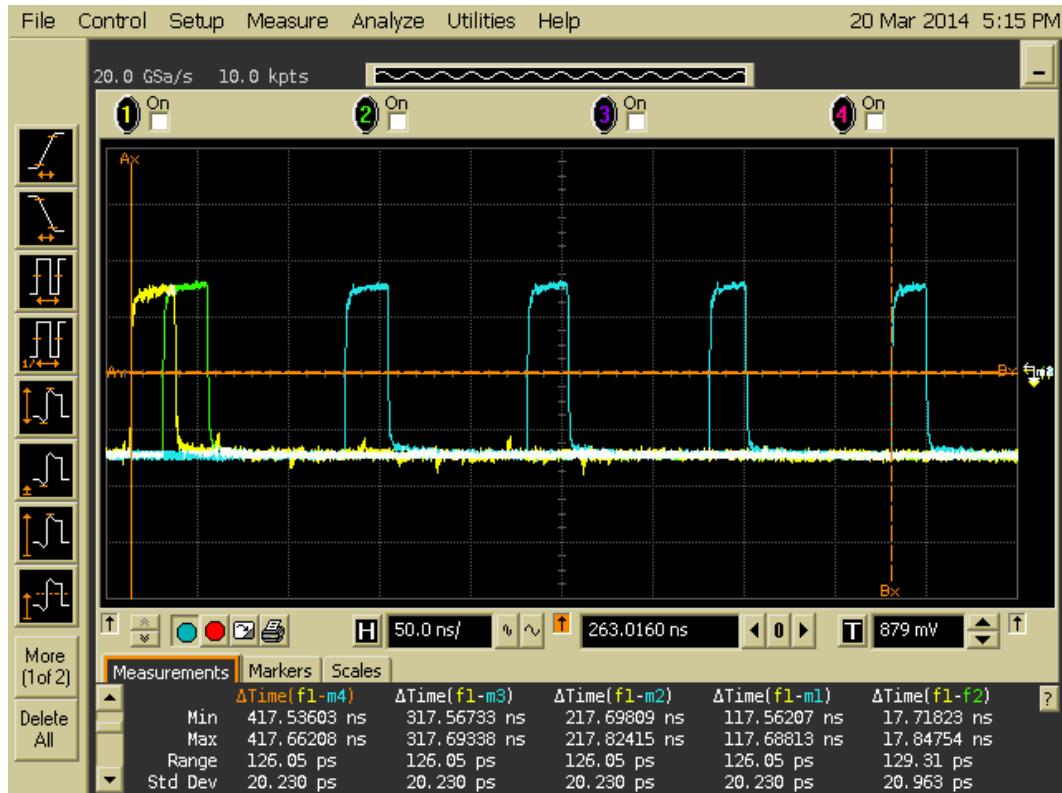


Figure 7.49: Input signal (yellow) and delayed 0 (green), 50, 100, 150 and 200 steps of 2 ns (blue) with DS1123LE-200.

### 7.5.10.3 Delay with an optical fiber reel

The delay can be implemented with a long optical fiber and the analog optical links described in section 7.4.2.2.2. The measurements shown in figures 7.47 and 7.48 show that this is a feasible option. With the 500 m length optical fiber, a delay of 2.53  $\mu$ s with a jitter of only 77 ps standard deviation was achieved, which is better than with any existing chip. However, this solution is very bulky and not very feasible to be implemented in an IACT.

## 7.5.11 Test conclusions

The tests have shown that the first prototype of the TIB can comply with most of the requirements. Most of the concepts have been successfully tested:

- The stereo trigger and the trigger gathering functions can be implemented in an FPGA, working at 400 MHz.
- A Raspberry Pi is very useful to configure the FPGA and perform the slow control functionalities, avoiding complex Ethernet implementations.
- The delay lines and the stretchers based in flip-flop chains work as expected, with a jitter limited by the FPGA clock frequency.

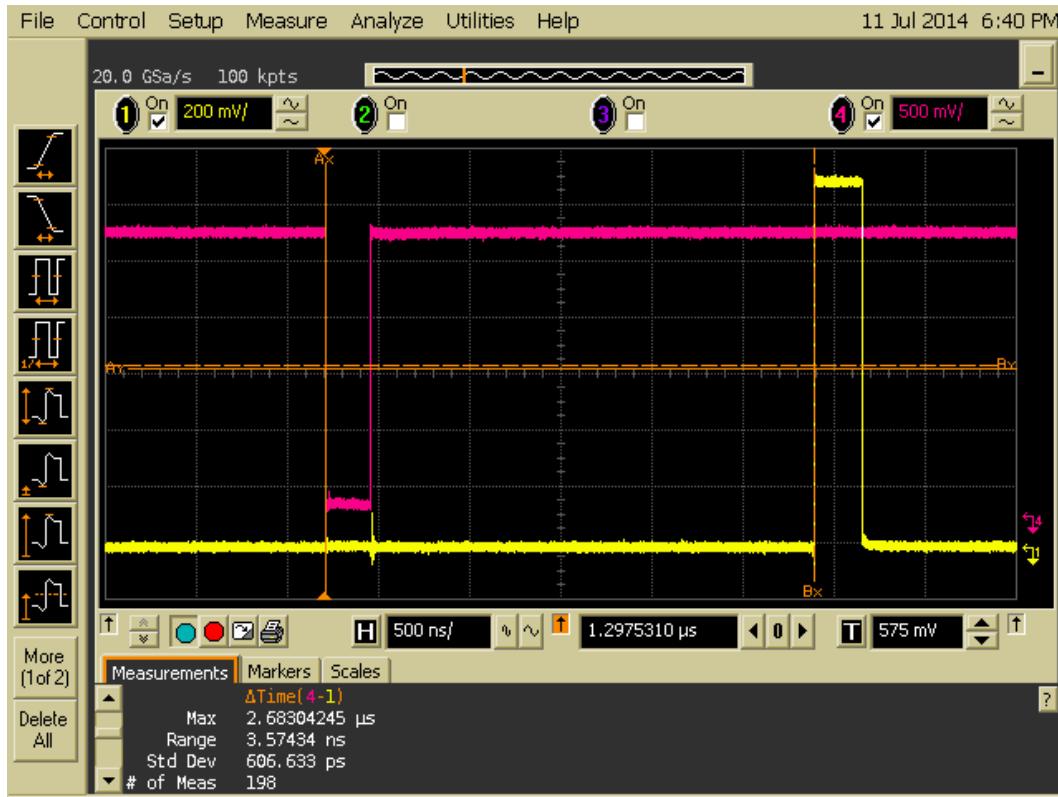


Figure 7.50: Delay measurement with 3D3428 delay line

- A complex logic has been developed, which can generate trigger outputs which are synchronous with a local Level 1 trigger signal, but not with the FPGA clock.
- The trigger type generation worked as expected.
- The trigger rates can be measured in the FPGA.
- The SPI control of external chips, such as the DS1123L or the thermometer worked properly.
- In spite of the board complexity, no crosstalk problems between lines were observed.
- The designed power supplies add very little noise.

In addition, there are two important points to improve in the next prototype version:

- The optical SFP transceivers must be replaced by the ones based on discrete VCSELs and PiN photodiodes, capable of working with trigger-like pulsed signals.
- The 8 delay chips DS1123LE-200 from Maxim must be replaced by one 3D3428 from Data Delay Devices, with much lower jitter.

Anyway, it must be pointed out that the first TIB prototype fulfils the requirements for the forthcoming integration tests, with only one camera. When the improvements, which are already

tested, will be included in the second TIB prototype, it will be possible to accomplish all the requirements of CTA LSTs and MSTs.

## Chapter 8

# Conclusion and Outlook

### 8.1 Conclusions

During the last four years I have been working at GAE-UCM, together with other Spanish groups from Ciemat, IFAE and UB and in coordination with other foreign institutions, specially from France and Japan, with the aim to build the best possible trigger system for the large and medium sized telescopes of the forthcoming Cherenkov Telescope Array. On the base of our previous knowledge and our experience with the MAGIC telescope, we conceived a system with a great expected performance according to MonteCarlo simulations (see section 3.2), and which is feasible to be constructed and operated.

The proposed trigger architecture follows a multi-level scheme, able to support many of the most powerful trigger techniques: majority trigger, sum trigger, variable trigger region sizes, partial readout, sliding window, two-thresholds strategies, Colibri, PMT transit time calibration, hardware stereo trigger and even software array trigger with the digitized data. Such a global architecture is the result of the collaboration between all the mentioned teams mentioned above. Nevertheless, each group developed a different hardware element: IFAE team designed the Level 0, Ciemat team is in charge of the backplane, UB worked in ASICs and at UCM-GAE we designed the Level 1 and the TIB, which are the core of my thesis.

The Level 1 implements successfully the required functionalities: it combines the inputs from sets of clusters and decides if the camera should be triggered or not. It does it in a very short time, with a negligible jitter, complying with the bandwidth requirement and adding very low noise. It is able to implement the sumtrigger scheme, it supports Colibri (as described in chapter 5) and includes the necessary hardware to implement the delay compensation system described in chapter 6. Several prototypes have been tested with the other systems and the current design is ready for industrial production. Additionally, the development of the Level 1 produced 2 extra-outcomes:

- Usability of microwave techniques and technologies adapted to short pulse handling. The typical spectrum of a PMT output pulse ranges from low frequencies to up to 1 GHz and, at these high frequencies the RF and microwave technologies can be useful. The case of the Wilkinson splitters [6] or the use of Schottky diodes are examples of this.

- Patent of a new family of logic gates, able to work with LVDS and other differential logic standards.

Regarding the TIB, two boards of the first prototype have been designed, manufactured and tested, and the results are very satisfactory. The current TIBs have been able to comply with the very demanding requirements needed to implement the LST hardware stereo logic, gathering the different trigger origins and generating the trigger type. The use of chains of flip-flops in a FPGA have showed the expected performance in the delay lines and in the stretchers, and the Raspberry Pi has been a good solution to implement the slow control communication and to configure the FPGA. Thus, the current prototypes are useful for the single camera demonstrator tests which will take place during this year. Two problems with the optical links and the external delays have been detected, and the solutions are ready to be implemented in the next version of the TIB, which is scheduled to be ready some time before two telescopes will be ready to work together in a stereo trigger scheme.

In short, it can be said that the work carried out during these years has made possible to present an excellent trigger system, able to comply with the demanding requirements of CTA LSTs and MSTs.

## **8.2 Outlook**

The CTA project is now at the end of its prototyping phase. From 2014 to 2016, prototypes for large demonstrators and complete MSTs and LSTs will be built, tested and assessed. These complete prototype telescopes will be also used to test and adjust the trigger distribution system, check the accuracy of the different calibration algorithms (flat-fielding, trigger amplitude, delays...) and to finish the implementation of all the details required for the correct data taking, such as those related with the data format, event building, time stamping, slow control, etc. In summary, all the details required to make CTA telescopes work, but which can not be tested without a complete camera, will be implemented and tested in this phase.

Additionally, building these first telescopes implies the first industrial production of several elements, such as the camera front-end boards and backplanes, and their assembly in clusters with PMTs. These elements must be tested before being mounted in the camera, according to a quality control protocol which still needs to be defined. Defining the measurements to be done in each step, the acceptable values, and developing the corresponding test setups is an intensive work which also needs to be done in this stage. Part of this work will be subcontracted to companies, but always under the control of the groups which developed the systems.

All this work will not leave much time for developing new ideas. However, there are two main innovative lines to be developed, as soon as the other tasks allow us.

### **8.2.1 Trigger integration in ASICs**

One interesting idea, with the aim of reducing the number of components, simplifying the assembly, reducing costs and power consumption, is to develop ASICs concentrating the different trigger functionalities. Our partners in ICCUB (Institute of Science of the Cosmos, University of Barcelona)

in Spain and our french colleagues at IRFU (Institut de Recherche sur les lois Fondamentales de l'Univers) have some experience developing ASICS ([58], [95], [98]), so that we (mainly ICC-UB and Ciemat, with UCM and IFAE collaborating in the specification and testing) have taken advantage of their experience and collaboration to design and manufacture ASICs for the trigger.

In this way, one ASIC for Level 0 and other for Level 1 have been designed, and a first version produced and tested, while other ASIC for the Level 0 fan-out function is in the design phase. Some functionalities like the ones related with the SPI slow control used in the Level 1 to adjust the threshold levels have been easy to include, because they have been already implemented for NECTAr. However, the ones related with differential to single-ended conversion or the addition of analog signals were more complicated requiring to be redesigned. This was so because several basic functions are easier to implement in an ASIC in a different way from how they are implemented with discrete components. For instance, the Wilkinson splitter functionality can be implemented in a more straightforward way replicating the signals with current mirrors. In general, replicating and adding currents, is preferable when working with ASICs.

Regarding the ASICs manufacturing, Europractice [170] has allowed us to share the silicon wafer with other projects, making the prototype production much cheaper. After the production, the ASICs are in the process of being fully characterized to check if they can substitute the Level 1 with discrete components.

The GAE-UCM group which I belong, has contributed with the Level 1 ASIC specification and will also help with its characterization. Before being directly soldered in the front-end board, a first batch of ASICs will be mounted on mezzanines compatible with the ones implemented with discrete components. In this way, the ASICs can be tested with the front-end boards, and their behaviour can be compared with the one obtained with discrete components. The GAE-UCM group will be in charge of the production of the L1 mezzanines with the Level 1 ASIC designed by the Ciemat team. The target is to have the ASICs characterized and ready for integration in the front-end boards and in the backplane for the massive production phase, when most of the telescopes will be built. If it is not possible, designs with discrete components are the default solution.

### 8.2.2 Topologic stereo trigger

In the case of the Trigger Interface Board, there are still a few improvements to include regarding firmware debugging and software development. As was mentioned in section 7.3, there are several advanced functionalities which could be implemented if required, although the baseline which consists of looking for temporal coincidences between 4 LSTs and gathering the different trigger origins is working as expected.

One of the most promising improvements is the topologic hardware stereo trigger. As it was briefly described in section 7.3.5, it consists of looking not only for coincidences inside a time window, but also for images compatible with Cherenkov showers. Adding this additional condition, most of the NSB triggers which happen by chance inside the time window can be rejected, while keeping the  $\gamma$ -ray-like showers. As the trigger rate can be further reduced, it is possible to lower the thresholds until reaching the maximum reading rate again at a smaller energy threshold.

A similar topologic scheme has been proposed for the MAGIC telescopes, which could serve as a baseline design for the CTA LSTs. The first simulations results, whose performance is represented in figure 8.1, show improvements above 20% in the collection area below 100 GeV [171]. In the case

of CTA LSTs, having 4 telescopes instead of only two, an even larger gain is expected. This case with 4 LSTs is currently under study with simulations.

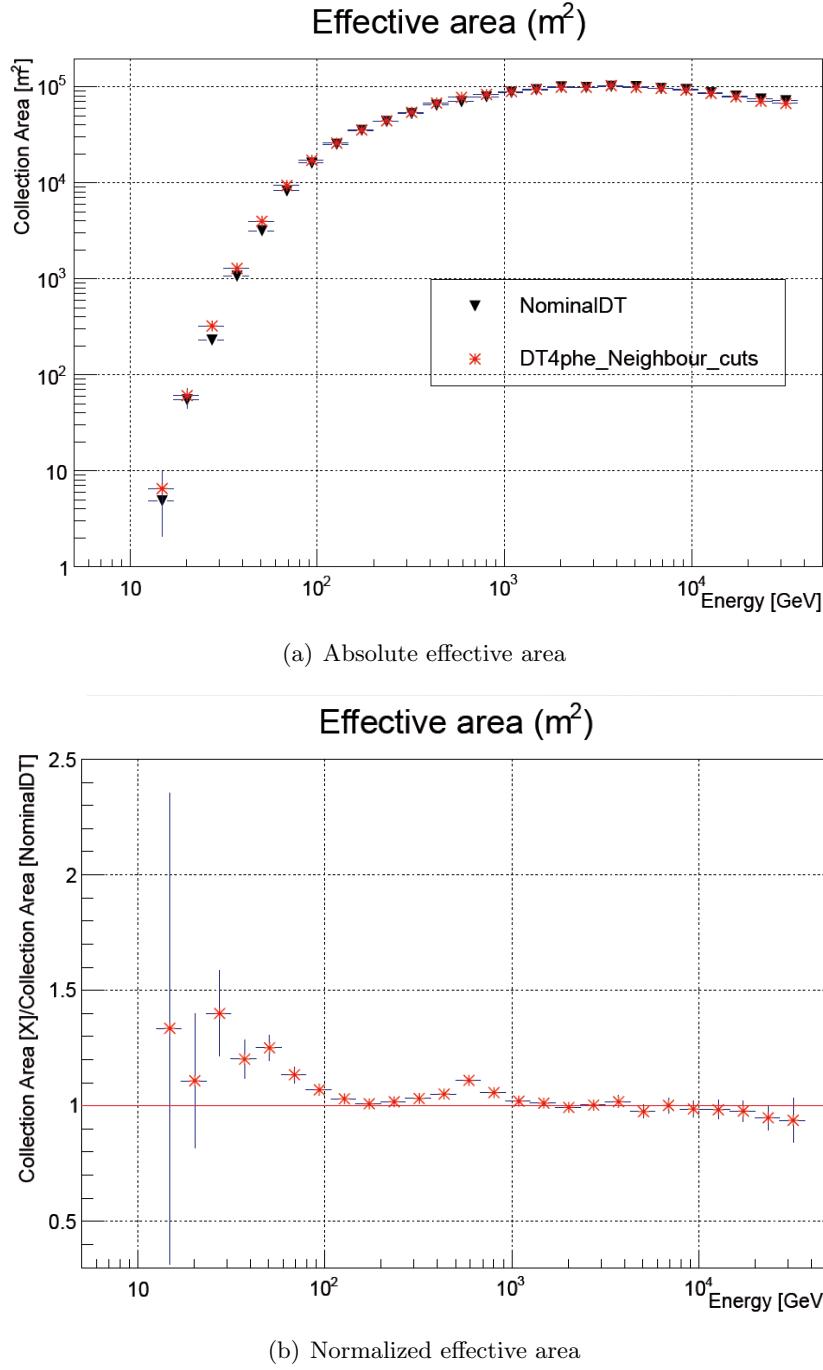


Figure 8.1: Simulation results of the topologic scheme for the MAGIC telescopes

The practical implementation of a topologic hardware stereo trigger in CTA would require some minor changes in the current trigger hardware. The trigger system presented in this thesis can handle all the trigger information in a pulse: a trigger pulse means that the trigger threshold has

been exceeded somewhere in the camera, a known amount of time before receiving the leading edge of the pulse. To implement the topologic scheme, the information about which cluster triggered, or at least which area of the camera was triggered, is required by the Trigger Interface Board to look for valid patterns.

There is only one spare line in the RJ45 interface between the TIB and the central backplane (see table 7.1), so in order to send more information to the TIB, this information must come from other backplanes apart from the central one. Considering this second option, two schemes have been proposed, which are described in subsections 8.2.2.1 and 8.2.2.2.

### 8.2.2.1 Sectorization

In these scheme the special backplanes which provide information to the TIB are the 7 ones around the central backplane. According to the current distribution scheme for the trigger, when one cluster is fired, it sends its trigger to a neighbour which, in turn, sends it to other neighbour and this process repeats until reaching the central cluster. The path followed by the trigger signal changes depending on the specific cluster, but always is composed of some “diagonal” jumps until finding their corresponding main path (or none if the fired cluster is in the main path), and some “radial” jumps until reaching the central cluster. This is illustrated with red arrows in figure 8.2.

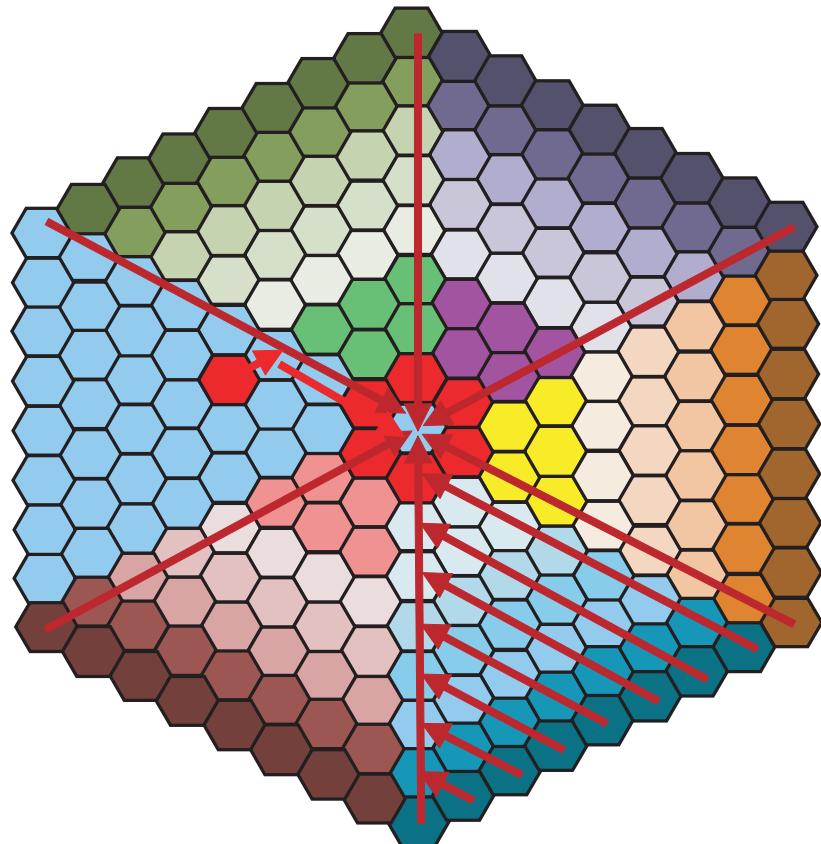


Figure 8.2: Sectorization scheme

This way of collecting the trigger signals means that, any of the six special backplanes surrounding the central one receives the triggers from a triangular sector which covers 1/6 of the camera. So, once the special cluster which received the trigger is known, it is possible to deduce in which camera sector it was generated. Additionally, if the number of jumps is encoded in the pulse width of the trigger pulse, it is possible to restrict even more the possible trigger origins to one of the areas with the same color in figure 8.2. The clusters corresponding to the last two jumps have been coloured with the same color (i.e. included in the same region) to avoid very small regions, however they can be divided in other two regions corresponding to one or two jumps away from the special cluster.

With this scheme, as it is described by figure 8.2, the TIB can know in which of the 37 regions of the camera the trigger was originated. This information can be codified with 6 bits and broadcasted through the optical links to the other LSTs. So, considering 4 LSTs, the TIB can manage a table with  $37^4 = 1874161$  possibilities: some of them will be accepted as images produced by a  $\gamma$ -ray shower, while others don't. If this granularity is not enough to get good results from the topologic trigger, the triangulation scheme can be used.

### 8.2.2.2 Triangulation

The triangulation scheme is more complex, but it allows to know exactly which cluster was triggered. When a cluster is triggered (orange in figure 8.3), it distributes a signal to all its neighbours, which in turn send their signals to their surrounding neighbours and so on, generating a trigger circular *wave front* which expands throughout the camera (red circumferences). The number of jumps is codified in the pulse width, so the special clusters (red ones in figure 8.3) can know how far from them a trigger has happened. In this way, the TIB, which will be additionally connected to these special clusters, also knows how far from each special cluster a trigger happened and can triangulate the position of the trigger origin.

The propagation of the trigger wave throughout the backplanes network would be independent from the standard trigger propagation, and could be done using spare lines in the connectors between neighbour clusters. However, the way in which it could be propagated to prevent the wave from coming back, or how would it solve special cases like two clusters triggering at the same time is still under development.

Additionally, knowing which cluster from the 265 in a camera was triggered in the 4 telescopes means  $265^4 \approx 5 \cdot 10^9$  possibilities to be analyzed by the TIB FPGA. This is probably too much to take the decision with a look-up table in a short time, so maybe some kind of region reduction would be required, partially loosing the greatest advantage of this scheme.

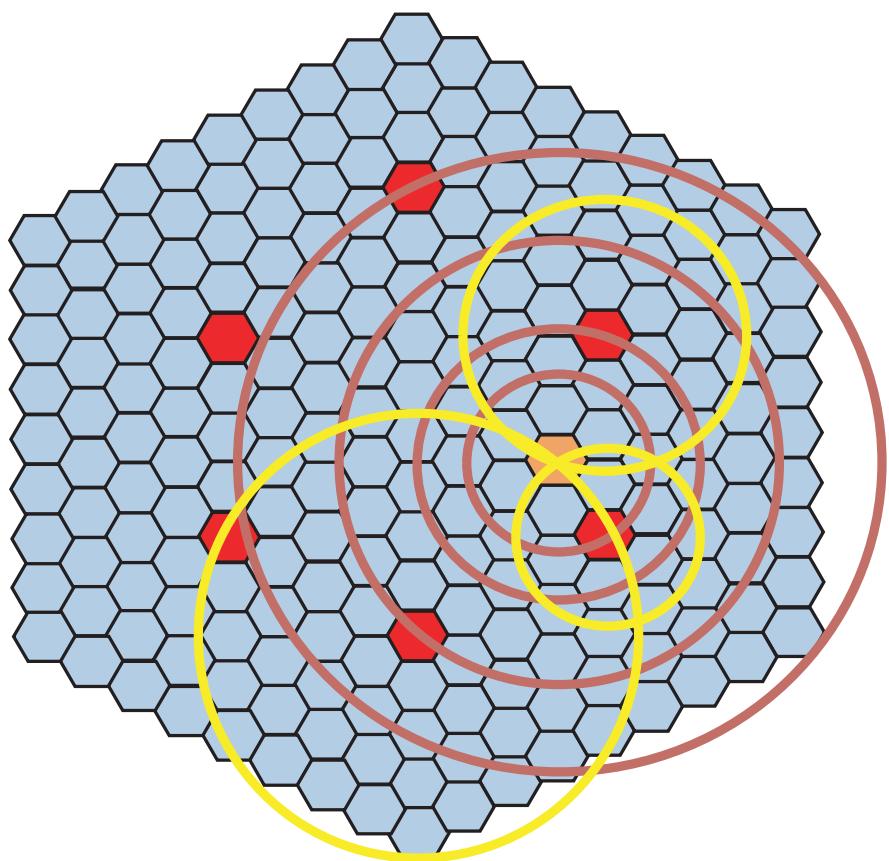


Figure 8.3: Triangulation scheme



# **Appendix A**

## **Schematics**

### **A.1 Level 1 schematics**

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SHEET NO.	SHEET NAME	BLOCK NAME
1	page1	l1delaymasterv3
2	page2	l1delaymasterv3
3	page1	diff2single
4	page1	divider3
5	page1	divider3
6	page1	adder4
7	page1	diff2singleeb
8	page1	div2
9	page1	div2
10	page1	attenuator
11	page1	attenuator
12	page1	lvds_lor
13	page1	lvds_lor
14	page1	3comparator
15	page1	3comparator
16	page1	lvds_and
17	page1	width2amp
18	page1	read_pulse_amp

TITLE:	L1 DELAY MASTER V3	DATE:
ENGINEER:	LUIS A. TEJEDOR	7/03/2013
		PAGE: 1

Figure A.1: L1: Schematic Index

## A. Schematics

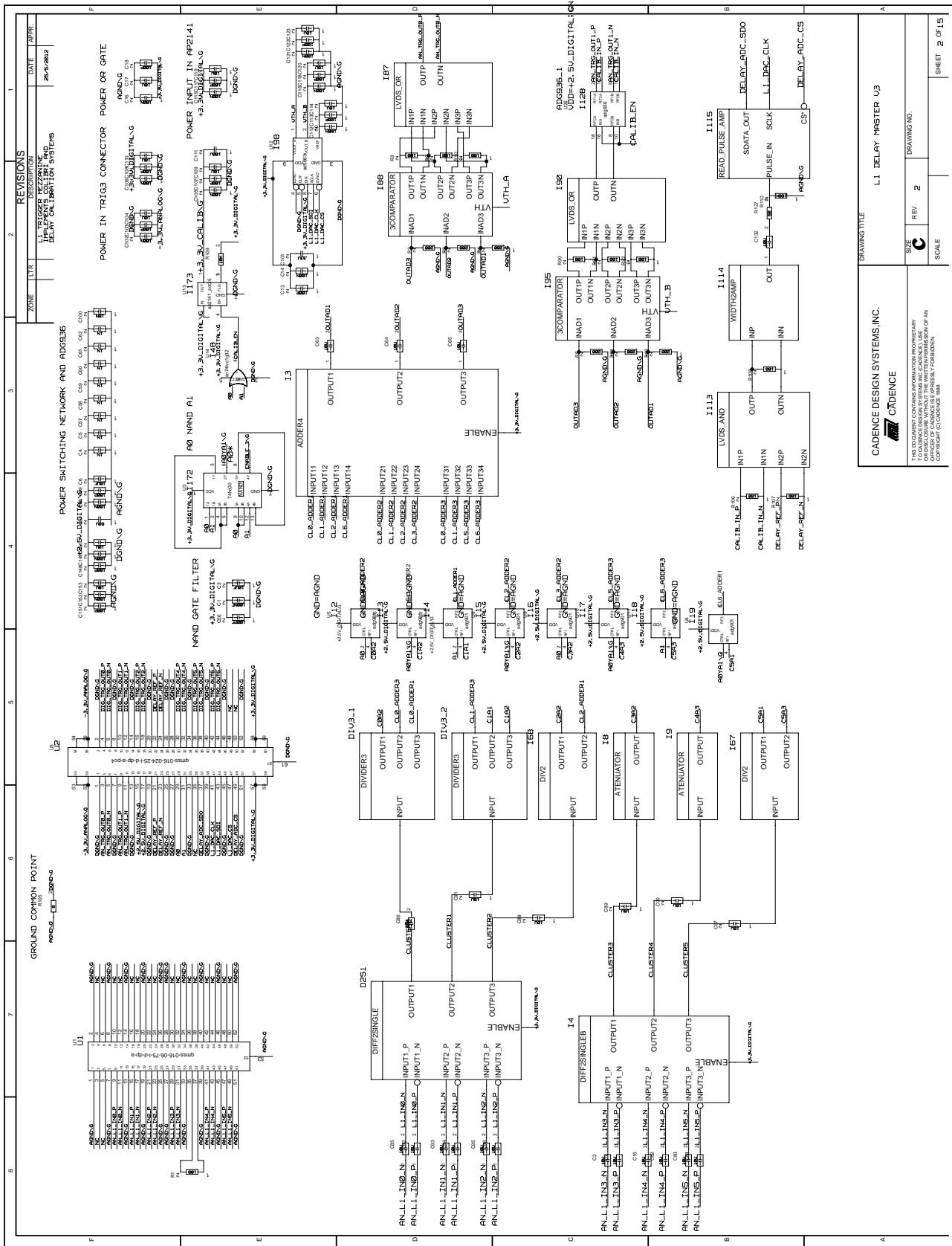


Figure A.2: L1: General Schematic

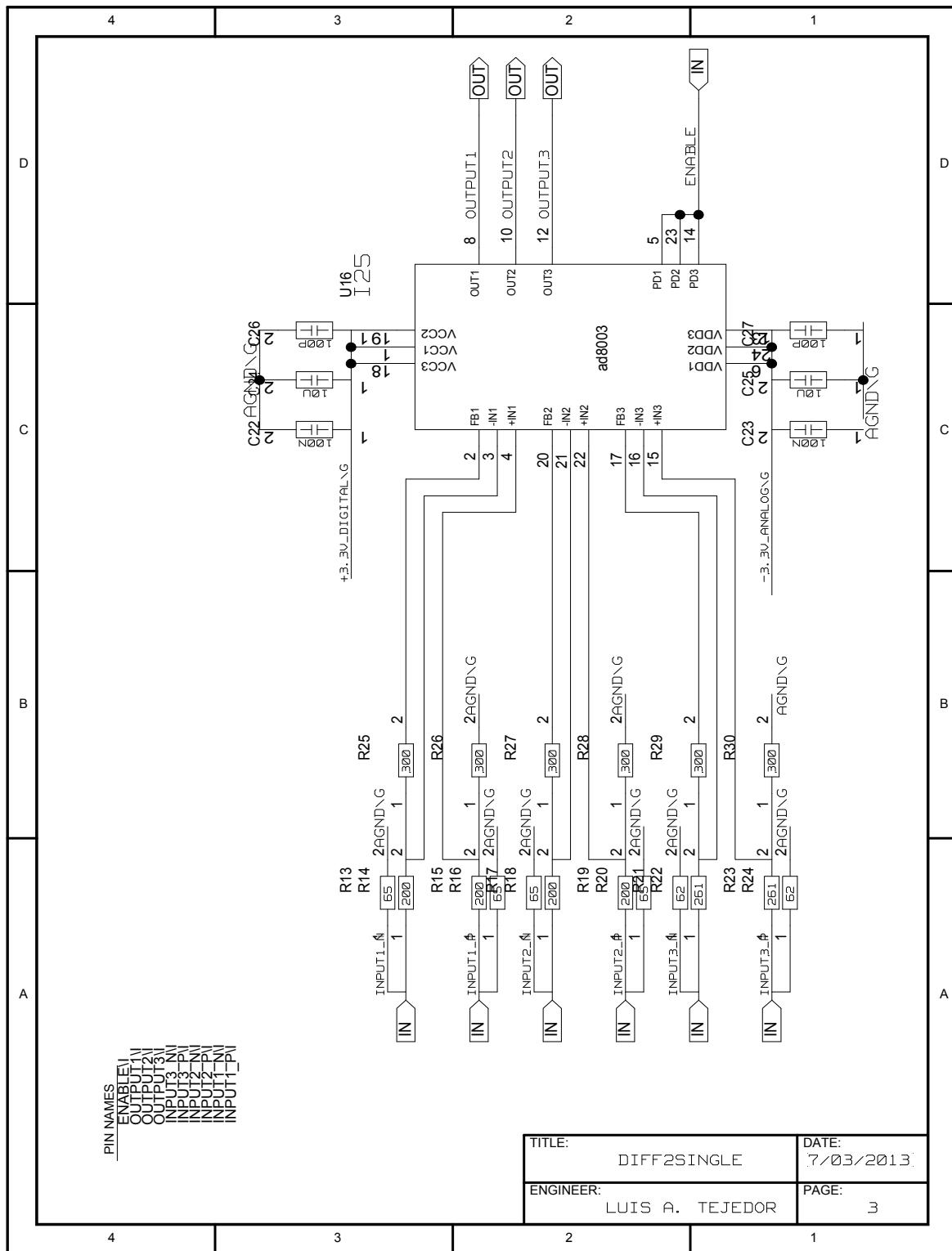
**A. Schematics**

Figure A.3: L1: Differential to Single-Ended (channels 0,1, and 2)

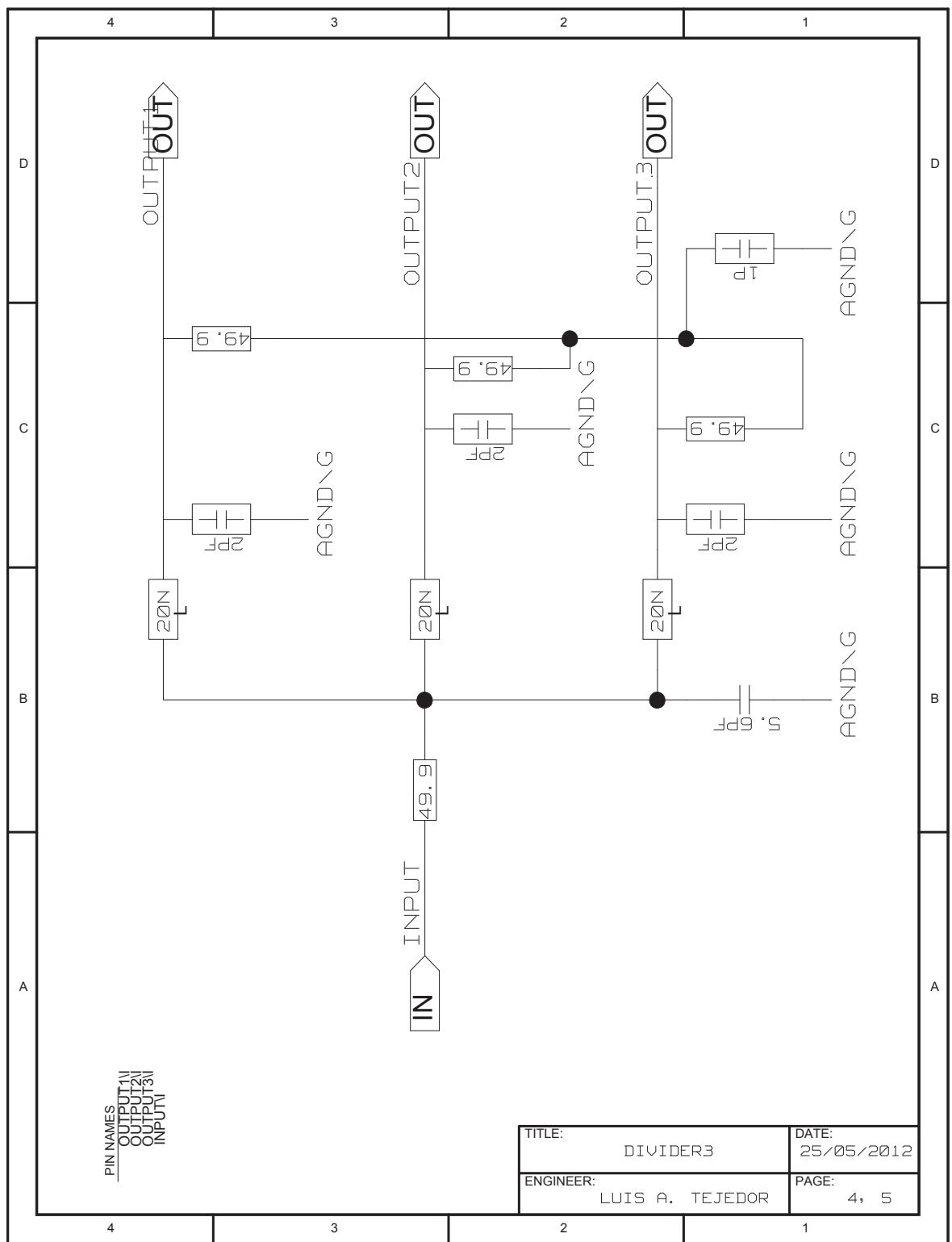


Figure A.4: L1: 3 branches splitter

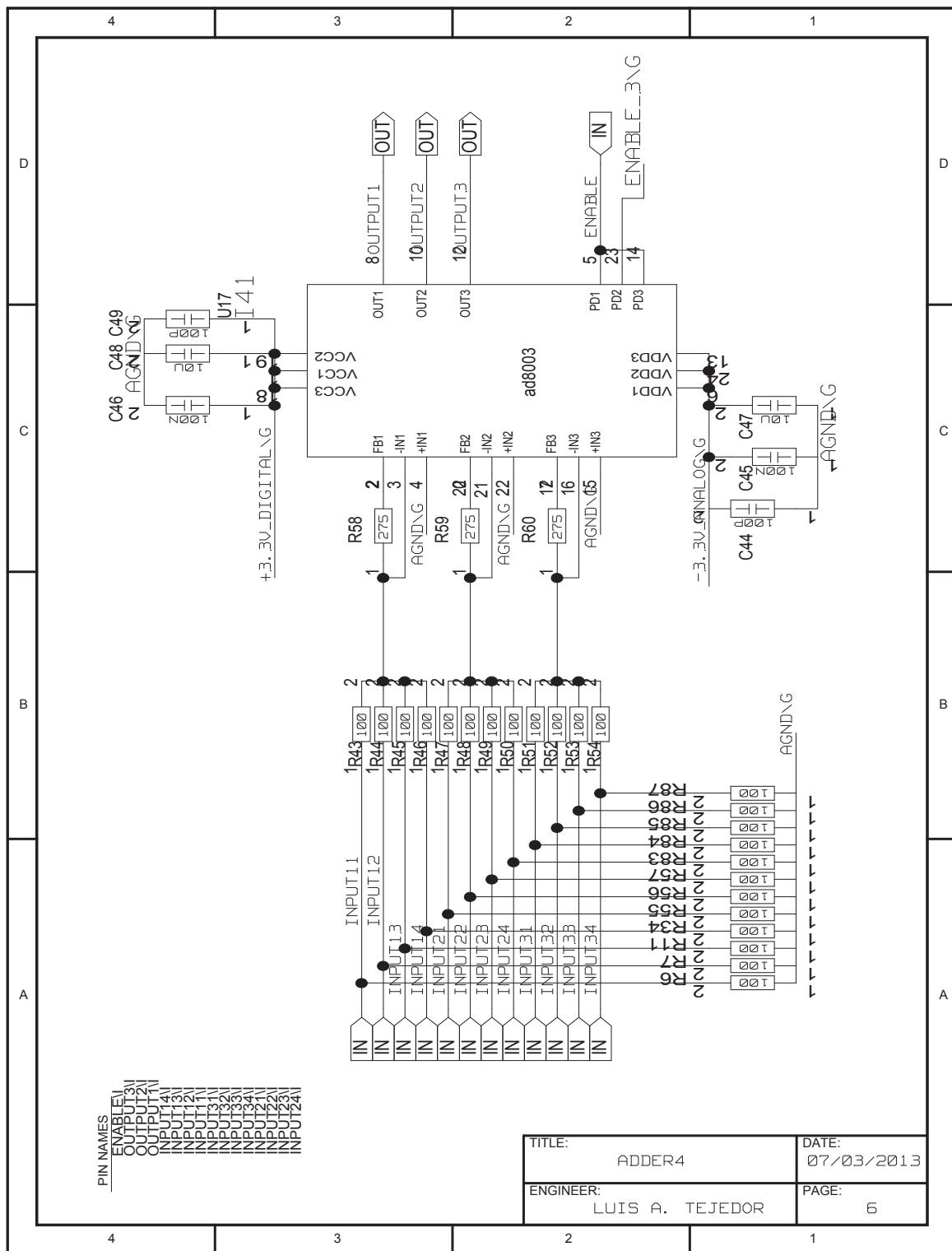


Figure A.5: L1: 4 inputs adders

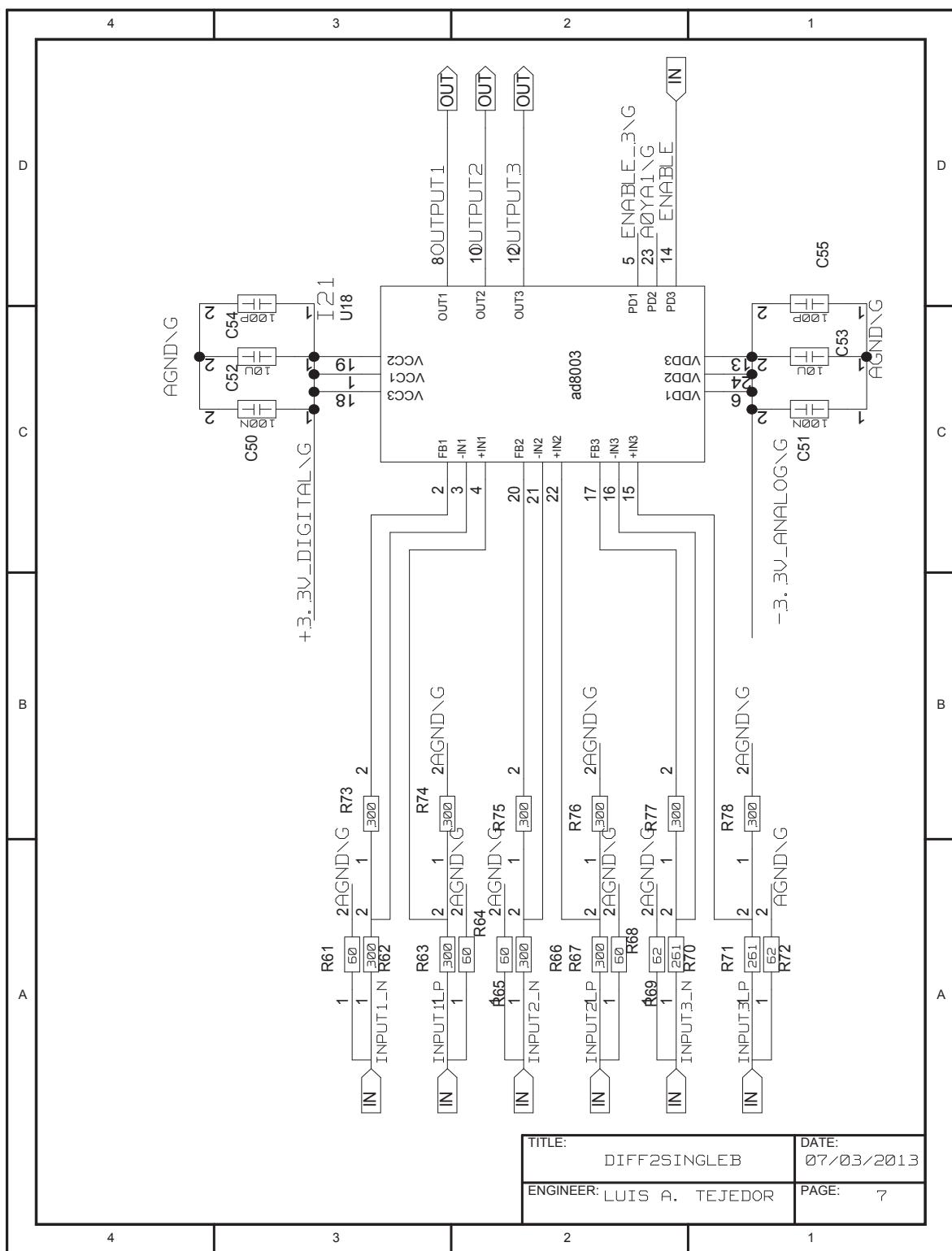


Figure A.6: L1: Differential to Single-Ended (channels 3, 4 and 5)

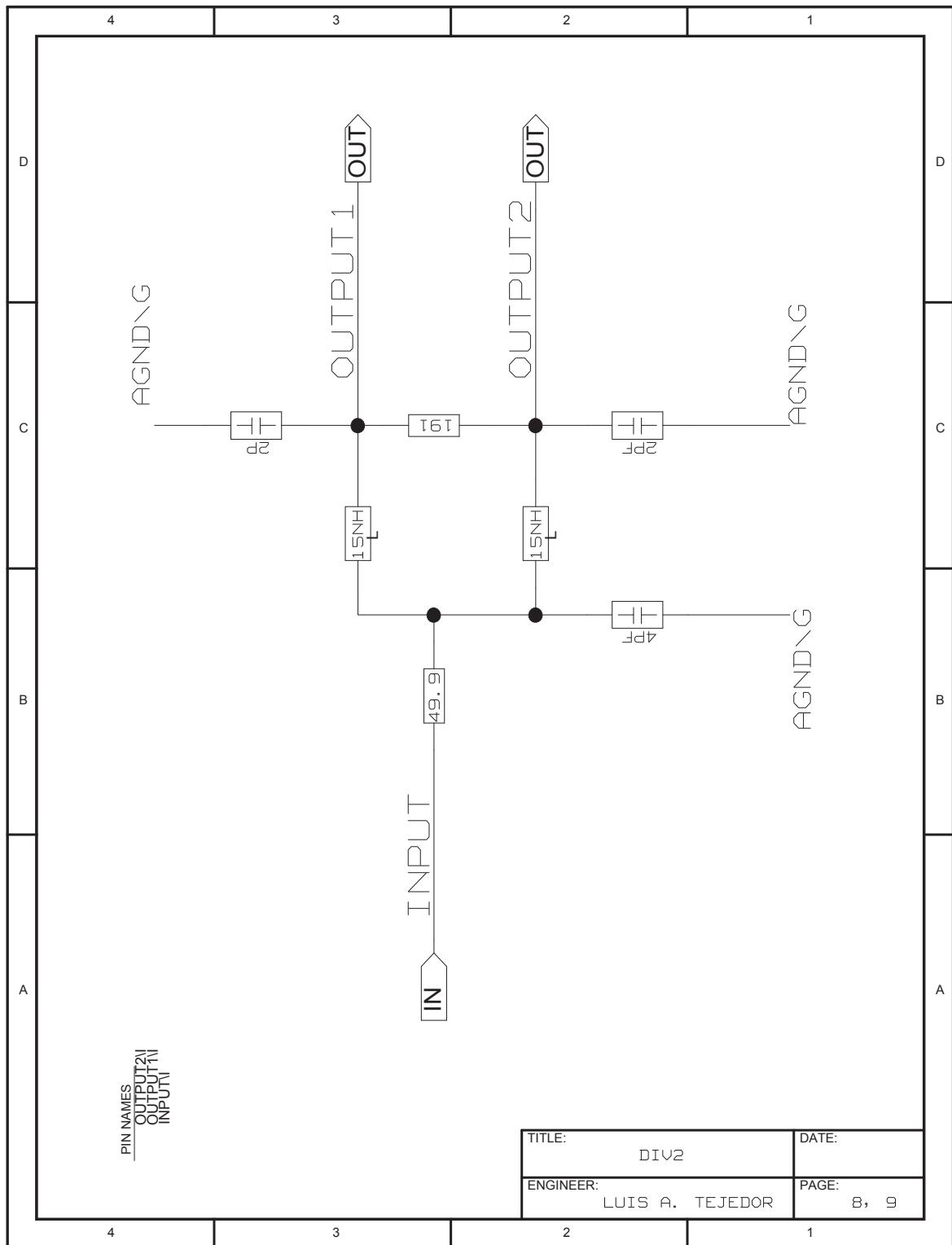


Figure A.7: L1: 2 branches splitter

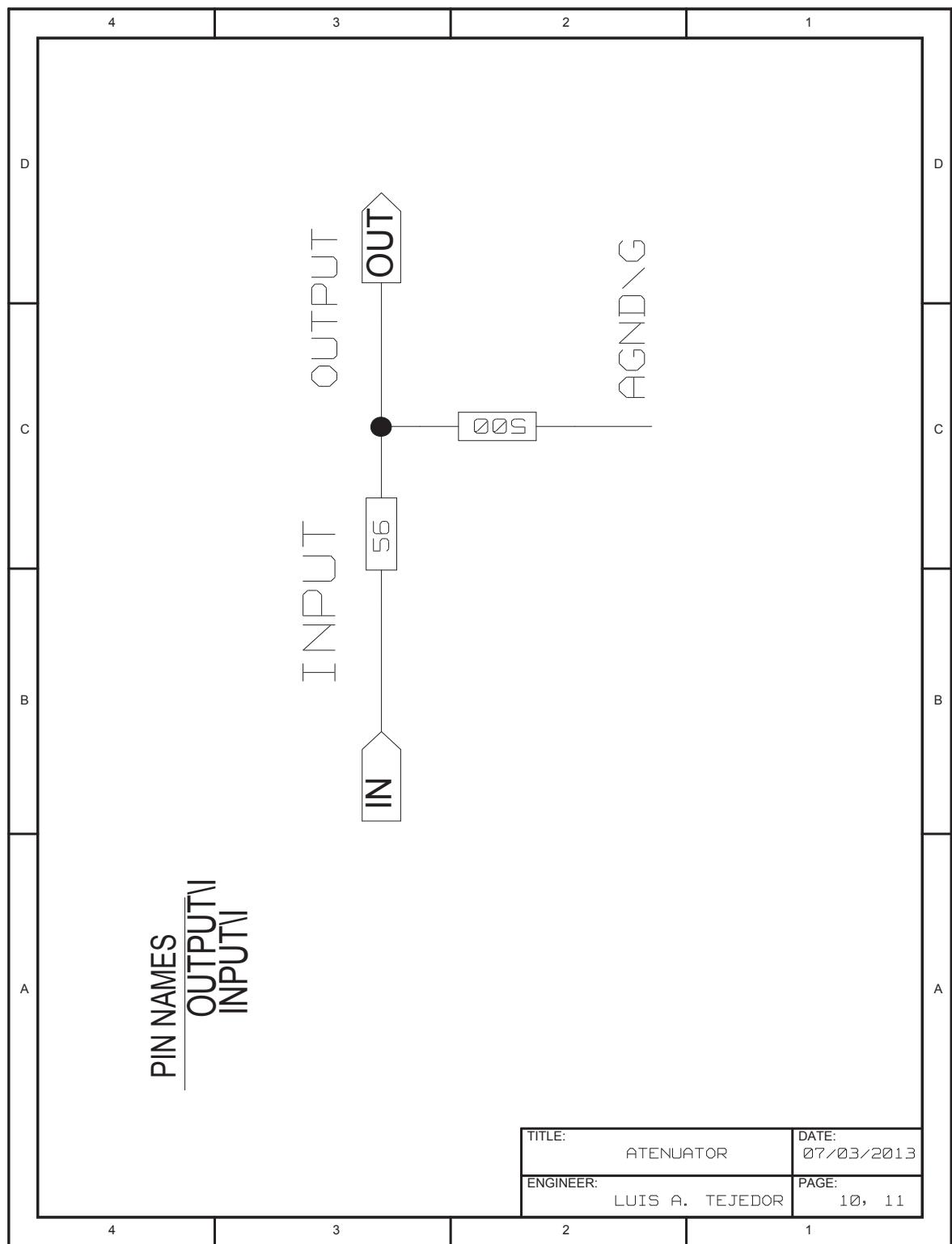


Figure A.8: L1: Attenuator

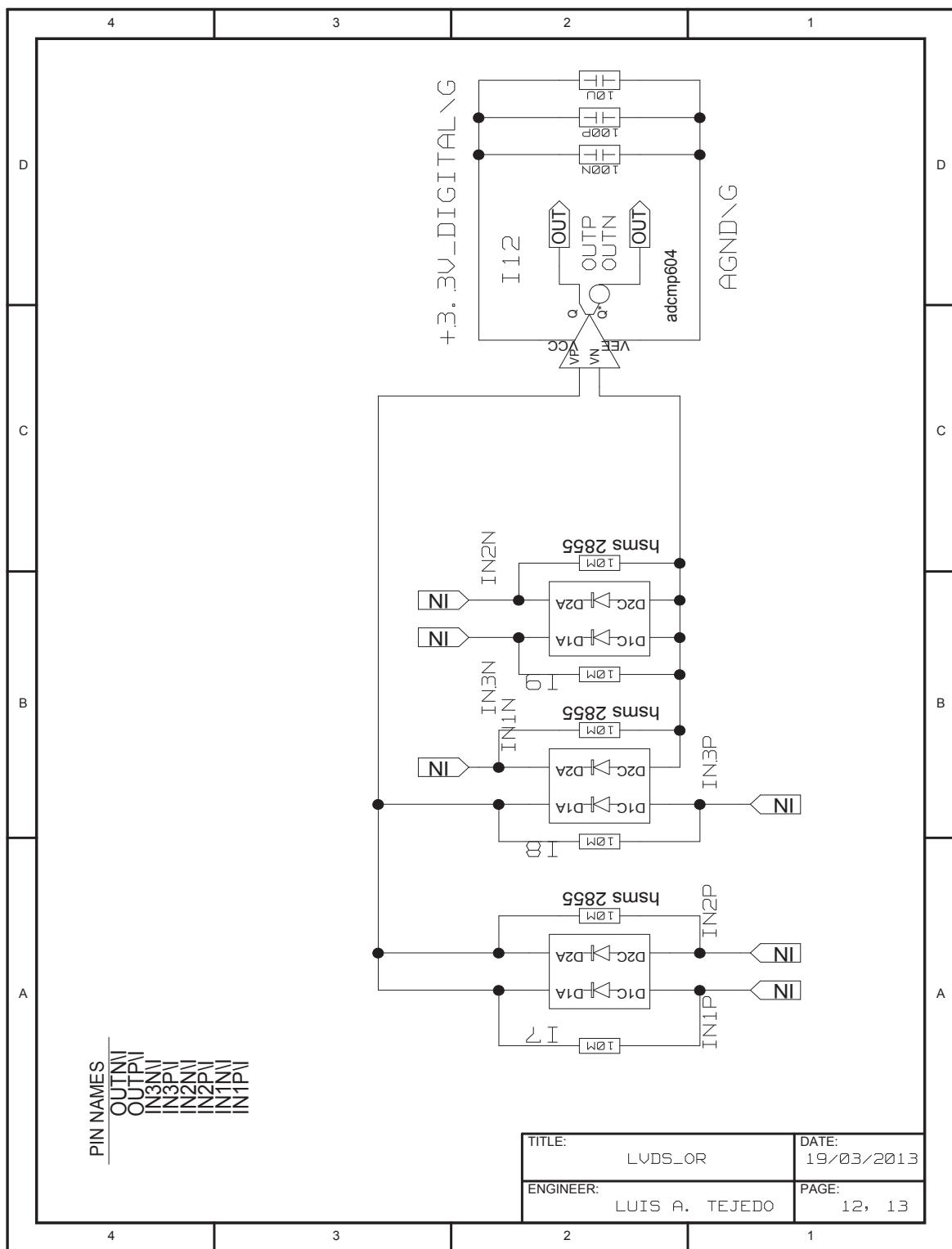


Figure A.9: L1: LVDS OR gate

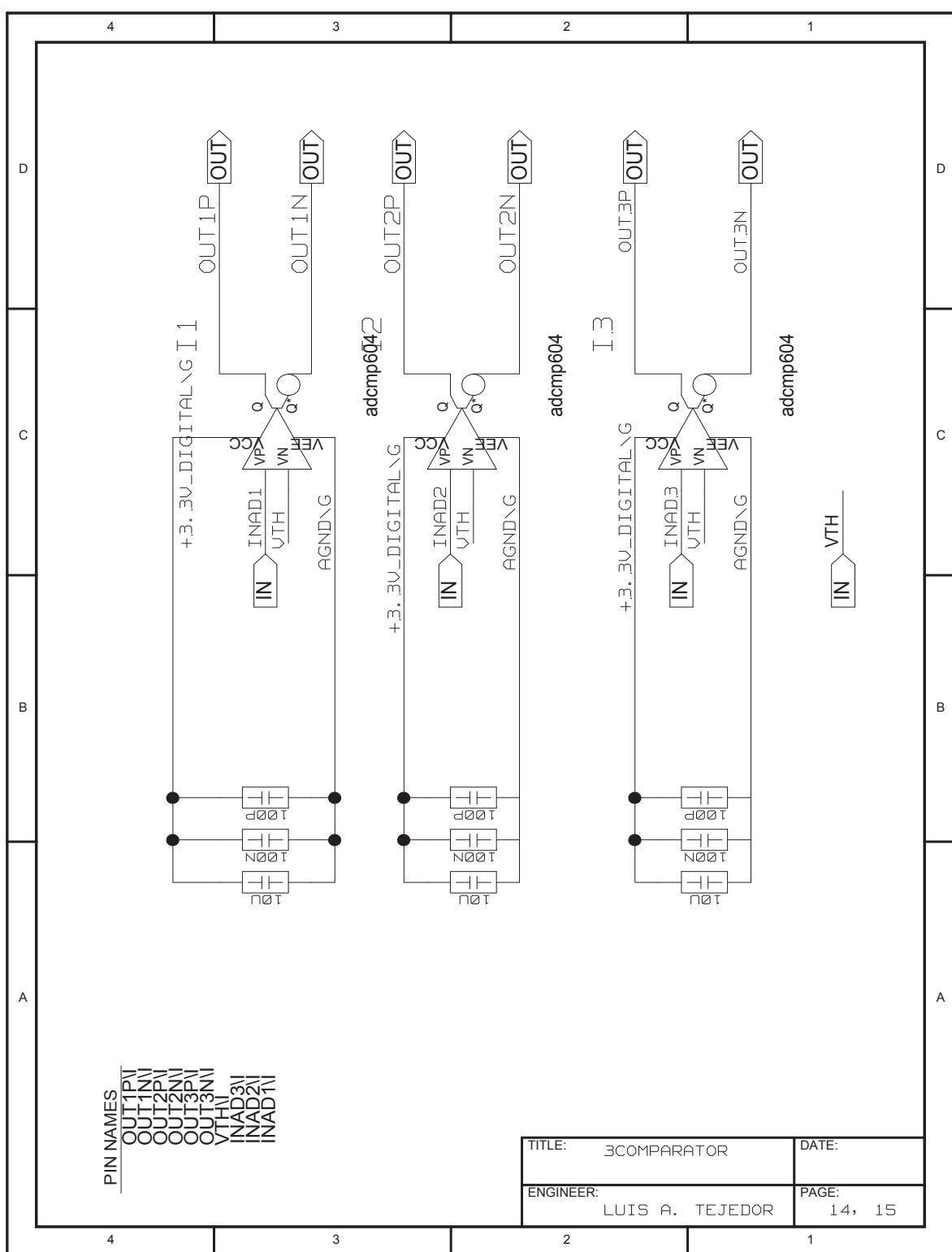


Figure A.10: L1: comparators

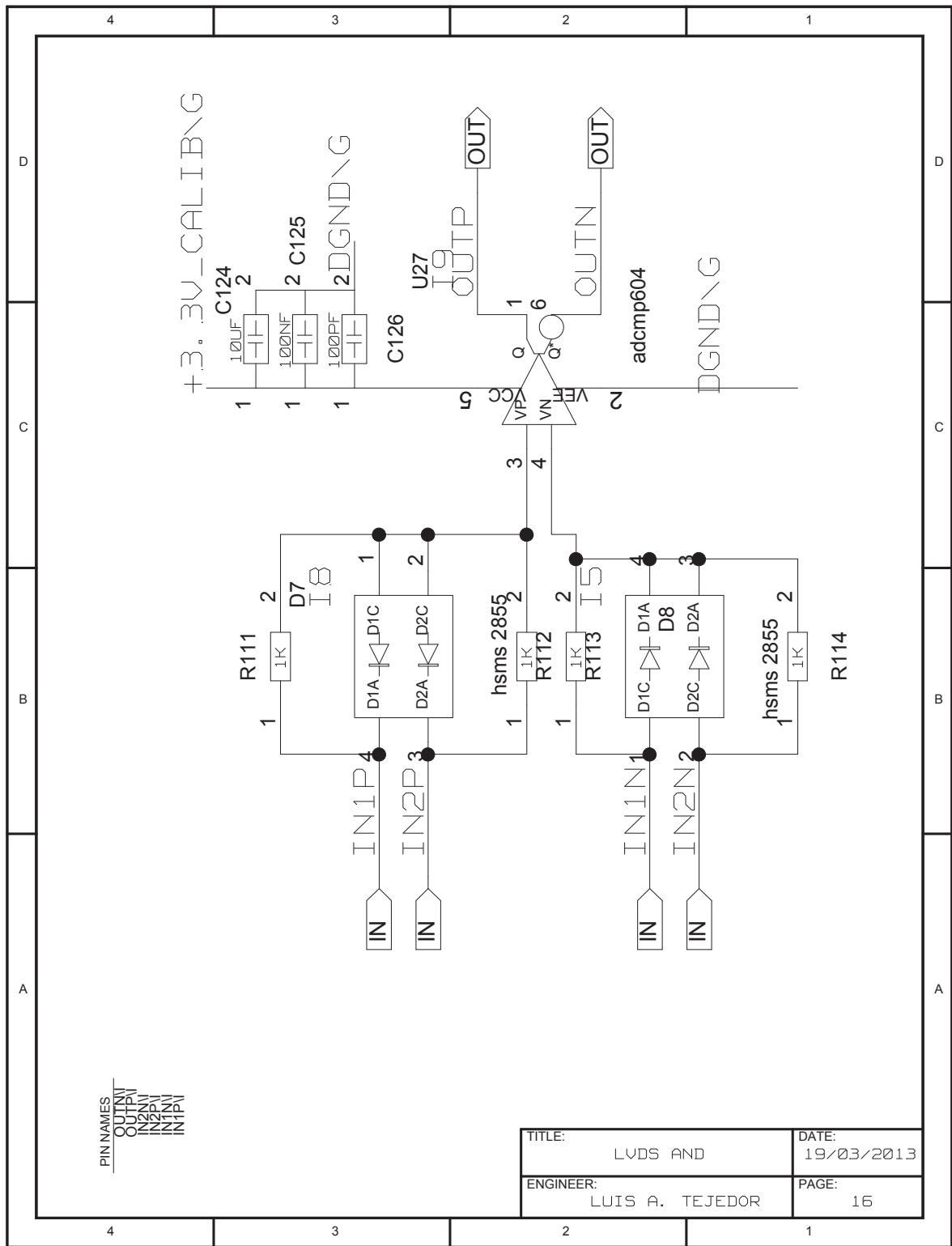


Figure A.11: L1: LVDS AND gate

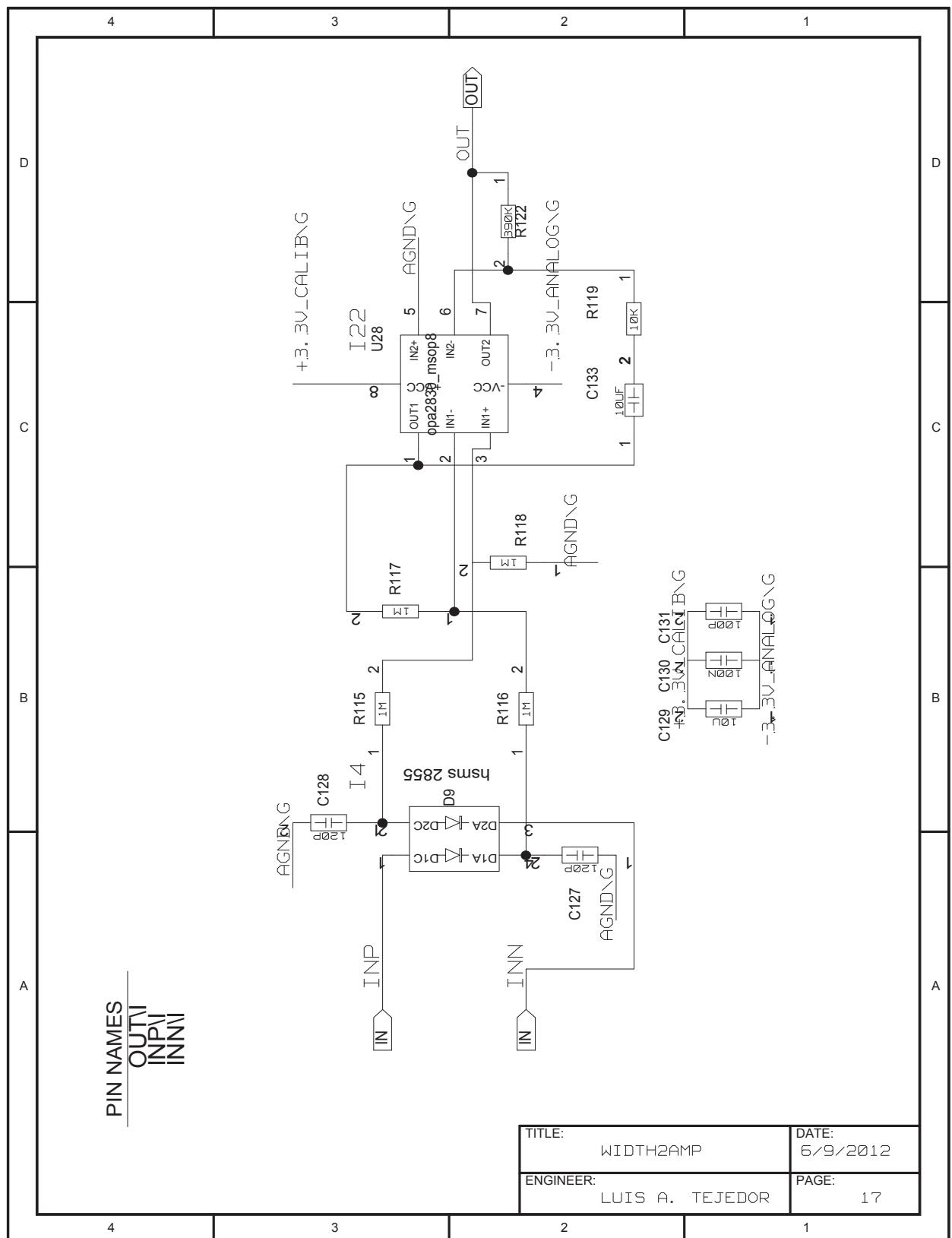


Figure A.12: L1: Width to Amplitude converter

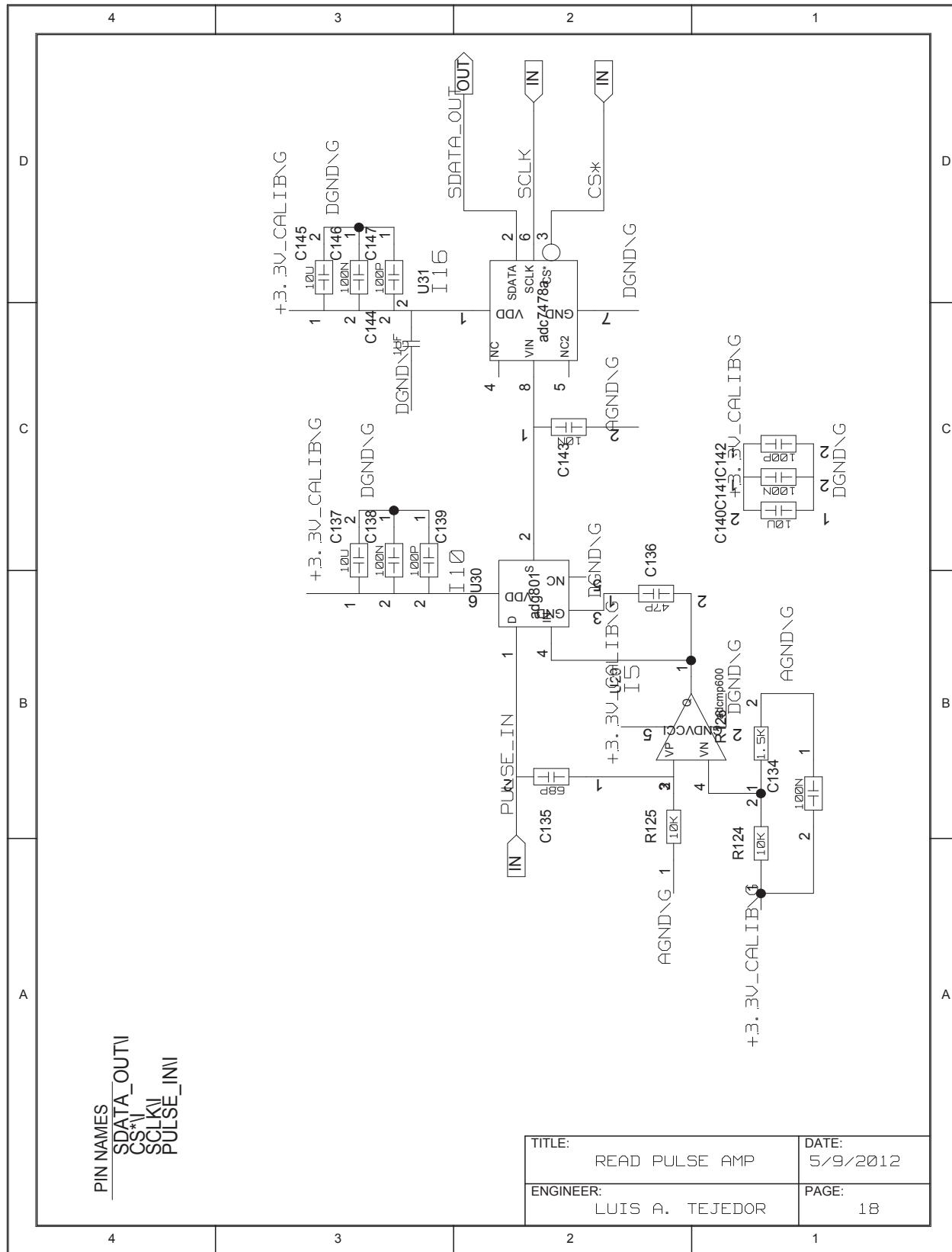
**A. Schematics**

Figure A.13: L1: Read Pulse Amplitude circuit

## A.2 Trigger interface board schematics

## A. Schematics

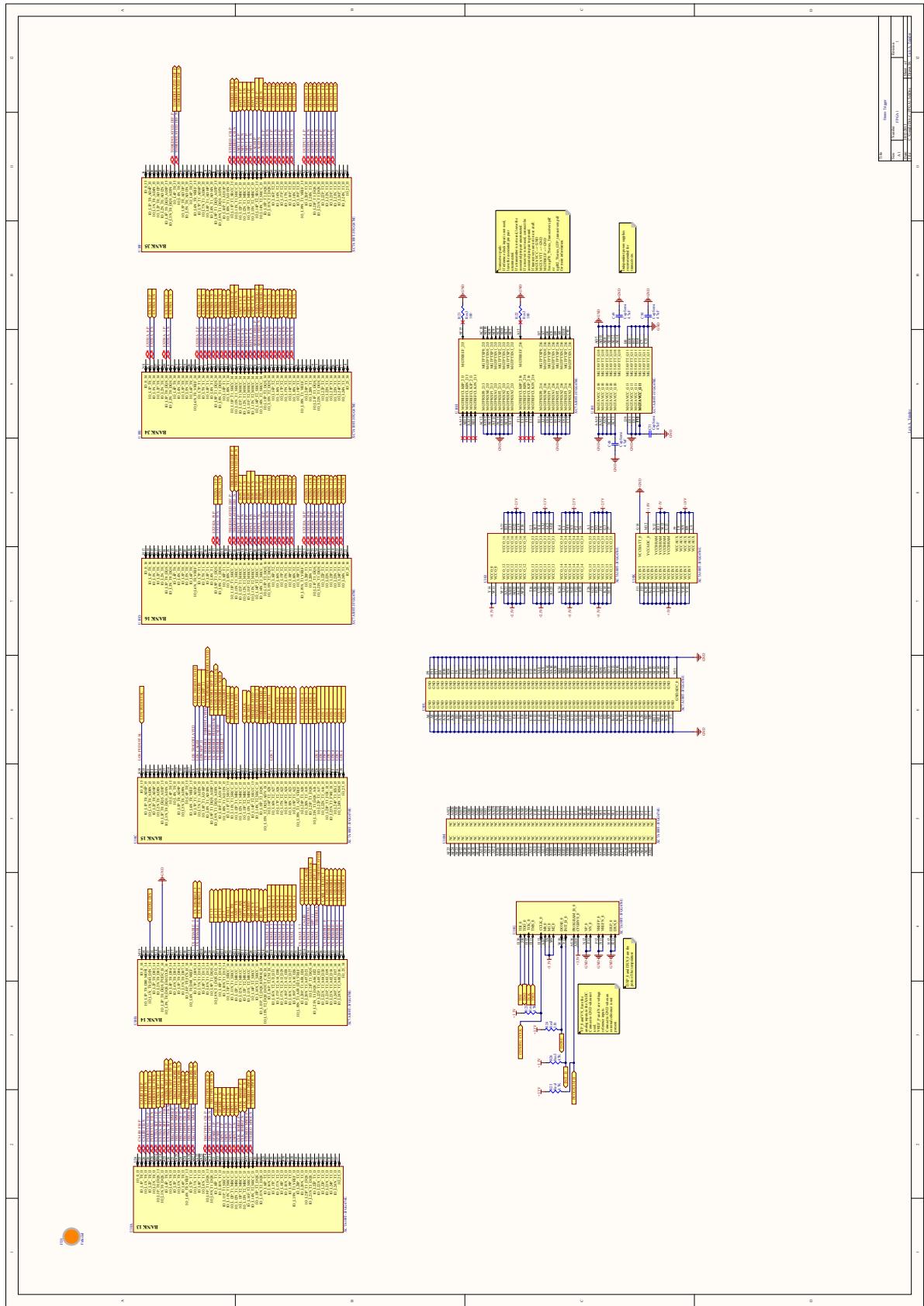


Figure A.14: TIB: FPGA pins

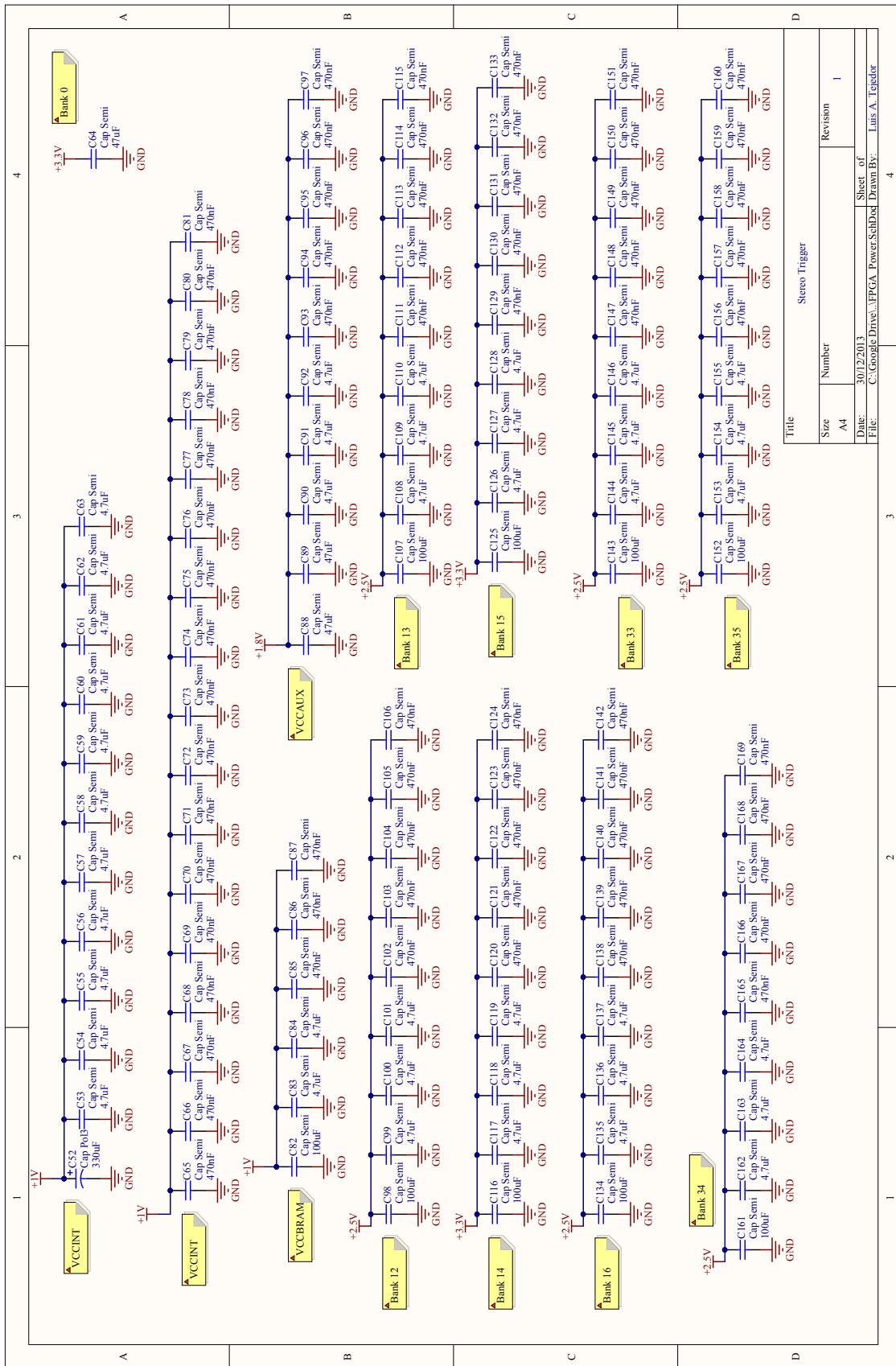


Figure A.15: TIB: FPGA power filtering

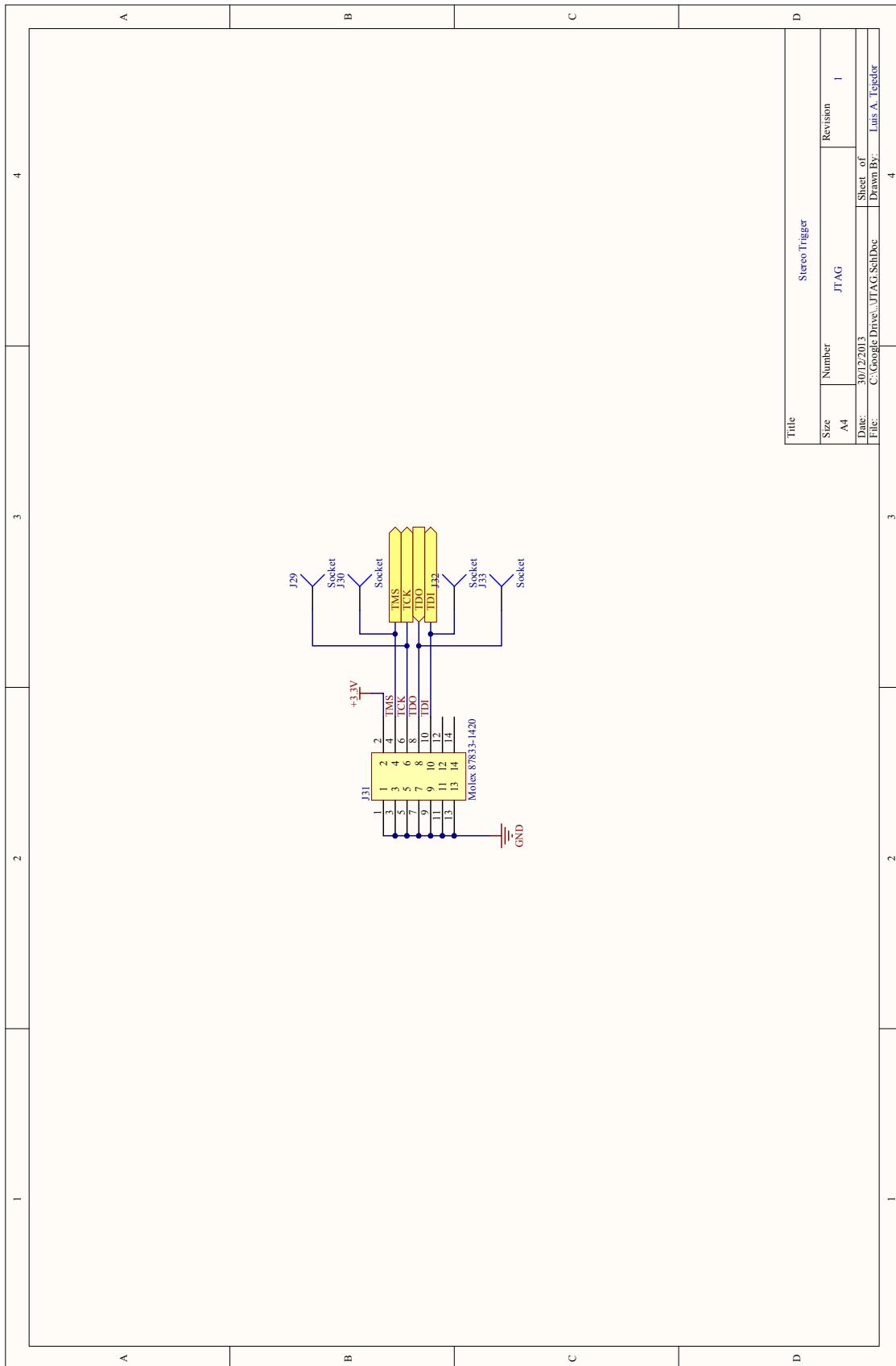
**A. Schematics**

Figure A.16: TIB: JTAG connector

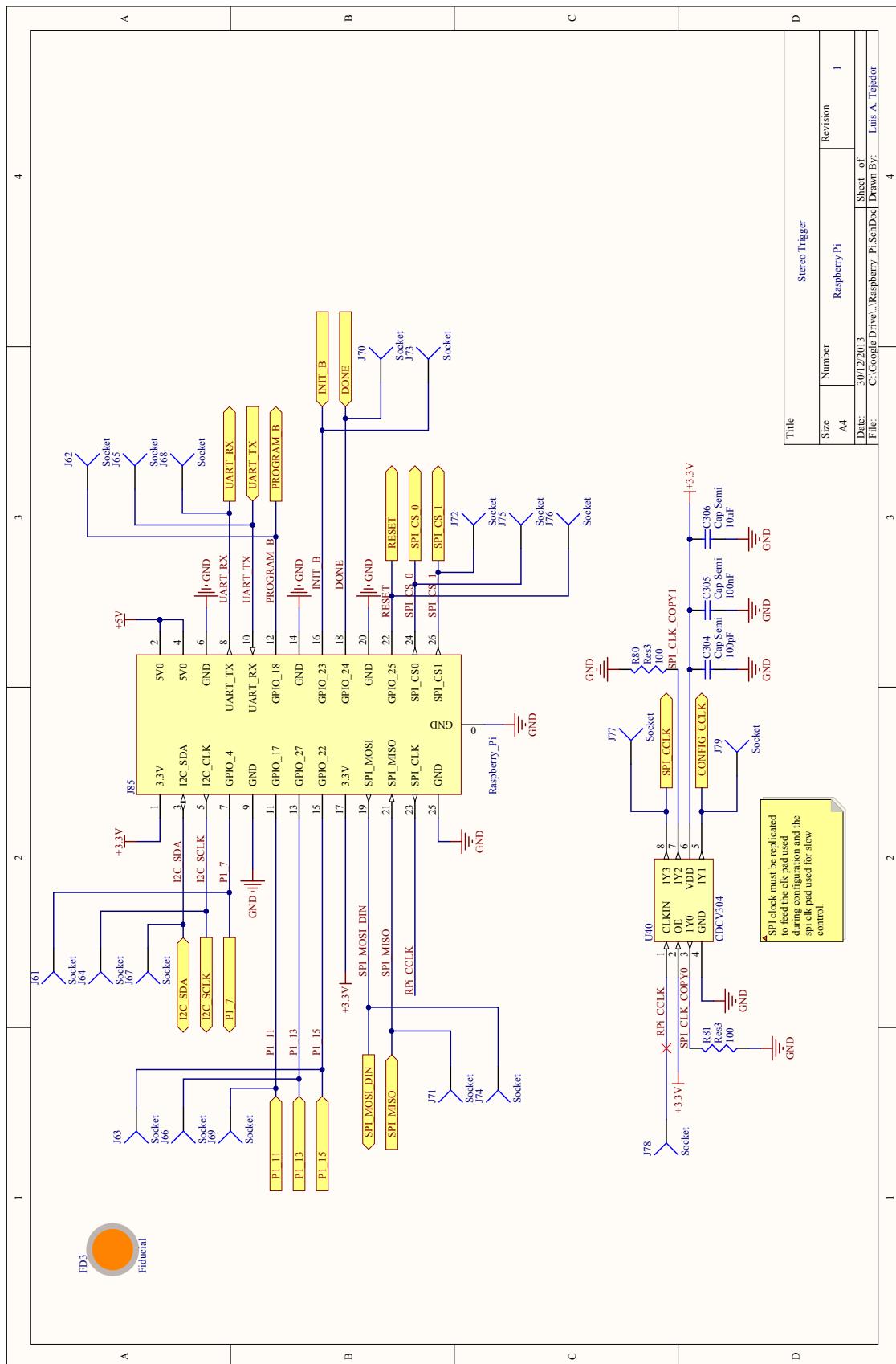


Figure A.17: TIB: Raspberry Pi pins

## A. Schematics

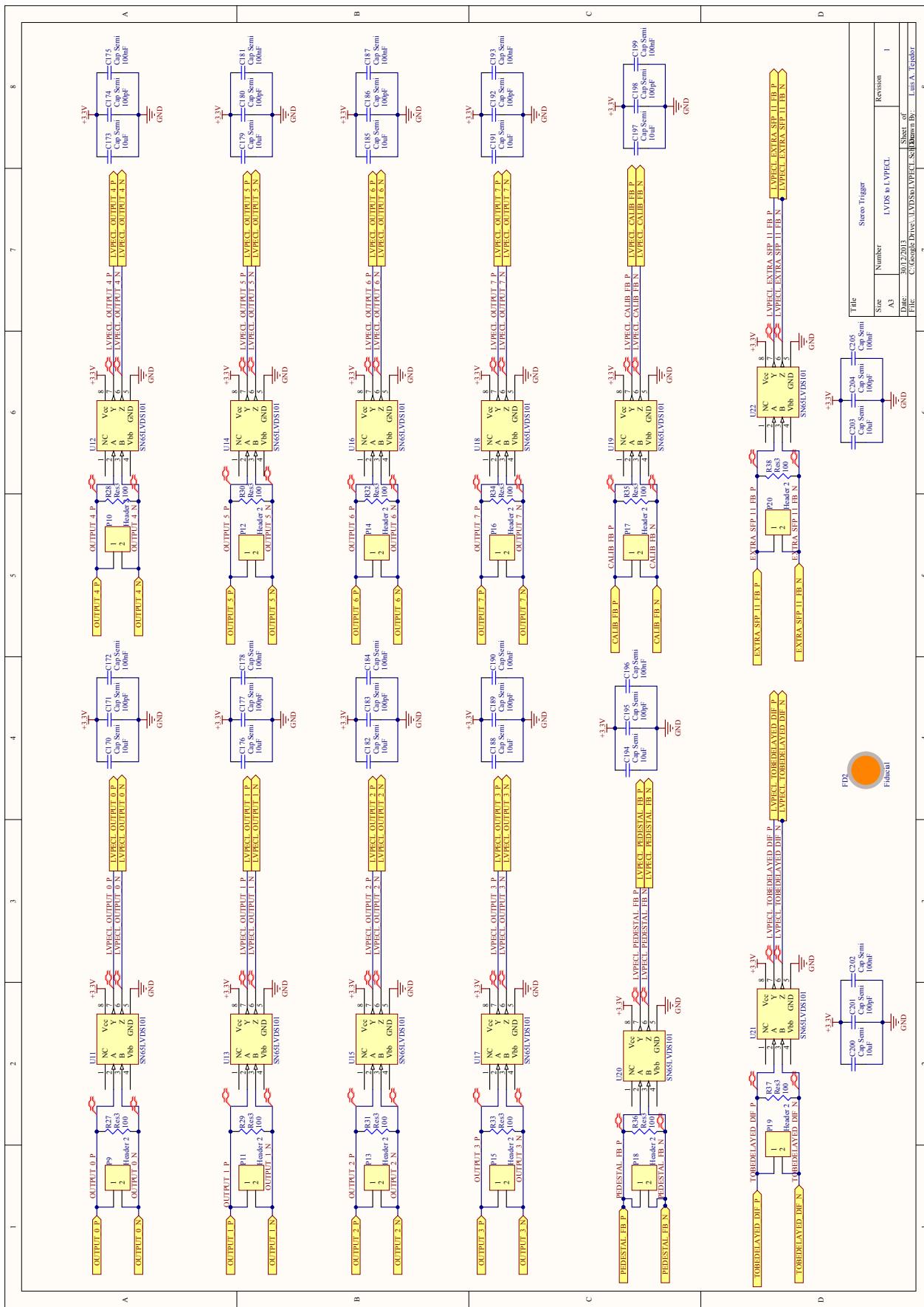


Figure A.18: TIB: LVDS to LVPECL translators

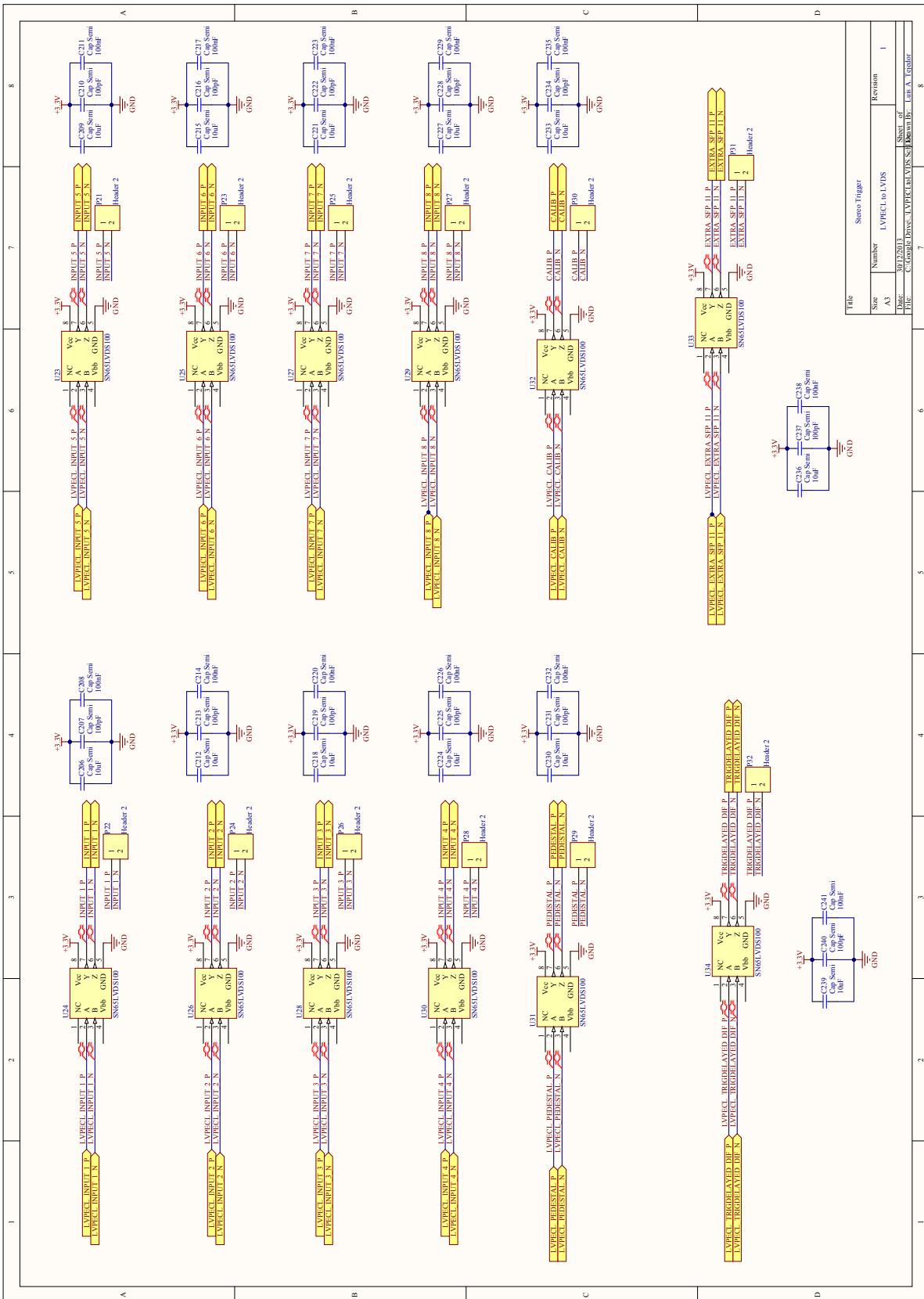


Figure A.19: TIB: LVPECL to LVDS translators

## A. Schematics

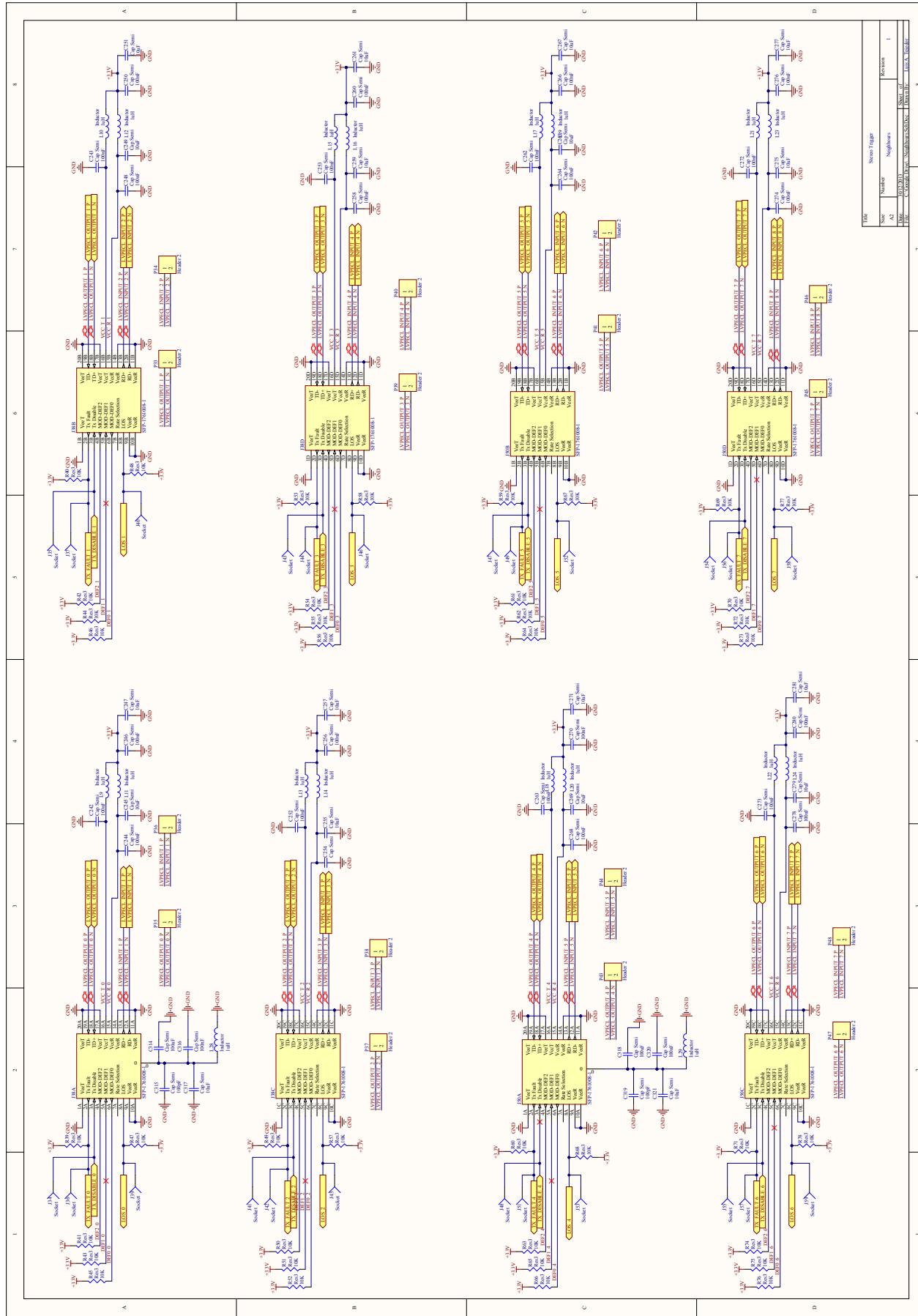


Figure A.20: TIB: Optical transceivers to/from neighbours

## A. Schematics

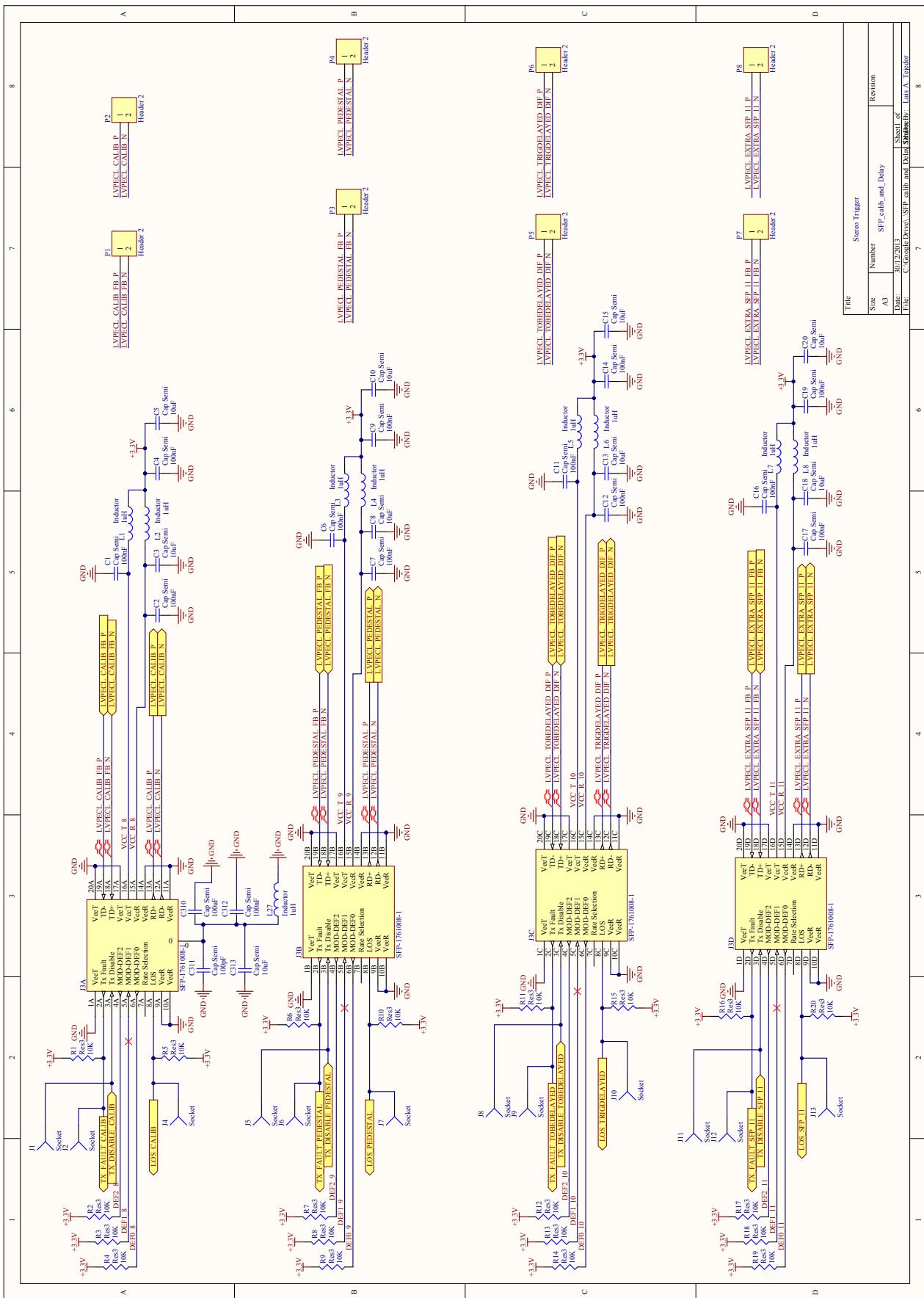


Figure A.21: TIB: Optical transceivers to/from calibration box

## A. Schematics

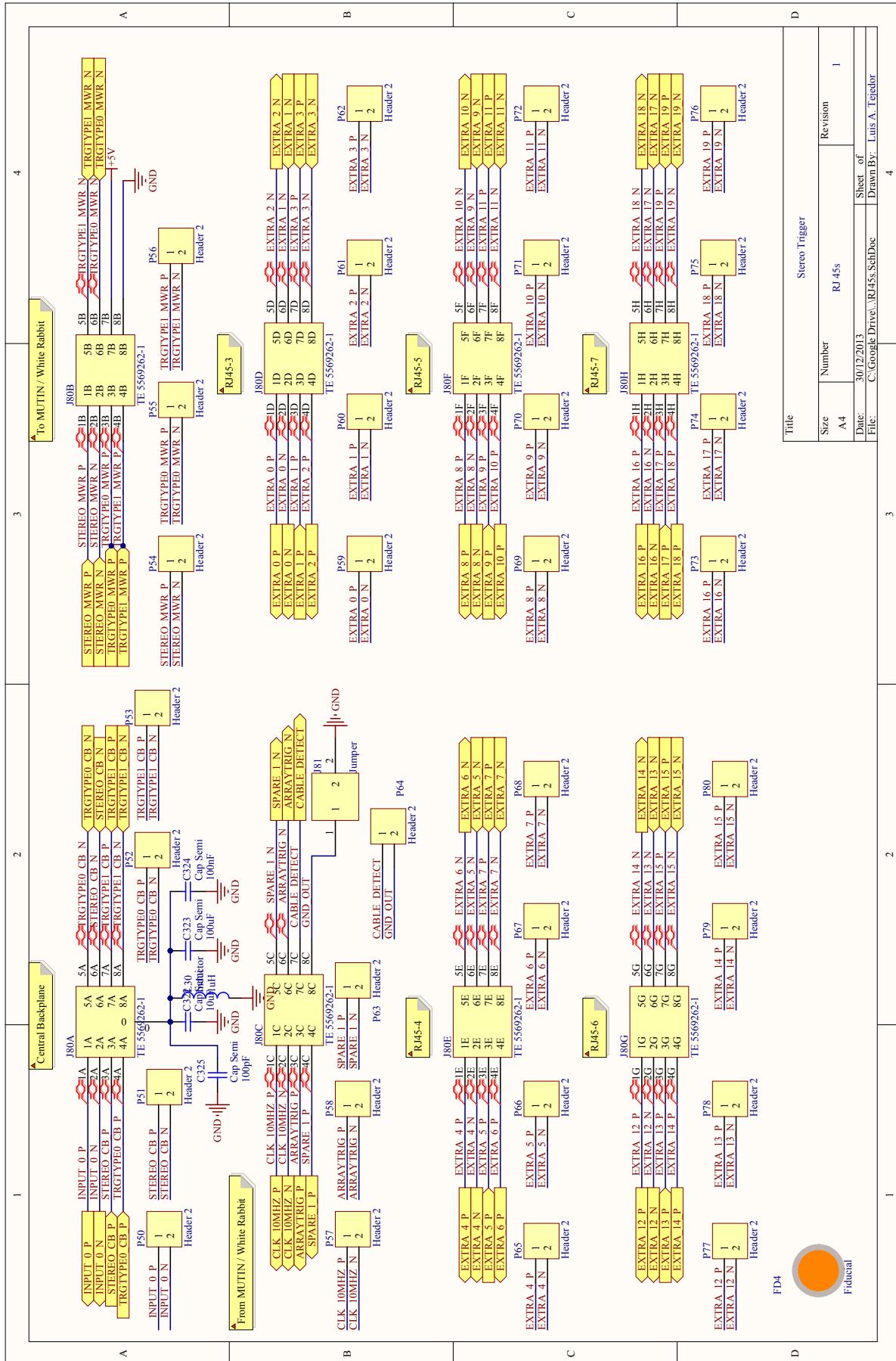


Figure A.22: TIB: RJ45 connectors

## A. Schematics

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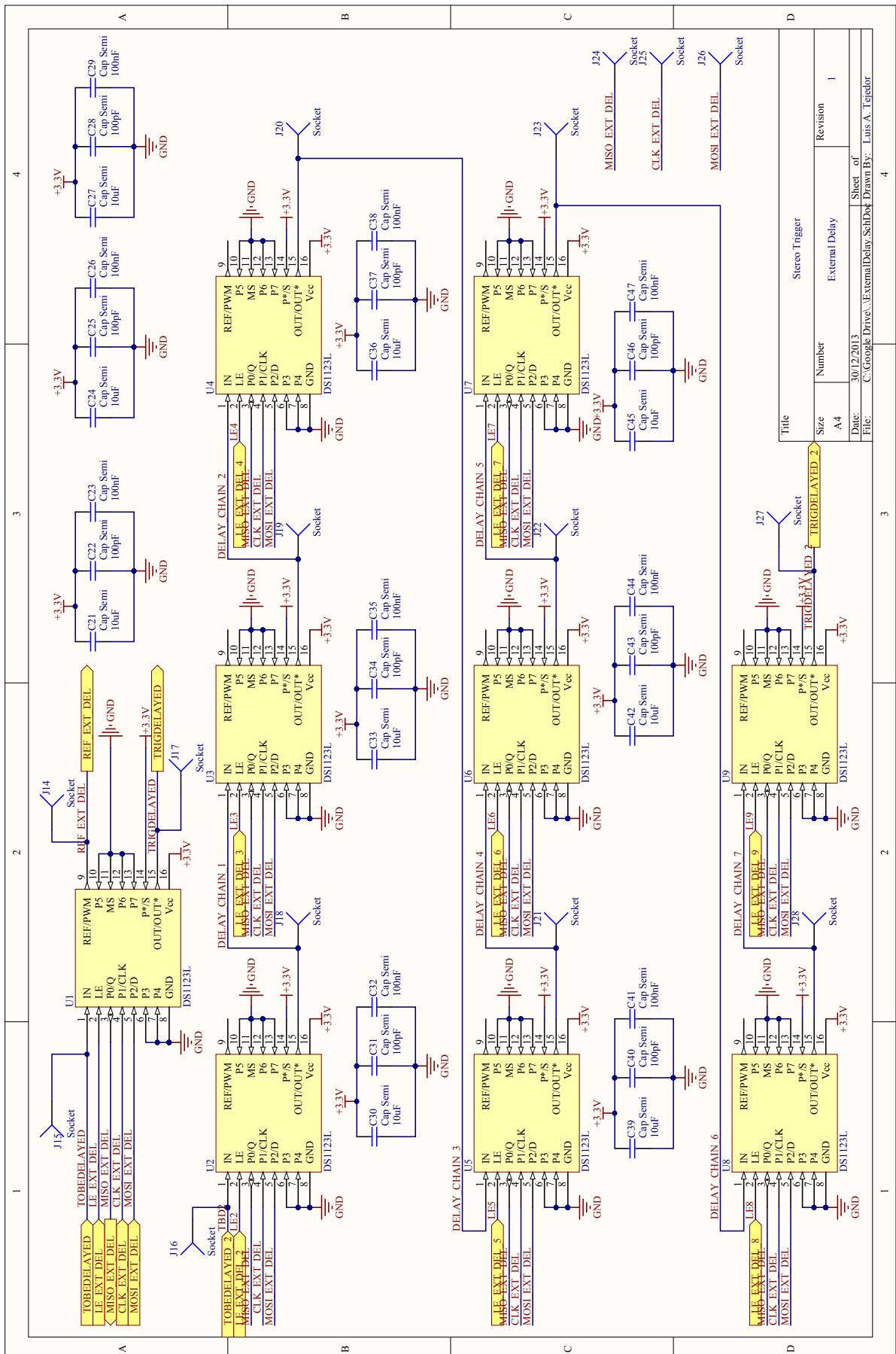


Figure A.23: TIB: External delays

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## A. Schematics

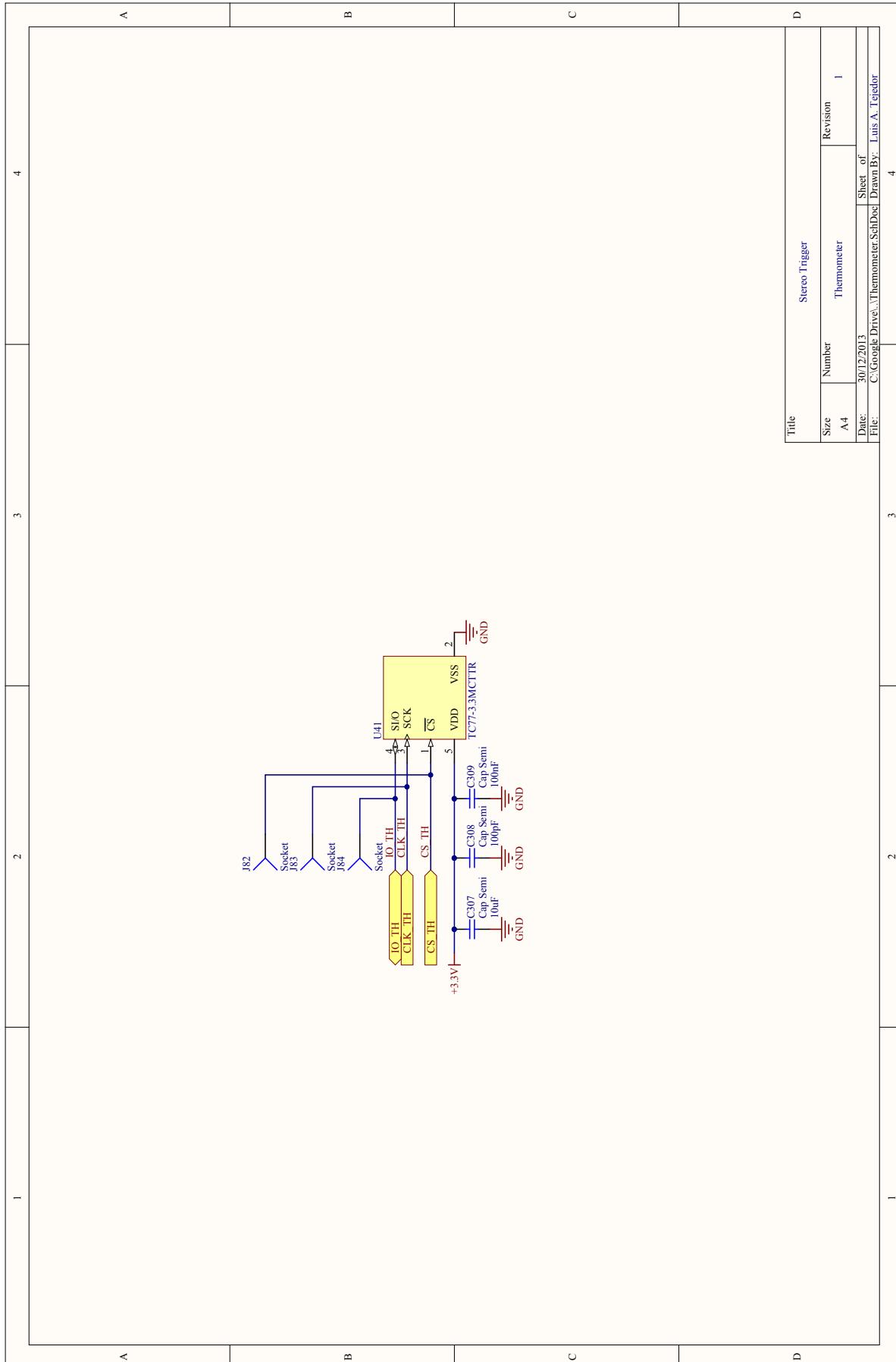


Figure A.24: TIB: Thermometer

## A. Schematics

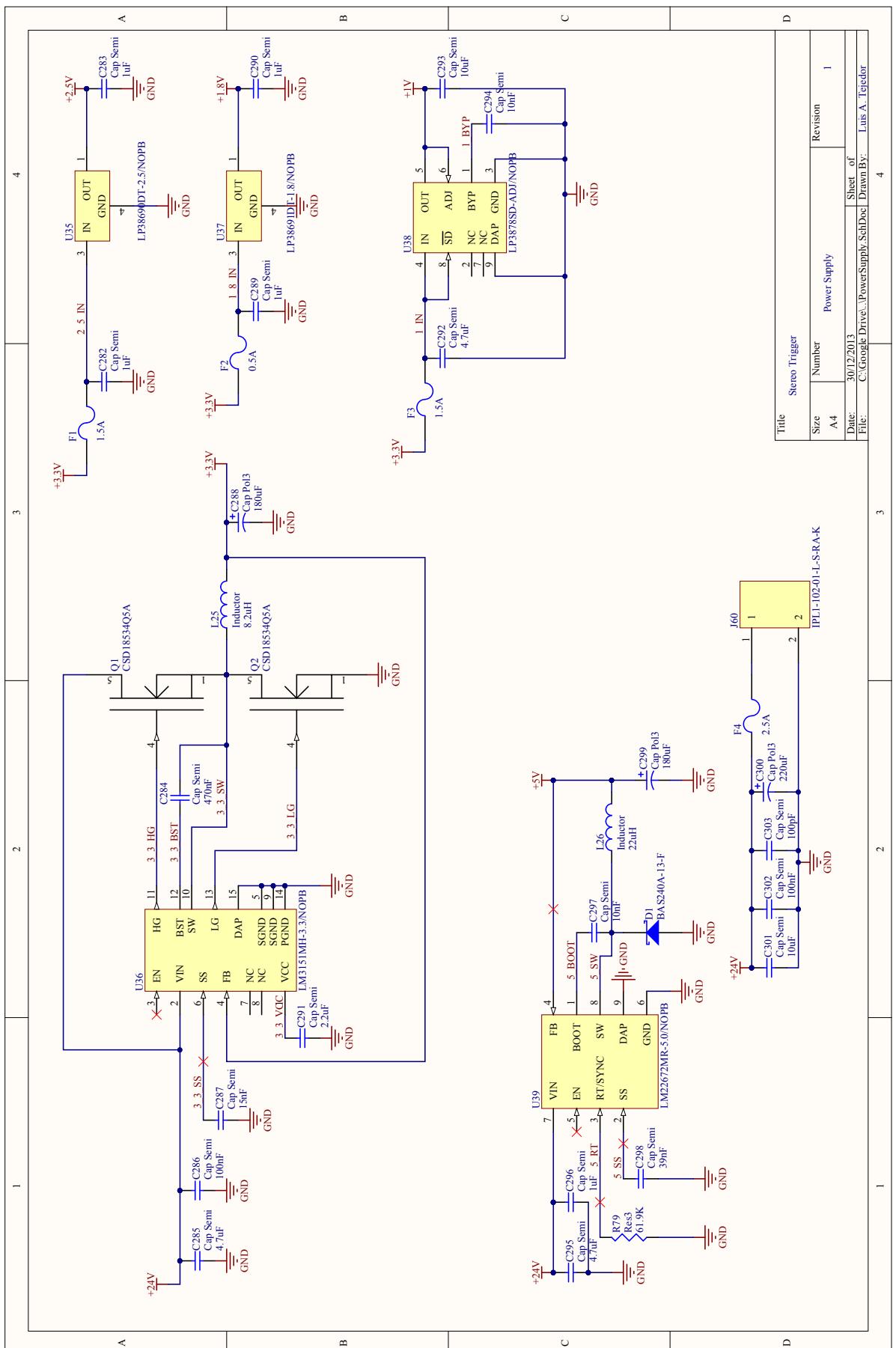


Figure A.25: TIB: Power supplies

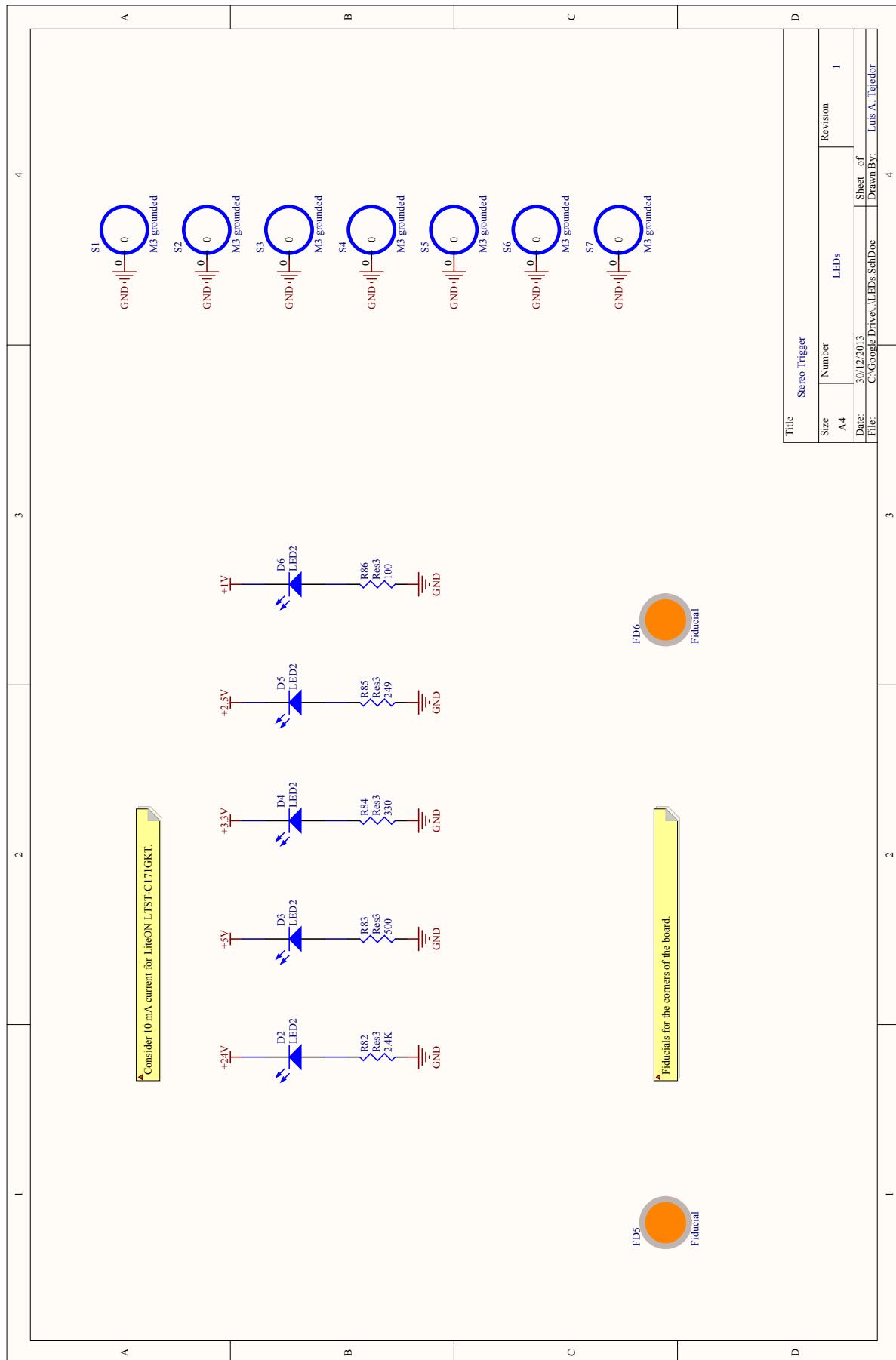
**A. Schematics**

Figure A.26: TIB: Power monitor LEDs, mechanical holes and grounding

# Appendix B

## Bill of materials

### B.1 Bill of materials of Level 1

The following table shows the cost of the different devices which are part of the Level 1 trigger subsystem:

Functionality	Reference	Manufacturer	Cost/unit(€)		Quantity	Total cost(€)	
			min	max		min	max
Differential to single-ended	AD8003	Analog Devices	2.92	3.44	2	5.84	6.88
	Resistors	Various	0.01	0.02	36	0.36	0.72
	Capacitors	Various	0.02	0.05	12	0.24	0.60
Splitter 3	Inductors	Tyco Electronics	0.10	0.15	6	0.60	0.90
	Resistors	Various	0.01	0.02	8	0.08	0.16
	Capacitors	Various	0.02	0.05	10	0.20	0.50
Splitter 2	Inductors	Tyco Electronics	0.10	0.15	4	0.20	0.40
	Resistors	Various	0.01	0.02	4	0.04	0.08
	Capacitors	Various	0.02	0.05	6	0.12	0.30
Attenuator	Resistors	Various	0.01	0.02	4	0.04	0.08
Switching Network	ADG901	Analog Devices	0.98	1.02	8	7.84	8.16
	Capacitors	Various	0.02	0.05	16	0.32	0.80
Matching and decoupling	Resistors	Various	0.01	0.02	19	0.19	0.38
	Capacitors	Various	0.02	0.05	22	0.44	1.10
Slow Control Logic	74HC00	NXP	0.10	0.15	1	0.10	0.15
	SN74LVC1G32	Texas Inst.	0.12	0.14	1	0.12	0.14
	Capacitors	Various	0.02	0.15	6	0.12	0.30
Adder	AD8003	Analog Devices	2.92	3.44	1	2.92	3.44
	Resistors	Various	0.01	0.02	27	0.27	0.54
	Capacitors	Various	0.02	0.05	6	0.12	0.30
Comparator	ADCMP604	Analog Devices	2.18	2.78	3	6.54	8.34
	Capacitors	Various	0.02	0.05	9	0.18	0.45
Comparator Colibri	ADCMP604	Analog Devices	2.18	2.78	3	6.54	8.34
	Capacitors	Various	0.02	0.05	9	0.18	0.45

LVDS OR gate	HSMS2855 ADCMP604 Resistors Capacitors	Avago Tech. Analog Devices Various Various	0.67 2.18 0.01 0.02	0.72 2.78 0.02 0.05	3 1 6 3	2.01 2.18 0.06 0.06	2.16 2.78 0.12 0.15
LVDS OR gate Colibri	HSMS2855 ADCMP604 Resistors Capacitors	Avago Tech. Analog Devices Various Various	0.67 2.18 0.01 0.02	0.72 2.78 0.02 0.05	3 1 6 3	2.01 2.18 0.06 0.06	2.16 2.78 0.12 0.15
LVDS AND gate Delay Calibration	HSMS2855 ADCMP604 Resistors Capacitors	Avago Tech. Analog Devices Various Various	0.67 2.18 0.01 0.02	0.72 2.78 0.02 0.05	2 1 4 3	1.34 2.18 0.04 0.06	1.44 2.78 0.08 0.15
Width to Amplitude Delay Calibration	HSMS2855 OPA2830 Resistors Capacitors	Avago Tech. Texas Inst. Various Various	0.67 0.76 0.01 0.02	0.72 1.00 0.02 0.05	1 1 6 6	0.67 0.76 0.06 0.12	0.72 1.00 0.12 0.30
Read Pulse Amplitude Delay Calibration	ADCMP600 ADG801 AD7478A Resistors Capacitors	Analog Devices Analog Devices Analog Devices Various Various	1.25 0.65 0.65 0.01 0.02	1.45 0.75 0.75 0.02 0.05	1 1 1 3 14	1.25 0.65 0.65 0.03 0.28	1.45 0.75 0.75 0.06 0.70
Output switch Delay Calib.	ADG936 Capacitors	Analog Devices Various	1.10 0.02	1.20 0.05	1 3	1.10 0.06	1.20 0.15
Power Supply Delay Calibration	AP2141 Resistors Capacitors	Diodes Zetex Various Various	0.30 0.01 0.02	0.35 0.02 0.05	1 1 7	0.30 0.01 0.14	0.35 0.02 0.35
DAC	AD5663R Capacitors	Analog Devices Various	3.10 0.02	3.50 0.05	1 12	3.10 0.24	3.50 0.60
<b>Total Components</b>				<b>319</b>	<b>55.26</b>	<b>70.40</b>	

Table B.1: Level 1 bill of materials per cluster: Component costs in €

Table B.1 comprise the costs of the components, which correspond to the final cost of the Level 1 once it will be integrated in the front-end boards. However, the cost of the mezzanines used for the first prototypes was somewhat more expensive. Table B.2 gathers the additional costs of each new manufactured mezzanine, while table B.3 shows the fixed costs of a PCB production, to be shared among all the manufactured boards.

Concept	Manufacturer	Unit price(€)		Quantity	Total cost(€)	
		min	max		min	max
Connector QMSS-016-06.75-L-D-DP-A	Samtec	5.00	6.65	1	5.00	6.65
Connector QMSS-016-06.75-L-D-DP-PC4	Samtec	7.00	7.99	1	7.00	7.99
Capacitors for power filtering	Various	0.02	0.05	6	0.12	0.30
FR4 multilayer PCB manufacturing	Lab Circuits	3.32	8.56	1	3.32	8.56
Board assembly	SETI Electrónica	19.94	30.40	1	19.94	30.40
<b>Additional mezzanine cost (€)</b>					<b>35.38</b>	<b>53.90</b>

Table B.2: Level 1 bill of materials per cluster: Mezzanine manufacturing costs in €

Concept	Manufacturer	Unit price(€)		Quantity	Total cost(€)	
		min	max		min	max
PCB manufacturing fixed costs	Lab Circuits	597.00	1056.00	1	597.00	1056.00
Silk Screen	SETI Electrónica	150.00	150.00	2	300.00	300.00
SMD Pick & Place program	SETI Electrónica	120.00	120.00	1	120.00	120.00
<b>Board batch production fixed cost (€)</b>					<b>1017.00</b>	<b>1476.00</b>

Table B.3: Level 1 mezzanine production fixed costs in €

## B.2 Bill of materials of the trigger interface board

Table B.4 contains all the costs required to manufacture one trigger interface board module. Unlike in the case of Level 1, the TIB is an independent module, so the costs of manufacturing the PCB and assembling the components must be always taken into account. Additionally, there will be also some fixed costs gathered in table B.5 to be shared between all the manufactured boards<sup>1</sup>. The total number of TIBs will quite smaller, so from the manufacturer point of view all of the boards will be considered as prototypes, which means more expensive prices.

Component	Value	Unit price (€)		Quantity	Cost (€)	
		min	max		min	max
LP38690DT-2.5		0.79	0.91	1	0.79	0.91
LM22672MR-5.0		2.00	2.72	1	2.00	2.72
CDCV304PWRG4		1.63	2.08	1	1.63	2.08
DS1123L-200		11.51	11.51	9	103.59	103.59
SFP box x4		24.93	27.61	3	74.79	82.83
LP38691DT-1.8		0.62	0.826	1	0.82	0.83
CSD18534Q5A		0.76	1.89	2	1.52	3.78
Artix-7 FPGA		203.50	203.50	1	203.50	203.50
B240A-13-F		0.057	0.079	1	0.06	0.08
JTAG connector		0.836	1.41	1	0.84	1.41
Jumper 2 vias		0.062	0.072	1	0.062	0.072
SN65LVDS101		2.68	4.19	12	32.16	50.28
LP3878SD-ADJ		0.92	1.87	1	0.92	1.87
SN65LVDS100		2.60	4.19	12	31.20	50.28
Raspberry Pi connector		3.03	10.13	1	3.03	10.13
RJ45 connector		15.79	17.74	1	15.79	17.74
Power connector		0.68	1.23	1	0.68	1.23
LM3151MHE-3.3		3.16	3.84	1	3.16	3.84
TC77		0.61	0.67	1	0.61	0.67
Green LED SMD		0.038	0.053	5	0.19	0.27
Fuse	0.5 A	0.775	1.141	1	0.78	1.14
Capacitor 0603 10V	1 $\mu$ F	0.003	0.009	4	0.01	0.04
Capacitor 0603 50V	1 $\mu$ F	0.032	0.1	1	0.03	0.1
Inductor 0805	1 $\mu$ H	0.055	0.092	24	1.32	2.21
Inductor 0603	1 $\mu$ H	0.044	0.11	4	0.18	0.44
Fuse	1.5 A	0.674	1.063	2	1.35	2.13
Capacitor 0805	2.2 $\mu$ F	0.077	0.168	1	0.08	0.17
Resistor 0603	2.4 k $\Omega$	0.009	0.016	1	0.01	0.02
Fuse	2.5 A	0.594	0.874	1	0.59	0.87
Resistor 0603	4.7 k $\Omega$	0.004	0.008	3	0.01	0.02
Capacitor 0805	4.7 $\mu$ F	0.183	0.51	2	0.37	1.02

<sup>1</sup>Considering LSTs and MSTs, in North and South observatories, around 50 operating TIBs are expected. Some more TIBs must be produced as spares

Capacitor 0603	4.7 $\mu\text{F}$	0.015	0.026	1	0.02	0.03
Capacitor 0402	4.7 $\mu\text{F}$	0.099	0.198	44	4.36	8.71
Inductor XAL1010	8.3 $\mu\text{H}$	2.55	2.78	1	2.55	2.78
Resistor 0603	10 k $\Omega$	0.006	0.011	60	0.36	0.66
Capacitor 0603	10 nF	0.008	0.014	2	0.02	0.03
Capacitor 0805 10V	10 $\mu\text{F}$	0.011	0.02	64	0.70	1.28
Capacitor 0805 25V	10 $\mu\text{F}$	0.083	0.143	1	0.08	0.14
Capacitor 0805	15 nF	0.008	0.013	1	0.01	0.01
Inductor XAL5050	22 $\mu\text{H}$	0.86	0.95	1	0.86	0.95
Capacitor 0603	39 nF	0.005	0.009	1	0.01	0.01
Capacitor 1812	47 $\mu\text{F}$	0.77	1.71	3	2.31	5.13
Resistor 0603	61.9 k $\Omega$	0.017	0.027	1	0.02	0.03
Resistor 0402	100 $\Omega$	0.006	0.01	2	0.01	0.02
Resistor 0603	100 $\Omega$	0.006	0.01	15	0.09	0.15
Capacitor 0603 25V	100 nF	0.007	0.012	75	0.53	0.90
Capacitor 0805	100 nF	0.011	0.024	1	0.01	0.02
Capacitor 0603 50V	100 nF	0.011	0.014	1	0.01	0.01
Capacitor 0603	100 pF	0.009	0.012	36	0.32	0.42
Capacitor 0402	100 pF	0.005	0.009	4	0.02	0.04
Capacitor 1206	100 $\mu\text{F}$	0.11	0.235	4	0.44	0.94
Capacitor 1210	100 $\mu\text{F}$	0.69	1.29	9	6.21	11.61
Al capacitor	180 $\mu\text{F}$	1.00	1.75	2	2.00	3.50
Al capacitor	220 $\mu\text{F}$	0.165	0.228	1	0.17	0.23
Resistor 0603	249 $\Omega$	0.006	0.011	1	0.01	0.01
Resistor 0603	330 $\Omega$	0.007	0.011	2	0.01	0.02
Ta Capacitor	330 $\mu\text{F}$	1.47	3.83	1	1.47	3.83
Capacitor 0603	470 nF	0.017	0.033	1	0.02	0.03
Capacitor 0402	470 nF	0.017	0.022	65	1.11	1.43
Resistor 0603	500 $\Omega$	0.009	0.016	1	0.01	0.02
Screw M2.5 plane	12 mm	0.0177	0.0213	11	0.19	0.23
Nut M2.5 plane	2 mm	0.0136	0.0163	9	0.12	0.15
Spacer M2.5	5 mm	0.092	0.152	9	0.83	1.37
Washer M2.5		0.023	0.028	9	0.21	0.25
Spacer M2.5	12.7 mm	0.041	0.0803	2	0.08	0.16
Raspberry Pi		39.00	39.00	1	39.00	39.00
SFP transceiver Avago AFBR5715ALZ		40.38	41.91	12	484.56	502.92
SFP connector		4.03	4.24	12	48.36	50.88
Al Rack box 1U	220 mm	30.80	32.75	1	30.80	32.75
Closed cover plate	220 mm	10.16	11.54	1	10.16	11.54
Ventilated cover plate	220 mm	17.20	19.57	1	17.20	19.57
PCB		411.17	411.17	1	411.17	411.17
Component assembly			1			
<b>Total components</b>				<b>570</b>	<b>1548.24</b>	<b>1548.24</b>

Table B.4: Bill of materials of 1 Trigger Interface Board

Concept	Manufacturer	Unit price(€)		Quantity	Total cost(€)	
		min	max		min	max
PCB manufacturing fixed costs	Lab Circuits	1468.00	1468.00	1	1468.00	1468.00
Silk Screen	SETI Electrónica			2		
SMD Pick & Place program	SETI Electrónica			1		
<b>Board batch production fixed cost (€)</b>					<b>1468.00</b>	<b>1468.00</b>

Table B.5: Fixed costs of the Trigger Interface Board

The costs of table B.4 correspond to the first TIB prototype. The costs of the final version which will be installed in the telescopes cameras will be slightly different. For instance, one of the most expensive components are the optical transceivers (c.a. 40 €each), of which there are 12 units in the prototype. In the real case, it is very unlikely to have more than 4 LSTs in each observatory, so there would be only 3 neighbours in the case of LSTs and 0 neighbours in the case of MSTs. Additionally, other optical link is an spare and other is reserved to check the performance of the optical delay of the signals. So in fact, only 5 from the 12 optical transceivers are strictly required for LSTs and 2 for MSTs, which involves saving up to 280 €in the boards installed in LSTs and 400 €in the ones placed in MST cameras. As was explained in section 7.4.2.2, all the TIBs will have the housing for the 12 transceivers mounted, but only the required transceivers will be installed. In the same way, another significant costs are the delay chips, which need to be tested before deciding to use them in the final version.

## Appendix C

# Reliability

In a large project as CTA, it is very important to estimate the reliability of the different systems properly in order to foresee the number of spares required, the human resources which should be dedicated to reparations, and in sum the budget required for maintenance. With this aim, all the subsystems must provide to the system engineers with their reliability estimations. This appendix contains the reliability estimations for the Level 1 (table C.1) and the Trigger Interface Board (table C.2). For this estimations, the Middle Time Between Failures (MTBF) or the Failure In Time (FIT) information provided by the manufacturers of the different active components has been used. However, for the pasive components this information is sometimes difficult to find, and due to the high number of elements and the different manufactures which can produce equivalent components, getting the MTBF or the FIT from the manufacturers would be an endless task. For this reason, the reliability of the passive components have been estimated with the generic prediction models included in the FIDES guide[172], instead of with their specific data. A free software tool implementing these prediction models have been used [173], as shown in figure C.1.

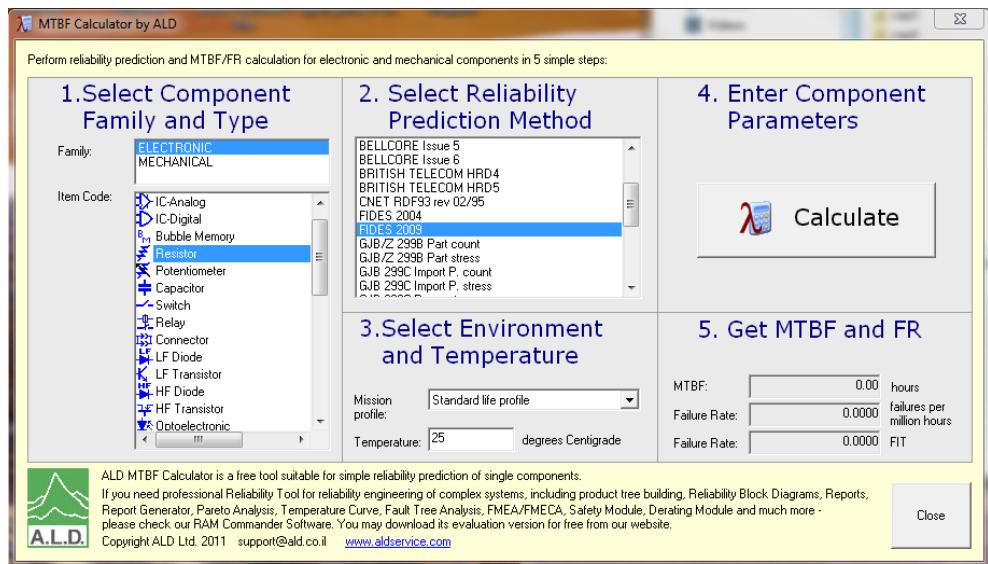


Figure C.1: Free MTBF calculator, from ALD [173]

Component	Value	Unit	MTBF (hours)	Quantity	FIT (in 1 hour)
Capacitor 0603	100 nF		$1.82 \cdot 10^{10}$	33	$1.81 \cdot 10^{-9}$
Capacitor 0805	10 $\mu$ F		$1.82 \cdot 10^{10}$	31	$1.70 \cdot 10^{-9}$
Capacitor 0603	10 $\mu$ F		$1.82 \cdot 10^{10}$	23	$1.26 \cdot 10^{-9}$
Capacitor 0603	100 pF		$1.82 \cdot 10^{10}$	32	$1.76 \cdot 10^{-9}$
Capacitor 0603	1 nF		$1.82 \cdot 10^{10}$	8	$4.39 \cdot 10^{-10}$
Capacitor 0603	4 pF		$1.82 \cdot 10^{10}$	2	$1.10 \cdot 10^{-10}$
Capacitor 0603	2 pF		$1.82 \cdot 10^{10}$	10	$5.49 \cdot 10^{-10}$
Capacitor 0603	5.6 pF		$1.82 \cdot 10^{10}$	2	$1.10 \cdot 10^{-10}$
Capacitor 0603	1 pF		$1.82 \cdot 10^{10}$	2	$1.10 \cdot 10^{-10}$
Capacitor 1206 Ta	68 $\mu$ F		$1.58 \cdot 10^9$	1	$6.33 \cdot 10^{-10}$
Capacitor 0603	10 nF		$1.82 \cdot 10^{10}$	2	$1.10 \cdot 10^{-10}$
Capacitor 0805	33 $\mu$ F		$1.82 \cdot 10^{10}$	1	$5.49 \cdot 10^{-11}$
Capacitor 0603	120 pF		$1.82 \cdot 10^{10}$	2	$1.10 \cdot 10^{-10}$
Capacitor 0603	68 pF		$1.82 \cdot 10^{10}$	1	$5.49 \cdot 10^{-11}$
Capacitor 0603	47 pF		$1.82 \cdot 10^{10}$	1	$5.49 \cdot 10^{-11}$
Capacitor 1206 Ta	100 $\mu$ F		$1.58 \cdot 10^9$	1	$6.33 \cdot 10^{-10}$
Capacitor 1206	1 $\mu$ F		$1.82 \cdot 10^{10}$	1	$5.49 \cdot 10^{-11}$
Inductor 0402	15 nH		$4.34 \cdot 10^9$	4	$9.22 \cdot 10^{-10}$
Inductor 0402	20 nH		$4.34 \cdot 10^9$	6	$1.38 \cdot 10^{-9}$
Resistor 0603	100 $\Omega$		$3.28 \cdot 10^{10}$	10	$3.05 \cdot 10^{-10}$
Resistor 0603	200 $\Omega$		$3.28 \cdot 10^{10}$	18	$5.49 \cdot 10^{-10}$
Resistor 0603	49.9 $\Omega$		$3.28 \cdot 10^{10}$	23	$7.01 \cdot 10^{-10}$
Resistor 0603	62 $\Omega$		$3.28 \cdot 10^{10}$	2	$6.10 \cdot 10^{-11}$
Resistor 0603	261 $\Omega$		$3.28 \cdot 10^{10}$	4	$1.22 \cdot 10^{-10}$
Resistor 0603	56 $\Omega$		$3.28 \cdot 10^{10}$	8	$2.44 \cdot 10^{-10}$
Resistor 0603	60.4 $\Omega$		$3.28 \cdot 10^{10}$	4	$1.22 \cdot 10^{-10}$
Resistor 0603	360 $\Omega$		$3.28 \cdot 10^{10}$	8	$2.44 \cdot 10^{-10}$
Resistor 0603	470 $\Omega$		$3.28 \cdot 10^{10}$	8	$2.44 \cdot 10^{-10}$
Resistor 0603	330 $\Omega$		$3.28 \cdot 10^{10}$	4	$1.22 \cdot 10^{-10}$
Resistor 0603	191 $\Omega$		$3.28 \cdot 10^{10}$	2	$6.10 \cdot 10^{-11}$
Resistor 0603	620 $\Omega$		$3.28 \cdot 10^{10}$	3	$9.15 \cdot 10^{-11}$
Resistor 0603	1 k $\Omega$		$3.28 \cdot 10^{10}$	2	$6.10 \cdot 10^{-11}$
Resistor 0603	0 $\Omega$		$3.28 \cdot 10^{10}$	1	$3.05 \cdot 10^{-11}$
Resistor 0603	100 k $\Omega$		$3.28 \cdot 10^{10}$	1	$3.05 \cdot 10^{-11}$
Resistor 0603	10 k $\Omega$		$3.28 \cdot 10^{10}$	4	$1.22 \cdot 10^{-10}$
Resistor 0603	1.8 k $\Omega$		$3.28 \cdot 10^{10}$	4	$1.22 \cdot 10^{-10}$
Resistor 0603	1 M $\Omega$		$3.28 \cdot 10^{10}$	4	$1.22 \cdot 10^{-10}$
Resistor 0603	390 k $\Omega$		$3.28 \cdot 10^{10}$	1	$3.05 \cdot 10^{-11}$
Resistor 0603	1.5 k $\Omega$		$3.28 \cdot 10^{10}$	1	$3.05 \cdot 10^{-11}$
Resistor 0603	3.3 k $\Omega$		$3.28 \cdot 10^{10}$	12	$3.66 \cdot 10^{-10}$
Diode HSMS2855			$1.50 \cdot 10^{11}$	9	$6.00 \cdot 10^{11}$
74HC00 logic gate			$1.51 \cdot 10^8$	1	$6.62 \cdot 10^{-9}$
ADG901 RF switch			$8.88 \cdot 10^8$	8	$9.01 \cdot 10^{-9}$

AP2141 power switch		$1.00 \cdot 10^9$	1	$1.00 \cdot 10^{-9}$
SN74LVC1G32 logic		$9.66 \cdot 10^8$	1	$1.04 \cdot 10^{-9}$
AD5663R DAC		$3.67 \cdot 10^9$	1	$2.73 \cdot 10^{-10}$
AD8003 Op.Amp.		$5.73 \cdot 10^9$	3	$5.23 \cdot 10^{-10}$
ADCMP604 comparator		$5.73 \cdot 10^9$	9	$1.57 \cdot 10^{-9}$
ADG936 RF switch		$8.88 \cdot 10^8$	1	$1.13 \cdot 10^{-9}$
OPA2830 Op.Amp.		$9.84 \cdot 10^7$	1	$1.02 \cdot 10^{-8}$
ADCMP600 comparator		$5.73 \cdot 10^9$	1	$1.74 \cdot 10^{-10}$
ADG801 switch		$3.67 \cdot 10^9$	1	$2.73 \cdot 10^{-10}$
AD7478A ADC		$3.67 \cdot 10^9$	1	$2.73 \cdot 10^{-10}$
<b>System FIT</b>				$4.77 \cdot 10^{-8}$
<b>System MTBF (hours)</b>				$2.09 \cdot 10^7$
<b>System MTBF (years)</b>				<b>2391</b>

Table C.1: Reliability estimation for the Level 1, only components

According with table C.1, An average of only 1 failure in each 2391 years is expected. This number is very high, because it corresponds to a relatively small subsystem. Considering that there will be 265 Level 1 modules in each camera, every camera will suffer one Level 1 failure in 9 years as an average. Additionally, it is important to notice that the estimation of table C.1 corresponds only to the components, considering that the Level 1 is integrated in the front-end board. If the Level 1 is installed as a mezzanine, the failure rate of the connectors must be taken into account. According to FIDES model, for a 52 contacts SMD connector, a MTBF of  $1.13 \cdot 10^8$  is expected. Once included in the estimation, an MTBF of  $1.53 \cdot 10^7$  hours (1745 years) is obtained for the Level 1 mezzanine.

Component	Value	Unit MTBF (hours)	Quantity	FIT (in 1 hour)
LP38690DT-2.5		$1.81 \cdot 10^9$	1	$5.51 \cdot 10^{-10}$
LM22672MR-5.0		$4.62 \cdot 10^8$	1	$2.17 \cdot 10^{-9}$
CDCV304PWRG4		$3.41 \cdot 10^8$	1	$2.93 \cdot 10^{-9}$
DS1123L-200		$7.13 \cdot 10^8$	9	$1.26 \cdot 10^{-8}$
SFP box x4		$9.14 \cdot 10^7$	3	$3.28 \cdot 10^{-8}$
LP38691DT-1.8		$1.81 \cdot 10^9$	1	$5.51 \cdot 10^{-10}$
CSD18534Q5A		$3.45 \cdot 10^8$	2	$5.80 \cdot 10^{-9}$
Artix-7 FPGA		$1.43 \cdot 10^8$	1	$7.00 \cdot 10^{-9}$
B240A-13-F		$4.34 \cdot 10^8$	1	$2.30 \cdot 10^{-9}$
JTAG connector		$3.64 \cdot 10^8$	1	$2.75 \cdot 10^{-9}$
Jumper 2 vias		$9.64 \cdot 10^8$	1	$1.04 \cdot 10^{-9}$
SN65LVDS101		$2.88 \cdot 10^8$	12	$4.17 \cdot 10^{-8}$
LP3878SD-ADJ		$1.99 \cdot 10^8$	1	$5.02 \cdot 10^{-9}$
SN65LVDS100		$2.88 \cdot 10^8$	12	$4.17 \cdot 10^{-8}$
Raspberry Pi connector		$2.67 \cdot 10^8$	1	$3.74 \cdot 10^{-9}$
RJ45 connector		$1.70 \cdot 10^8$	1	$5.87 \cdot 10^{-9}$
Power connector		$9.64 \cdot 10^8$	1	$1.04 \cdot 10^{-9}$

LM3151MHE-3.3		$4.62 \cdot 10^8$	1	$2.17 \cdot 10^{-9}$
TC77		$2.99 \cdot 10^8$	1	$3.34 \cdot 10^{-9}$
Green LED SMD		$5.39 \cdot 10^8$	5	$9.28 \cdot 10^{-9}$
Fuse	0.5 A	$2.04 \cdot 10^8$	1	$4.90 \cdot 10^{-9}$
Capacitor 0603 10V	1 $\mu\text{F}$	$1.82 \cdot 10^{10}$	4	$2.20 \cdot 10^{-10}$
Capacitor 0603 50V	1 $\mu\text{F}$	$1.82 \cdot 10^9$	1	$5.49 \cdot 10^{-11}$
Inductor 0805	1 $\mu\text{H}$	$4.34 \cdot 10^9$	24	$5.53 \cdot 10^{-9}$
Inductor 0603	1 $\mu\text{H}$	$4.34 \cdot 10^9$	4	$9.22 \cdot 10^{-10}$
Fuse	1.5 A	$2.06 \cdot 10^8$	2	$9.69 \cdot 10^{-9}$
Capacitor 0805	2.2 $\mu\text{F}$	$1.82 \cdot 10^{10}$	1	$5.49 \cdot 10^{-11}$
Resistor 0603	2.4 k $\Omega$	$3.28 \cdot 10^{10}$	1	$3.05 \cdot 10^{-11}$
Fuse	2.5 A	$2.05 \cdot 10^8$	1	$4.88 \cdot 10^{-9}$
Resistor 0603	4.7 k $\Omega$	$3.28 \cdot 10^{10}$	3	$9.15 \cdot 10^{-11}$
Capacitor 0805	4.7 $\mu\text{F}$	$1.82 \cdot 10^{10}$	2	$1.10 \cdot 10^{-10}$
Capacitor 0603	4.7 $\mu\text{F}$	$1.82 \cdot 10^{10}$	1	$5.49 \cdot 10^{-11}$
Capacitor 0402	4.7 $\mu\text{F}$	$1.82 \cdot 10^{10}$	44	$2.42 \cdot 10^{-9}$
Inductor XAL1010	8.3 $\mu\text{H}$	$2.63 \cdot 10^7$	1	$3.80 \cdot 10^{-8}$
Resistor 0603	10 k $\Omega$	$3.28 \cdot 10^{10}$	60	$1.83 \cdot 10^{-9}$
Capacitor 0603	10 nF	$1.82 \cdot 10^{10}$	2	$1.10 \cdot 10^{-10}$
Capacitor 0805 10V	10 $\mu\text{F}$	$1.82 \cdot 10^{10}$	64	$3.51 \cdot 10^{-9}$
Capacitor 0805 25V	10 $\mu\text{F}$	$1.82 \cdot 10^{10}$	1	$5.49 \cdot 10^{-11}$
Capacitor 0805	15 nF	$1.82 \cdot 10^{10}$	1	$5.49 \cdot 10^{-11}$
Inductor XAL5050	22 $\mu\text{H}$	$2.63 \cdot 10^7$	1	$3.80 \cdot 10^{-8}$
Capacitor 0603	39 nF	$1.82 \cdot 10^{10}$	1	$5.49 \cdot 10^{-11}$
Capacitor 1812	47 $\mu\text{F}$	$1.82 \cdot 10^{10}$	3	$1.65 \cdot 10^{-10}$
Resistor 0603	61.9 k $\Omega$	$3.28 \cdot 10^{10}$	1	$3.05 \cdot 10^{-11}$
Resistor 0402	100 $\Omega$	$3.28 \cdot 10^{10}$	2	$6.10 \cdot 10^{-11}$
Resistor 0603	100 $\Omega$	$3.28 \cdot 10^{10}$	15	$4.57 \cdot 10^{-10}$
Capacitor 0603 25V	100 nF	$1.82 \cdot 10^{10}$	75	$4.12 \cdot 10^{-9}$
Capacitor 0805	100 nF	$1.82 \cdot 10^{10}$	1	$5.49 \cdot 10^{-11}$
Capacitor 0603 50V	100 nF	$1.82 \cdot 10^{10}$	1	$5.49 \cdot 10^{-11}$
Capacitor 0603	100 pF	$1.82 \cdot 10^{10}$	36	$1.98 \cdot 10^{-9}$
Capacitor 0402	100 pF	$1.82 \cdot 10^{10}$	4	$2.20 \cdot 10^{-10}$
Capacitor 1206	100 $\mu\text{F}$	$1.82 \cdot 10^{10}$	4	$2.20 \cdot 10^{-10}$
Capacitor 1210	100 $\mu\text{F}$	$1.82 \cdot 10^{10}$	9	$4.94 \cdot 10^{-10}$
Al capacitor	180 $\mu\text{F}$	$1.82 \cdot 10^9$	2	$1.10 \cdot 10^{-9}$
Al capacitor	220 $\mu\text{F}$	$1.82 \cdot 10^9$	1	$5.48 \cdot 10^{-10}$
Resistor 0603	249 $\Omega$	$3.28 \cdot 10^{10}$	1	$3.05 \cdot 10^{-11}$
Resistor 0603	330 $\Omega$	$3.28 \cdot 10^{10}$	2	$6.10 \cdot 10^{-11}$
Ta Capacitor	330 $\mu\text{F}$	$1.58 \cdot 10^9$	1	$6.34 \cdot 10^{-10}$
Capacitor 0603	470 nF	$1.82 \cdot 10^{10}$	1	$5.49 \cdot 10^{-11}$
Capacitor 0402	470 nF	$1.82 \cdot 10^{10}$	65	$3.57 \cdot 10^{-9}$
Resistor 0603	500 $\Omega$	$3.28 \cdot 10^{10}$	1	$3.05 \cdot 10^{-11}$
Raspberry Pi		$2.00 \cdot 10^6$	1	$5.00 \cdot 10^{-7}$

SFP transceiver Avago AFBR5715ALZ		$3.49 \cdot 10^7$	12	$3.44 \cdot 10^7$
<b>System FIT</b>				$1.15 \cdot 10^{-6}$
<b>System MTBF (hours)</b>				$8.68 \cdot 10^5$
<b>System MTBF (years)</b>				<b>99</b>

Table C.2: Reliability estimation for the Trigger Interface Board

In the case of the Trigger Interface Board, a MTBF of  $8.65 \cdot 10^5$  hours (99 years) is obtained. This is much smaller than the MTBF of the Level 1 because the system has more components and because there are two components specially critical: the SFP transceivers and the Raspberry Pi.

It is difficult to find reliability information about the Raspberry Pi, but it is known that its reliability is limited by the MTBF of the SD card used as hard disk drive (to store the operating system, the slow control software, etc.). The best SD cards have an MTBF of around 2 million hours. Nevertheless, this estimation considers that the SD card is read and write quite often, as in the case of using it in a photograph camera, reaching the maximum number of times that the card can be written. In the case of the Raspberry Pi used in the TIB, the SD card contains the software running in the computer, but it is not used to store data, so it will be written only for software updating. Therefore, a longer lifetime for the SD card could be possible.

Regarding the SFP transceivers, there is not much to do to enlarge their lifetime, apart from avoiding to work at high temperatures. Anyway, as there is only one Trigger Interface Board per camera, 99 years of MTBF is acceptable.



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[173] Advanced Logistics Development

*ALD MTBF Calculator*

<http://www.aldservice.com/en/reliability-software/free-mtbf-calculator.html>





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