Characterization of analogue ASIC for L1 trigger decision.

Abstract

A test for the quality control of the L1 trigger system ASIC has been performed to characterize its behaviour and features. Different parts of the ASIC were tested and the information obtained has been analyzed in order to obtain data about the gain, offset and noise. A total of 389 ASICs are included in this analysis.

In addition to the characterization, an alternative method to calculate the offset in an indirect way has been developed, as a result of a voltage rate scan.

1. Introduction

Analysis of the features of the ASIC for the L1 trigger system is necessary for calibration, interpretation of the data retrieved by the camera and to identify not working ASICs.

To guarantee that every ASIC delivered fulfills its specifications is mandatory. For that reason, an automatic quality test has been designed, which is able to measure features such as gain, offset and noise coming from different parts of the ASIC.

The structure of this document is the following:
In section 2, the quality control test procedure is described.
In section 3, those features are presented for the 389 ASICs.
In section 4, an alternative way to calculate the offset of the ASIC, using a lineal fit of an input voltage rate scan, is discussed and applied.
In section 5, analysis and results from the previous sections are commented.

2. Quality Control Test

The quality control test consisted in different checks that evaluate the behaviour of the ASICs in its different parts.

The Voltage test measures the gain of all seven input single channels and the two outputs for 10 different voltages (from 100mV to 1000mV) using a rate scan methodology, consisting on the comparison of the input trigger rate from a generator on the evaluation setup and the ASIC trigger output rate.

The Analog offset test consists in the measurement of the offset in the Analog Adder Output test, which is the output of a multiplexor that selects among the available analog output adder, plus a buffer for the output pins. The measurement is directly from the differential output pin of the ASIC by a Multimeter.

The Digital offset test procedure was the measurement of the offset in the LVDS digital outputs, 0 and 1, by the evaluation of the output status as a funtion of the threshold. The methodology consist on increasing the threshold from 0 Volts using the DAC's values until find the minimum value that the output crosses from 1 to 0, and the maximum cross from 0 to 1. The voltage between this two points is the noise of the digital output, and the mean point is the offset. Setting the Threshold to 0 it is possible 3 different behaviors:
If the status of the digital output is a logic "1" (tagged as type "Pos") it is possible to measure the

minimum and the maximum points and therefore it is possible to calculate the Offset and the noise.
If the status of the digital ouput is a logic '0' (tagged as type "Neg"), it is not possible to measure neither the minimum nor the maximum point, and then a value of zero is assigned by the program both to the noise and the offset.
Finlly, if the status of the digital ouput is switching (tagged as type "Com"), it is only possible to measure the maximum value, and the other is assigned to 0. In this case the noise is understimated and the threshold is overstimated.

3 Characterization

3.1 Gain.

From the test voltage, it was possible to measure the gain for the seven input channels, the three adders and two output discriminators. *Figure 1* shows the distribution of the gains for the 389 ASICs

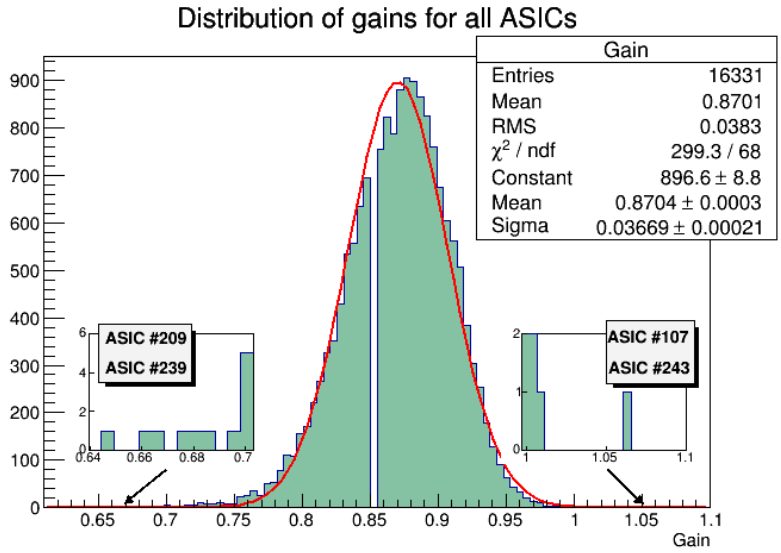

Figure 1: *Gain distribution for all ASICs. The red line represents a gaussian fit with mean 0,8704 and sigma 0,3669. The zoom-ins show several outliers with gains very deviated from the average.*

The distribution of gains has a mean value of 0,8701 and RMS 0,0383. In the extremes of the distribution some outliers are spotted with gains that are far away from the mean. This points correspond to some channels in ASICs 209, 239, 107 and 243. As a criteria to discard this outliers, the gaussian fit has been used to calculate the probability that an ASIC could have those gain values. For a gain lower than 0,7 the probability is less than 0,025%, so those ASICs won't be used and won't be considered in the next parts of the characterization. For a gain over 1,01 the probability is less than 0,8%, but for a gain over 1,05 the probability falls to 0,007%, so ASIC.

Without the outliers, the distribution is showed in *figure 2*, where the mean gain is 0,8702 and RMS 0,03795. We can conclude with this first analysis that the typical ASIC should have a gain of 0,870 +- 0,038 averaged to all its channels, adders and discriminators.

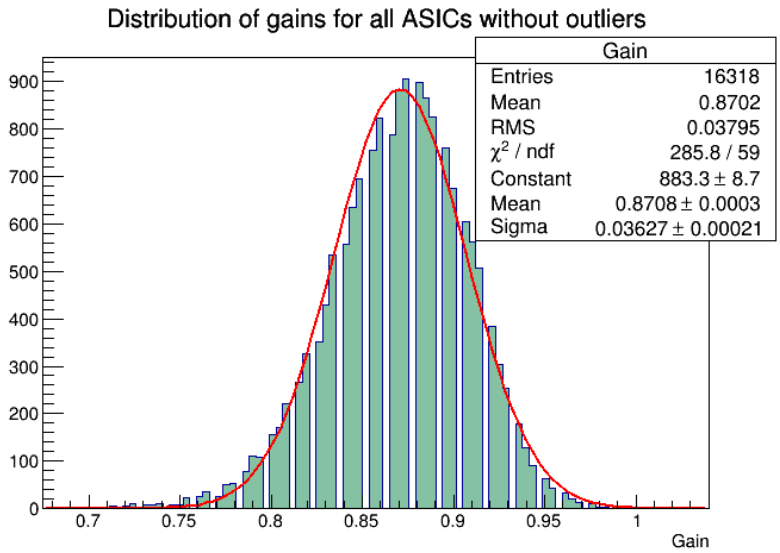

Figure 2: *Gain distribution for all ASICs where outliers have been discarded.*

The previous analysis permitted to characterize the typical gain that should be expected to measure in any part of the typical ASIC. Following, a characterization per channel is made, to analyze the behaviour of the seven channels of each ASIC separately.

In *figure 3* are showed the mean values of the gains for each channel, averaged to all the ASICs.

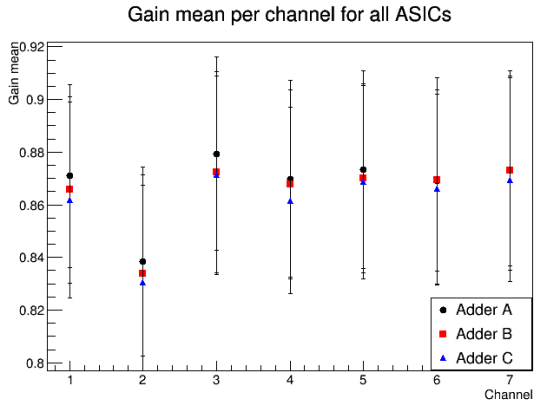

Figure 3: *Gain mean of all ASICs per channel, for the three adders.Vertical bars represent the RMS.*

It can be observed that the second channel has a lower gain than the others. Also, the third channel seems to have a slightly higher gain. (This effects come from the setup configuration during the test. The third channel is directly connected to the pulse generator while the others receive a replic of the original signal. The second channel had to be fed with a cable of different lenght, causing a lower gain to be measured.)

In *table 1* the mean values of the gain in the seven channels, averaged to all the ASICs, are showed, being the values expected from the typical ASIC.

Channel	Gain Mean	RMS
1	0,871	0,035
2	0,839	0,036
3	0,880	0,037
4	0,873	0,036
5	0,876	0,036
6	0,873	0,036
7	0,878	0,036

***Table 1**: Mean values of the gain for the seven channels.*

Finally, to fully characterize the gain of the typical ASIC in detail, in *table 3 (page 17)* are presented the values for the gain measured in every single channel-adder-discriminator combination, averaged to all the ASICs studied.

The next step is to study how the measurements of the gain behaves depending on the part of the ASIC that is being tested, and from one ASIC to another. The aim is to stablish if there is any part of the ASIC that dominates the fluctuations of the gain..
The analysis consisted in trying to find a correlation between channels, the adders or the discriminators.

First of all, the channel-channel correlation was studied. In this case gains from pairs of channels are plotted keeping the adder and the discriminator fixed. *Figure 4* shows the correlation plot for one of the combinations studied, being the rest of them similar to this one.

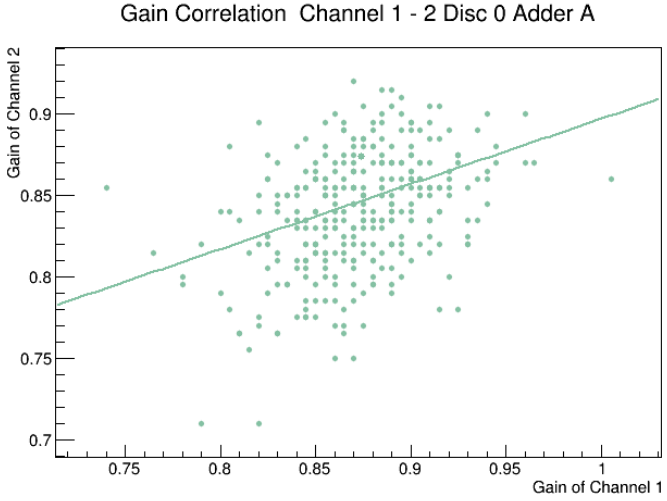

***Figure 4:** Correlation of the gain between channels for fixed adder and discriminator. All possible combinations of channel pairs have been considered.*

A quantization in the gain is observed due to the rate scan methodology, since the gain is obtained as the slope of the linear fit that comes from two quantized quantities: the input voltage and the threshold probed. In the plot, it can be observed a slight correlation between channels. Doing a linear fit, the averaged correlation factor for all pairs of channels is ~0,48 (see *table 2, page 12*).

The same study was done for the three adders, comparing the gain from different adders keeping the channel and discriminator fixed. In figure 5 one of the possible combinations is showed.

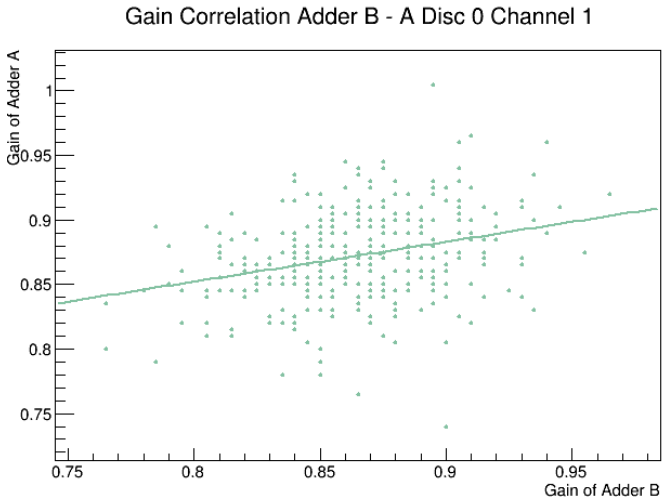

Figure 5: *Correlation of the gain between adders for fixed channel and discriminator. All possible combinations of adder pairs were plotted.*

In this case the correlation is smaller but still exists, with a correlation factor of ~ 0,42.
Finally, the correlation between the two discriminators was also studied, giving results as the plot in figure 6.

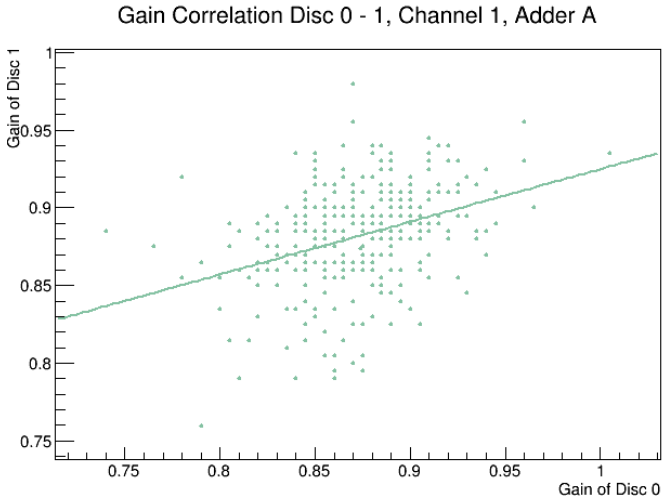

Figure 6: *Correlation of the gain between discriminators for fixed channel and adder.*

Discriminators show the smaller correlation, with a factor of ~0,39.

This correlation study does not point towards an element dominating the gain variance from ASIC to ASIC. On the contrary, main functional blocks of the ASICS seem to contribute to the total gain in a similar way.

3.2 Offset.

The offset of the ASICs was measured in the quality control test by two different techniques. First of all, an analog offset was measured directly at the output of the adders using a multimeter. In this case, discriminators are not taken into account for the analysis. In *figure 7* the distribution of analog offset is showed. Due to a problem in the configuration for the test, it was not possible to measure the analog offset for ASICs from #100 to #130 so they have been excluded from the distribution.
For the analog offset, the mean value of all distributions is -6,138 mV with RMS of 13,01 mV.

Secondly a digital offset was measured at the discriminators, using the rate scan methodology described in section 1. Note that due to the methodology, the offset cannot be measured for all the adders in certain ASICs, only for the ones with an output status tagged as “Pos”. The rest of them are assigned a value of “0”, therefore they have been excluded from the distribution of *figure 8*.

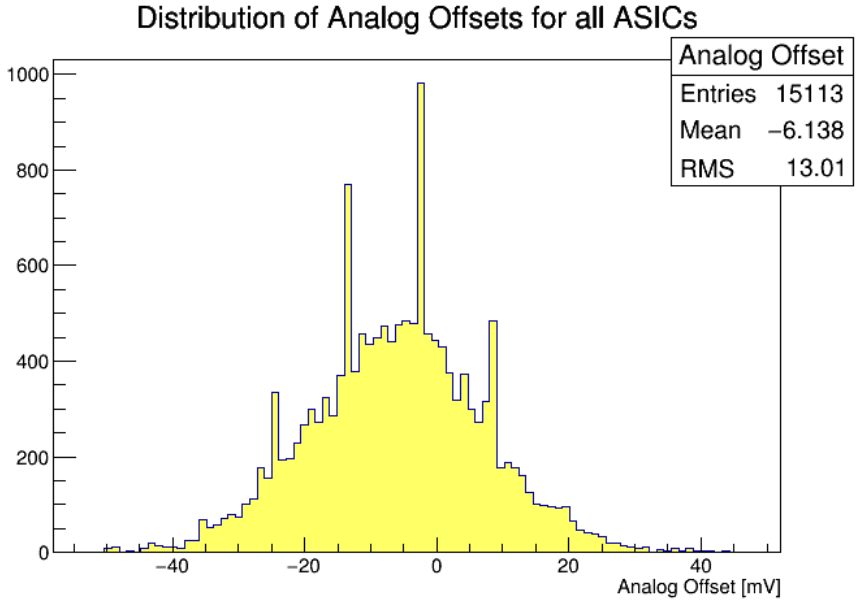

Figure 7: *Analog offset distribution for all ASICs. There are four peaks in the distribution that outline the general profile. This peaks correspond to four offset values (-2, 9, -13 and -24) that are repeated through several ASICs and several channel-adder-discriminator combinations, without any apparent relation.*

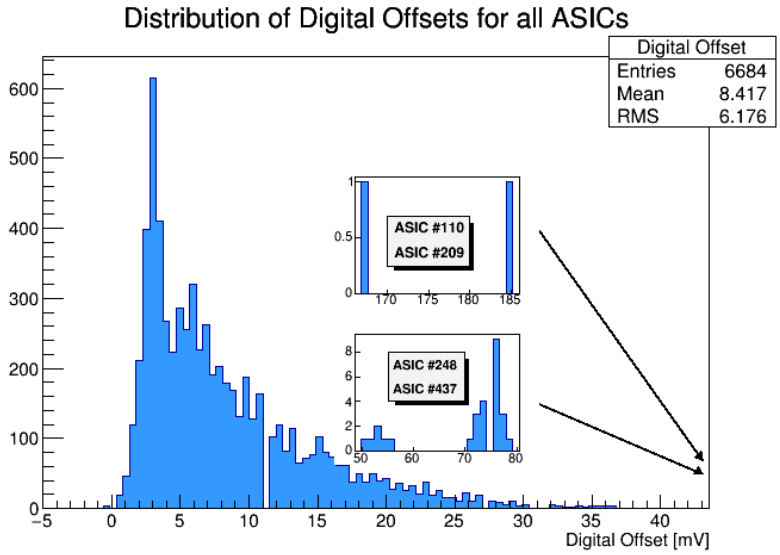

Figure 8: *Digital offset distribution for all ASICs. The zoom-ins show some outliers very far from the mean.*

For the digital offset the mean value is 8,417 mV with RMS of 6,17. Several outliers has been detected, with digital offset very deviated from the mean, in ASICs #110,209,248 and 437. Comparing the digital offset value with the analog offset for this ASICs, there is no correspondence at all, in fact, most of the analog offsets for this outliers have negative values. Because of this, the outliers have been substracted from the characterization.

In *figure 9* there is shown the correlation between the two measured offsets. The linear fit gives a line with a slope of 1,06 and origin ordinate of -4,116, with a pearson correlation factor of 0,74. This result means that there is a correspondence between the two measures and both ways of measuring the offset gives a similar value.

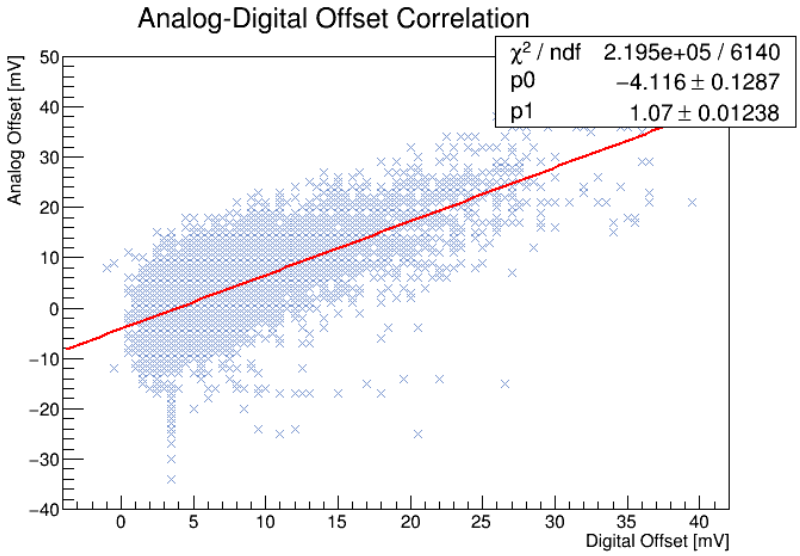

Figure 9: *Correlation between values of the analog offset and the digital offset measured in the quality control test.*

The mean values for the offset obtained in the previous result, give the measures that should be expected from a typical ASIC, averaged to all its inner parts.

To study the offset in more detail, it can be splitted for the seven channels, to see what is the general behaviour in each of them. In *figures 10* and *11* are showed the offsets mean values per channel and adder, averaged to all ASICs.

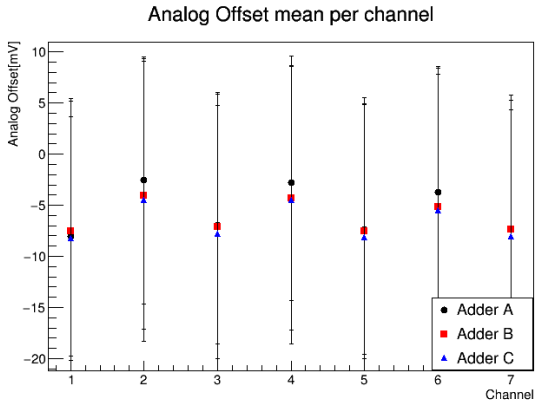

Figure 10: *Analog Offset mean per channel for the three adders.Vertical bars represent the RMS.*

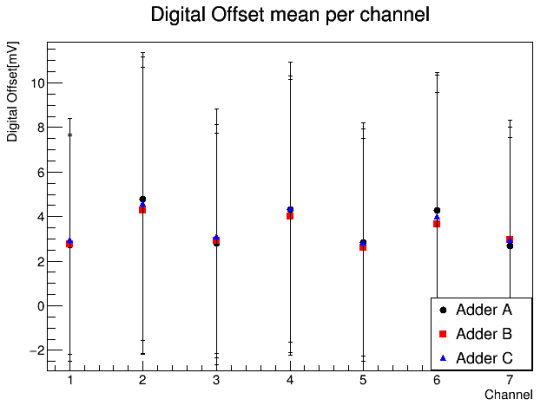

Figure 11: *Digital Offset mean per channel for the three adders. Vertical bars represent the RMS.*

It can be seen that for all the channels the offset has a similar mean value without any outliers.

For a more detailed characterization, in *table 3*, the offsets for each channel, adder and discriminator combination are listed. This values, which has been averaged to all the ASICs, are the expected from the typical ASIC.

Next step, is to study the correlation of the offset in the channels, adders and discriminators separately, to learn how the different parts of the ASIC behave respect to the offset.

First of all, the offsets correlation between channels was studied, fixing the adder and the discriminator. In *figure 12* the correlation plots for a certain combination are presented for both the analog offset and the digital offset.

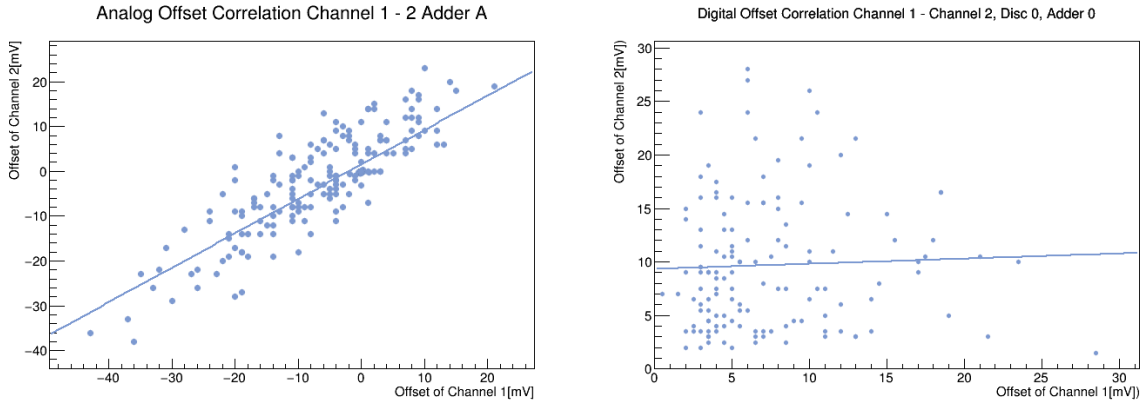

Figure 12: *Correlation plots for analog offset (left) and digital offset (right) between channels for fixed adder and discriminator in the case of digital offset. All possible combinations of channel pairs were plotted.*

A clear correlation for the analog offset is observed between channels, being the averaged correlation factor of 0,83 (see *table 2*). This means that the cause for the fluctuation of the offset in two independent channels for a give ASIC with respect the mean is common.

The same study was made for the adders, and the plot for a certain combination is presented in *figure 13.*

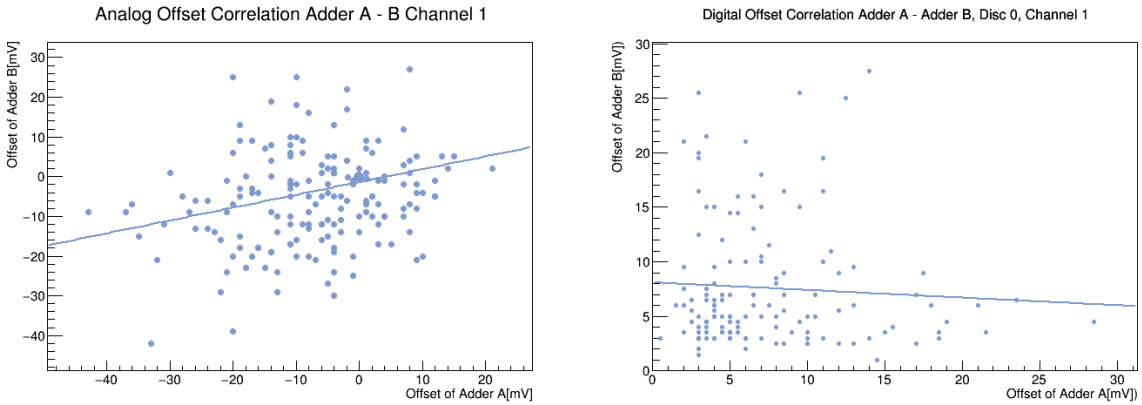

Figure 13: *Correlation plots for analog offset (left) and digital offset (right) between adders for fixed channel and discriminator in the case of digital offset. All possible combinations of adder pairs were plotted.*

In this case, the correlation for the analog offset is much smaller, being the averaged correlation factor of ~0,4. The meaning of this result is that the offset measured in the adders is independent from each other so it should not be influeced by any other part of the ASIC. The conclusion is that the adders are the part that introduces the main contribution to the offset measured in the ASIC.

In the digital offset no correlation is observed at all, but it must be due to the bias introduced by measuring only positive values. It is not possible to substract any conclusion from the correlation of the digital offset in this case.

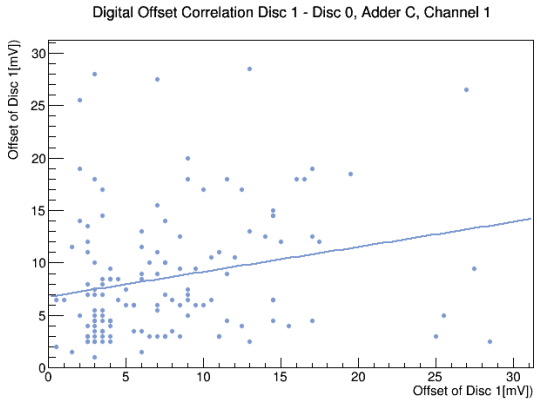

Figure 14: *Correlation plot for digital offset between discriminators for fixed adder and channel.*

3.3 Noise

The noise introduced in the ASIC signals has been measured thanks to the digital offset test of the quality control. Similar to the digital offset, only the adders which the output status was tagged as “Pos” has measured values of noise. The rest of them were assigned a value of “0” and are excluded from the analysis.
The distribution of all the noise values measured is presented in *figure 15*.

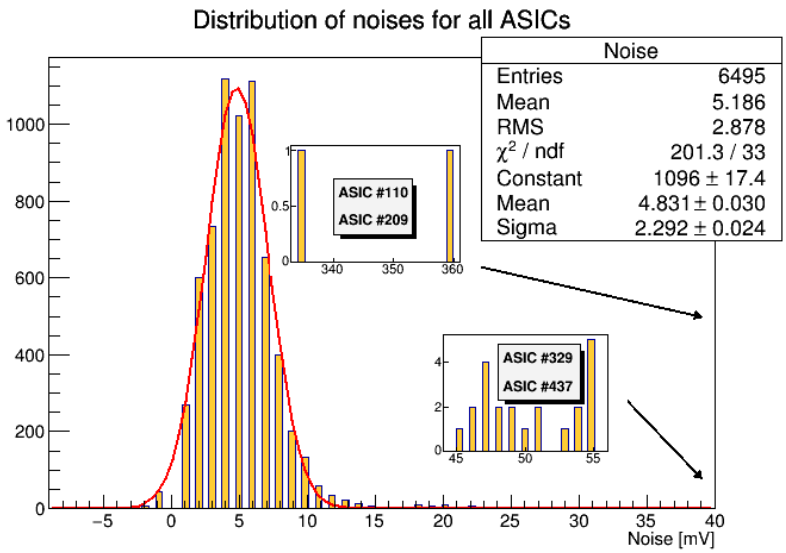

Figure 15: *Noises distribution for all ASICs. Zoom-ins represent outliers with noises measures very deviated from the average.*

The mean value of all the noises in all ASICs is 5,186 mV, with RMS of 2,878 mV. This can be considered the noise for the typical ASIC. Several outliers have been detected, three of them which also had very deviated values of digital offset. It is possible to fit a gaussian to the distribution and therefore calculating the probability of having such outliers. The probability of having outliers with noises over 40 mV is ~ 0%, while the probability of having noises over 10 mV is less than 1%. This ASICs are excluded from the mean calculation.

In figure 16, it is showed the mean noises measured for all the ASICs separated by the seven channels and three adders.

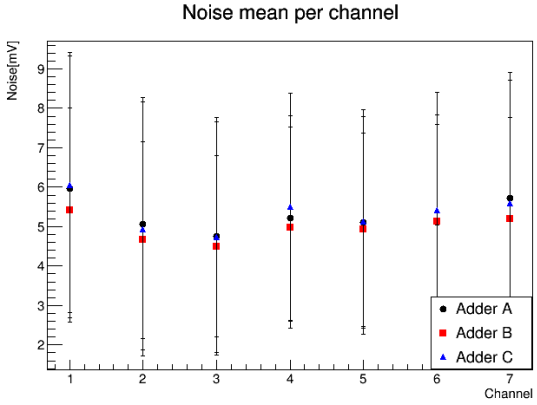

Figure 15: *Noise mean per channel for the three adders. Vertical bars represent the RMS.*

For a detailed characterization of the noise expected for the different parts of the typical ASIC see *table 3*. Those values has been averaged to all the ASIC studied.

The noise in the different parts of the ASIC has also been studied through correlation. In *figure 16*, the plot shows the correlation between noises from pairs of channels for fixed discriminator and adder. There is not a noticeable correlation, being the correlation coefficient of 0,02 (see *table 2*).

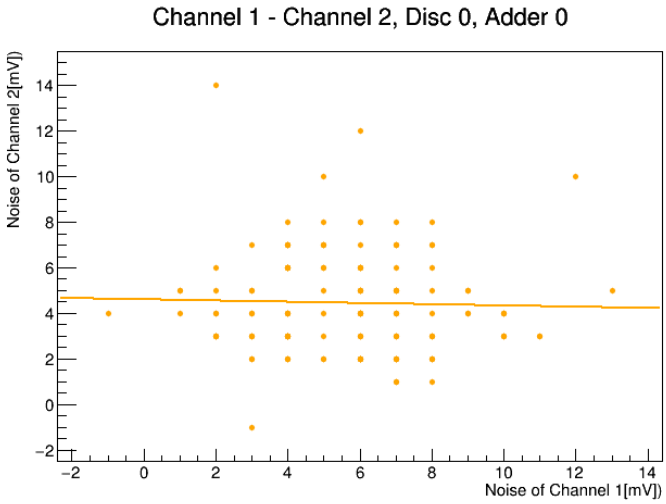

Figure 16: *Correlation plot for noise, between channels for fixed adder and discriminator. All possible combinations of channel pairs were plotted.*

Regarding the correlation between adders, *figure 17* shows no correlation at all, being the pearson correlation factor ~0.

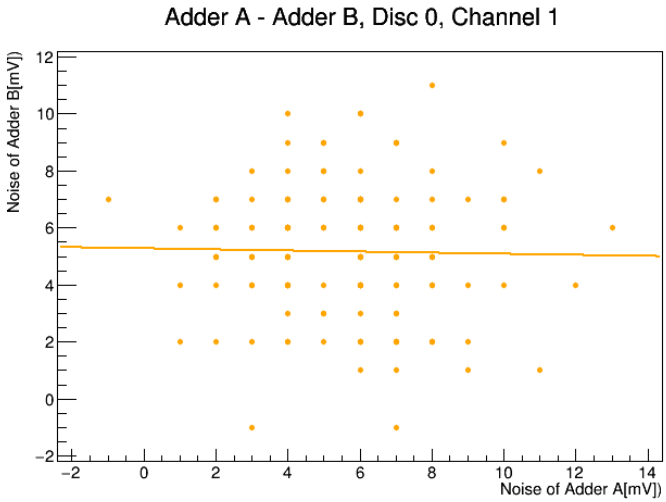

Figure 17: *Correlation plot for noise, between adders for fixed channel and discriminator. All possible combinations of adder pairs were plotted.*

For discriminator, similar result is found in figure 18, with an averaged correlation factor of 0,04.

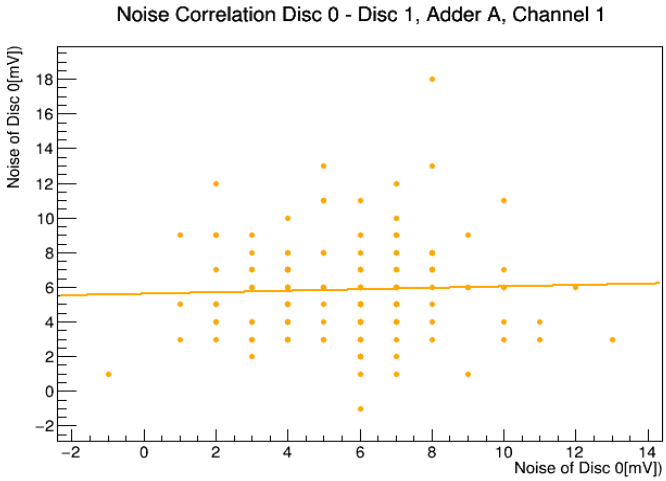

Figure 18: *Correlation plot for noise, between discriminators, for fixed adder and channel.*

From this results we can say that a similar noise is introduced in every part of the ASIC, having the typical mean values presented in *table 3*.

	Corr. Factor Mean	Corr. Factor RMS	Chi2 Mean	Chi2 RMS	NDF
Analog Offset Ch-Ch	0.83787	0.0797831	9510.95	5298.51	387
Analog Offset Add-Add	0.402399	0.090969	26058.7	3447.51	387
Digital Off Ch-Ch	0.0402217	0.0977128	5662.46	1132.02	151.762
Digital Off Add-Add	0.0159922	0.090079	5694.98	1630.13	153.571
Digital Off Disc-Disc	0.152429	0.160245	5432.6	1560.36	151.762
Noise Ch-Ch	0.0210633	0.0885024	925.045	249.055	151.762
Noise Add-Add	-0.00218032	0.102373	845.033	205.65	153.571
Noise Disc-Disc	0.0471226	0.118144	917.351	209.484	151.762
Gain Ch-Ch	0.479205	0.0835731	0.311512	0.0702183	387
Gain Add-Add	0.422922	0.0919769	0.332614	0.071122	387
Gain Disc-Disc	0.39167	0.0369931	0.342987	0.0540679	387
Fit Offset Ch-Ch	0.668336	0.192364	159124	556521	387
Fit Offset Add-Add	0.114982	0.0962141	189410	537969	387
Fit Offset Disc-Disc	0.760724	0.222289	144667	541227	387
Offsets diff. Ch-Ch	0.510537	0.147869	152528	594981	387
Offsets diff. Add-Add	0.410999	0.0861314	147804	557192	387
Offsets diff. Disc-Disc	0.568198	0.0779438	135010	520831	387

Table 2: *Mean value of the pearson correlation factor and Chi square for all the correlation plots done regarding the different features of the ASICs.*

4. Offset calculation from fitting the rate scan result.

As described in section 2, in the quality control test a rate scan of ten input pulses was performed in order to measure the gain of the ASICs. Plotting the input voltage versus the rate scan result voltage it can be observed that the relation is quite lineal, specially for low voltages under 500 mV (see *figure 19*).

We are going to assume a model where the input voltage is linearly related to the rate scan voltage through the expression:

$$(1)\quad V_{rs} = V_{in} * Gain + Offset.$$

Where V_{rs} represents the voltage for the rate scan response, and V_{in} represent the input voltage. Therefore, if we control the input signal and measure the rate scan voltage, we will be able to obtain the offset without having to measure it directly in the ASIC.

In order to find a good fitting to calculate the offset, it is needed to find a range of input voltages where linearity is optimal.

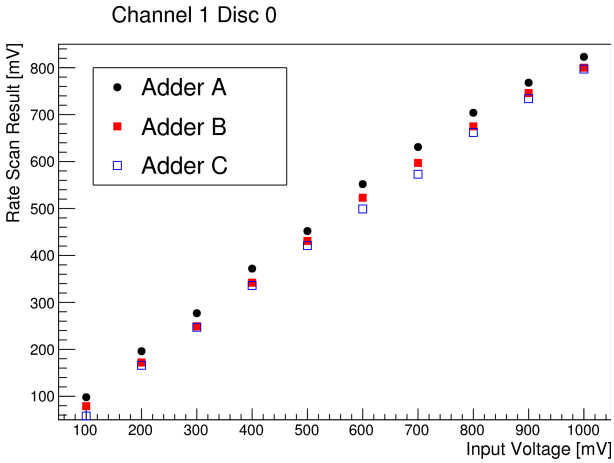

Figure 19: *Rate scan result from one of the voltage tests for ASIC #61. It can be observed a linear tendency which deteriorates at high voltages. Similar plots where obtained from the rest of channel-adder-discriminator combinatios.*

To do so, using data from one of the ASICs (#61), the offset obtained from the fit has been compared with the analog offset measured during the authomatic test.

We assume that the range with the best linearity would be the one where the difference between the offset from the fit and the analog offset measured directly in the test, is minimun.

In *figure 20* plots of the offsets for different ranges are presented where it can be observed the difference between fit and analog offset.

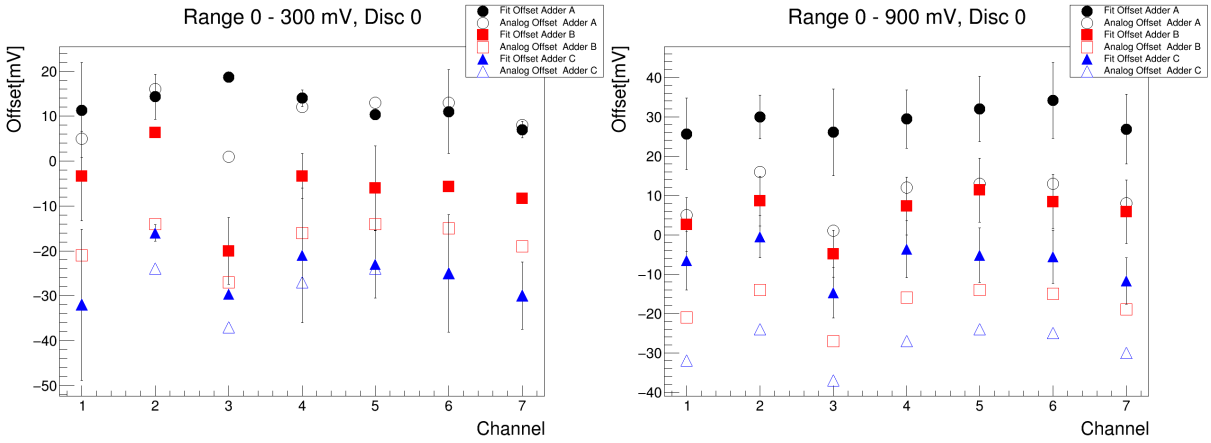

Figure 20: *Offset calculated from the fit(empty icons) and offset measured directly in the test for ASIC #61(filled icons). The difference in mV between them increases for ranges that include higher voltages, so we assume that the best linearity is reached at the minimun possible range, which is 0-300 mV.*

Ten different ranges were tested measuring the offsets differences, including intermediate ranges not starting from 0mV. Finally the range from 0 to 300 mV was selected as the one with better linearity and therefore the minimun difference.

Once selected the range, using the result of the fit, the offset (FO) for all the ASICs was computed, and also the difference of such offset with the analog offset(AO) was calculated and presented in distribution histograms (*figure 21*).

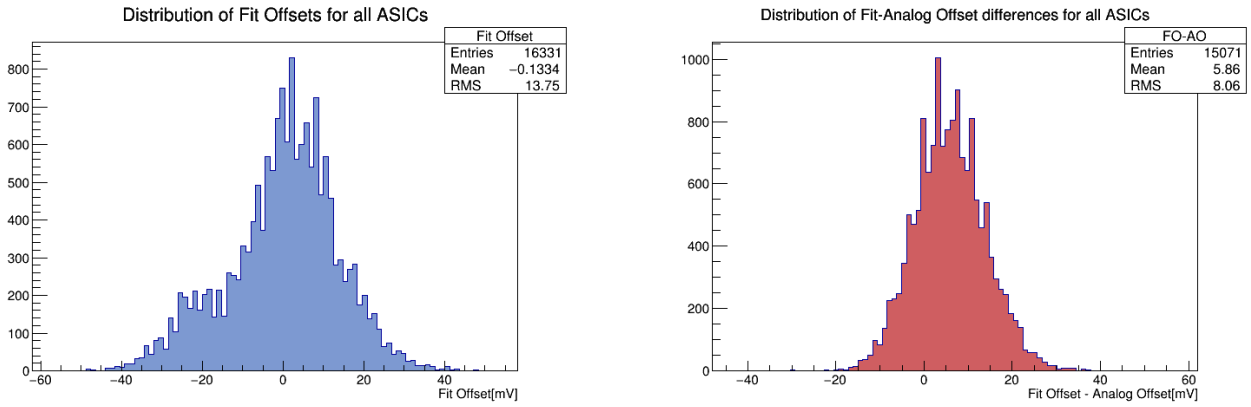

Figure 21: *Distribution of fit offsets (left) and offsets difference (right) for all the ASICs tested.*

From the distributions,the mean of the FO-AO difference is of 5,55 mV with an RMS of ~8,71 mV. The mean of the FO is of -0,1334 mV and the RMS is 13,75 mV.

In addition it is useful to check how the two offsets are related through a correlation plot. In this case, if the two measures are corresponding, they should have a linear relation with a slope close to 1. In *figure 22* such plot is showed.

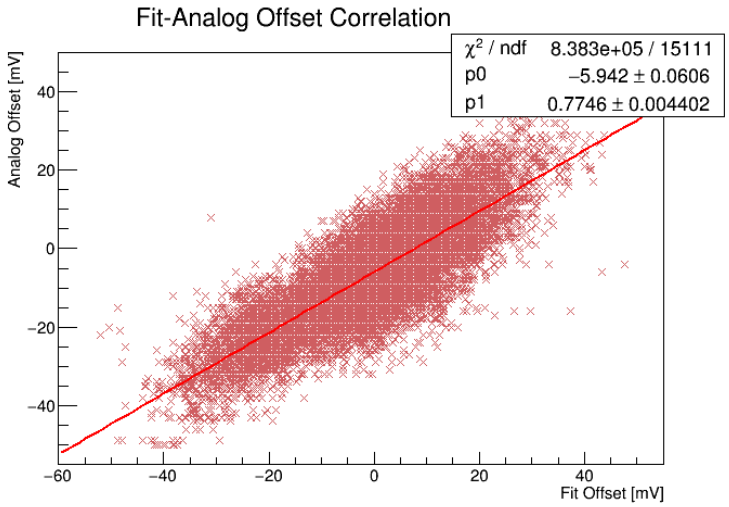

Figure 22*: Correlation plot between analog offset and fit offset for all ASICs tested.*

The data has a pearson correlation factor of 0,82, the slope of the linear fit is 0,7746 and the origin ordinate -5,942. This result guarantee that the two offsets are clearly correlated, but the correspondence is not as clear as for digital offset. In this case the slope is slightly lower than 1, being 0,77, suggesting that a factor relating the two offsets is missing.

Following, it was studied the correlation of the fit offset and the difference for the different channels, adders and discriminators. *Figure 23* shows the correlation plots between channels for fixed adder and discriminator; adders for fixed channel and discriminator; and discriminators for fixed channel and adder.

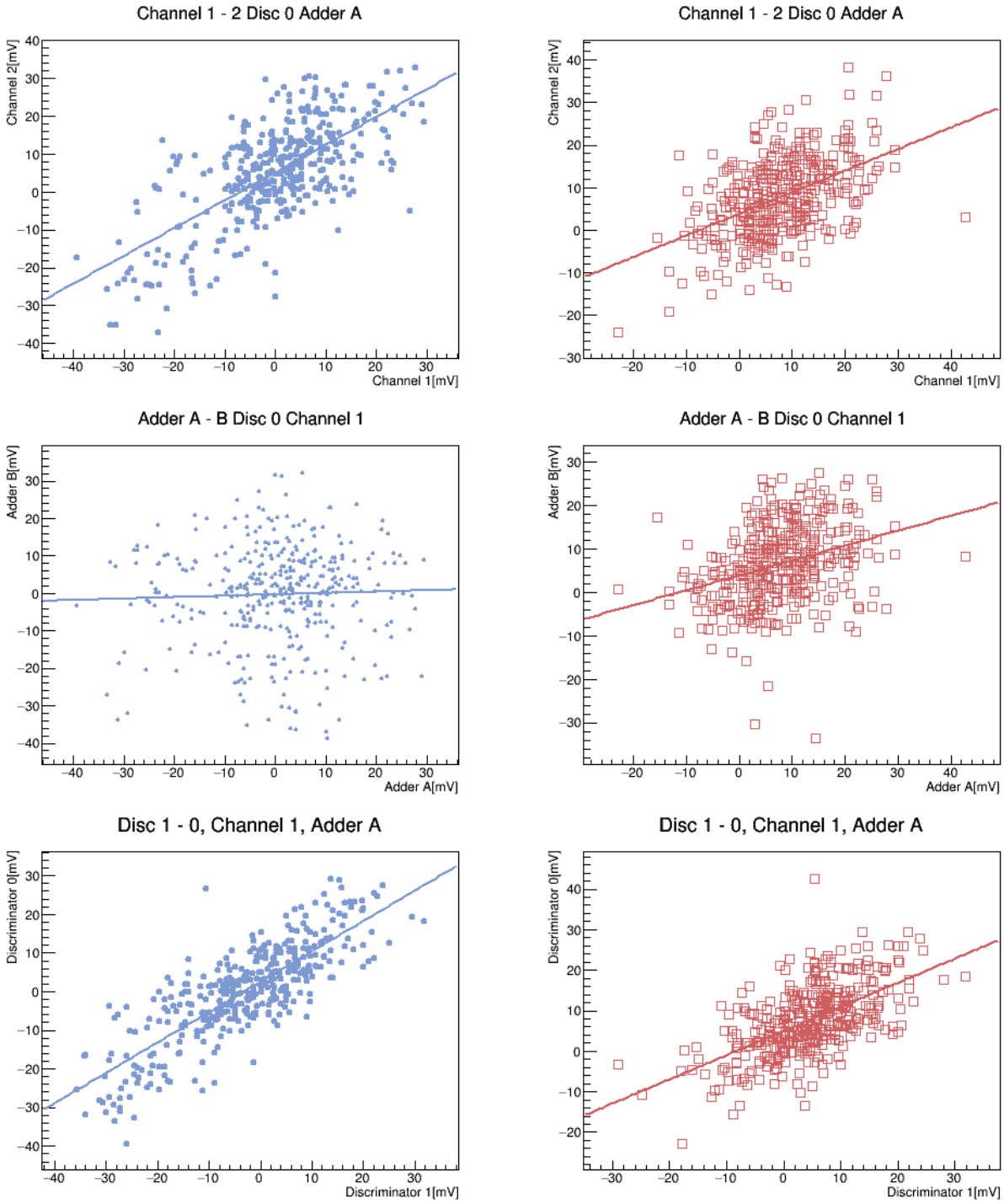

Figure 23: *Plots of correlations of the offset calculated from the fit of the rate scan(blue dots), together with the difference with the analog offset (red squares). On top is presented the correlation between two channels for fixed adder and discriminator. Middle plot is the correlation between two adders for fixed channel and discriminator. Bottom corresponds to the correlation between the two discriminators for fixed channel and adder. All possible combinations for correlations were plotted and the results are similar to these.*

There is a clear correlation of the Fit Offset in channels and discriminators, with correlation factors of 0,668 and 0,740 respectively (see *table 2*), but in adders there is no correlation at all, with an averaged correlation factor of 0,115. This result shows that the part of the ASIC that is responsible for introducing the offsets are the adders, reaching the same conclusion obtained from the analysis of the Analog offset.

From this section we can summarize that the fitting method gives a measure of the ASICs offset

which can differ from the one measured with a multimeter, by ~ 6mV.

5. Summary.

5.1 Gain.

The gain measured in the ASIC has a typical value of about 0,87+-0,038, having two channels that slightly differ from the rest. Is the case of the channels (2 and 3), that for all ASICs seem to have a deviation from the general mean, this effect is explanable by the setup configuration of the rate scan test. There are two ASICs where gain has a very low value, under 0,7, in several of their channels.
Relative to the correlation study, there is not a strong correlation for the gain in any part of the ASICs, having all of them a correlation coefficient below 0,5.

5.2 Offset.

The analog offsets measured in the test have a negative mean value, while the digital offset, as the rate scan only can provide possitive offsets, gives a positive mean value.
In the correlation plots for the analog offset, it can be observed a positive correlation between channels , with correlation coefficients ~0,8 which means that for a high offset in one channel it is also high in all the rest. For the adders however, the correlation observed in the plot is much lower, and the correlation coefficient is under 0.5 , concluding that in the adders, the offset measured is independent from each other, so they are the parts of the ASIC where the offset is introduced.
In the case of the digital offset, no correlation is observed at all, with coefficients very close to 0. It is needed to take into account that the data of digital offset is biased by the rate scan conditions.
From the correlation plot of digital and analog offset, we can say that both offsets have a correspondence and we are measuring the same feature, having a linear correlation with slope ~ 1.
In summary, the offset expected from a typical ASIC would be of -6 +- 13 mV.

5.3 Noise

As for the digital offset, the noise measured by the rate scan methodology gave only possitive values, and not all ASICs could be measured.
No correlation is observed for the noise in any part of the ASIC, therefore we can assume that all parts of the ASIC contribute to introduce noise in the signal.
The noise expected from a typical ASIC would be 5,18 +- 2,87.

5.4 Offset calculated from fitting the rate scan.

A method to calculate the offset of the ASIC in a indirect way was developed assuming a model where the input signal and the rate scan result have a linear relation.
The offset calculated by this method have in average, a difference with the analog offset of 5,86+- 8 mV.
The correlation between the fit offset and the analog offset showed that they have a linear correlation by a factor of 0,774.
The study of the fit offset in the different parts of the ASICs supported the idea that the adders are responsible for introducing the offset in the ASIC.

This work has serve to characterize the main features expected for a typical ASIC which are

presented in *tables 3*. Deviations from this measures could point to a problem in the performance of an ASIC.

In addition, an indirect method to calculate the offset has been developed, that could help to measure the offset directly from the cammera, without the necessity to access the ASIC directly.

Disc	Ch	Add	Gain	RMS	Analog Offset[mV]	RMS[mV]	Digital Offset[mV]	RMS[mV]	Fit Offset[mV]	RMS[mV]	Noise[mV]	RMS[mV]
0	1	1	0,865733	0,0354431	-2,56825	12,0754	9,26942	6,00255	5,42159	13151	4,73869	2,65657
0	1	2	0,861889	0,0372319	-6,90529	11,6572	7,38961	5,61574	0,459297	13,2761	4,40559	2,48136
0	2	0	0,838466	0,035875	-2,82682	11,5199	8,88718	5,92886	4,81186	12,0241	5,08421	2,35825
0	2	1	0,833886	0,0374605	-7,35196	12,2333	7,90845	5,88134	0,506872	13,5916	5	2,55973
0	2	2	0,830387	0,0369065	-3,70752	12,1045	8,92932	6,18108	3,99229	12,8837	4,79679	2,44105
0	3	0	0,879369	0,0367518	-7,35933	11,7325	7,87132	5,64872	0,784061	13,1786	5,64662	3,484
0	3	1	0,872314	0,0381587	-7,52089	12,7001	7,58562	5,68263	-0,450728	13,1254	5,22917	2,54056
0	3	2	0,871234	0,0377928	-4,04735	13,1041	9,25946	6,80006	3,55013	14,3746	4,32	2,18838
0	4	0	0,869755	0,0373787	-7,07521	12,9157	8,36331	6,00024	0,205656	13,5603	4,19231	2,25012
0	4	1	0,867655	0,0359559	-4,30168	12,8884	8,9435	6,38963	2,65292	13278	4,65497	2,18266
0	4	2	0,861649	0,0354134	-7,55153	12,4649	7,70956	5,78174	0,0951152	13,1499	4,81395	2,60223
0	5	0	0,873273	0,0374989	-5,17827	12,9837	8,79697	6,41468	1,78835	13,7437	4,80921	2,19069
0	5	1	0,870116	0,0359688	-7,37604	12,6522	8,36525	5,49044	-0,487576	13,7508	5,05839	2,46957
0	5	2	0,868586	0,0368392	-8,2312	13,7086	8,84926	6,51816	-0,999143	14,8268	5,9771	3,5693
0	6	0	0,86892	0,0393618	-4,48189	13,8268	9,7963	7,14917	3,15424	15,5242	4,8895	3,11456
0	6	1	0,869291	0,0343526	-7,76602	13,8442	8,83929	6,63897	-0,61611	14,7812	4,48462	2,61721
0	6	2	0,866015	0,0360581	-4,48324	14,1144	9,44624	6,93439	3,11168	14,9143	5,3587	2,9565
0	7	0	0,873033	0,0379731	-8,15042	13,6576	8,28777	6,33279	-0,973436	14,9387	4,92537	2,75526
0	7	1	0,872879	0,0360707	-5,50418	14,0574	9,41124	7,01801	1,49357	14,6893	5,28402	3,06379
0	7	2	0,869562	0,0386874	-8,07242	13,8974	8,32168	6,35307	-0,732647	14,9372	5,6383	2,63978
1	1	0	0,881697	0,0341451	-8,04178	11,7013	7,4927	5,56054	-3,03256	12605	6,04444	3,70158
1	1	1	0,876093	0,0328864	-2,56825	12,0754	9	6,24797	2,56555	12,6045	5,40816	3,62626
1	1	2	0,872108	0,0318161	-6,90529	11,6572	7,15753	5,46745	-2,59383	12,1416	5,12057	3,43424
1	2	0	0,847899	0,0314701	-2,82682	11,5199	8,46073	5,71851	1,5189	11,4802	5,34737	2,79574
1	2	1	0,845232	0,0323591	-7,34819	12,2164	7,43103	5,58897	-3,17824	13,3383	5,1958	2,79425
1	2	2	0,838856	0,0329706	-3,70752	12,1045	8,5582	5,93878	0,9006	12,3124	5,41711	2,95009
1	3	0	0,890874	0,0358411	-7,35933	11,7325	7,37132	5,31715	-3,06684	12,7281	5,78195	2,88199
1	3	1	0,884409	0,0339822	-7,52089	12,7001	7,07483	5,47237	-3,13453	13,5406	5,6069	2,64522
1	3	2	0,883612	0,0325719	-4,04735	13,1041	8,89503	6,50563	0,259641	13,9549	5,01156	2,73066
1	4	0	0,882881	0,034909	-7,07521	12,9157	7,51034	5,7519	-2,88689	13,3739	4,77698	2,30121
1	4	1	0,878196	0,0336269	-4,30168	12,8884	8,66384	6,19265	-0,0876289	13,5648	5,28977	2,82262
1	4	2	0,875941	0,0309881	-7,55153	12,4649	7,20438	5,55088	-3,23393	13001	5,03759	2,28893
1	5	0	0,887686	0,034171	-5,17827	12,9837	8,5122	6,00304	-0,83976	12,6118	5,41718	2,66956
1	5	1	0,881864	0,0329572	-7,37604	12,6522	7,61986	5,27637	-3,32048	12,9181	5,34028	2,65666
1	5	2	0,877262	0,0327925	-8,2312	13,7086	7,81071	5,98285	-3,39332	14,0924	6,13971	3,1557
1	6	0	0,880771	0,0354957	-4,48189	13,8268	9,3288	6,61699	0,871464	14,3059	4,99444	3,31913
1	6	1	0,878608	0,0332089	-7,76602	13,8442	8,63603	6,52525	-3,29734	13,35	4,96296	3,16791
1	6	2	0,87653	0,031666	-4,48324	14,1144	9,18362	6,59579	-0,118557	13,5596	5,63793	2,83065
1	7	0	0,887339	0,0345601	-8,15042	13,6576	7,87037	6,10918	-3,0437	13,7544	5,31579	2,9389
1	7	1	0,88383	0,033284	-5,50418	14,0574	8,97059	6,77424	-0,674379	13,6534	5,5503	2,8985
1	7	2	0,881967	0,0317656	-8,07242	13,8974	7,93478	5,91143	-3,7892	14,0832	5,56115	3,54846

Table 3: *Values of the gain, offset (measured by three different methods) and noise for the different parts of the typical ASIC, obtained averaging to all the ASICs tested.*