CIEMAT – BASIC RESEARCH AND ELECTRONIC UNIT

Analogue Sum ASIC for L1 Trigger Decision in Cherenkov Telescopes Cameras

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Introduction

A mixed signal Application Specific Integrated Circuit (ASIC) has been specifically developed implementing the functionality of analog **level 1 trigger decision** prototype [1] for CTA **Cherenkov Telescope cameras** [2] based in the detection of a concentration of signal both in space and time. The ASIC comprises 7 input differential analogue channels and 2 output digital differential channels. Analogue inputs are provided by the previous trigger stage implemented in the so-called L0 ASIC [3]. The two basic functionalities of L1 ASIC are the calculation of the sum of three configurable sets of inputs channels and provides the discrimination of the resulting voltage pulses in order to generate digital trigger output signals when any of the sums is above configurable voltage thresholds. The analogue signal processing stage has been specifically developed for this application by means of a low noise differential architecture that provides 500MHz bandwidth.

ASIC Description

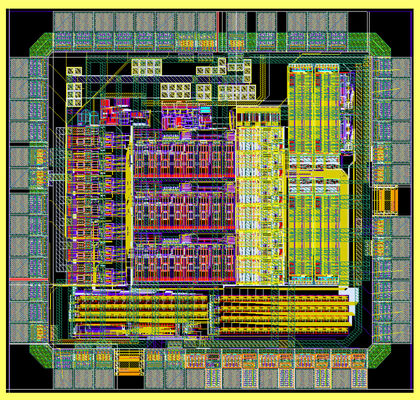

Figure 1: Level 1 ASIC layout

➢ Design was submitted in June 2013 in Austria Microsystems (AMS) 0.35 µm S35 SiGe BiCMOS technology and received in September 2013:

- ***Size: 2.061 x 1.861 mm***
- ***Area: 3.853mm²***
- ***30 units Packaged on 48pin QFN.***

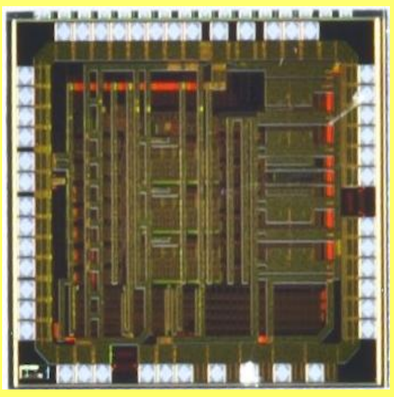

Figure 2: Picture of the Level 1 ASIC die

The basic fully differential, low noise and high bandwidth architecture (Fig. 3) has the following features:

- **Input**: Comprises 7 differential analogue inputs channels with a range of 0 - 1.2 V.
- **Input stage**: Input pulses are replicated by 3 and connected to individually controllable analogue high bandwidth switches.
- **Adders**: 3 analogue adders are able to sum up to 7 inputs channels each.
  → **Flexibility**: Any subset of signals can be summed up in any of the 3 adders.
  → **Gain**: 0,85 linear up to 1V (100phe) and **500MHz bandwidth**.
- **Discriminators**: Six differential leading edge voltage discriminators are used for trigger signal generation, one per adder and per voltage threshold.
- **DACs**: Voltage thresholds are generated by two independent differential Voltage DACs of 10 bits with a 1,27 mV (0.1 phe) resolution and 1,2 V range.
- **Output**: The outputs of the discriminators are combined in two OR gates, which outputs are connected to LVDS transmitters that provide the 2 digital trigger outputs of the ASIC with independent threshold definition.
- **Slow Control**: Serial link based. 7 registers (16-bit wide each) store switches enabling, DAC codes and output enables

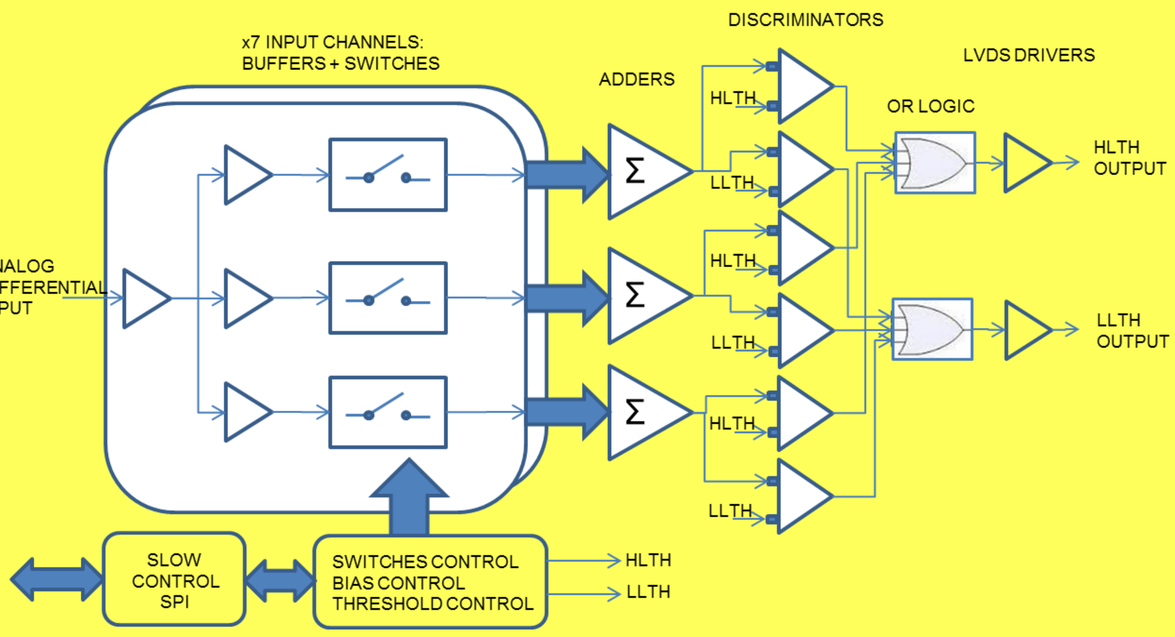

Figure 3: Block diagram architecture of the Level 1 ASIC

Performance

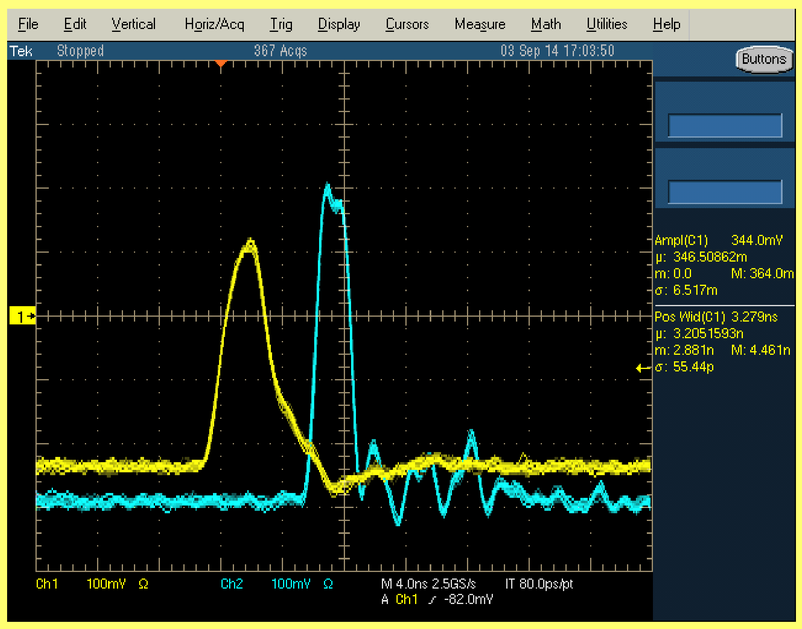

Figure 4 : Input and output signals of the ASIC with two active channels added

Figure 4 shows an example of a fast differential analog pulsed signal (yellow) of 346 mV amplitude and 3.3 ns time width, injected in two different enabled channels. The sum of the two signals, provide **588mV** (346mV*2*0.85) at discriminator input, which overcome in an overwhelming manner the threshold of **370 mV**. In blue the digital LVDS output trigger.

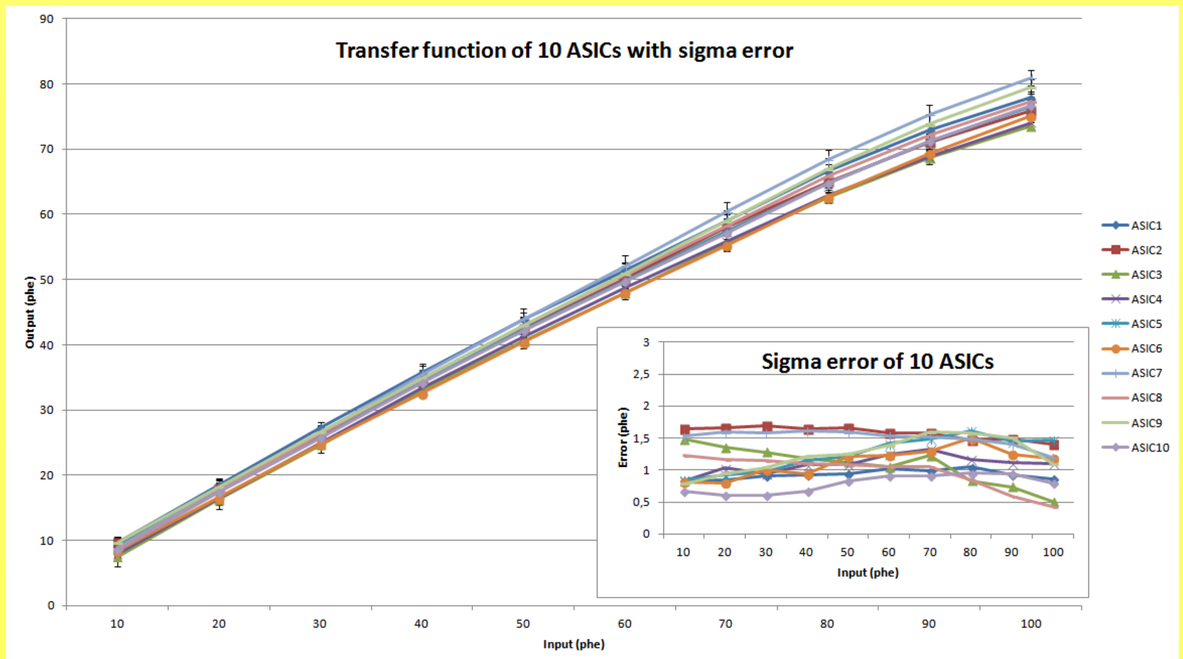

Figure 5: Measurement of the transfer function of 10ASICs, showing the dynamic range with linearity better than 10%

- A measurement of the transfer function of 10 ASCs (Fig. 5) shows the **linearity <10% in a dynamic range of 1 V** or 100 phe (10mV/phe).
- **350mW @ 3.3V power**
- **Jitter: down to 15 ps (RMS)** depending on threshold and overdrive.
- **Noise: 0,2 phe** per added channel.
- Signal-to-Noise ratio > 5
- **Delay 5-6 ns** depending on threshold.

The transfer functions by rate scan of different sum combinations is showed in Fig. 6. It can be observed that the gain is compatible for different sum combinations, when signal is injected in just one channel or distributed in 2, 3 or 4 different channels.

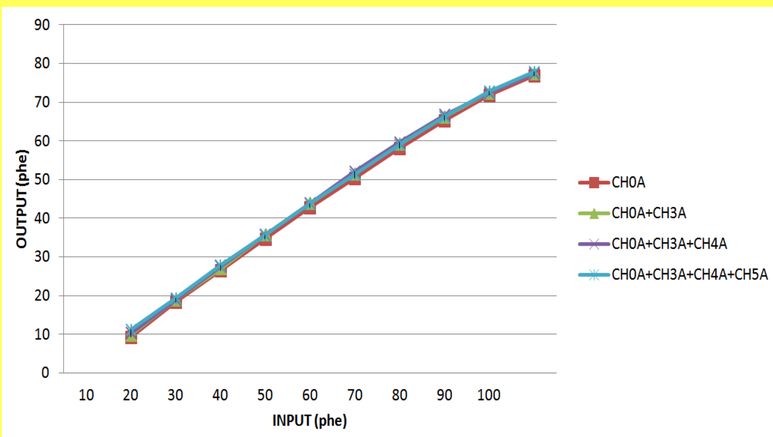

Figure 6 : Transfer functions of different Sum combinations by rate scans methods

Conclusion

A first version of the ASIC has been designed and develop for analog sum based trigger decision for next future Cherenkov telescope cameras with the following features: fully differential, low noise, high bandwidth, 1V (100 phe) dynamic range, multi channel, good linearity and flexibility. The ASIC was submitted to 350nm SiGe BICMOS Multi-Project Wafer run last June 2013 and has been received and tested. **The results of the full characterization of 30 ASICs are very satisfactory**.

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