Computer Architecture

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Taken from: M.
Mano/Computer Design and
Architecture 3rd Ed.

Microoperations Types

Data transfer only

- 1. Register Transfer microoperations transfer binary information from one register to another
- 2. Arithmetic microoperations perform arithmetic operation on numeric data stored in registers.
- 3. Logic microoperations perform bit manipulation operations on non numeric data stored in registers.
- 4. Shift microoperations perform shift operations data stored in registers.

Changes data during transfer

Arithmetic Microoperations

Basic: addition, subtraction, increment, decrement & shift

Multiplication and division are not basic

Arithmetic Microoperations

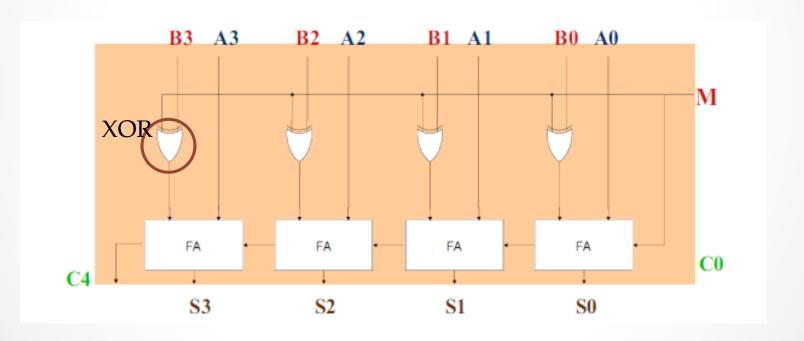
There are two identical operations

TABLE 4-3 Arithmetic Microoperations

| Symbolic designation | Description |
|--|--|
| $R3 \leftarrow R1 + R2$ | Contents of R1 plus R2 transferred to R3 |
| $R3 \leftarrow R1 - R2$ | Contents of R1 minus R2 transferred to R3 |
| $R2 \leftarrow \overline{R2}$ | Complement the contents of R2 (1's complement) |
| $R2 \leftarrow \overline{R2} + 1$ | 2's complement the contents of R2 (negate) |
| $R3 \leftarrow R1 + \overline{R2} + 1$ | R1 plus the 2's complement of R2 (subtraction) |
| $R1 \leftarrow R1 + 1$ | Increment the contents of R1 by one |
| $R1 \leftarrow R1 - 1$ | Decrement the contents of R1 by one |

Binary Adder-Subtractor

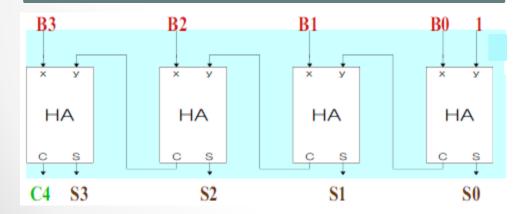
- M =0 : Adder
- $B \oplus M + C_0 = B \oplus 0 + 0 = B \implies S = A + B$
- M =1: Subtractor $B \oplus M + C_0 \longrightarrow B \oplus 1 + 1 = B' + 1 = -B \Rightarrow S = A B$



Binary Incrementer

Sequential circuit using a binary counter

Combinational circuit using half adders



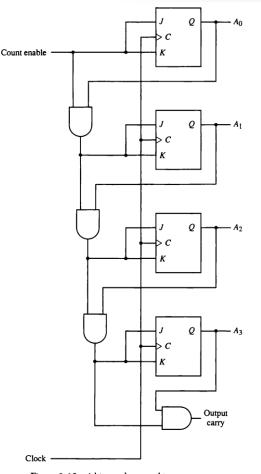
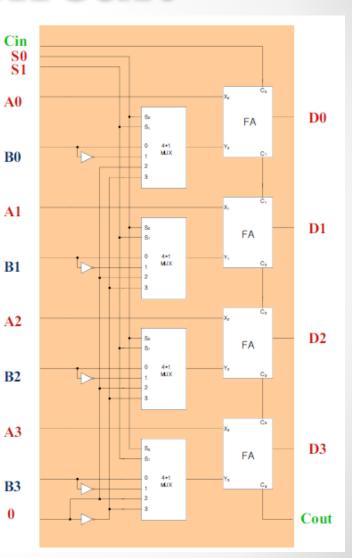


Figure 2-10 4-bit synchronous binary counter.

TABLE 4-4 Arithmetic Circuit Function Table

| | Select | | . | • | |
|------------------|--------|-------|----------------|-----------------------------|----------------------|
| $\overline{S_1}$ | | | Input Y | Output $D = A + Y + C_{in}$ | Microoperation |
| 0 | 0 | 0 [| В | D = A + B | Add |
| 0 | 0 | J 1 L | В | D = A + B + 1 | Add with carry |
| 0 | 1 | 0 | \overline{B} | $D = A + \overline{B}$ | Subtract with borrow |
| 0 | 1 | 1 | \overline{B} | $D=A+\overline{B}+1$ | Subtract |
| 1 | 0 | 0 | 0 | D = A | Transfer A |
| 1 | 0 | 1 | 0 | D=A+1 | Increment A |
| 1 | 1 | 0 | 1 | D = A - 1 | Decrement A |
| 1 | 1 | 1 | 1 | D = A | Transfer A |



 $\mathbf{0}$

TABLE 4-4 Arithmetic Circuit Function Table

| | Select | | Innut | Output | |
|------------------|--------|----------|----------------|-----------------------------|----------------------|
| $\overline{S_1}$ | So | C_{in} | Input Y | Output $D = A + Y + C_{in}$ | Microoperation |
| 0 | 0 | 0 | В | D = A + B | Add |
| 0 | 0 | 1 | <u>B</u> | D = A + B + 1 | Add with carry |
| 0 | 1 | 0 | \overline{B} | $D = A + \overline{B}$ | Subtract with borrow |
| 0 | _1 | 1 | \overline{B} | $D = A + \overline{B} + 1$ | Subtract |
| 1 | 0 | 0 | 0 | D = A | Transfer A |
| 1 | 0 | 1 | 0 | D=A+1 | Increment A |
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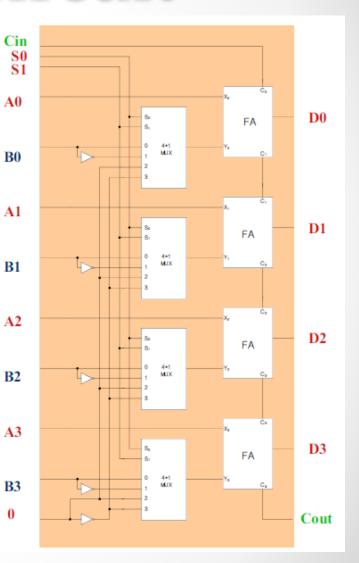
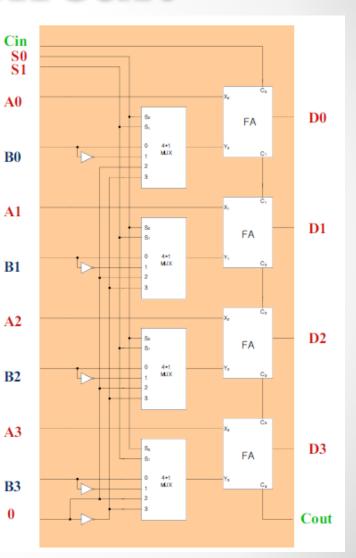


TABLE 4-4 Arithmetic Circuit Function Table

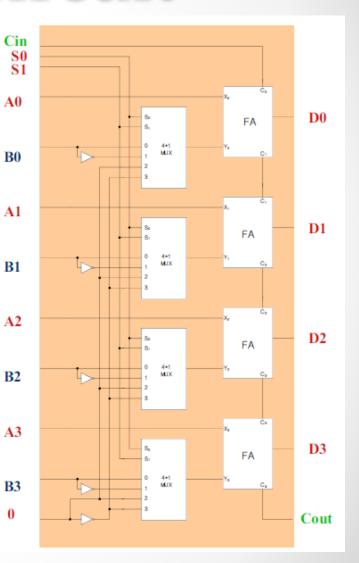
| | Select | | Innut | Output | |
|------------------|--------|----------|----------------|-----------------------------|----------------------|
| $\overline{S_1}$ | So | C_{in} | Input Y | Output $D = A + Y + C_{in}$ | Microoperation |
| 0 | 0 | 0 | В | D = A + B | Add |
| 0 | 0 | 1 | В | D = A + B + 1 | Add with carry |
| 0 | 1 | 0 | \overline{B} | $D = A + \overline{B}$ | Subtract with borrow |
| 0 | _1_ | 1 | \overline{B} | $D=A+\overline{B}+1$ | Subtract |
| 1 | 0 | 0 | 0 | D = A | Transfer A |
| 1 | | 1 | 0 | D=A+1 | Increment A |
| 1 | 1 | 0 | 1 | D = A - 1 | Decrement A |
| 1 | 1 | 1 | 1 | D = A | Transfer A |



 $\mathbf{0}$

TABLE 4-4 Arithmetic Circuit Function Table

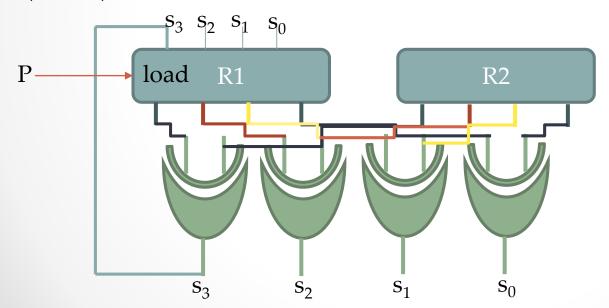
| | Select | | Tanut | Output | |
|------------------|--------|----------|----------------|-----------------------------|----------------------|
| $\overline{S_1}$ | So | C_{in} | Input Y | Output $D = A + Y + C_{in}$ | Microoperation |
| 0 | 0 | 0 | В | D = A + B | Add |
| 0 | 0 | 1 | В | D = A + B + 1 | Add with carry |
| 0 | 1 | 0 | \overline{B} | $D = A + \overline{B}$ | Subtract with borrow |
| 0 | 1 | 1 | \overline{B} | $D=A+\overline{B}+1$ | Subtract |
| 1 | 0 | 0 | 0 | D = A | Transfer A |
| 1 | 0 | 1 | 0 | D=A+1 | Increment A |
| 1 | 1 | 0 (| 1 | D = A - 1 | Decrement A |
| 1 | 1 | 1 | 1 | D = A | Transfer A |



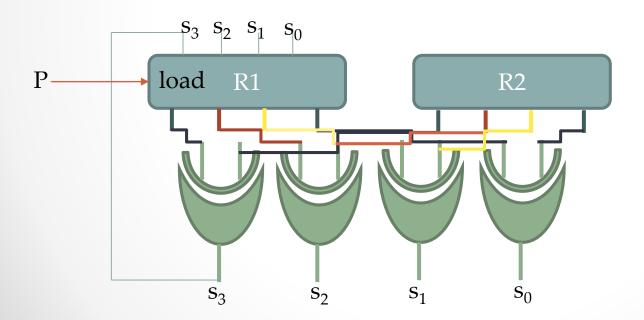
Logic microoperations consider **each bit of the register separately** and treat them as binary variables

Example: XOR

if (P = = 1) then $R1 \leftarrow R1 \oplus R2$ or in RTL $P: R1 \leftarrow R1 \oplus R2$



R1: 1001R2: 1100R1: 0101 $s_3 s_2 s_1 s_0$



Special symbols in RTL:

Left side - condition

Or denoted by +
And denoted by •
complement denoted by '

Right side - operation

Or denoted by \
And denoted by \
complement denoted by
Arith. Plus denoted by +
Arith. Mult. denoted by *

Example:

P+Q: R1
$$\leftarrow$$
 R1 + R2, R3 \leftarrow R4 \vee R5

or

addition

or

| TABLE 4-5 | Truth | Tables for | 16 Functions | of Two | Variables |
|-----------|-------|------------|--------------|--------|-----------|
|-----------|-------|------------|--------------|--------|-----------|

| | | 1 | | | | _ | | | | | | | | | | F ₁₄ | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-----------------|-------------|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 1 1 |
| 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |



| TABLE 4-5 | Truth 7 | Tables fo | or 16 | Functions | of Two | Variables |
|-----------|---------|-----------|-------|-----------|--------|-----------|
|-----------|---------|-----------|-------|-----------|--------|-----------|

| х | у | F ₀ | $\overline{F_1}$ | F ₂ | <i>F</i> ₃ | F ₄ | <i>F</i> ₅ | <i>F</i> ₆ | F ₇ | F ₈ | F ₉ | F ₁₀ | F ₁₁ | F ₁₂ | F ₁₃ | F ₁₄ | F ₁₅ |
|---|----|----------------|------------------|----------------|-----------------------|----------------|-----------------------|-----------------------|----------------|----------------|----------------|-----------------|-----------------|------------------|-----------------|-----------------|-----------------|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 1 0 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| 1 | _1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |



| TABLE 4-5 | Truth 7 | Tables fo | or 16 | Functions | of Two | Variables |
|-----------|---------|-----------|-------|-----------|--------|-----------|
|-----------|---------|-----------|-------|-----------|--------|-----------|

| х | у | F_0 | F_1 | F ₂ | <i>F</i> ₃ | F ₄ | F ₅ | F ₆ | F ₇ | F ₈ | F ₉ | F ₁₀ | F ₁₁ | F_{12} | F ₁₃ | F ₁₄ | F ₁₅ |
|---|----|-------|-------|----------------|-----------------------|----------------|----------------|----------------|----------------|----------------|----------------|-----------------|-----------------|------------------|-----------------|-----------------|-----------------|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 1 0 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 11 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| 1 | _1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |



| x | у | F ₀ | F_1 | F_2 | <i>F</i> ₃ | F ₄ | <i>F</i> ₅ | <i>F</i> ₆ | F ₇ | <i>F</i> ₈ | <i>F</i> ₉ | F ₁₀ | F_{11} | F ₁₂ | F ₁₃ | F ₁₄ | F ₁₅ |
|---|---|----------------|-------|-------|-----------------------|----------------|-----------------------|-----------------------|----------------|-----------------------|-----------------------|------------------|----------|-----------------|-----------------|-----------------|-----------------|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 0 1 0 | 1 | 1 | 1 | 1 | 1 |
| 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 11 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 11 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |



| TABLE 4-5 | Truth | Tables | for 16 | S Functions | of Two | Variables |
|------------------|-------|--------|--------|--|--------|------------|
| | HUULI | | 101 11 | <i>,</i> , , , , , , , , , , , , , , , , , , | | * allabics |

| <u> </u> | у | F ₀ | F_1 | F_2 | <i>F</i> ₃ | F ₄ | <i>F</i> ₅ | F ₆ | F ₇ | <i>F</i> ₈ | F ₉ | F ₁₀ | F ₁₁ | F ₁₂ | F ₁₃ | F ₁₄ | F ₁₅ |
|----------|---|----------------|-------|-------|-----------------------|----------------|-----------------------|----------------|----------------|-----------------------|----------------|------------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 0 1 0 | 1 | 1 | 1 | 1 | 1 |
| 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 11 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 11 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |



TABLE 4-6 Sixteen Logic Microoperations

| | TABLE | 4-5 | Truth | Tables | for | 16 |
|--|--------------|-----|-------|--------|-----|----|
|--|--------------|-----|-------|--------|-----|----|

| x | у | F ₀ | F_1 | F ₂ | F ₃ | F ₄ | F ₅ | F ₆ | F ₇ |
|---|---|------------------|-------|----------------|----------------|----------------|-----------------------|----------------|----------------|
| 0 | 0 | o | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| 1 | 1 | 0 0 0 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |

| x | у | F ₈ | F ₉ | F ₁₀ | F ₁₁ | F ₁₂ | F ₁₃ | F ₁₄ | F ₁₅ |
|---|---|----------------|----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |

| Boolean function | Microoperation | Name |
|-----------------------|--------------------------------------|----------------|
| $F_0 = 0$ | $F \leftarrow 0$ | Clear |
| $F_1 = xy$ | $F \leftarrow A \wedge B$ | AND |
| $F_2 = xy'$ | $F \leftarrow A \wedge \overline{B}$ | |
| $F_3 = x$ | $F \leftarrow A$ | Transfer A |
| $F_4 = x'y$ | $F \leftarrow \overline{A} \wedge B$ | |
| $F_5 = y$ | $F \leftarrow B$ | Transfer B |
| $F_6 = x \oplus y$ | $F \leftarrow A \oplus B$ | Exclusive-OR |
| $F_7 = x + y$ | $F \leftarrow A \lor B$ | OR |
| $F_8 = (x + y)'$ | $F \leftarrow \overline{A \vee B}$ | NOR |
| $F_9 = (x \oplus y)'$ | $F \leftarrow \overline{A \oplus B}$ | Exclusive-NOR |
| $F_{10}=y'$ | $F \leftarrow \overline{B}$ | Complement B |
| $F_{11}=x+y'$ | $F \leftarrow A \vee \overline{B}$ | |
| $F_{12}=x'$ | $F \leftarrow \overline{A}$ | Complement A |
| $F_{13}=x'+y$ | $F \leftarrow \overline{A} \vee B$ | |
| $F_{14}=(xy)'$ | $F \leftarrow \overline{A \wedge B}$ | NAND |
| $F_{15}=1$ | $F \leftarrow \text{all 1's}$ | Set to all 1's |

LM – HW implementaion

- Logic gates are inserted for each bit or pair of bits in the registers.
- Most computers use only 4 operations: AND, OR, XOR and complement.
- All 12 others can be derived.

(a) Logic diagram

Figure 4-10 One stage of logic circuit.

- Logic microoperations are very useful for *manipulating individual bits* or *a portion of a word* stored in a register
- Used to <u>change bit values</u>, delete a group of bits, or insert new bit values

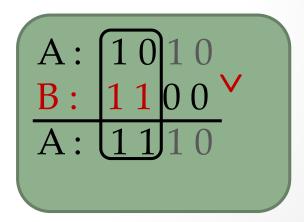
Selective set:

 $A \leftarrow A \vee B$

Sets to 1 the bits in register A where there are corresponding 1's in register B.

It does not effect bit positions that

It does not effect bit positions that have 0's in B.

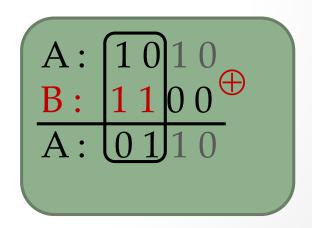


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- Used to <u>change bit values</u>, delete a group of bits, or insert new bit values

Selective complement:

 $A \leftarrow A \oplus B$

Complements to 1 the bits in register A where there are corresponding 1's in register B. It does not effect bit positions that have 0's in B.



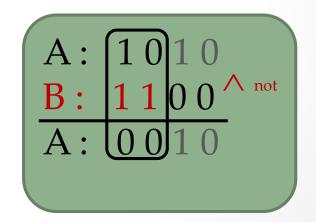
- Logic microoperations are very useful for *manipulating individual bits* or *a portion of a word* stored in a register
- Used to <u>change bit values</u>, delete a group of bits, or insert new bit values

Selective clear:

 $A \leftarrow A \wedge \overline{B}$

Clears to **0** the bits in register A where there are corresponding 1's in register B.

It does not effect bit positions that have 0's in B.

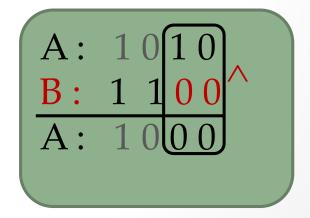


- Logic microoperations are very useful for *manipulating individual bits* or *a portion of a word* stored in a register
- Used to <u>change bit values</u>, delete a group of bits, or insert new bit values

Selective mask:

 $A \leftarrow A \wedge B$

The mask operation is similar to the selective-clear operation. Except that the bits of A are cleared only where there are corresponding 0's in B.



Insert:

- The insert operation inserts a new value into a group of bits.
- This is done by:
 - 1. Masking the bits
 - 2. QRing them with the required value

We would like to change the two rightmost bits of A to 01

A: 1010 B: 1100 A: 1000

A: 1000 B: 0001 A: 1001

Clear the bits you want to change

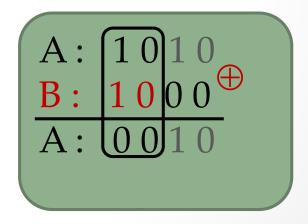
Set the bits to the desired pattern

- Logic microoperations are very useful for *manipulating individual bits* or *a portion of a word* stored in a register
- Used to <u>change bit values</u>, delete a group of bits, or insert new bit values

Clear operaion:

 $A \leftarrow A \oplus B$

The clear operation compares the words in A and B and produces an all 0's result if the two numbers are equal.



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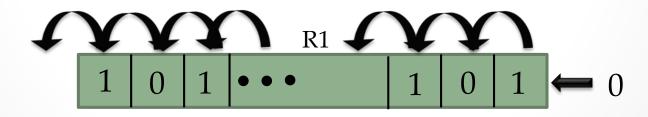
Shift Microoperations

- Shift microoperations can be used for serial transfer of data.
- Three types of shift microoperation : *Logical, Circular,* and *Arithmetic*

A *logical shift* transfers 0 through the serial input.

The bit transferred to the end position through the serial input is assumed to be 0 during a logical shift.

Shl – for shift left (insert 0 from rightmost side)



$$R1 \leftarrow shl R1$$

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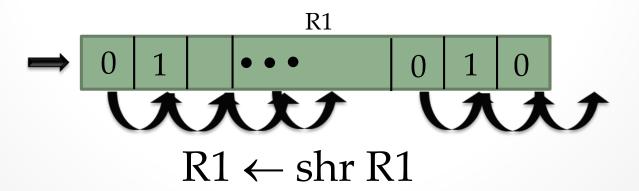
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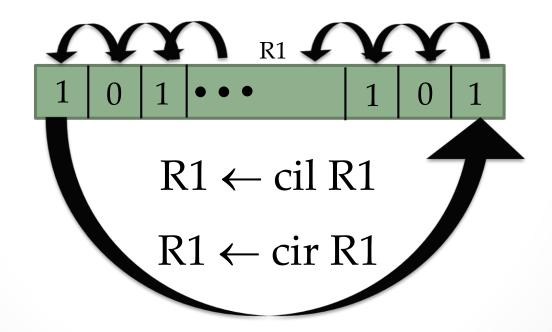
The bit transferred to the end position through the serial input is assumed to be $\mathbf{0}$ during a logical shift.

Shr – for shift right (insert 0 from leftmost side)



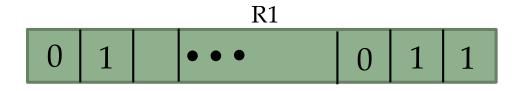
Circular shift

A *circular shift* circulates bits of the register around the two ends without loss of any bit.



Circular shift

A *circular shift* circulates bits of the register around the two ends without loss of any bit.



$$R1 \leftarrow cil R1$$

Arithmetic shift

- An *arithmetic shift* shifts a signed binary number to the left or right.
- An arithmetic shift-left (ashl) multiplies a signed binary number by 2.
- An arithmetic shift-right (ashr) divides a signed binary number by 2.
- Arithmetic shifts must leave the sign bit unchanged.

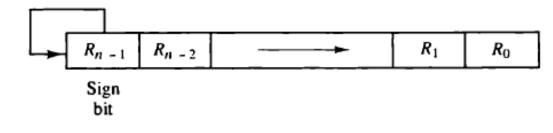


Figure 4-11 Arithmetic shift right.

Arithmetic shift-left

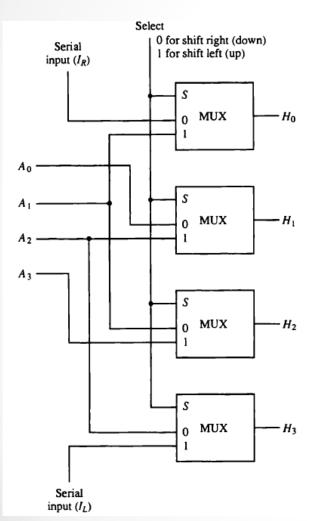
- The arithmetic shift-left insert 0 into R_0 , and shifts all other bits to the left.
- R_{n-2} becomes R_{n-1} and R_{n-1} lost and becomes the sign bit.
- A sign reversal occurs (overflow) if the bit in R_{n-1} changes its value after shift.

Example: a 4 bit signed R: 1 0 0 1 (= -7)

$$OF \leftarrow R_{n-1} \oplus R_{n-2}$$

$$OF = 0 \text{ ashl} \qquad 0 \text{ of } 0$$

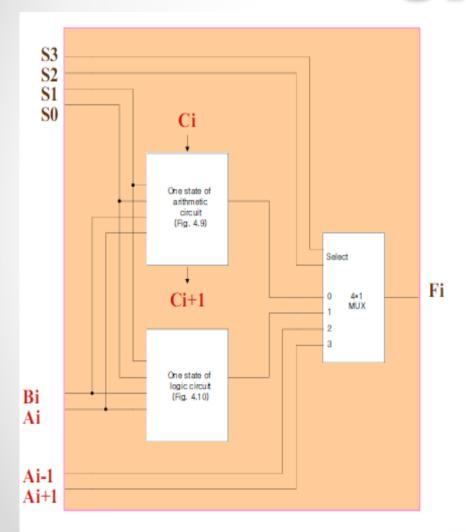
Shift – HW implementaion



| Function table | | | | | | | | | | |
|----------------|--------|----------------|----------------|-----------------------|--|--|--|--|--|--|
| Select | Output | | | | | | | | | |
| S | H_0 | H_1 | H ₂ | <i>H</i> ₃ | | | | | | |
| 0 | I_R | A_0 | A_1 | A_2 | | | | | | |
| 1 | A_1 | A ₂ | A ₃ | IL | | | | | | |

- When S=0, the input data is shifted right (down in the diagram).
- When S=1, the input data is shifted left (up in the diagram).
- A shifter with n data inputs, requires n multiplexers.

ALU - Arithmetical Logical Unit



- The contents of specific source registers are placed in the input of the ALU.
- The ALU performs the operation, and the result is then transferred to a destination register.
- The ALU is a combinational circuit, therefore the data transferred from source to destination through the ALU is performed during one clock pulse period.

ALU - Arithmetical Logical Unit

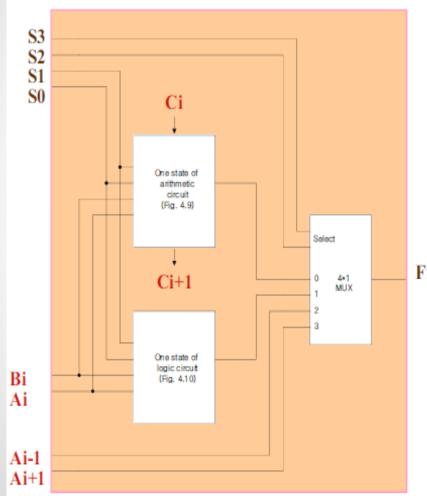


TABLE 4-8 Function Table for Arithmetic Logic Shift Unit

| | | Ope | ration | select | | | |
|---|-------|-----|--------|--------|----------|----------------------------|----------------------|
| | S_3 | S2 | S_1 | So | C_{in} | Operation | Function |
| | 0 | 0 | 0 | 0 | 0 | F = A | Transfer A |
| | 0 | 0 | 0 | 0 | 1 | F = A + 1 | Increment A |
| | 0 | 0 | 0 | 1 | 0 | F = A + B | Addition |
| | 0 | 0 | 0 | 1 | 1 | F = A + B + 1 | Add with carry |
| | 0 | 0 | 1 | 0 | 0 | $F = A + \overline{B}$ | Subtract with borrow |
| i | 0 | 0 | 1 | 0 | 1 | $F = A + \overline{B} + 1$ | Subtraction |
| | 0 | 0 | 1 | 1 | 0 | F = A - 1 | Decrement A |
| | 0 | 0 | 1 | 1 | 1 | F = A | Transfer A |
| | 0 | 1 | 0 | 0 | X | $F = A \wedge B$ | AND |
| | 0 | 1 | 0 | 1 | × | $F = A \vee B$ | OR |
| | 0 | 1 | 1 | 0 | X | $F = A \oplus B$ | XOR |
| | 0 | 1 | 1 | 1 | X | $F = \overline{A}$ | Complement A |
| | 1 | 0 | X | X | × | $F = \operatorname{shr} A$ | Shift right A into F |
| | 1 | 1 | × | × | × | $F = \operatorname{shl} A$ | Shift left A into F |

ALU - Arithmetical Logical Unit

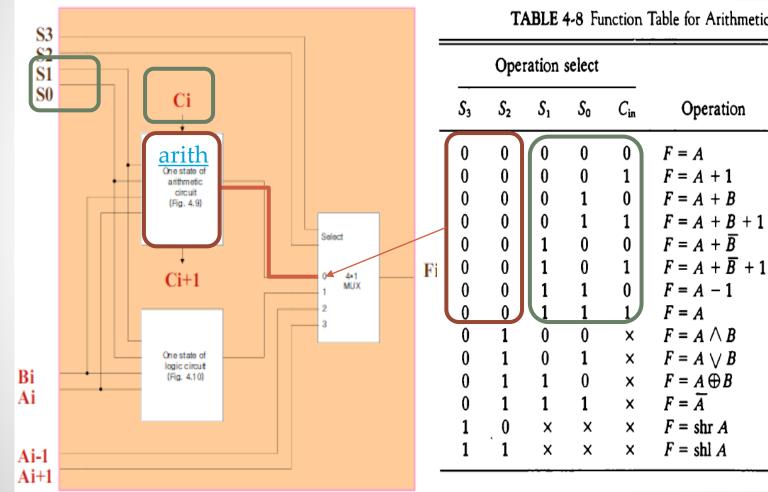


TABLE 4-8 Function Table for Arithmetic Logic Shift Unit

| Function |
|---|
| Transfer A Increment A Addition Add with carry Subtract with borrow Subtraction Decrement A |
| Transfer A |
| AND OR |
| XOR |
| Complement A |
| Shift right A into F |
| Shift left A into F |

ALU - Arithmetical Logical Unit

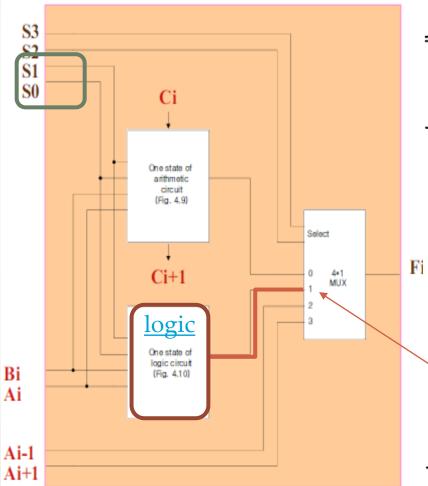


TABLE 4-8 Function Table for Arithmetic Logic Shift Unit

| | | Ope | ration | select | | | |
|---|----------------|-----|--------|----------------|----------|----------------------------|----------------------|
| | S ₃ | S2 | Sı | S ₀ | C_{in} | Operation | Function |
| | 0 | 0 | 0 | 0 | 0 | F = A | Transfer A |
| | 0 | 0 | 0 | 0 | 1 | F = A + 1 | Increment A |
| | 0 | 0 | 0 | 1 | 0 | F = A + B | Addition |
| | 0 | 0 | 0 | 1 | 1 | F = A + B + 1 | Add with carry |
| | 0 | 0 | 1 | 0 | 0 | $F = A + \overline{B}$ | Subtract with borrow |
| i | 0 | 0 | 1 | 0 | 1 | $F = A + \overline{B} + 1$ | Subtraction |
| | 0 | 0 | 1 | 1 | 0 | F = A - 1 | Decrement A |
| | 0 | 0 | 1 | _1 | 1 | F = A | Transfer A |
| | 0 | 1 | 0 | 0 | X | $F = A \wedge B$ | AND |
| | 0 | 1 | 0 | 1 | X | $F = A \vee B$ | OR |
| | 0 | 1 | 1 | 0 | X | $F = A \oplus B$ | XOR |
| l | 0 | 1 | 1 | _1 | X | $F = \overline{A}$ | Complement A |
| | 1 | 0 | X | X | × | $F = \operatorname{shr} A$ | Shift right A into F |
| | 1 | 1 | X | X | X | $F = \operatorname{shl} A$ | Shift left A into F |

ALU - Arithmetical Logical Unit

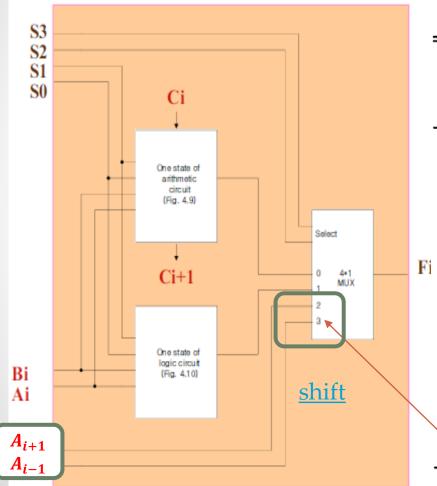


TABLE 4-8 Function Table for Arithmetic Logic Shift Unit

| | | Ope | ration | select | | | |
|---|-------|----------------|--------|--------|----------|----------------------------|----------------------|
| | S_3 | S2 | Sı | So | C_{in} | Operation | Function |
| | 0 | 0 | 0 | 0 | 0 | F = A | Transfer A |
| | 0 | 0 | 0 | 0 | 1 | F = A + 1 | Increment A |
| | 0 | 0 | 0 | 1 | 0 | F = A + B | Addition |
| | 0 | 0 | 0 | 1 | 1 | F = A + B + 1 | Add with carry |
| | 0 | 0 | 1 | 0 | 0 | $F = A + \overline{B}$ | Subtract with borrow |
| i | 0 | 0 | 1 | 0 | 1 | $F = A + \overline{B} + 1$ | Subtraction |
| | 0 | 0 | 1 | 1 | 0 | F = A - 1 | Decrement A |
| | 0 | 0 | 1 | 1 | 1 | F = A | Transfer A |
| | 0 | 1 | 0 | 0 | X | $F = A \wedge B$ | AND |
| | 0 | 1 | 0 | 1 | × | $F = A \vee B$ | OR |
| | 0 | 1 | 1 | 0 | X | $F = A \oplus B$ | XOR |
| | 0 | 1 | 1 | 1 | X | $F = \overline{A}$ | Complement A |
| 1 | 1 | 0 | × | X | × | $F = \operatorname{shr} A$ | Shift right A into F |
| | 1 | [.] 1 | × | X | × | $F = \operatorname{shl} A$ | Shift left A into F |