Paging (ch. 18)

Operating Systems

Based on: Three Easy Pieces by Arpaci-Dusseaux

Moshe Sulamy

Tel-Aviv Academic College

Paging

Improving on segmentation

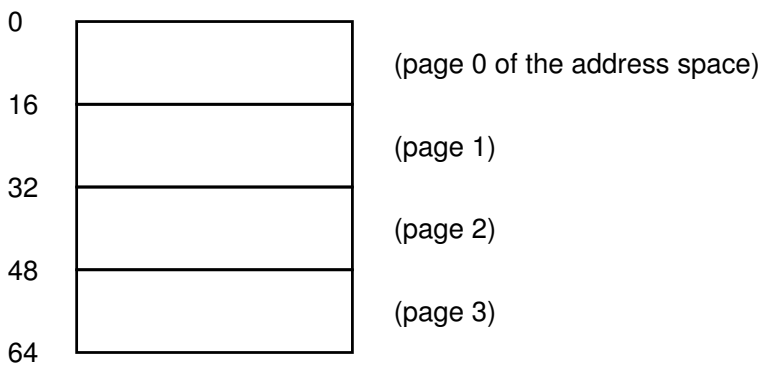
- Transparent to user mode code.
- No need for compactification. Ever.
- Basic idea: Small fixed size parts of process spread ‘randomly’ in physical memory.

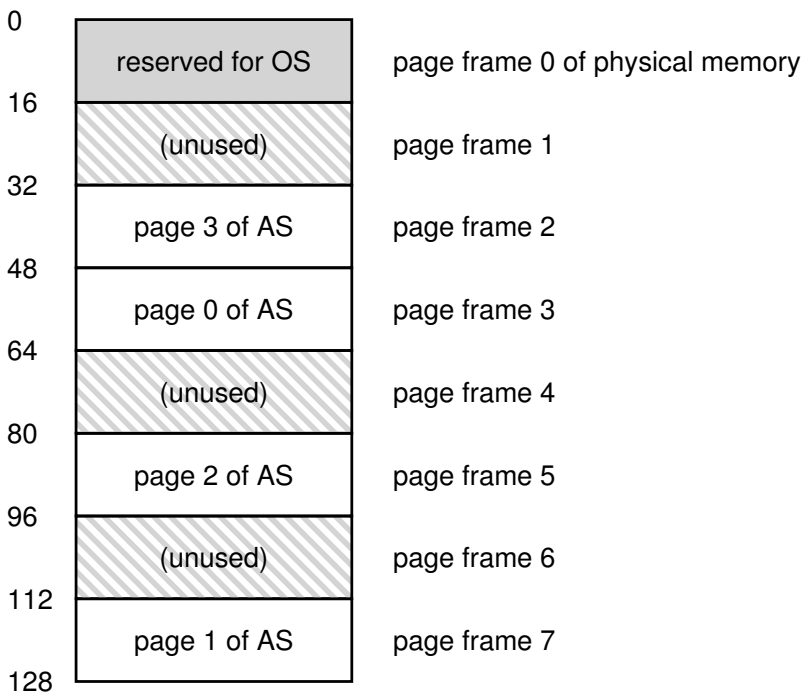
Paging

- Divide process address space into fixed-size pieces
- Each fixed-size unit is a (virtual) **page**
- Divide physical memory into **page frames** (physical page)

Paging

- For example:
  - 64-bytes address space, 16-byte pages, 128-bytes RAM



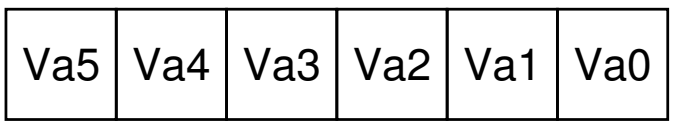


Paging

- **Page table**
  - Records where each virtual page is placed in physical memory
  - Per-process structure
  - **Address translation** for virtual pages

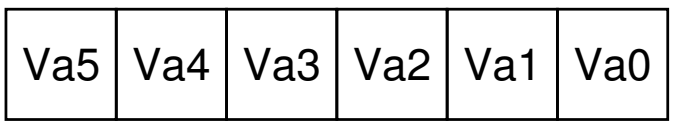
Paging

- To **translate** a virtual address:
  - Split into **virtual page number (VPN)** and **offset**
  - For 64-bytes, virtual address size is 6 bits:

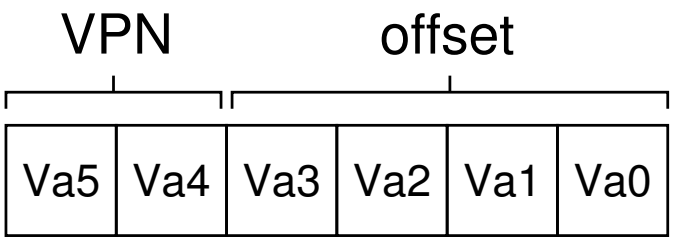


Paging

- To **translate** a virtual address:
  - Split into **virtual page number (VPN)** and **offset**
  - For 64-bytes, virtual address size is 6 bits:

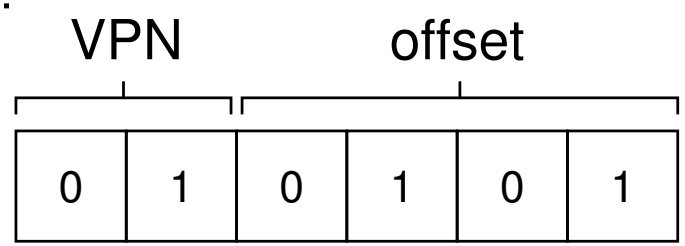


  - Address space is 4 pages, thus:



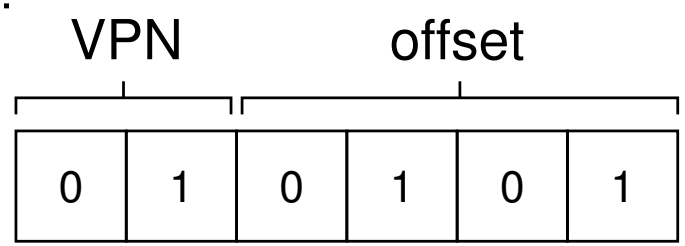
Paging

- Let's translate an address!
  - Virtual address 21:

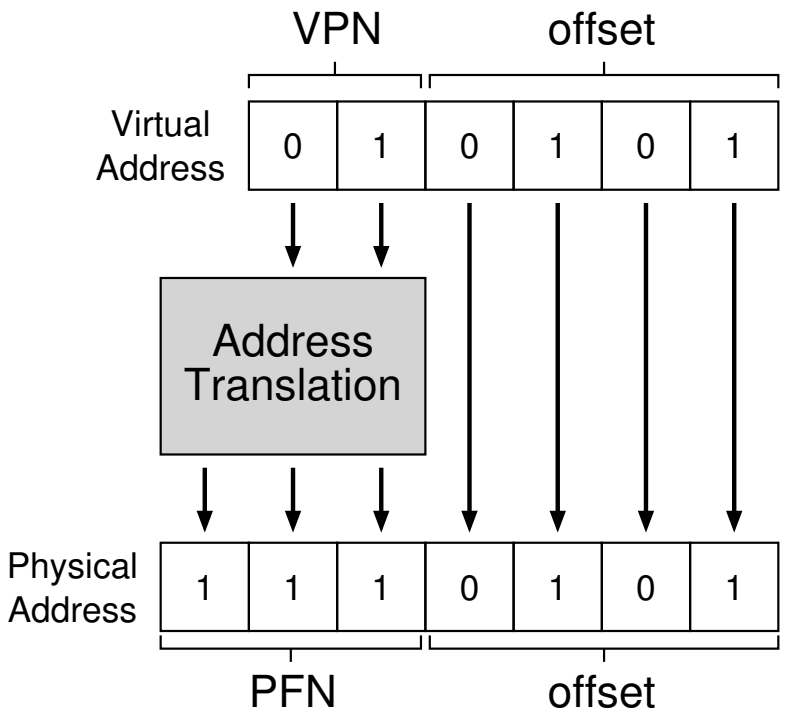


Paging

- Let's translate an address!
  - Virtual address 21:



  - 5th byte of page 1 $\rightarrow$ **physical frame number (PFN)** 7:



Bitology

Page Size	Low Bits		
16 bytes			

Bitology

Page Size	Low Bits		
16 bytes	4		
1KB			

Bitology

Page Size	Low Bits		
16 bytes	4		
1KB	10		
1MB			

Bitology

Page Size	Low Bits		
16 bytes	4		
1KB	10		
1MB	20		
512 bytes			

Bitology

Page Size	Low Bits		
16 bytes	4		
1KB	10		
1MB	20		
512 bytes	9		
4KB			

Bitology

Page Size	Low Bits		
16 bytes	4		
1KB	10		
1MB	20		
512 bytes	9		
4KB	12		

Bitology

Page Size	Low Bits	V.Addr Bits	High Bits	
16 bytes	4	10		
1KB	10	20		
1MB	20	32		
512 bytes	9	16		
4KB	12	32		

Bitology

Page Size	Low Bits	V.Addr Bits	High Bits	
16 bytes	4	10	6	
1KB	10	20		
1MB	20	32		
512 bytes	9	16		
4KB	12	32		

Bitology

Page Size	Low Bits	V.Addr Bits	High Bits	
16 bytes	4	10	6	
1KB	10	20	10	
1MB	20	32		
512 bytes	9	16		
4KB	12	32		

Bitology

Page Size	Low Bits	V.Addr Bits	High Bits	
16 bytes	4	10	6	
1KB	10	20	10	
1MB	20	32	12	
512 bytes	9	16		
4KB	12	32		

Bitology

Page Size	Low Bits	V.Addr Bits	High Bits	
16 bytes	4	10	6	
1KB	10	20	10	
1MB	20	32	12	
512 bytes	9	16	5	
4KB	12	32		

Bitology

Page Size	Low Bits	V.Addr Bits	High Bits	
16 bytes	4	10	6	
1KB	10	20	10	
1MB	20	32	12	
512 bytes	9	16	5	
4KB	12	32	20	

Bitology

Page Size	Low Bits	V.Addr Bits	High Bits	# V.Pages
16 bytes	4	10	6	
1KB	10	20	10	
1MB	20	32	12	
512 bytes	9	16	5	
4KB	12	32	20	

Bitology

Page Size	Low Bits	V.Addr Bits	High Bits	# V.Pages
16 bytes	4	10	6	64
1KB	10	20	10	
1MB	20	32	12	
512 bytes	9	16	5	
4KB	12	32	20	

Bitology

Page Size	Low Bits	V.Addr Bits	High Bits	# V.Pages
16 bytes	4	10	6	64
1KB	10	20	10	1K
1MB	20	32	12	
512 bytes	9	16	5	
4KB	12	32	20	

Bitology

Page Size	Low Bits	V.Addr Bits	High Bits	# V.Pages
16 bytes	4	10	6	64
1KB	10	20	10	1K
1MB	20	32	12	4K
512 bytes	9	16	5	
4KB	12	32	20	

Bitology

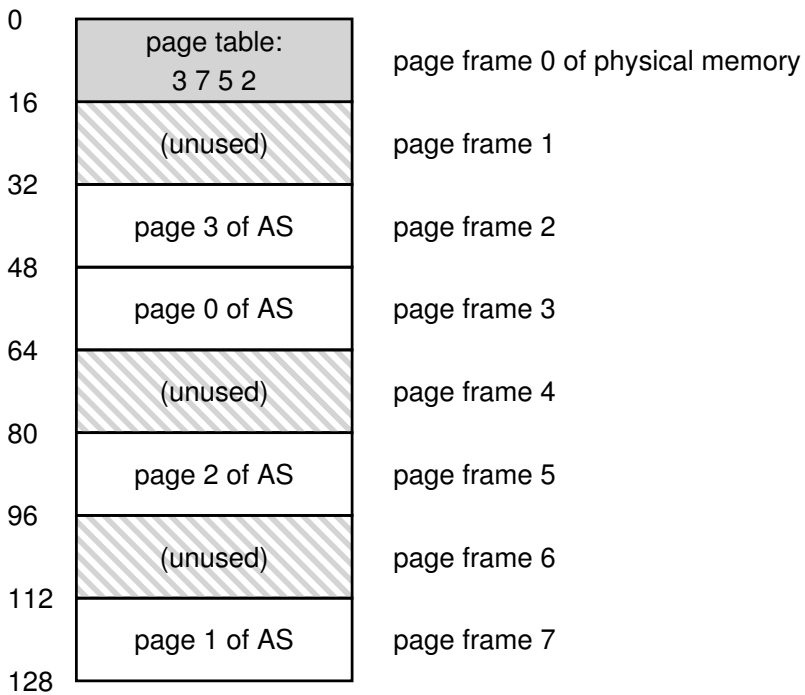
Page Size	Low Bits	V.Addr Bits	High Bits	# V.Pages
16 bytes	4	10	6	64
1KB	10	20	10	1K
1MB	20	32	12	4K
512 bytes	9	16	5	32
4KB	12	32	20	

Bitology

Page Size	Low Bits	V.Addr Bits	High Bits	# V.Pages
16 bytes	4	10	6	64
1KB	10	20	10	1K
1MB	20	32	12	4K
512 bytes	9	16	5	32
4KB	12	32	20	1M

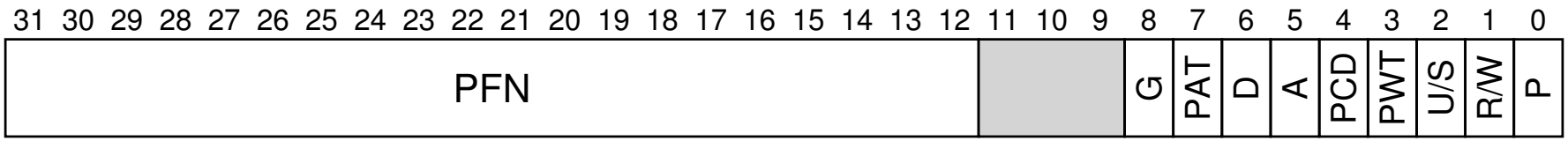
Where Are Page Tables Stored?

- Typical 32-bit address space with 4KB pages:
  - 20-bit VPN and 12-bit offset
  - 4 bytes per **page table entry (PTE)**
  - 4GB programs yields 4MB of memory for each page table
  - Promil overhead. However: Huge continuity demand!
  - Danger of compactification creeping back in.
  - 100 processes: 400MB just for address translations!



What's Actually In The Page Table?

- Simplest form: **linear page table**
  - Array, indexed by VPN, looks up PTE to find PFN
  - Register of array length!
  - **Valid bit**: whether the translation is valid
    - Unused space is **invalid**, access will trap into OS
    - Sparse address space: no physical frame for invalid
  - **Protection bits**: read, write, execute
  - **Present bit**: in physical memory or disk (discussed later)
  - **Dirty bit**: whether page has been modified
  - **Reference bit**: indicating page has been accessed



Issues

- HUGE CONTINUITY DEMAND.
- Too slow
  - To get PTE, starting location of page table is needed
  - Page table too big to store in MMU
  - Extra memory reference for every memory reference
- Internal fragmentation
  - Page size may not match needed size

Issues

- HUGE CONTINUITY DEMAND.
- Too slow
  - To get PTE, starting location of page table is needed
  - Page table too big to store in MMU
  - Extra memory reference for every memory reference
- Internal fragmentation
  - Page size may not match needed size

Solving the continuity demand

Lower continuity demands (ch. 20)

Bigger Pages

- Same address space, **16KB** pages
  - 18-bit **VPN** and 14-bit **offset**
  - $\frac{2^{32}}{2^{14}} \cdot 4\text{bytes} = \mathbf{1MB}$ per page table
- Major problem:

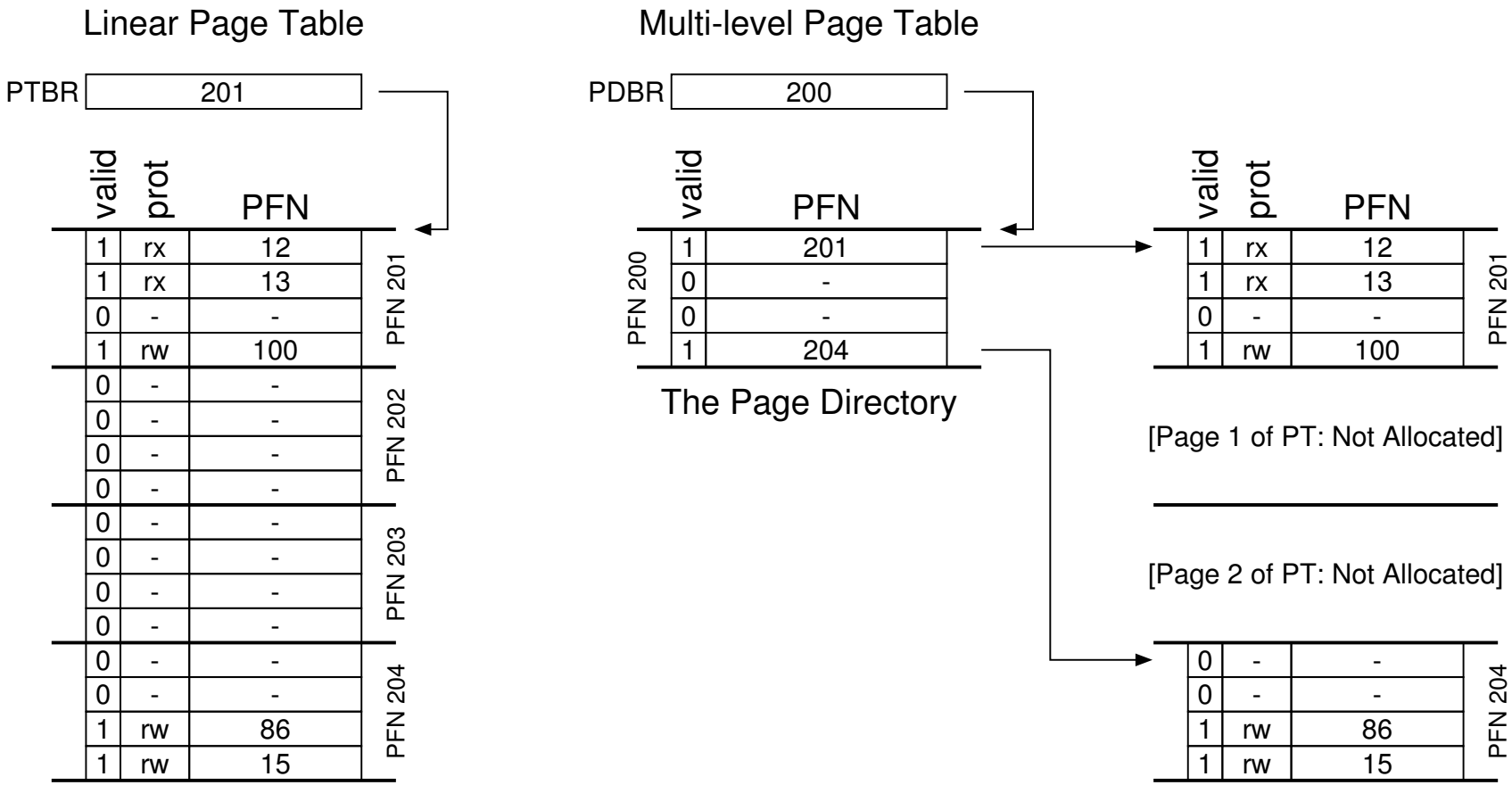
Bigger Pages

- Same address space, **16KB** pages
  - 18-bit **VPN** and 14-bit **offset**
  - $\frac{2^{32}}{2^{14}} \cdot 4\text{bytes} = \mathbf{1MB}$ per page table
- Major problem: **internal fragmentation**

Multi-Level Page Tables

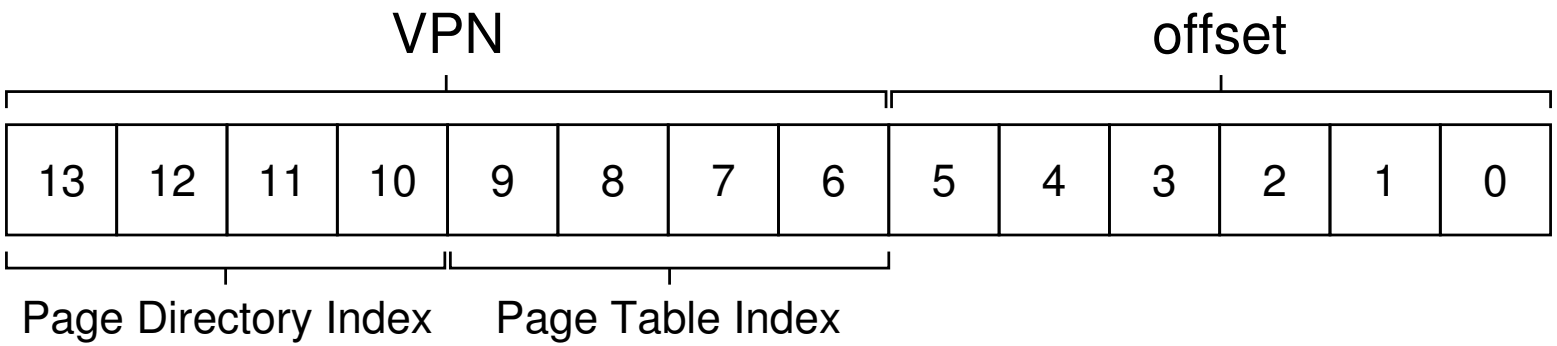
- Turn the page table into a tree
  - Split page table into page-sized units
  - Entire page of entries invalid? Don't allocate it
  - Track in a **page directory**

Multi-Level Page Tables



Multi-Level Page Tables

- **Page directory**
  - One **page directory entry (PDE)** per page of page table
  - Valid bit and PFN



Multi-Level Page Tables

- Pros:
  - Allocate space in proportion to use
  - Each portion fits within a page
    - Easier to manage memory
- Cons:
  - Add a **level of indirection** (**time-space trade-off**)
  - Increased complexity

More Than Two Levels

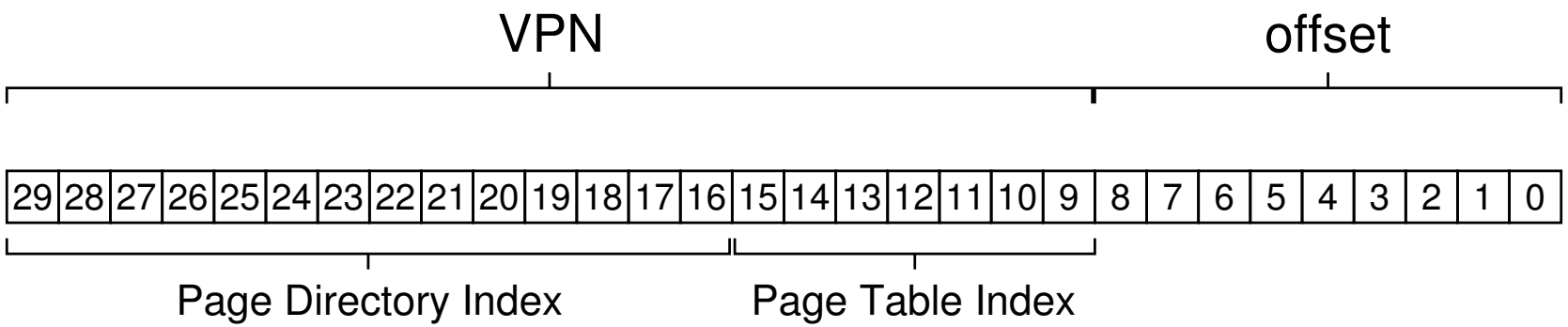
- In some cases, a deeper tree is possible (and needed)
- Let's assume (for example):
  - 30-bit virtual address space, 512 bytes page

More Than Two Levels

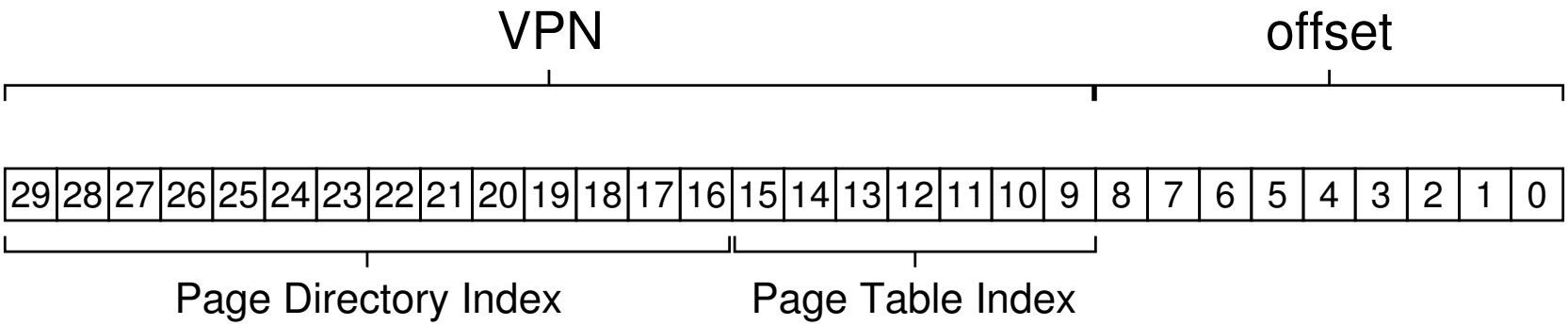
- In some cases, a deeper tree is possible (and needed)
- Let's assume (for example):
  - 30-bit virtual address space, 512 bytes page
  - 21-bit VPN and 9-bit offset
  - How many entries in a page?

More Than Two Levels

- In some cases, a deeper tree is possible (and needed)
- Let's assume (for example):
  - 30-bit virtual address space, 512 bytes page
  - 21-bit VPN and 9-bit offset
  - How many entries in a page?
    - 512 bytes, PTE of 4 bytes: 128 PTEs on a single page

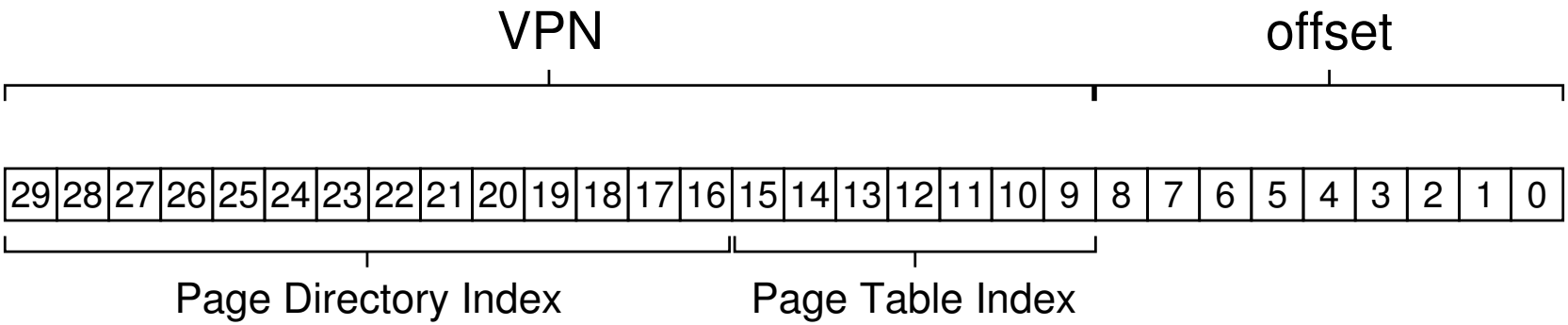


More Than Two Levels

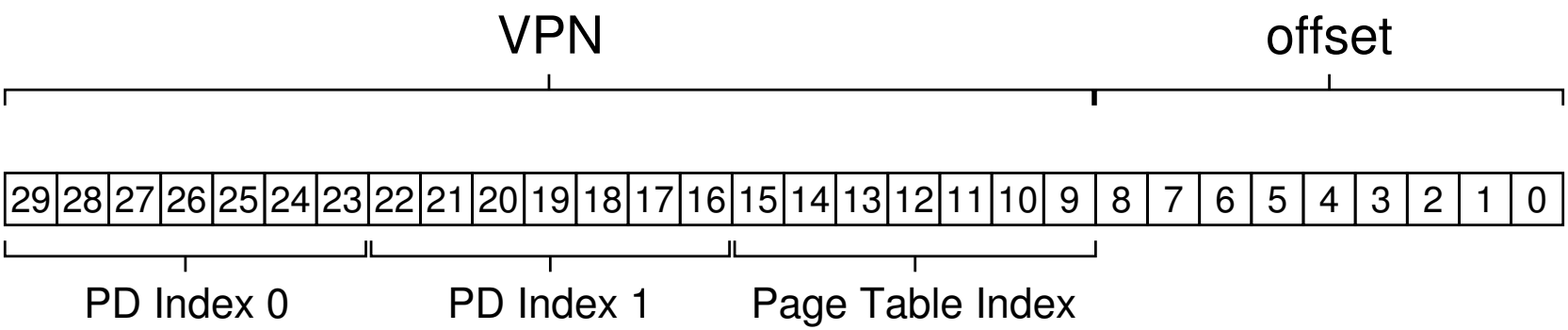


- 14 bits left for page directory
  - 2^{14} entries, spans 128 pages

More Than Two Levels



- 14 bits left for page directory
  - 2^{14} entries, spans 128 pages
  - Can add a directory to the directory!



Inverted Page Tables

Interesting idea. Unreasonable limitation.

- Keep a single page table
  - Entry for each physical page
  - Keeps which process is using the page, virtual page it maps to
  - Use hash table to speed up lookups

Swapping

- Relax assumption that physical memory suffices
- Page tables may be too big to fit into memory
- Use **kernel virtual memory**
  - Virtual memory allows us to **swap** pages to disk
  - Our next topic

Summary

- Fixed size pages, mapped to physical page frames
- **Multi-level page tables**
  - Divide page table into pages
  - The **page directory**