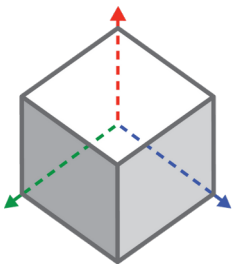

VectorBlox
embedded supercomputing

VectorBlox MXP Programming Guide for Xilinx

February 24, 2016

VectorBlox

http://vectorblox.com

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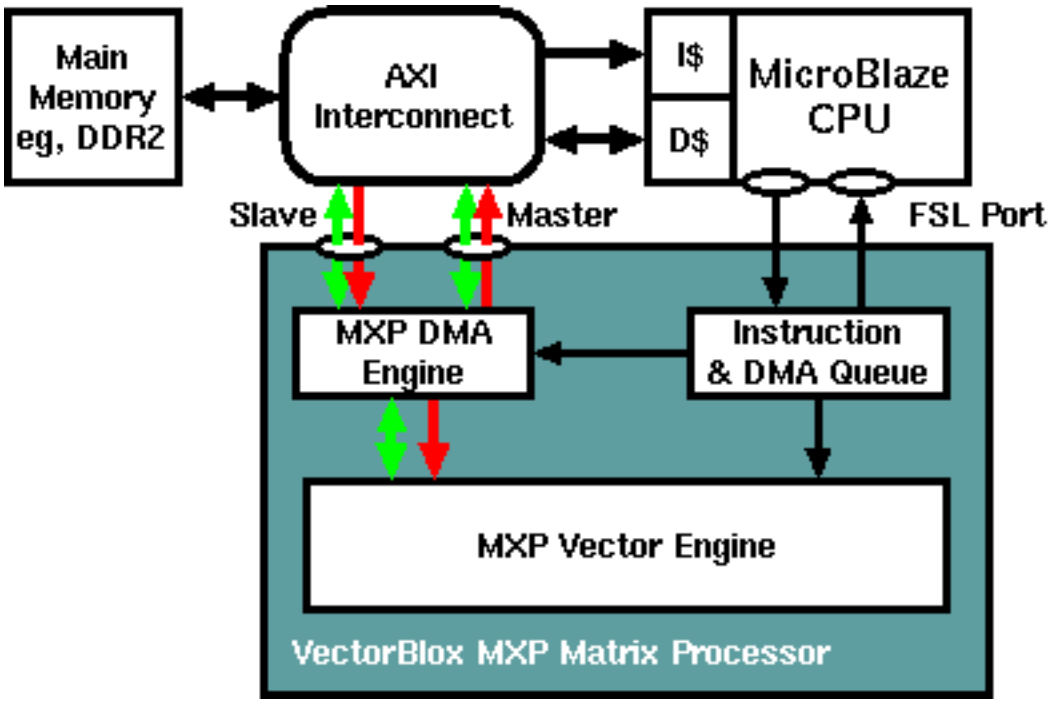

Figure 1: VectorBlox MXP System with MicroBlaze

1.1 Architecture Overview

The VectorBlox MXP matrix processor is an extremely high-performance processor capable of speedups in excess of 1000× faster than MicroBlaze or Nios II/f. The design of the processor was inspired by the vector processors used in scientific supercomputers made by Cray, Fujitsu and NEC. However, the MXP is not a simple clone of one of these processors. It has been redesigned from the ground up to perform well on embedded applications which operate primarily on various integer widths and fixed-point data types. It has also been designed from the start to map exceptionally well into modern FPGAs in a way that exploits their hard RAM blocks and hard multiplier or DSP blocks.

The VectorBlox MXP matrix processor is an update on the classical vector processor. Instead of operating merely on vectors, it can also operate on 2D and 3D matrices. It performs parallel calculations directly on sets of data stored directly in a private scratchpad memory, rather than a register file.

To achieve speedups in excess of 1000×, the VectorBlox MXP employs several strategies to maximize parallelism and to reduce overhead such as address calculations. This ensures the parallel ALUs employed by the MXP are working to their full potential on actual data calculations.

The parallelism available in MXP exceeds that of traditional scalar CPUs, fixed-width SIMD operations, and even variable-length vector CPUs. This goes beyond the number of parallel ALUs employed, as we have witnessed speedups of 20× or higher using just a single vector lane! Here are some of the reasons why you may expect speedups that exceed the number of ALUs on your own code:

- Unlike scalar CPUs or fixed-width SIMD operations, loop counters and branches are not necessary and can be eliminated from the inner loop. This eliminates the overhead of counting/incrementing, comparisons, conditional branches, and branch mispredictions.

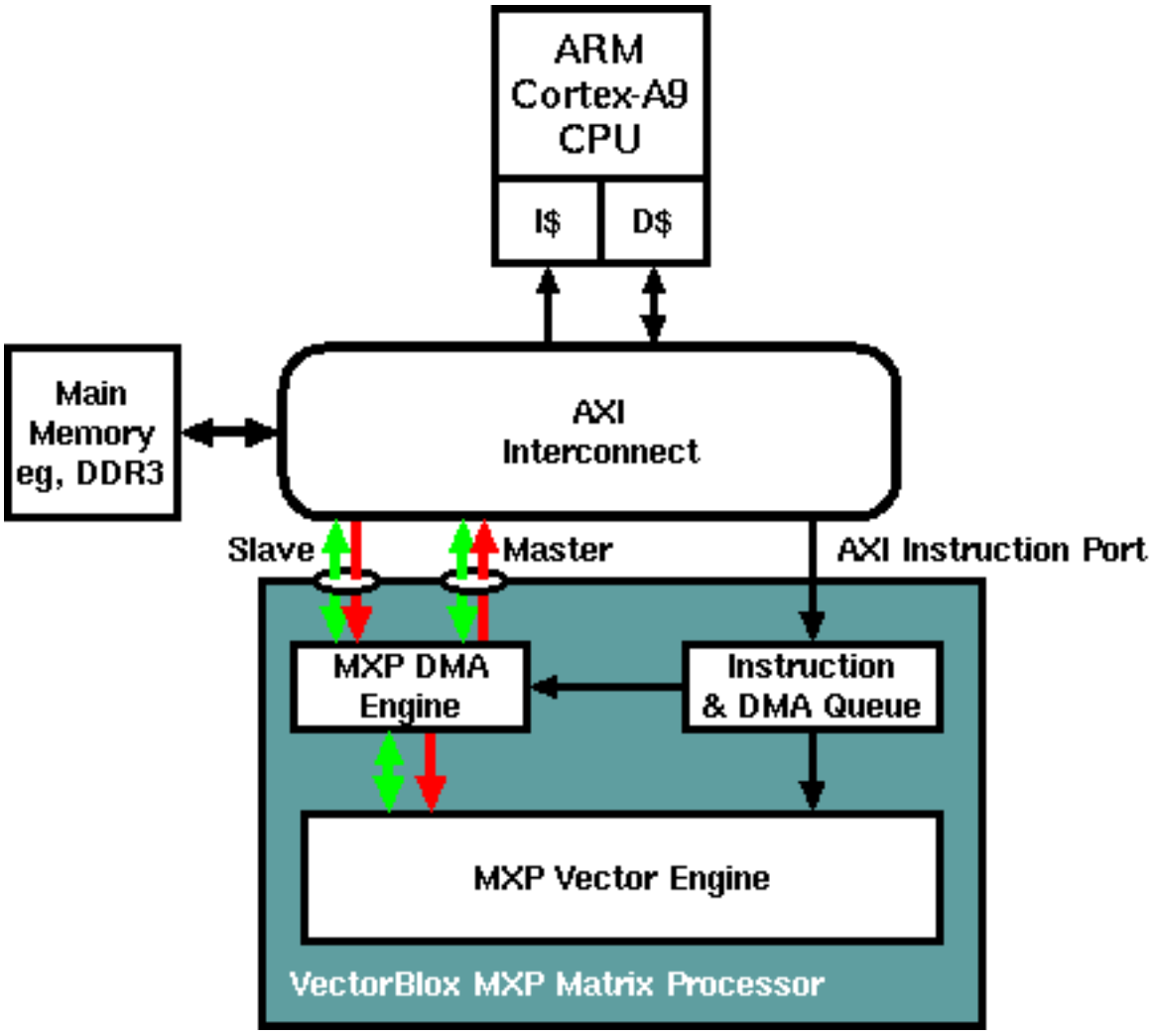

Figure 2: VectorBlox MXP System with ARM Cortex-A9 in Zynq-7000 FPGAs

- Unlike traditional scalar vector CPUs, each ALU in MXP can perform 2 parallel calculations on halfwords (16-bit integers) or 4 parallel calculations on bytes (8-bit integers).
- Unlike scalar CPUs or fixed-width SIMD operations, load and store instructions are not necessary and can be eliminated from the inner loop. These normally transfer data from a cache to the register file, and may even result in a cache miss. Instead, the MXP operates memory-to-memory on data already in the scratchpad and never suffers from a cache miss.
- Traditional vector CPUs support a fixed number of named vectors, each with a maximum size. Instead, the MXP can partition its large and flexible scratchpad arbitrarily into any number of vectors, of any length, starting at any address, that is subject only to overall scratchpad capacity. This improves overall data availability and significantly reduces data copying.
- The MXP scratchpad is easily double-buffered, allowing all memory latency to be hidden.

1.2 Scratchpad

The MXP does not operate on data directly stored in memory. Instead, data must first be DMA-transferred into a private local memory called a scratchpad. Like a cache, the scratchpad is designed to provide fast, parallel access to data. However, unlike a cache, the scratchpad is not managed automatically for the programmer. Instead, the programmer must explicitly transfer data from host to scratchpad, or from scratchpad to host.

The scratchpad is byte addressable. A vector, matrix, or submatrix is identified explicitly by a pointer to its starting address in the scratchpad. The contents of a vector are striped across several parallel block memories, allowing full parallel readout when a vector is accessed sequentially. All vector operations start at the lowest address and proceed to the highest address, subject to the length of the vector. Operations on long vectors are carried out over multiple clock cycles, one ***wavefront*** of data at a time. No matter what the starting address (aligned or not), a full wavefront which spans the full width of the scratchpad can always be read in one clock cycle.

1.3 Data Organization: Vectors, 2D Matrices and 3D Matrices

The most efficient way to use MXP is to organize data in memory contiguously into vectors, or as packed 2D or packed 3D matrices.

By a 2D packed matrix, we mean a series of rows of data that are placed end-to-end, possibly with some fixed amount of padding between each pair of adjacent rows. There must be a constant difference between the starting addresses of any two adjacent rows.

By a 3D packed matrix, we mean a series of 2D matrices that are placed end-to-end, possibly with some fixed amount of padding between each pair of 2D adjacent matrices. There must be a constant difference between the starting addresses of any two adjacent 2D matrices.

Before operating on any data, the MXP processor must also be told the size or dimensions of the vector or matrix. This information is provided to the processor in advance of the instructions and remembered in its configuration state.

The minimal information required for vector instructions is the ***vector length***. As will be described later, more information is also required for 2D and 3D matrix operations, such as the number of rows.

1.4 Vector Instructions

A typical instruction is provided with three explicit operands: pointers to the destination, to the source operand A, and to the source operand B. In addition, type information is explicitly provided to specify the data element size (byte, halfword or word), signed or unsigned operation, as well as special cases for operands A and B. The special

cases that are permitted are replacing vector operand A with a scalar value, and replacing vector operand B with an enumerated vector. An enumerated vector provides an ordinal number for each element indicating its position in the vector.

1.5 Vector Lanes

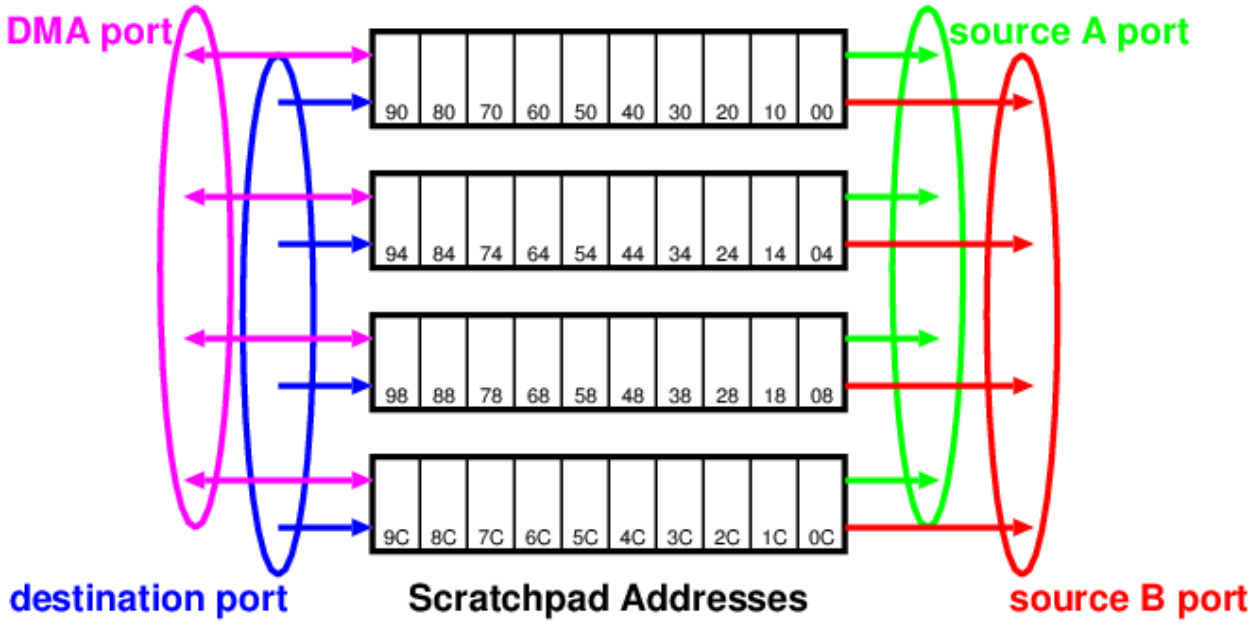

Figure 3: Quadruple-ported Scratchpad and Addressing

Calculations within MXP are performed by parallel 32-bit vector lanes. A processor configuration that is referred to as MXP-V4, for example, consists of four parallel vector lanes. Likewise, a V1 contains just one vector lane and V16 contains sixteen vector lanes.

The vector lanes can be instructed to operate upon three different data sizes: bytes (8 bits), halfwords (16 bits), or words (32 bits). When operating on smaller data sizes, the amount of parallelism increases proportionately. That is, a V4 configuration can perform either 16 parallel byte-size operations per cycle, or 8 parallel halfword-size operations per cycle.

Each lane contains a slice of the scratchpad memory, so wider vector processors are provided with a wider scratchpad memory. This scales the available memory bandwidth in a natural way to match the compute capacity of the MXP vector lanes.

As shown in the figure above, the scratchpad contains four access ports, and each is byte-addressable. Two dedicated read ports and one dedicated write port allows the processor to read its operands and write back a result every clock cycle. The fourth port, a DMA port, can be dynamically configured to either read or write data. The DMA system can access the scratchpad without interrupting a computation in progress.

Furthermore, addresses in the scratchpad are striped across the vector lanes, in a similar way that data blocks are striped across disks in RAID-0. Each lane can store one word, two halfwords, or four bytes. Hence, scratchpad addresses increase by 4 when crossing from one lane to an adjacent lane.

Unlike a typical register-based processor, there is no preset limit imposed by the MXP instruction set architecture (ISA) on the number of vectors or the vector length. However, the size of the scratchpad forms a practical upper bound on the vector length and various other matrix parameters. Hence, at one extreme, the entire scratchpad can be filled by a single vector of bytes. At the other extreme, the entire scratchpad can be filled entirely by vectors that are each one byte long.

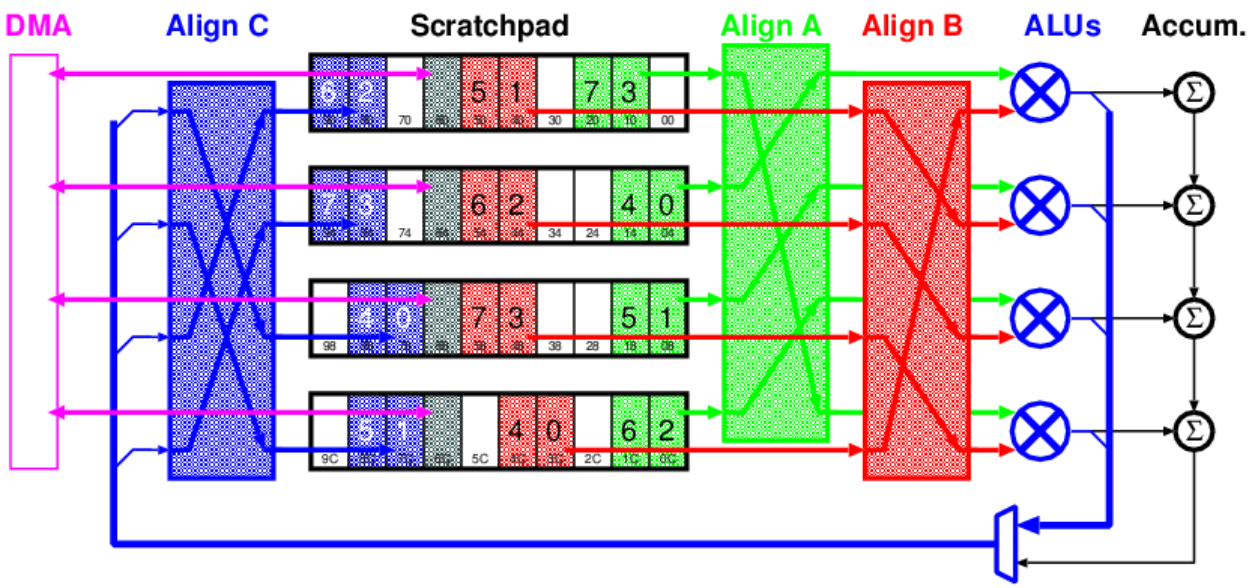

Figure 4: VectorBlox MXP Vector Engine

While the ISA does not limit the number of vectors stored in the scratchpad, it is important to note that all scratchpad pointers are calculated and stored by the host scalar processor. Since the scalar register file is fixed in size and the operation of many registers are predetermined by its compiler application binary interface (ABI) specifications, using more than 8 to 16 vectors will likely involve spilling contents of the scalar register file to main memory.

2 Programming Model

Programs written for the VectorBlox MXP use a combination of ANSI-C with VectorBlox C extensions. Basic ANSI-standard C code is run entirely on the host scalar processor. The VectorBlox C extensions are used to to specify the data-parallel operations that are to be computed by the MXP vector engine. These extensions are especially useful for image processing and similar applications where operations are applied to sets of data (such as pixels). The VectorBlox MXP Matrix Processor provides two engines that run completely in parallel with the host processor: the MXP DMA engine, and the MXP vector engine.

2.1 MXP DMA Engine

The MXP direct-memory access (DMA) engine provides a means to perform block data transfers between the host's external memory and the vector scratchpad. These transfers are performed asynchronously from the host processor.

The contents of the scratchpad are not managed automatically like a cache. Instead, the programmer must explicitly transfer memory from the host to the vector scratchpad, or vice versa.

Only one DMA transfer can be active at a time. Additional requests are queued by the system until the active transfer is complete. To ensure correctness, DMA transfers are always executed in FIFO or program order. Since DMA transfers can be interleaved with vector instructions, they are deposited into a common ***Instruction and DMA Request Queue***. The MXP processor will automatically allow DMA transfers to bypass in-flight instructions, or vice versa, provided there are no data hazards between them. These data hazards are determined exclusively by the scratchpad address(es) being read or written. When a hazard exists, the MXP processor will insert a bubble into the pipeline, allowing current operations to complete before allowing a hazardous operation to make forward progress.

2.2 MXP Vector Engine

The MXP vector engine operates naturally on 8 bit bytes, 16 bit halfwords, or 32 bit words. The engine is organized into a set of vector lanes, where refer to the size of the vector engine as V1 or V128 for 1 or 128 vector lanes, respectively. The number of lanes must be a power of 2, where each lane incorporates a 32-bit ALU and a 32-bit slice of the scratchpad. Each vector lane can be subdivided on an instruction-by-instruction basis into two halflanes which operate on halfwords, or four bytelanes which operate on bytes. Thus, maximum parallelism is provided on byte-wide data.

The vector lanes of the MXP vector engine are only one means of achieving parallel execution. Even a single-lane MXP V1 with one 32-bit ALU can provide speedups over 20x compared to the host processor. This parallelism may come from many sources:

- byte or halfword parallelism
- elimination of load and store instructions from the instruction stream
- double-buffered asynchronous DMA operations overlap memory latency with computation
- hardware-based loop counters and auto-incrementing address arithmetic
- hardware-based looping avoids branch mispredictions
- overlapped scalar instructions with vector instructions and DMA operations

2.3 MXP Programming Overview

The general process for programming the MXP is:

1. Allocate vectors in scratchpad.
2. Transfer data from memory to scratchpad.
3. Operate on vectors in scratchpad.
4. Transfer data from scratchpad to memory.
5. Deallocate vectors in scratchpad.

The scratchpad is a region of fast, on-chip parallel memory for holding and operating upon vector data. A minimum of 4KB per vector lane is provided, and this is usually enough for most applications.

The scratchpad is addressable by the scalar host, but care must be taken whether to cache the scratchpad or not. By default, scratchpad addresses are cached.

A simple vector program which adds three vectors is provided below:

2.3.1 Simple Example

```
#include "vbx.h"

int A[] = {1, 2, 3, 4};
int B[] = {5, 6, 7, 8};
int C[] = {-1, -1, -1, -1};
int main()
{
    int vector_len = 4;
    int num_bytes = vector_len * sizeof(int);

    /* step 1 */
    vbx_word_t * v_a = vbx_sp_malloc( num_bytes );
    vbx_word_t * v_b = vbx_sp_malloc( num_bytes );
    vbx_word_t * v_c = vbx_sp_malloc( num_bytes );

    /* step 2 */
    vbx_dma_to_vector( v_a, A, num_bytes );
    vbx_dma_to_vector( v_b, B, num_bytes );

    /* step 3 */
    vbx_set_vl( vector_len );
    vbx( VVW, VADD, v_c, v_a, v_b );

    /* step 4 */
    vbx_dma_to_host( C, v_c, num_bytes );

    /* step 5 */
    vbx_sp_free();

    vbx_sync();
    printf( "C[] = %d, %d, %d, %d\n",
    C[0], C[1], C[2], C[3] );

    return 0;
```

```
}
```

This example could possibly run into some caching issues, information on how to avoid these issues, as well as using dynamic allocation can be found in the data-sharing section.

3 MicroBlaze and ARM Programming

The MicroBlaze host processor has the following properties:

- 3- or 5-stage pipeline, roughly 1 instruction per clock cycle
- single-issue, in-order execution
- 4GB address space
- optional direct-mapped, non-coherent caches

VectorBlox typically configures the MicroBlaze in its demonstration systems as follows:

- 5-stage pipeline
- 8KB instruction cache with 8-word cache lines
- 4KB write-back data cache with 8-word cache lines
- no MMU
- hardware multiplier (one cycle latency)
- hardware barrel shifter
- support for pattern compare instructions
- branch target cache with 256 entries

Xilinx Zynq-7000 FPGAs contain two ARM Cortex-A9 CPUs with the following properties:

- variable-length pipeline
- up to two instructions issued per cycle
- support for out-of-order execution
- branch prediction using a 4096-entry global branch history buffer (GHB) and a 512-entry branch target address cache (BTAC)
- 4GB address space
- memory management unit for address translation and access protection
- NEON Media Processing Engine supporting the ARM v7 advanced SIMD and vector floating-point v3 (VFPv3) instruction sets
- 32KB L1 instruction and data caches, 4-way set-associative, write-back, 32-byte cache line size
- 512KB L2 cache shared by both Cortex-A9 cores, 8-way set-associative, write-through or write-back, 32-byte cache line size

3.1 Caching

MicroBlaze does not provide any mechanism for hardware cache coherence. Hence, programmers must manually flush the instruction or data cache when necessary (e.g. when data needs to be shared with another bus master). Flushing consists of writing back a data cache line (if dirty), and then invalidating the cache line.

The ARM Cortex-A9 MPCore subsystem in the Zynq-7000 FPGAs incorporates two Cortex-A9 CPU cores and a Snoop Control Unit (SCU). The SCU manages data cache coherency between the two Cortex-A9 CPUs and provides an Accelerator Coherency Port (ACP) AXI Slave to simplify sharing of data with other bus masters (such as DMA engines) as long as they don't have their own caches. Reads over the ACP are first looked up in the CPU caches and writes over the ACP will invalidate any affected cache lines in the CPU caches, so the programmer does not have to perform explicit data cache flushing to share data with ACP-connected bus masters. However, if a bus master needs to move a large amount of data that does not need to be frequently accessed by the Cortex-A9 CPUs, it may not be efficient to use the ACP. VectorBlox does not currently support connection of the MXP DMA engine to the ACP, so the programmer will still need to properly manage the caches when sharing data withe MXP.

Xilinx's Standalone BSP provides two functions to flush the data cache:

- `#include "xil_cache.h"` (required header file)
- `Xil_DCacheFlush()` flushes the entire data cache.
- `Xil_DCacheFlushRange(Addr, Len)` flushes the specified memory region from the data cache.

Similarly, the instruction cache can be invalidated with

- `Xil_ICacheInvalidate()`, or
- `Xil_ICacheInvalidateRange(Addr, Len)`

Note that `Xil_DCacheFlushRange()` must walk through the entire memory region of `Len` bytes (incrementing by the cache line size in the inner loop). For a sufficiently large memory region, it will be faster to just flush the entire data cache and start over.

3.2 VBX Portability Library

To simplify the porting of MXP programs between different scalar host CPUs (e.g. MicroBlaze and ARM Cortex-A9), VectorBlox provides a common cache management and timestamp timer API.

The functions in the portability library are listed below. More details can be found in the *VectorBlox MXP Programming Reference*.

```
vbx_timestamp_start()
vbx_timestamp_freq()
vbx_timestamp()
vbx_uncached_malloc()
vbx_uncached_free()
vbx_dcache_flush_all()
vbx_dcache_flush(PTR,len) or vbx_dcache_flush_line(PTR)
vbx_remap_cached(PTR,len)
vbx_remap_uncached(PTR) or vbx_remap_uncached_flush(PTR,len)
```

The cache management calls assume that memory accesses can bypass the data cache by setting address bit 31 to 1. The section on uncached access to cached memory regions describes how this can be accomplished on MicroBlaze and ARM Cortex-A9 systems.

- `vbx_dcache_flush(PTR,len)` considers the length of data being flushed. If it is too large, it will flush the entire data cache instead. Xilinx's version loops over the entire length of the data.
- `vbx_remap_uncached(PTR)` remaps and flushes only a single cache line
- `vbx_remap_uncached_flush(PTR,len)` remaps and flushes a region, but the region is flushed using `vbx_dcache_flush(PTR,len)`

The functions below convert a pointer between cached and uncached mode by toggling bit 31:

- `void *vbx_remap_cached(volatile void *ptr, u32 len)` returns a cached pointer.
- `volatile void *vbx_remap_uncached_flush(void *ptr, u32 len)` returns an uncached pointer. When mapping to uncached, the memory region will also be flushed.

The functions below allocate and deallocate uncached memory:

- `volatile void *vbx_uncached_malloc (size_t size)` allocates memory, returns an uncached pointer.
- `void vbx_uncached_free(volatile void *ptr)` unallocates an uncached region.

3.3 MXP Initialization with a Standalone BSP

3.3.1 vbx_timestamp Initialization

In order to use the `vbx_timestamp*()` functions, the system must provide some sort of hardware timer.

On MicroBlaze-based systems, the `vbx_timestamp` functions require an an axi_timer instance. The axi_timer instance must be registered with Xilinx's TmrCtr driver, as well as with the `vbx_timestamp` functions. Initialization can be done as follows (replace `TMRCTR_0` with the canonical instance ID of the timer instance you wish to use):

```
#include "xparameters.h"
#include "xil_types.h"
#include "vbx.h"
#include "xtmrctr.h"

XTmrCtr vbx_tmr_inst;

void my_vbx_tmr_init()
{
    int status;
    u16 tmrctr_dev_id  = XPAR_TMRCTR_0_DEVICE_ID;
    u32 tmrctr_freq_hz = XPAR_TMRCTR_0_CLOCK_FREQ_HZ;

    status = XTmrCtr_Initialize(&vbx_tmr_inst, tmrctr_dev_id);
    if (status != XST_SUCCESS) {
        VBX_PRINTF("ERROR: XTmrCtr_Initialize failed.\n");
        VBX_FATAL(__LINE__, __FILE__, -1);
    }
    vbx_timestamp_init(&vbx_tmr_inst, tmrctr_freq_hz);
}
```

On ARM-based systems, the `vbx_timestamp` functions make use of the Cortex-A9's PMU timer. The PMU timer's frequency must be registered with the `vbx_timestamp` functions as in this example (the PMU timer runs at half the CPU frequency):

```
#include "xparameters.h"
#include "xil_types.h"
#include "vbx.h"

void my_vbx_tmr_init()
{
    u32 tmrctr_freq_hz = XPAR_CPU_CORTEXA9_0_CPU_CLK_FREQ_HZ/2;
    vbx_timestamp_init(tmrctr_freq_hz);
}
```

3.3.2 Mapping Instruction Port to Device Memory (ARM systems only)

On ARM systems, the MMU should be configured to set the memory type of the the MXP's AXI Instruction Slave port to "Device memory", so that writes to the instruction port bypass the data caches and are posted (do not wait for acknowledgement from the final destination).

The following shows how this can be done using `Xil_SetTlbAttributes()` from the standalone BSP:

```
#include "xil_mmu.h"

extern u32 MMUTable;

int vbx_zynq_set_instr_port_device_memory()
{
    // Change memory attributes of 1MB region starting at base address of
    // AXI instruction port.
    // shareable device:
    //   S=b0 TEX=b000 AP=b11, C=b0, B=b1 => 0xC06
    Xil_SetTlbAttributes(XPAR_VECTORBLOX_MXP_ARM_0_S_AXI_INSTR_BASEADDR,
                         0xc06);
    return XST_SUCCESS;
}
```

3.3.3 Support for Uncached Access to Cached Memory Region

The VBX API library provides some functions to simplify sharing of data between the host CPU and the MXP without requiring the application programmer to explicitly flush data cache lines. These functions include `vbx_shared_malloc()`, `vbx_shared_free()`, `vbx_remap_uncached()`, and `vbx_remap_cached()`.

The library assumes that the host CPU can access a cached memory region in an uncached manner (i.e. bypassing the data cache) simply by setting the most significant bit of the address to 1.

MicroBlaze does not have a built-in mechanism to bypass the data cache this way, but the same functionality can be added by adding some bus connections and placing some restrictions on the MicroBlaze's address map. Details can be found in the *MXP-M Quickstart Guide* that is distributed with the hardware IP core.

On an ARM-based system, the translation table in the CPU's Memory Management Unit (MMU) can be used to alias the physical address range of a shared memory to two logical address ranges that differ only in address bit

31. The memory attributes of the lower address range are set to “normal cacheable”, whereas the attributes of the upper address range are set to “strongly-ordered” to make the region non-cacheable.

For example, on the ZedBoard, the physical address range of the DDR3 DRAM is 0x0-0x1fff_ffff (512MB) and the virtual address range 0x0-0x1fff_ffff is mapped to this physical range and the memory attribute set to cacheable. The virtual address range 0x8000_0000 to 0x9fff_ffff (512 MB) can also be mapped to the same physical address range but with the memory attribute set to strongly-ordered, allowing uncached access to DRAM.

The `vbx_zynq_remap_ddr_uncached()` function in `software/lib/vbxtest/vbx_test.c` illustrates how this can be done:

```
#include "xpseudo_asm.h"
#include "xil_mmu.h"

extern u32 MMUTable;

// Map (virtual) address range 0x8000_0000 to 0x9fff_ffff (512 MB) to
// DDR physical address range 0x0-0x1fff_ffff and set memory attributes to
// strongly-ordered.
// Based in Xil_SetTlbAttributes() in xil_mmu.c.
int vbx_zynq_remap_ddr_uncached()
{
    u32 addr;
    // Section descriptor bits 19:0 for
    // strongly-ordered:
    //   S=b0 TEX=b000 AP=b11, C=b0, B=b0 => 0xC02
    // (Short-descriptor translation table format, FigB3-4, p. B3-1325 of
    // ARM Architecture Reference Manual DDI0406C.b)
    u32 attrib = 0xc02;
    u32 *ptr;
    u32 section;

    mtcp(XREG_CP15_INVAL_UTLB_UNLOCKED, 0);
    dsb();

    // One descriptor per 1 MB region; iterate over 512 descriptors covering
    // 512MB in range 0x8000_0000 to 0x9fff_ffff.
    for (addr = 0x80000000; addr < 0xa0000000; addr += 0x100000) {
        // Index into translation table
        section = addr / 0x100000;
        ptr = &MMUTable + section;
        // Map to physical addresses in range 0x0 to 0x1fff_ffff,
        // i.e. clear bit 31.
        *ptr = (addr & 0x7FF00000) | attrib;
    }
    dsb();

    mtcp(XREG_CP15_INVAL_UTLB_UNLOCKED, 0);
    /* Invalidate all branch predictors */
    mtcp(XREG_CP15_INVAL_BRANCH_ARRAY, 0);

    dsb(); /* ensure completion of the BP and TLB invalidation */
    isb(); /* synchronize context on this processor */

    return XST_SUCCESS;
}
```

4 Data Sharing

The code in the following subsections are variations of the vector addition code given earlier (simple example) using the VBX Portability Library.

The original code has no caching issues because the data is statically allocated in the data segment, so it is initialized into the data segment and untouched by the processor. However, the new code uses the processor to dynamically allocate and initialize the data, hence a copy of the data may be residing in the cache.

However, the first example shows one approach of managing cache coherence by flushing the shared regions out of the data cache. The source memory regions, `A` and `B`, must be flushed before the DMA transfer because the CPU has modified their values and dirty lines are being retained in the write-back cache. The memory region for the final answer, `C`, must be flushed because a stale copy or dirty copy may be in the data cache. Even if the CPU did not initialize the array `C`, elements at the beginning or end of C may have been brought into the cache because of locality and the sharing of cache lines with adjacent data. As a result, it can be difficult to keep track of whether to flush the data.

Instead, the second example shows our preferred approach of managing cache coherence. It works by marking shared regions as uncached data during allocation. Then, all scalar accesses will be to uncached data, but there will not be any coherence issues. This is the easiest way to program, but it may result in performance issues when the scalar processor initializes shared inputs or reads shared results. We still recommend this style, but suggest that you address performance issues by explicitly switching to a cached pointer where necessary. This is shown for array `A` in the final example.

4.1 Data Sharing Examples

4.1.1 Example showing flushing of cached regions

```
#include "vbx.h"
#include "vbx_port.h"

int main()
{
    int A[] = {1, 2, 3, 4};
    int B[] = {5, 6, 7, 8};
    int C[] = {-1, -1, -1, -1};

    int vector_len = 4;
    int num_bytes = vector_len * sizeof(int);

    /* step 1 */
    vbx_word_t *va = vbx_sp_malloc( num_bytes );
    vbx_word_t *vb = vbx_sp_malloc( num_bytes );
    vbx_word_t *vc = vbx_sp_malloc( num_bytes );

    /* step 2 */
    vbx_dcache_flush( A, num_bytes );
    vbx_dcache_flush( B, num_bytes );
    vbx_dma_to_vector( va, A, num_bytes );
    vbx_dma_to_vector( vb, B, num_bytes );

    /* step 3 */
    vbx_set_vl( vector_len );
    vbx( VVW, VADD, vc, va, vb );
```

```
    /* step 4 */
    vbx_dcache_flush( C, num_bytes );
    vbx_dma_to_host( C, vc, num_bytes );

    /* step 5 */
    vbx_sp_free();

    printf( "C[] = %d, %d, %d, %d\n",
            C[0], C[1], C[2], C[3] );
    return 0;
}
```

4.1.2 Example with shared regions allocated as uncached

```
#include "vbx.h"

int main()
{
    int vector_len = 4;
    int num_bytes = vector_len * sizeof(int);

    int *A; A = vbx_shared_malloc( num_bytes );
    int *B; B = vbx_shared_malloc( num_bytes );
    int *C; C = vbx_shared_malloc( num_bytes );

    A[0] = 1; A[1] = 2; A[2] = 3; A[3] = 4;
    B[0] = 5; B[1] = 6; B[2] = 7; B[3] = 8;

    /* step 1 */
    vbx_word_t *va = vbx_sp_malloc( num_bytes );
    vbx_word_t *vb = vbx_sp_malloc( num_bytes );
    vbx_word_t *vc = vbx_sp_malloc( num_bytes );

    /* step 2 */
    vbx_dma_to_vector( va, A, num_bytes );
    vbx_dma_to_vector( vb, B, num_bytes );

    /* step 3 */
    vbx_set_vl( vector_len );
    vbx( VVW, VADD, vc, va, vb );

    /* step 4 */
    vbx_dma_to_host( C, vc, num_bytes );

    /* step 5 */
    vbx_sp_free();

    printf( "C[] = %d, %d, %d, %d\n",
            C[0], C[1], C[2], C[3] );
    return 0;
}
```

4.1.3 Example combining shared (uncached) and cached regions

```c
#include "vbx.h"
#include "vbx_port.h"

int main()
{
    int vector_len = 4;
    int num_bytes = vector_len * sizeof(int);

    int *A; A = vbx_shared_malloc( num_bytes );
    int *B; B = vbx_shared_malloc( num_bytes );
    int *C; C = vbx_shared_malloc( num_bytes );

    int *cachedA = vbx_remap_cached( A, num_bytes );
    cachedA[0] = 1; cachedA[1] = 2;
    cachedA[2] = 3; cachedA[3] = 4; // cached, faster
    vbx_dcache_flush( cachedA, num_bytes );
    B[0] = 5; B[1] = 6;
    B[2] = 7; B[3] = 8; // uncached, slower

    vbx_word_t *va = vbx_sp_malloc( num_bytes );
    vbx_word_t *vb = vbx_sp_malloc( num_bytes );
    vbx_word_t *vc = vbx_sp_malloc( num_bytes );

    vbx_dma_to_vector( va, A, num_bytes );
    vbx_dma_to_vector( vb, B, num_bytes );

    vbx_set_vl( vector_len );
    vbx( VVW, VADD, vc, va, vb );

    vbx_dma_to_host( C, vc, num_bytes );

    vbx_sp_free();

    printf( "C[] = %d, %d, %d, %d\n",
             C[0], C[1], C[2], C[3] );
    return 0;
}
```