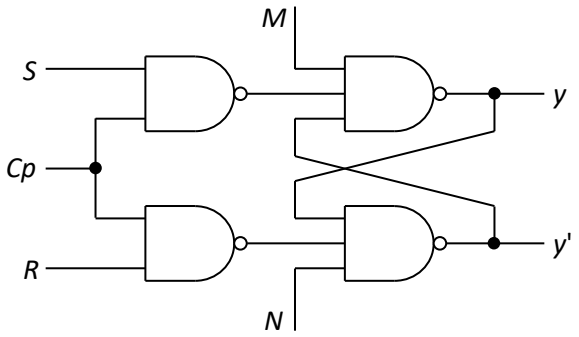
Lab 4: Sequential Circuit Design Using Schematics (updated 10/17/2019)

In this lab, you will create schematics for sequential circuits using flip-flops and basic gates. Registers and counters are two examples of the class of circuits known as sequential circuits. Sequential circuits have the property that their outputs are functions not just of the current input values, but of past input values as well, controlled by a clock signal.

Assignments:

1. Analyze the latch circuit below. *M* and *N* are the *Preset* (sets *y* to 1) and *Clear* (sets *y* to 0) inputs. *Cp* is the clock signal.
    a. Determine which is which, and also determine what the normal state of these inputs should be; i.e., are they active low or active high? These must not be left unconnected when used in a circuit. In particular, assuming that the clock pulse is inactive, construct a truth table with *M* and *N* as inputs and *y* and *y′* as outputs. Use this to determine what *M* and *N* do. After identifying *M* and *N*, determine whether the clock *Cp* is active high or active low. Do this before building the circuit.
    b. Build the latch circuit in Quartus and test it on a DE10 board. Use one of the push buttons for the clock signal. Push buttons are low when pressed. Push buttons are debounced while switches are not. Use four of the toggle switches for the *S*, *R*, *M*, and *N* inputs. Connect *y* and *y′* to LEDs. With the clock input inactive, test that the *M* and *N* inputs work correctly. Then, with *M* and *N* inactive, test that the *S* and *R* inputs work correctly along with the clock.
    c. Demonstrate it to the instructor/TA on the board.



2. In this part, you will design a counter and implement it using Quartus. You can obtain the specifications for a counter from the lab assistant.
    a. Design the circuit using three D flip-flops and whatever other gates are required. The circuit must be *minimized; i.e., it should use the minimum number of logic gates possible.* Predict the output when the counter is set to one of the unused states. **Your K-maps and logic expressions must be uploaded.**
    b. Implement your circuit in Quartus and test it on a DE10 board. Use the DFF primitive from the library for the flip flops. Don't forget to connect the clear

(CLRN) and preset (PREN) signals of DFFs, which are active low. Connect them to switches when doing pin assignment. Use a pushbutton for the clock. Test the circuit on a DE10 board after you have generated a .sof file.

c. Demonstrate that the main cycle is produced properly. Force the circuit into each of the three unused states (using the *Clear* and *Preset* inputs) and verify your predictions of unused states.

3. You can obtain a state machine table online. Design the circuit using two D flip-flops and whatever other gates are required.

   a. Using Karnaugh maps, generate minimum expressions for the excitation functions D_1, D_2, and for the output function z. The circuit must be minimized; i.e., it should use the minimum number of logic gates possible. **Your K-maps and logic expressions must be uploaded.**

   b. Implement your circuit in Quartus and test/debug it on a DE10 board. Demonstrate to the TA/Instructor after you have verified that your circuit generates the correct sequence shown on the assignment paper.

Checklist

- ☐ **1.a.** **I have figured out the *Preset* and *Clear* signals and can explain. I have determined the correct polarity, i.e. active high or low, of the *Preset*, *Clear*, and clock signals and can explain.**
- ☐ **1.b.** **I have built and tested the circuit on a DE10 and it works.**
- ☐ **2.a.** **Circuit diagram for the counter is complete. K-maps and logic expressions have been uploaded.**
- ☐ **2.c.** **I have built and tested the circuit on a DE10 and it works.**
- ☐ **3.a.** **Circuit diagram for the state machine is complete. K-maps and logic expressions have been uploaded.**
- ☐ **3.b.** **I have built and tested the circuit on a DE10 and it works.**