数字逻辑设计

计数器示例

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示例1

```
//4bit计数器
module counter (
    input wire clk   ,
    input wire rst   ,
    input wire button
);

reg [3:0] cnt    ;
reg       cnt_inc;

wire rst_n = ~rst;

wire cnt_end = cnt_inc & (cnt == 4'h9);

always @ (posedge clk or negedge rst_n) begin
    if (~rst_n)       cnt_inc <= 1'b0;
    else if (button)  cnt_inc <= 1'b1;
    else if (cnt_end) cnt_inc <= 1'b0;
end

always @ (posedge clk or negedge rst_n) begin
    if (~rst_n)       cnt <= 4'h0;
    else if (cnt_end) cnt <= 4'h0;
    else if (cnt_inc) cnt <= cnt + 4'h1;
end

endmodule
```

示例2

```
//计数器串联
module counter (
    input wire clk    ,
    input wire rst    ,
    input wire button
);

reg [7:0] cnt1    ;
reg [3:0] cnt2    ;
reg       cnt_inc;

wire rst_n = ~rst;

wire cnt1_end = cnt_inc & (cnt1 == 8'h80);
wire cnt2_end = cnt1_end & (cnt2 == 4'h9);
```

```
always @ (posedge clk or negedge rst_n) begin
    if (~rst_n)         cnt_inc <= 1'b0;
    else if (button)    cnt_inc <= 1'b1;
    else if (cnt2_end) cnt_inc <= 1'b0;
end

always @ (posedge clk or negedge rst_n) begin
    if (~rst_n)         cnt1 <= 8'h00;
    else if (cnt1_end) cnt1 <= 8'h00;
    else if (cnt_inc)  cnt1 <= cnt1 + 8'h01;
end

always @ (posedge clk or negedge rst_n) begin
    if (~rst_n)         cnt2 <= 4'h0;
    else if (cnt2_end) cnt2 <= 4'h0;
    else if (cnt1_end) cnt2 <= cnt2 + 4'h1;
end

endmodule
```

开始实验