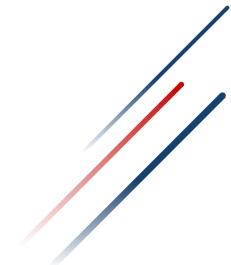
数字逻辑设计 计数器示例

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```
//4bit计数器
module counter (
    input wire clk
    input wire rst
    input wire button
L);
reg [3:0] cnt ;
reg
     cnt inc;
wire rst n = ~rst;
wire cnt end = cnt inc & (cnt == 4'h9);
lalways @ (posedge clk or negedge rst n) begin
    else if (button) cnt inc <= 1'b1;</pre>
    else if (cnt end) cnt inc <= 1'b0;
-end
always @ (posedge clk or negedge rst n) begin
    if (~rst n) cnt <= 4'h0;</pre>
    else if (cnt end) cnt <= 4'h0;
    else if (cnt inc) cnt <= cnt + 4'h1;</pre>
end
endmodule
```

示例2

```
//计数器串联
module counter (
    input wire clk ,
    input wire rst ,
    input wire button
);

reg [7:0] cnt1 ;
reg [3:0] cnt2 ;
reg cnt_inc;

wire rst_n = ~rst;

wire cnt1_end = cnt_inc & (cnt1 == 8'h80);
wire cnt2_end = cnt1_end & (cnt2 == 4'h9);
```

```
always @ (posedge clk or negedge rst n) begin
     if (~rst_n) cnt_inc <= 1'b0;</pre>
     else if (button) cnt inc <= 1'b1;</pre>
     else if (cnt2 end) cnt inc <= 1'b0;</pre>
end
always @ (posedge clk or negedge rst n) begin
     if (~rst n) cnt1 <= 8'h00;</pre>
     else if (cnt1 end) cnt1 <= 8'h00;</pre>
     else if (cnt inc) cnt1 <= cnt1 + 8'h01;</pre>
end
always @ (posedge clk or negedge rst n) begin
     if (~rst n) cnt2 <= 4'h0;</pre>
     else if (cnt2 end) cnt2 <= 4'h0;</pre>
     else if (cnt1 end) cnt2 <= cnt2 + 4'h1;</pre>
end
endmodule
```

开始实验

