Daniel Min Chang

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Education

University of California, Berkeley **[Expected May 2025]**

B.S. Electrical Engineering and Computer Sciences **GPA: 3.8/4.0**

- **Relevant Coursework:** Data Structures & Algorithms; Designing Information Devices & Systems; Signals & Systems; Computer Architecture & Engineering; Digital Design & Integrated Circuits; Microelectronic Devices & Circuits; Integrated Circuit Devices; Microfabrication Technology; Bring-up Test IC Chips designed in Tapeout; Egyptian Hieroglyphs
- **Organizations:** Eta Kappa Nu; Tau Beta Pi; Alpha Pi Mu; IISE @ Berkeley; IEEE @ Berkeley; Cal Judo

Experiences

Undergraduate Researcher | Berkeley Wireless Research Center **Berkeley, CA**

Sept 2022 - present

- Implemented the Top-Down Hierarchical Flow of Hammer(Highly Agile Masks Made Effortlessly from RTL), a framework for building physical chip design generators for digital VLSI flows. Configuring from the Top level to the partition level, it automatically runs corresponding Innovus commands for the given set of dependencies of the design
- Translated the hierarchical design structure into Innovus TCL commands, and then automated the process of running the design in a Top-Down flow in Python
- Now finalizing the implementation of early rail analysis, a feature that performs power analysis with rough routing at the early stage of the design using inputs such as power mesh density

CS 61C Academic Intern **Berkeley, CA**

Feb 2023 - May 2023

- Operated office hours for the introductory course to low-level programming and computer architecture, specifically on C programming, RISC-V, Logisim, and the RISC-V datapath
- Primarily assisted labs and projects such as coding snake game in C, classifying handwritten digits from the MNIST dataset using matrix multiplication in RISC-V, and eventually building a RISC-V processor in Logism

Projects

Common Source Amplifier Design **Berkeley, CA**

- Implemented a degenerated Common Source Amplifier using the BS170 NMOS transistor that satisfies the design specifications(mid-band gain, low and high -3dB frequency, and the output swing)
- Conducted both hand calculations and simulations using LTspice/Cadence to optimize component values. With the simulated amplifier design, built the circuit in a lab bench setting.
- Verified the performance of the physical amplifier through biasing experiments and Bode plot analysis, meeting all criteria

CPU Design Project **Berkeley, CA**

- Developed a three-stage RISC-V CPU with instruction decoding, ALU, and synchronous memory integration
- Used Verilog, System Verilog, and Synopsys tools for comprehensive testing of the pipelined design that can handle Data and Control Hazards accompanied by adding stalling and forwarding logic appropriately
- Designed a 4kiB direct-mapped, write-back cache in a Finite State Machine structure. It borrows the Skywater 130nm SRAM library thus the design can be fabricated. The final design was validated during the place-and-route via Innovus GUI, achieving a 2.04x performance improvement in cycle count benchmarks.
- The Critical Path was 42.685 ns and the Slack was 2.315 ns with the Clock Period configured as 45 ns with an operating frequency of 22.2 MHz. The Floor plan area was approximately 1093419 um^2 with a total power consumption of 6mW.

Branch Predictor Design **Berkeley, CA**

- Developed and tested 4 branch prediction algorithms(tournament, global share, combined of the two, and perceptron) for the BOOM (Berkeley Out-of-Order Machine) Core, improving CPI by 20-50% and achieving misprediction rates as low as 2% in Dhrystone Benchmark testing
- Conducted detailed performance analysis on benchmarks like Qsort and Multiply that extensively tests the branch predictor on specific mathematical operations, demonstrating significant improvements in CPI and branch prediction accuracy

Additional Information

Skills: JAVA, C, RISC-V, Python, Innovus GUI, Verilog/System Verilog, Chipyard, MATLAB, LTspice, oscilloscope, function generator